

MC74HC4067A

Quad Analog Switch/ Multiplexer/Demultiplexer

High-Performance Silicon-Gate CMOS

The MC74HC4067A utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316A.

Features

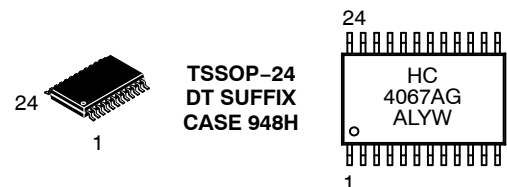
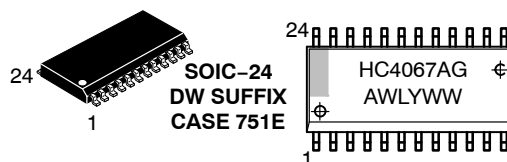
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Analog Input Voltage Range ($V_{CC} - GND$) = 0 to 6.0 V
- Improved Linearity and Lower ON Resistance over Input Voltage
- Low Noise
- These are Pb-Free Devices



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MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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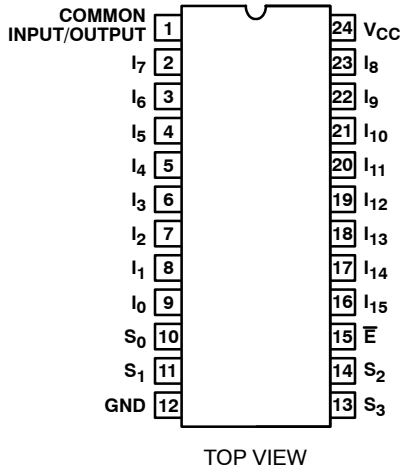


Figure 1. Pin Assignment

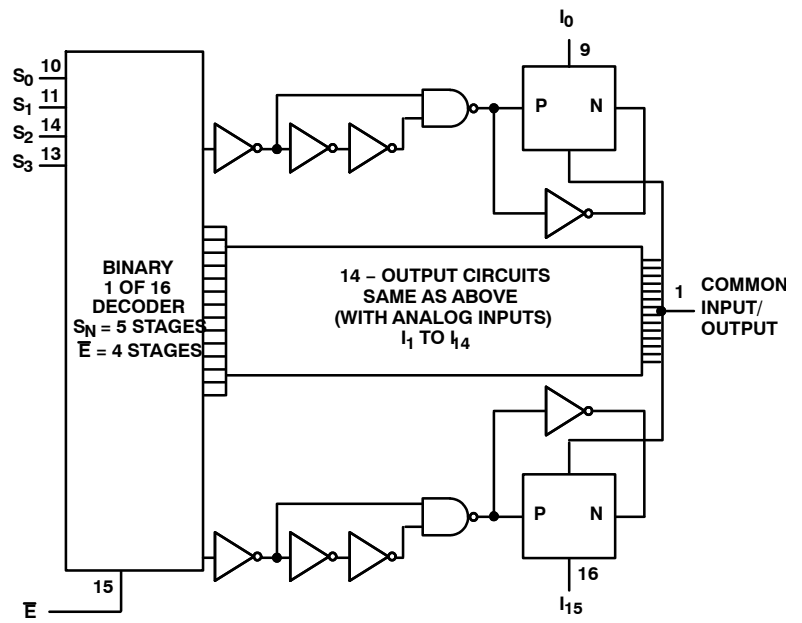


Figure 2. Function Diagram

TRUTH TABLE

S ₀	S ₁	S ₂	S ₃	\bar{E}	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level
 L= Low Level
 X= Don't Care

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V	
V _{IS}	Analog Input Voltage	-0.5 to V _{CC} + 0.5	V	
V _{IN}	Digital Input Voltage	-0.5 to V _{CC} + 0.5	V	
I _{IK}	Input Clamping Current	V _{IN} < -0.5 V or V _{IN} > V _{CC} + 0.5 V	±20	mA
I _{SK}	Switch Input Clamping Current	V _{IS} < -0.5 V or V _{IS} > V _{CC} + 0.5 V	±20	mA
I _{IS}	DC Switch Current		±25	mA
I _O	DC Output Source / Sink Current		±25	mA
I _{CC}	DC Supply Current per Supply Pin		±100	mA
I _{GND}	DC Ground Current per Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T _J	Junction Temperature under Bias		+150	°C
θ _{JA}	Thermal Resistance	SOIC TSSOP	97 148	°C/W
P _D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35%	UL-94-V0 (0.125 in)	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	>3000 >200	V
I _{Latchup}	Latchup Performance	Above V _{CC} and Below GND at 85°C (Note 3)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{IS}	Analog Input Voltage (Referenced to GND)	GND	V _{CC}	V	
V _{in}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V	
V _{IO*}	Static or Dynamic Voltage Across Switch	-	1.2	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Rate (Digital Inputs)	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

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DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Conditions	V _{CC} (V)	Guaranteed Limit						Unit	
				25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		2.0	1.5			1.5			1.5	V
			3.0	2.1			2.1			2.1	
			4.5	3.15			3.15			3.15	
			6.0	4.2			4.2			4.2	
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			6.0			1.8		1.8		1.8	
I _{IN}	Input Leakage Current, Control Inputs	V _{IN} = V _{CC} or GND	6.0			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Supply Current per Package	V _{IN} = V _{CC} or GND, I _O =0 V _{IS} = GND or V _{CC} , V _{OS} = V _{CC} or GND	6.0			4.0		40		80	μA
R _{ON}	ON Resistance	I _O = 1 mA V _{IN} = V _{CC} or GND, V _{IS} = V _{CC} or GND	4.5		70	160		200		240	Ω
			6.0		60	140		175		210	
R _{ON(peak)}	ON Resistance (peak)	I _O = 1 mA V _{IN} = V _{CC} to GND, V _{IS} = V _{CC} to GND	4.5		90	180		225		270	Ω
			6.0		80	160		200		240	
ΔR _{on}	ON Resistance Mismatch Between Any 2 Switches		4.5 6.0		10 8.5						Ω
I _{OFF}	OFF-State Leakage Current, All Channels	SW OFF, V _{IS} = V _{CC} or GND	6.0			±0.8		±8		±8	μA
I _{ON}	ON-State Leakage Current	SW OFF, V _{IS} = V _{CC} or GND	6.0			±0.8		±8		±8	μA

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AC CHARACTERISTICS (INPUT $t_r, t_f = 6$ ns)

Symbol	Parameter	Conditions	V_{CC} (V)	Guaranteed Limits						Unit		
				25 °C			-40 to 85 °C		-55 to 125 °C			
				Min	Typ	Max	Min	Max	Min		Max	
t_{PLH}, t_{PHL}	Propagation Delay Switch In to Out	$C_L = 50$ pF	2.0			75		95		110	ns	
			4.5			15		19		22		
		$C_L = 15$ pF	5.0		6.0							
t_{ON}	Switch Turn-ON Time										ns	
	\bar{E} to Out	$C_L = 50$ pF	2.0			275		345		415		
			4.5			55		69		83		
			$C_L = 15$ pF	5.0		23						
	SN to Out	$C_L = 50$ pF	2.0			300		375		450		
4.5					60		75		90			
		$C_L = 15$ pF	5.0		25							
t_{OFF}	Switch Turn-OFF Time										ns	
	\bar{E} to Out	$C_L = 50$ pF	2.0			275		345		415		
			4.5			55		69		83		
			$C_L = 15$ pF	5.0		23						
	SN to Out	$C_L = 50$ pF	2.0			290		365		435		
4.5					58		73		87			
		$C_L = 15$ pF	5.0		21							
C_{in}	Input Capacitance, Control Pins				3.5	10		10		10	pF	
C_{PD}	Power Dissipation Capacitance (Note 4)	$C_L = 15$ pF	5.0			29					pF	

4. C_{PD} is used to determine the dynamic power consumption, per multivibrator.

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ANALOG SWITCH CHANNEL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	Limit* 25°C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads - 3 dB R _L = 50 Ω, C _L = 10 pF	4.5	90	MHz
-	Off-Channel Feedthrough Isolation	f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 4.5	-65 -75	dB
-	Feedthrough Noise E, Sn to Switch	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	4.5 4.5	60 30	mV _{PP}
-	Crosstalk Between Any Two Switches	f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 4.5	-70 -80	dB
THD	Total Harmonic Distortion	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 V _{PP} sine wave	4.5	0.04	%
C _S	Switch Input Capacitance			5	pF
C _{COM}	Switch Common Capacitance			45	pF

*Limits not tested. Determined by design and verified by qualification.

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TYPICAL CHARACTERISTICS

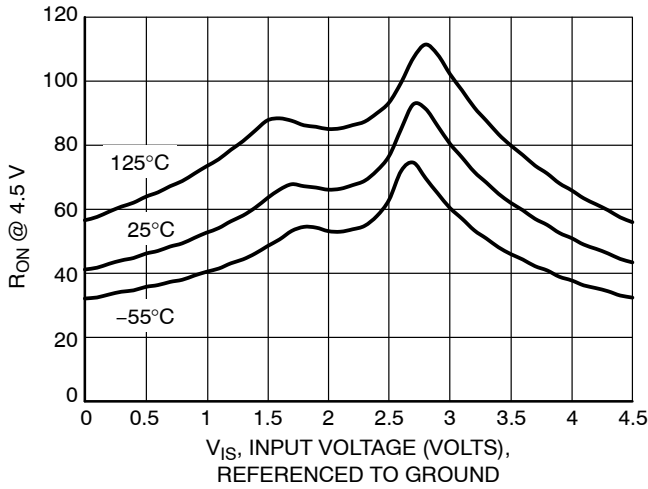


Figure 3. Typical On Resistance, $V_{CC} = 4.5\text{ V}$

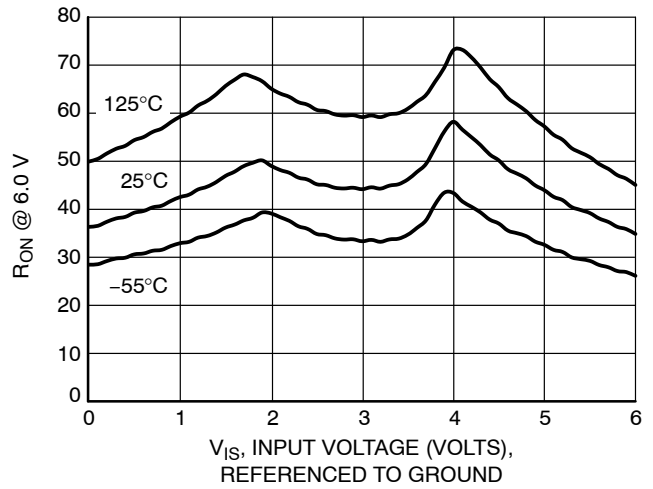


Figure 4. Typical On Resistance, $V_{CC} = 6.0\text{ V}$

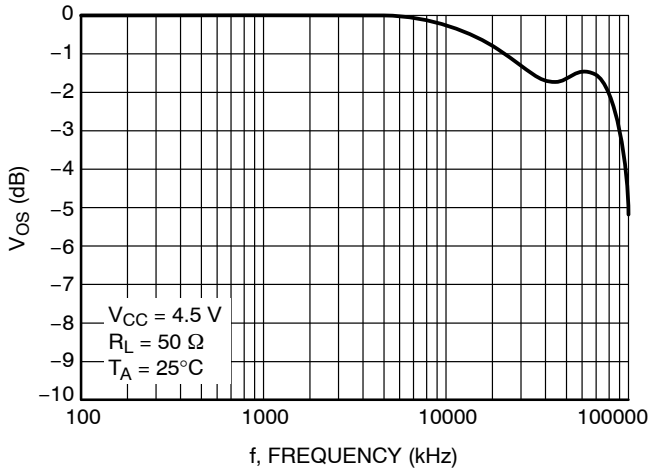


Figure 5. Typical Switch Frequency Response

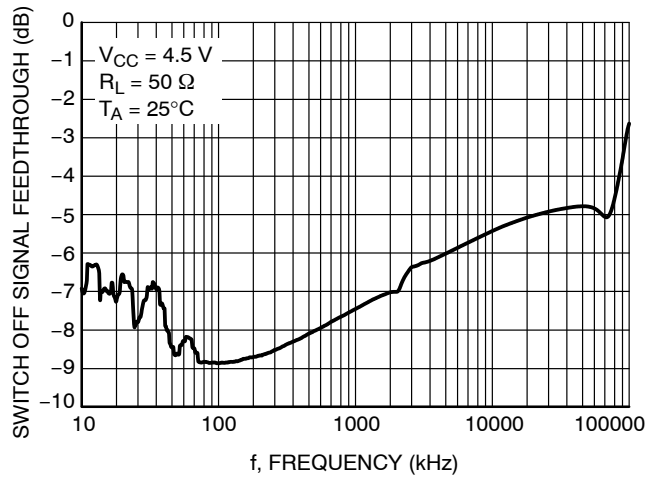


Figure 6. Typical Switch OFF Signal Feedthrough vs Frequency

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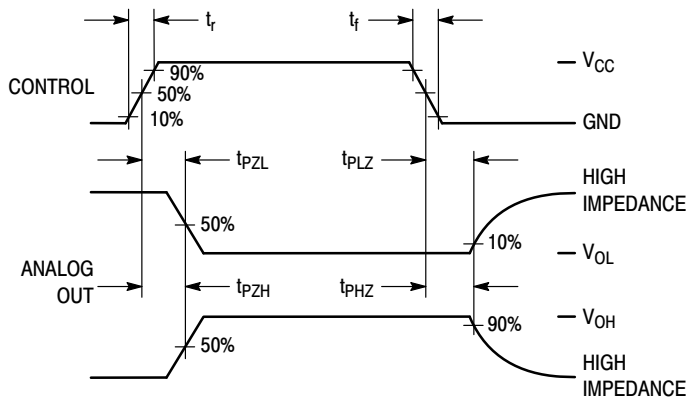
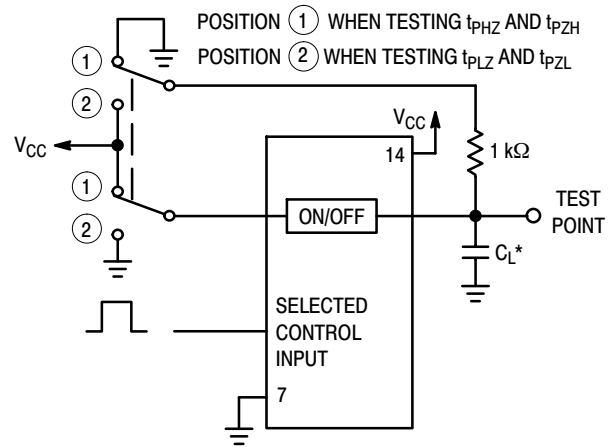


Figure 12. Turn-ON / Turn-OFF Times



*Includes all probe and jig capacitance.

Figure 13. Turn-ON / Turn-OFF Time Test Setup

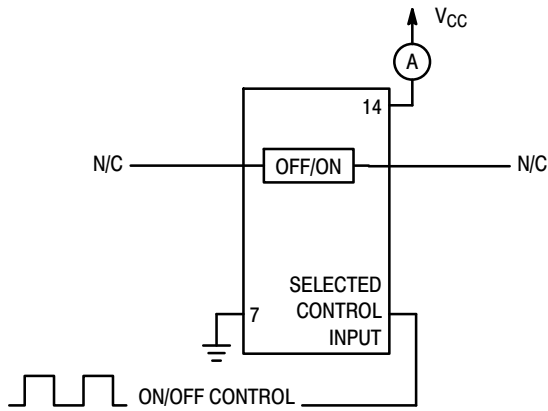
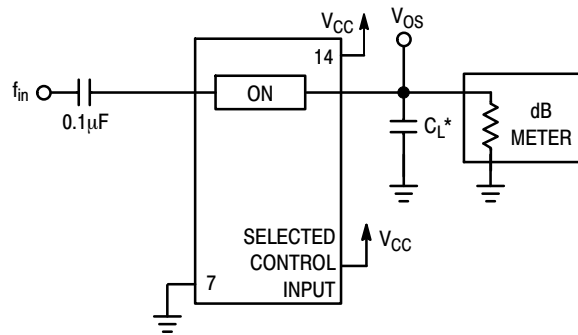
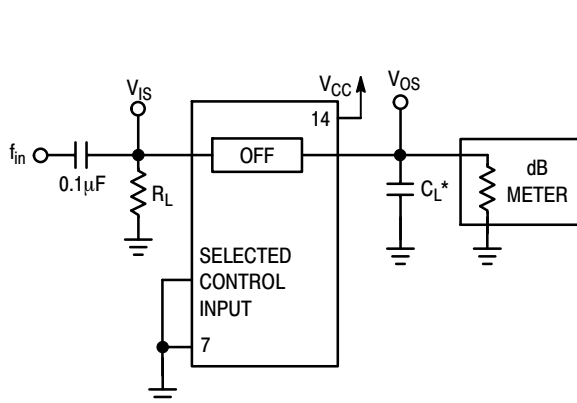


Figure 14. Power Dissipation Capacitance Test Setup



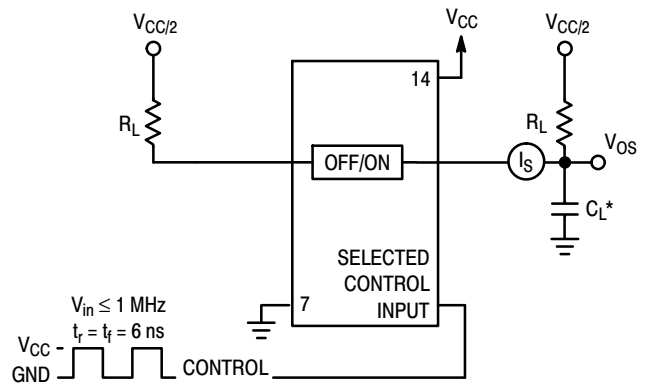
*Includes all probe and jig capacitance.

Figure 15. ON Channel Bandwidth Test Setup



*Includes all probe and jig capacitance.

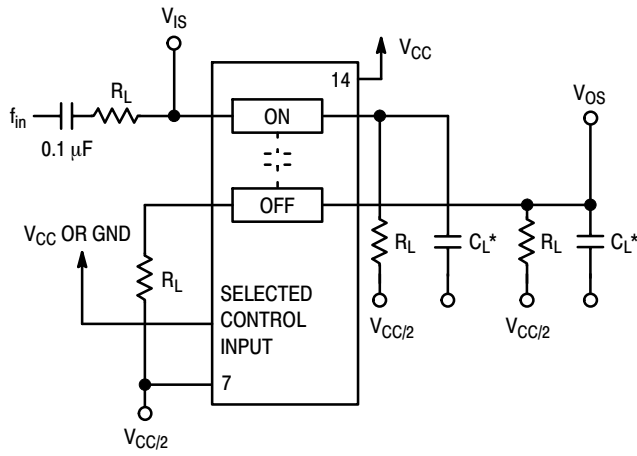
Figure 16. OFF Channel Feedthrough Isolation Test Setup



*Includes all probe and jig capacitance.

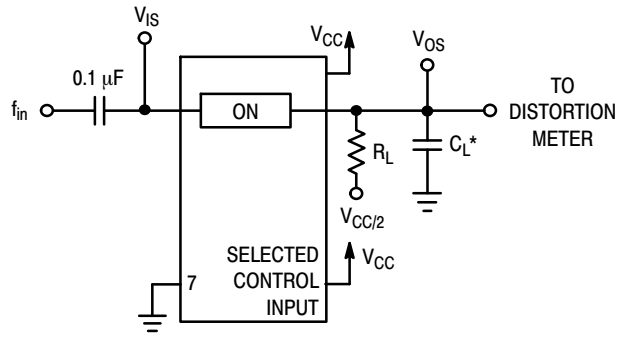
Figure 17. Feedthrough Noise Test Setup

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*Includes all probe and jig capacitance.

Figure 18. Crosstalk Between Any Two Switches Test Setup



*Includes all probe and jig capacitance.

Figure 19. Total Harmonic Distortion Test Setup

ORDERING INFORMATION

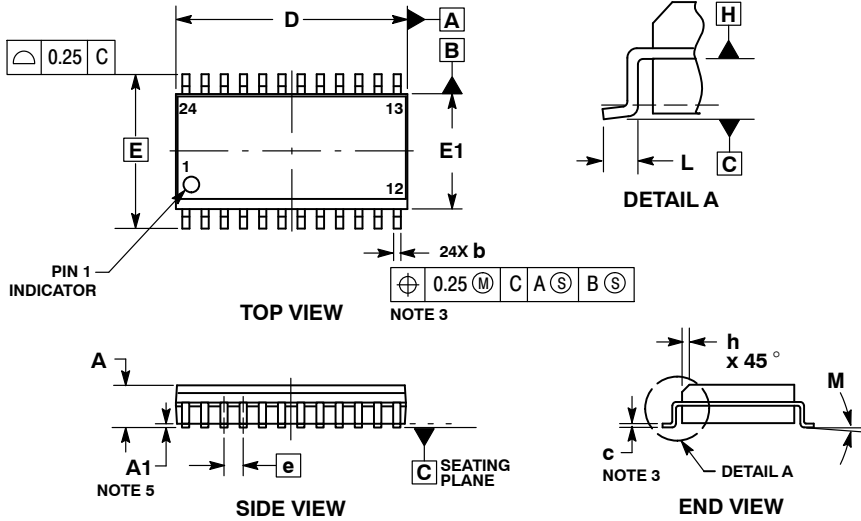
Device	Package	Shipping†
MC74HC4067ADWG	SOIC-24 (Pb-Free)	30 Units / Tube
MC74HC4067ADWR2G	SOIC-24 (Pb-Free)	1000 / Tape & Reel
MC74HC4067ADTG	TSSOP-24 (Pb-Free)	62 Units / Tube
MC74HC4067ADTR2G	TSSOP-24 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

SOIC-24 WB
CASE 751E-04
ISSUE F

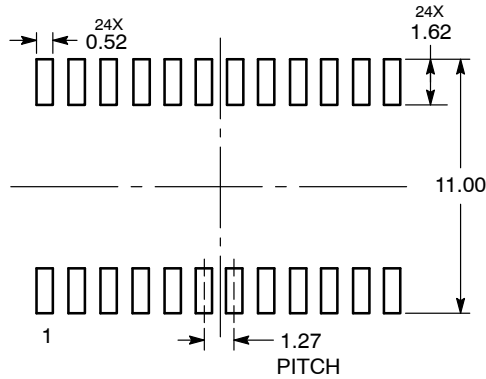


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
b	0.35	0.49
c	0.23	0.32
D	15.25	15.54
E	10.30 BSC	
E1	7.40	7.60
e	1.27 BSC	
h	0.25	0.75
L	0.41	0.90
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



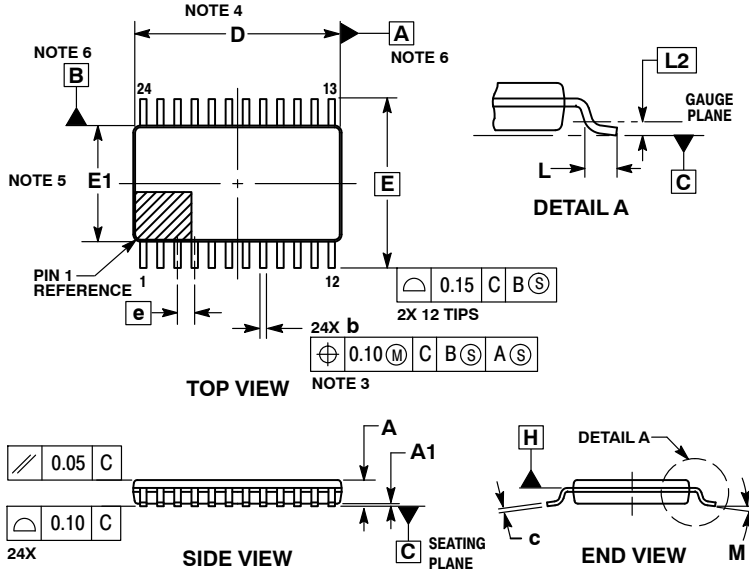
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP24 7.8x4.4, 0.65P
CASE 948H
ISSUE B

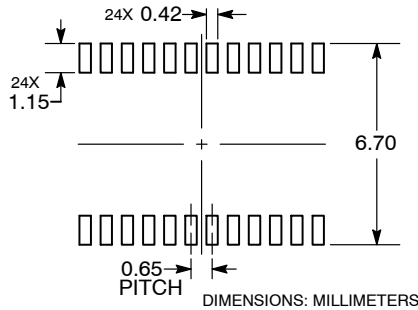


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



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