
# PSMN0R7-25YLD

## N-channel 25 V, 0.7 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

**15 April 2015** **Objective data sheet**

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Ultra low $Q_G$, $Q_{GD}$ and $Q_{OSS}$ for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 150 °C
- Wave solderable; exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | | - | - | 25 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 291 | W |

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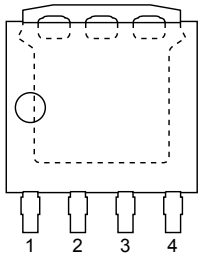
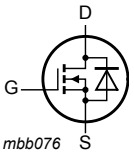
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $T_j$ | junction temperature | | | -55 | - | 150 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C | | - | 0.72 | 0.9 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C | | - | 0.56 | 0.7 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 12 V; Fig. 4 | | - | 10.8 | - | nC |
| $Q_{G(tot)}$ | total gate charge | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $V_{DS}$ = 12 V; Fig. 4 | | - | 49 | - | nC |
| **Source-drain diode** | | | | | | | |
| S | softness factor | $I_S$ = 25 A; $V_{GS}$ = 0 V; $dI_S/dt$ = -100 A/µs; $V_{DS}$ = 12 V; Fig. 5 | | - | [tbd] | - | |

[1] Continuous current is limited by package.

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |   **LFPAK56; Power-SO8 (SOT1023)** |   |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain[1] | | |

[1] Schottky performance achieved without the high temperature leakage current of a traditional Schottky diode.

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN0R7-25YLD | LFPAK56; Power-SO8 | Plastic single-ended surface-mounted package (LFPAK56); 4 leads | SOT1023 |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | | - | 25 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | | - | 25 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 291 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C | [1] | - | 100 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C | | - | 100 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | [tbd] | A |
| $T_{stg}$ | storage temperature | | | -55 | 150 | °C |
| $T_j$ | junction temperature | | | -55 | 150 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | | [tbd] | - | V |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | [tbd] | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 25 A; $V_{sup}$ ≤ 25 V; $R_{GS}$ = 50 Ω; unclamped; $t_p$ = 10 ms | [2] | - | 4190 | mJ |

[1] Continuous current is limited by package.
[2] Protected by 100% test

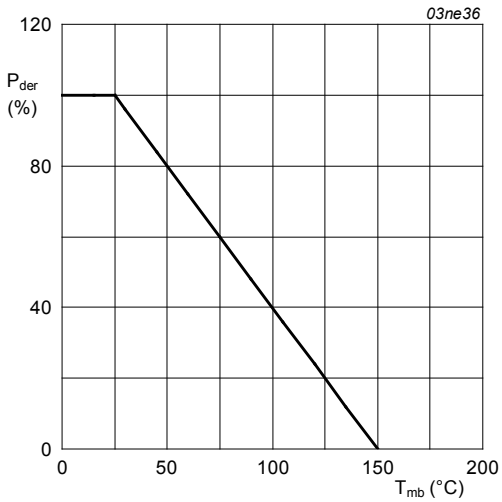



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P(tot)}{P_{tot(25°C)}} \times 100\,\%$$

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | | | - | 0.35 | 0.43 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | Fig. 2 | | - | 50 | - | K/W |
| | | Fig. 3 | | - | 125 | - | K/W |

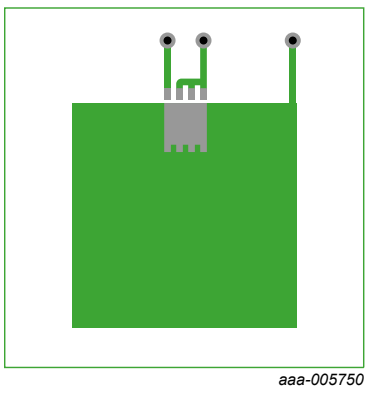



**Fig. 2. PCB layout for thermal resistance junction to ambient 1” square pad; FR4 Board; 2oz copper**

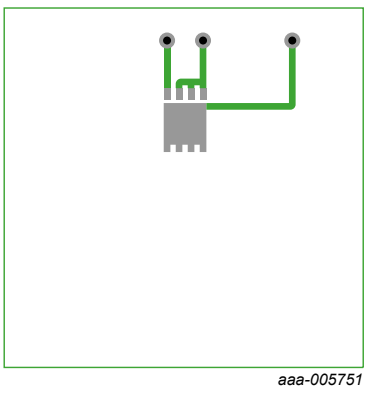



**Fig. 3. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 25 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 22.5 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 2 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C | | 1.2 | 1.7 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | [tbd] | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | [tbd] | - | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C | | - | 0.72 | 0.9 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 150 °C | | - | - | [tbd] | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C | | - | 0.56 | 0.7 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C | | - | - | [tbd] | mΩ |
| $R_G$ | gate resistance | f = 1 MHz | | - | 1.4 | - | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 12 V; $V_{GS}$ = 10 V; Fig. 4 | | - | 106.4 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; Fig. 4 | | - | 49 | - | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | | - | 56.1 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; Fig. 4 | | - | 18.3 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 11.7 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 6.6 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 10.8 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 12 V; Fig. 4 | | - | 2.6 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 12 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C | | - | 8013 | - | pF |
| $C_{oss}$ | output capacitance | | | - | 3242 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 484 | - | pF |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 12 V; $R_L$ = 0.4 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω | | - | [tbd] | - | ns |
| $t_r$ | rise time | | | - | [tbd] | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | [tbd] | - | ns |
| $t_f$ | fall time | | | - | [tbd] | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 12 V; f = 1 MHz; $T_j$ = 25 °C | | - | 58.5 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.78 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 12 V; Fig. 5 | | - | [tbd] | - | ns |
| $Q_r$ | recovered charge | | [1] | - | [tbd] | - | nC |
| $t_a$ | reverse recovery rise time | | | - | [tbd] | - | ns |
| $t_b$ | reverse recovery fall time | | | - | [tbd] | - | ns |
| S | softness factor | | | - | [tbd] | - | |

[1] includes capacitive recovery

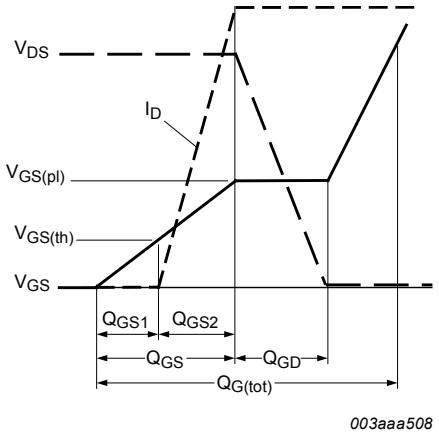



Fig. 4. Gate charge waveform definitions

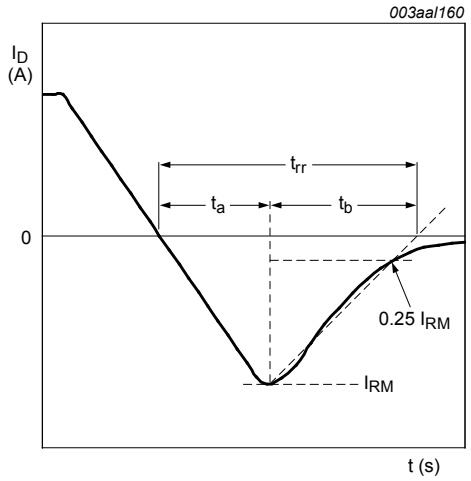
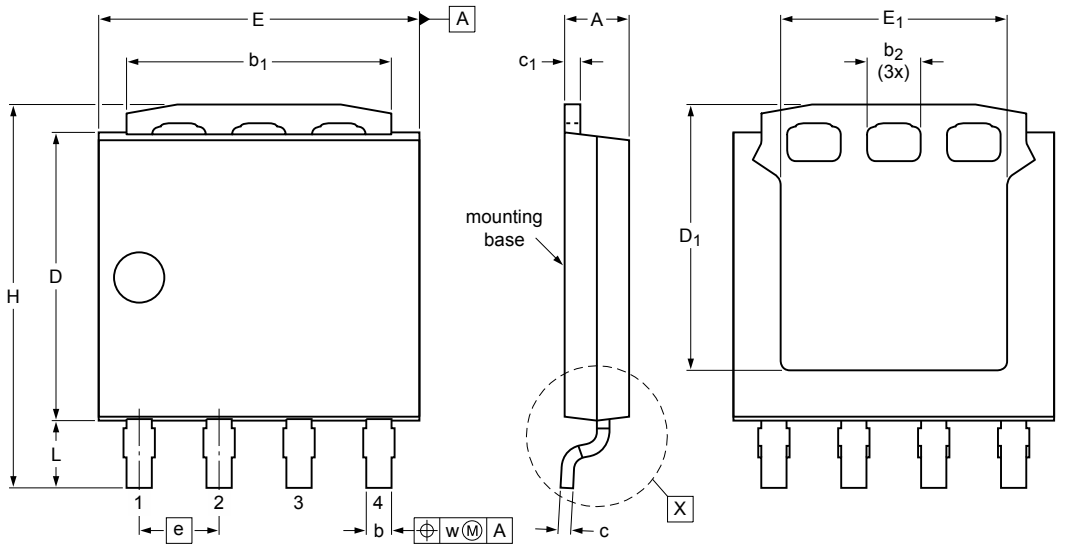



Fig. 5. Reverse recovery timing definition

# 10. Package outline

**Plastic single-ended surface-mounted package (LFPAK56); 4 leads** **SOT1023**




0 2.5 5 mm

scale

Dimensions

| Unit | | A | $A_1$ | b | $b_1$ | $b_2$ | c | $c_1$ | $D^{(1)}$ | $D_1{}^{(1)}$ | $E^{(1)}$ | $E_1{}^{(1)}$ | e | H | L | $L_p$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.10 | 0.15 | 0.50 | 4.41 | | 0.25 | 0.30 | 4.70 | 4.45 | 5.30 | 3.7 | | 6.2 | 1.3 | 0.85 | | | 8° |
| | nom | | | | | 0.85 | | | | | | | 1.27 | | | | 0.25 | 0.1 | |
| | min | 0.95 | 0.00 | 0.35 | 3.62 | | 0.19 | 0.24 | 4.45 | | 4.95 | 3.5 | | 5.9 | 0.8 | 0.40 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

*sot1023_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1023 | | | | | | ~~11-12-09~~ 13-03-05 |

**Fig. 6. Package outline LFPAK56; Power-SO8 (SOT1023)**

# 11. Legal information

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|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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## 12. Contents





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**Date of release: 15 April 2015**