TLE9222

TLE9222PX

FlexRay Transceiver

Data Sheet

Rev. 1.0, 2015-06-12

Automotive Power

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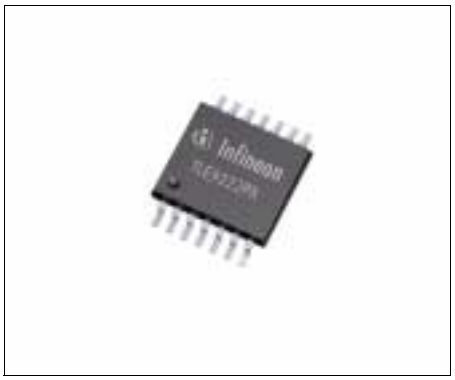
1 Overview



PG-TSSOP-14

Features

- Compliant with the FlexRay Electrical Physical Layer Specification version 3.0.1 and ISO 17458-4
- Optimized for time triggered in-vehicle networks with data transmission rates from 1 Mbit/s up to 10 Mbit/s
- Supports minimum bit times down to 60 ns
- Automatic voltage adaptation on the digital interface pins
- Bus failure protection and error detection
- Very high ESD robustness; ± 8 kV according to IEC61000-4-2
- Optimized for high Electromagnetic Compatibility (EMC); Very low emission and high immunity to interference
- Green Product (RoHS compliant)
- AEC Qualified

Modes of Operation and Wake-up Features

- Low power standby operation mode with very low quiescent current consumption
- Remote wake-up detection via wake-up patterns and a dedicated wake-up frame

Protection and Diagnostic

- Short-circuit protection on the bus pins
- Overtemperature protection
- Undervoltage monitoring of the V_{CC} power supply and the V_{IO} logic voltage level reference
- Error and wake-up indication on the ERRN output
- Status register for detailed diagnostic information through a simplified SPI interface
- Integrated Bus Guardian interface with enhanced safety feedback path
- Bus pins high impedance when device unpowered

Description

The TLE9222 FlexRay transceiver is designed for data transmission rates from 1 Mbit/s up to 10 Mbit/s according to the FlexRay Electrical Physical Layer Specification 3.0.1. The Bus Driver (BD) realizes the physical interface between a FlexRay node and the communication channel. It provides differential transmit and receive capability to the bus, allowing the node bidirectional time-multiplexed binary data stream transfer. In

Type	Package	Marking
TLE9222PX	PG-TSSOP-14	9222

Overview

addition to transmit and receive functions, the TLE9222 provides low power standby operation, supply voltage monitoring (undervoltage detection) as well as bus failure detection and represents an ESD-protection barrier between the bus and the ECU.

The TLE9222 supports the following FlexRay functional classes:

- Functional class “Bus driver - bus guardian interface”
- Functional class “Bus driver logic level adaptation”
- Functional class “Bus driver remote wakeup”
- Functional class “Bus driver increased voltage amplitude transmitter”

In BD_Standby mode the quiescent current is decreased to a minimal level while still being able to detect wake-up requests on the bus.

Fail Safe features, like failure detection and the power supply monitoring, combined with an easy accessible status register support requirements for safety related applications with extended diagnostic features.

The TLE9222 is internally protected against transients on the bus pins, BP and BM. This makes it possible to use the TLE9222 for implementing ECUs without additional external bus protection circuitry while fulfilling ESD and ISO pulse requirements of car manufacturers. With its excellent EMC performance the TLE9222 provides a very high immunity against RF disturbances over a broad frequency range and transmits only a minimal level of electromagnetic emission onto the bus.

The TLE9222 is integrated in a RoHS compliant PG-TSSOP-14 package. Using the latest Infineon Smart Power Technology it is especially tailored to withstand the harsh conditions of the automotive environment and qualification according to the AEC-Q100 standard.

2 Block Diagram

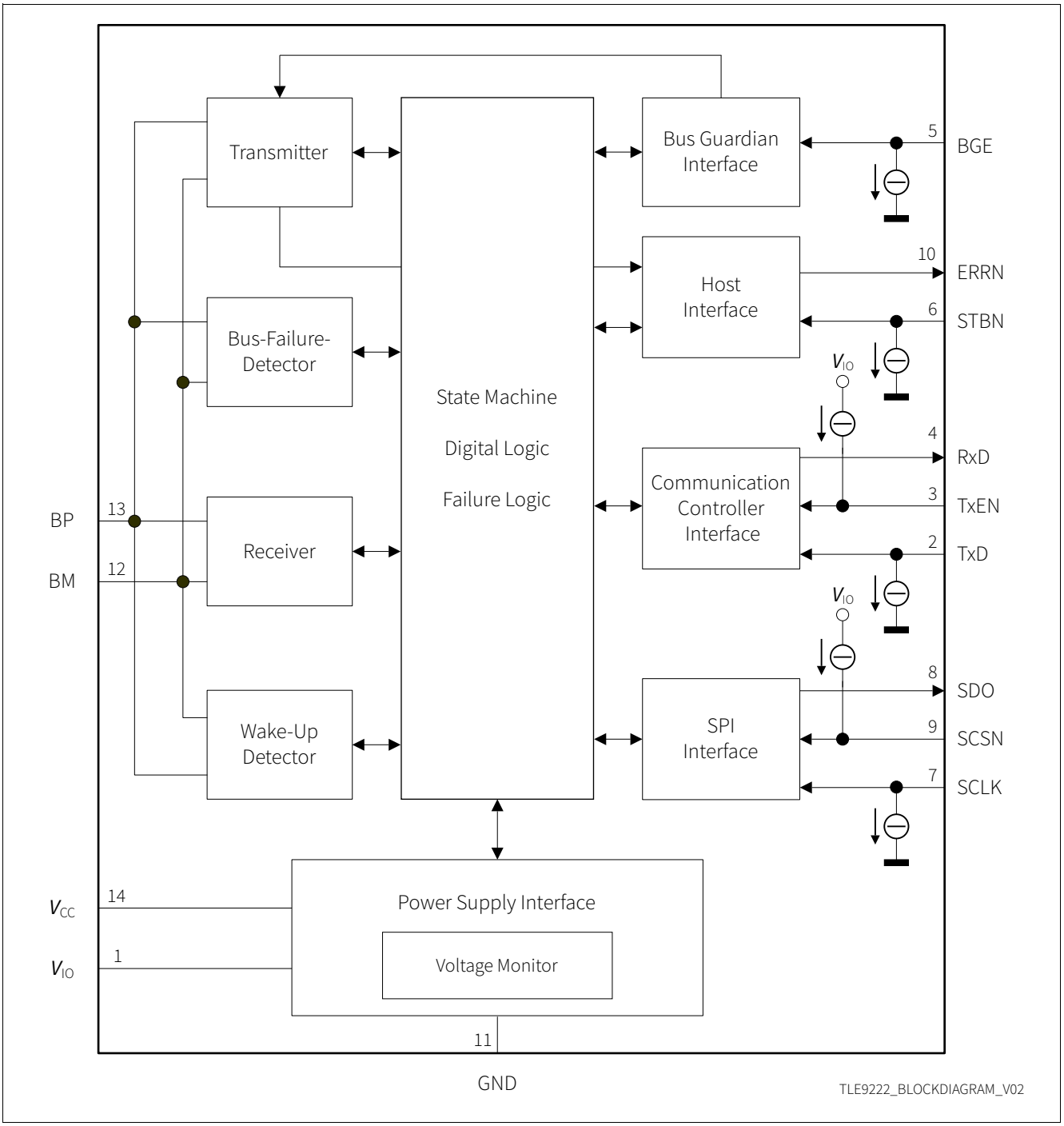


Figure 1 Block diagram

3 Pin Configuration

3.1 Pin Assignment

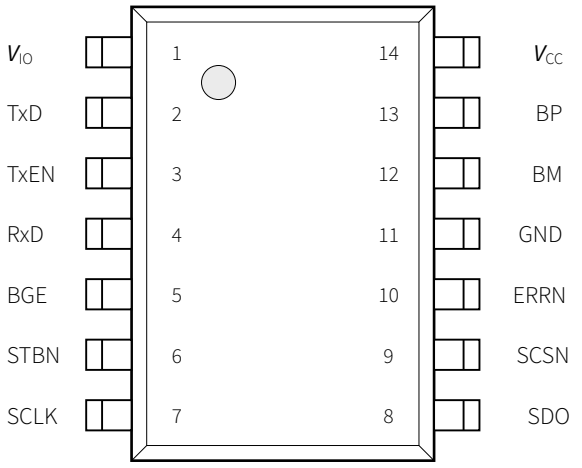


Figure 2 Pin configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	V_{IO}	**Digital Reference Voltage;** Digital reference voltage supply for the logic input and output pins, 100 nF decoupling capacitor to GND recommended.
2	TxD	**Transmit Data Input;** Integrated pull-down to GND.
3	TxEN	**Transmitter Enable Not Input;** Logical “low” to enable the transmitter output stage, Integrated pull-up to V_{IO}.
4	RxD	**Receive Data Output;** Output voltage level adapted to the voltage level of V_{IO}.
5	BGE	**Bus Guardian Enable Input;** Logical “high” to enable the transceiver output stage, Integrated pull-down to GND.
6	STBN	**Standby Not Mode Control Input;** Digital input for mode selection, logical “high” for BD_Normal mode, Integrated pull-down to GND.
7	SCLK	**SPI Clock Input;** Integrated pull-down to GND.

Pin Configuration

Pin	Symbol	Function
8	SDO	**SPI Data Output;**
9	SCSN	**SPI Chip Select Not Input;** Integrated pull-up to V_{IO}.
10	ERRN	**Error Not Diagnosis Output;** Logical “low“ in failure cases or when wake-up pattern detected.
11	GND	**Ground;**
12	BM	**Bus Line Minus;** Negative input / output terminal of the FlexRay bus.
13	BP	**Bus Line Plus;** Positive input / output terminal of the FlexRay bus.
14	V_{CC}	**Supply Voltage;** Transceiver 5V supply voltage, 100 nF decoupling capacitors to GND recommended.

4 Functional Description

The TLE9222 realizes the physical interface between the FlexRay node and the communication channel. Differential transmit and receive capability to the FlexRay bus is provided, allowing the node bidirectional time multiplexed binary data stream transfer.

The differential bus voltage is measured between two signal lines, denoted BP (Bus Plus) and BM (Bus Minus), defined as *uBUS* = *uBP* - *uBM*. Three different bus states are defined for the FlexRay bus; Idle, Data_0 and Data_1. For the Idle state no differential voltage is driven to BP or to BM. The common mode bus biasing level will depend on the operation mode of all nodes on the bus. For the Data_1 state a positive differential voltage is driven between BP and BM, whereas for the Data_0 state a negative differential voltage is driven between BP and BM.

4.1 Operation Modes

The TLE9222 supports two functional operation modes, BD_Normal mode and BD_Standby mode. In addition, the BD_Off condition describes the behavior of the TLE9222 when unsupplied.

Mode transitions of the TLE9222 are triggered by host commands, undervoltage events and during power-up / -down, see **Figure 3** and **Table 1**.

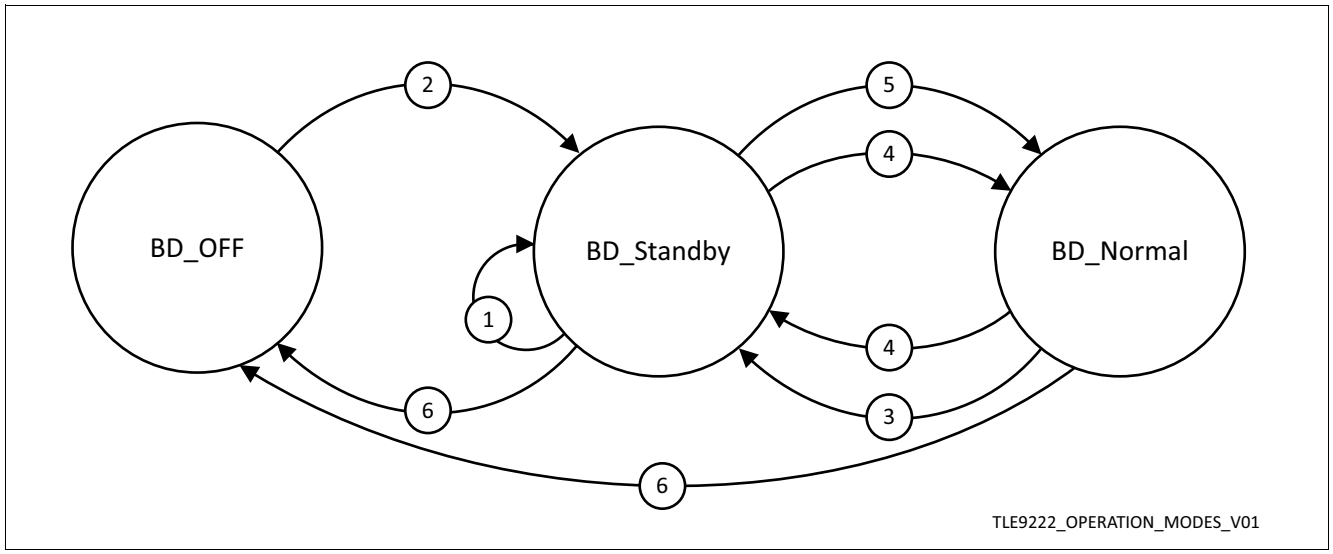


Figure 3 Operation mode state diagram

Table 1 Operation mode transitions

Nr	Reason for transition	Comment
1	Wake-up detection	–
2	Power-on detection	Supply voltage sufficiently supplied via V_{CC} after being unpowered.
3	Undervoltage detection	After V_{CC} and / or V_{IO} undervoltage detection, BD_Standby mode is forced.
4	Host command	Triggered by host command.
5	Undervoltage recovery	Undervoltage recovery while host command requests BD_Normal mode.
6	Power-off	Supply voltage falls below the power-on threshold.

4.1.1 BD_Normal Mode

In BD_Normal mode all interfaces and functions of the TLE9222 are in operating condition. The communication controller interface is fully active; the RxD output reflects the data on the bus pins, the TxD drives the data to the transmitter and the TxEN input enables or disables the transmitter. When the transmitter is activated, fail safe functionality like the transmitter time-out, overtemperature detection and bus error detection are also enabled. The bus biasing is connected to V_{CC} / 2 via the internal common mode resistors. With the RxEN flag in the status register the bus states idle or active can be read out through the SPI interface.

The host interface is active and fully functional, as well as status register read-out on the SPI interface. Through the bus guardian interface, the transmitter can be activated or disabled.

The wake-up detector is active, but received wake-up information is not flagged while in BD_Normal mode.

The power supply interface including voltage monitor on both V_{CC} and V_{IO} is active. Undervoltage events are signalled on the ERRN output and in the status register, and trigger a mode transition to BD_Standby mode. BD_Normal mode can only be entered with a valid host command while both power supplies are within their operational range.

4.1.2 BD_Standby Mode

After power-up the TLE9222 automatically enters BD_Standby, an idle mode with optimized low power consumption. In BD_Standby mode neither sending nor receiving data is possible, both the transmitter and the receiver are disabled. The bus biasing is connected to GND through the internal common mode resistors.

The communication controller interface is inactive. The TxD and the TxEN inputs are not functional. The RxD output is used for signalling wake-up or error information, depending on the host command. The host interface is active and fully functional, as well as status register read-out on the SPI interface.

The bus guardian interface is inactive and detection of bus transmission through the RxEN flag in the status register is not possible. The bus failure detector is not active, no bus failure can be detected.

The wake-up detector is active and signals wake-up requests on the ERRN and RxD outputs while the host command is BD_Standby mode.

The power supply interface with voltage monitoring on both V_{CC} and V_{IO} is active. If the TLE9222 is forced to BD_Standby mode because of undervoltage events while the host command is BD_Normal mode, this is signalled on the ERRN output. Additionally, the information is stored in the status register.

4.1.3 BD_Off Condition

The TLE9222 enters the BD_Off condition when the V_{CC} power supply drops below the $uBDPDV_{CC}$ power-on-reset threshold. In this state the transmitter and the receiver are turned off, the wake-up function is not operational, the RxD and ERRN outputs are “low” and the SDO output is in high impedance state. If the V_{IO} reference supply is available, the logical inputs are set to their default states as given in **Table 2**.

Table 2 Logic inputs when unconnected / default states

Input Signal	Default State
TxD	Low
TxEN	High
STBN	Low
BGE	Low

Table 2 Logic inputs when unconnected / default states

Input Signal	Default State
SCSN	High
SCLK	Low

4.2 Communication Controller Interface

The communication controller interface is the link between the TLE9222 and the FlexRay communication controller, comprising three digital signals:

- TxEN (Transmit Data Enable Not) input
- TxD (Transmit Data) input
- RxD (Receive Data) output

The logical I/O levels of all three digital pins are adapted to the V_{IO} digital reference voltage supply.

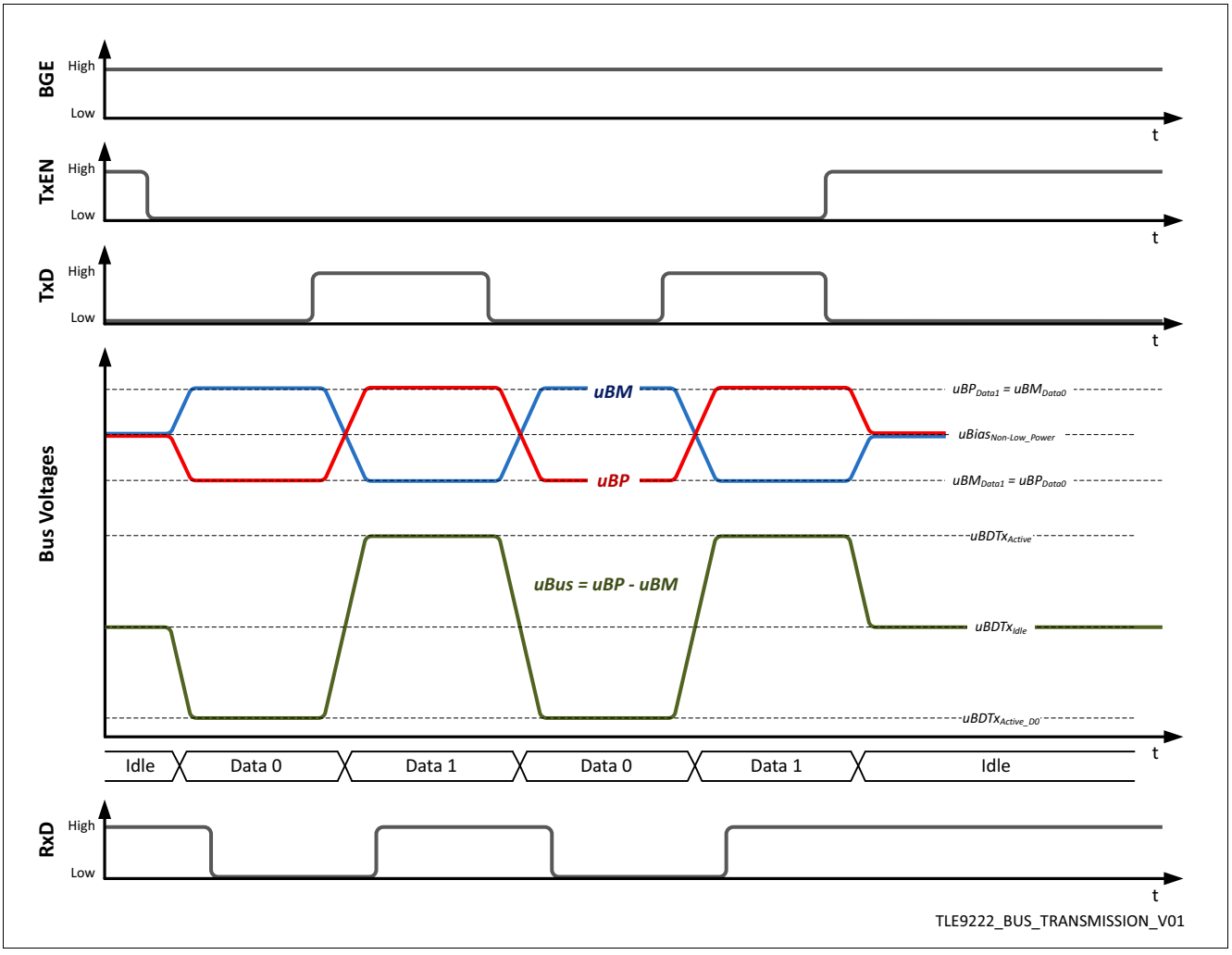


Figure 4 FlexRay physical layer bus signals

The communication controller interface drives the serial digital data stream available on the TxD input to the FlexRay bus via the transmitter. Simultaneously the receiver of the TLE9222 monitors the data on the FlexRay bus and transfers the data to a serial digital data stream back to the RxD output. A logical “low” signal on the

TxD input drives a Data_0 signal on the FlexRay bus; a Data_0 signal on the FlexRay bus results in a logical “low” signal on the RxD output. Vice versa a logical “high” on TxD drives a Data_1 signal on the FlexRay bus and results in a logical “high” signal on the RxD output. The RxD output is also used to signal wake-up events while the transceiver is in BD_Standby mode.

The TxEN input is only functional in BD_Normal mode and requires a transition from “high” to “low” for initiating bus transmissions. After TxEN has been set “low” while the BGE input is “high”, a “low” level on the TxD input enables the transmitter.

For avoiding unintentional blocking of the FlexRay bus in case of failures, the transmitter is protected with a time-out function. In case a time-out occurs, the transmitter will automatically be disabled and the error will be signalled by the ERRN output and in the status register. A more detailed description of this fail safe function is given in **Chapter 4.7.3**.

4.3 Bus Guardian Interface

The bus guardian interface allows an external supervision device to immediate interrupt any bus transmission of the TLE9222. A logical “low” signal on the BGE input disables the transmitter of the TLE9222 while operating in BD_Normal mode, regardless of the signals on the TxD and TxEN inputs.

For increasing the ECU system safety level, an enhanced redundant feedback path has been implemented for the bus guardian interface. A monitoring circuit directly at the transmitter output stages provides reliable feedback by setting the ERRN output “low” and indication with the BGE flag in the status register after the transmitter has been disabled through the Bus Guardian interface.

The logical I/O level of the BGE input is adapted to the digital reference voltage level uV_{IO}. Together with the TxEN input, the BGE input is monitored for the transmitter time-out function (see **Chapter 4.7.3**).

Additionally, the status register includes the RxEN (Receive Enable NOT) flag that indicates activity (Data_0 or Data_1) on the FlexRay bus. This detection is only active in BD_Normal Mode. The RxEN bit can be read out with the SPI Interface as described in **Chapter 4.8**.

4.4 Host Interface

The host interface enables the host to control the operation mode of the TLE9222 and to flag status information. The host interface is implemented using *hard wired signals, Option A* according to the FlexRay EPL Spec. 3.0.1.

Table 3 Host Command

STBN	Resulting operation mode
High	BD_Normal
Low	BD_Standby

The STBN (Standby Not) input controls the operation mode of the TLE9222. Unless the TLE9222 is being forced to BD_Standby mode because of undervoltage events, the host command will set operation mode as given in **Table 3**. Mode change by host command is completed within the time $dBD_{ModeChange}$ after the host command is applied. Voltage spikes on the STBN input that are shorter than $dBDLogic_{Filter}$ are filtered out and ignored.

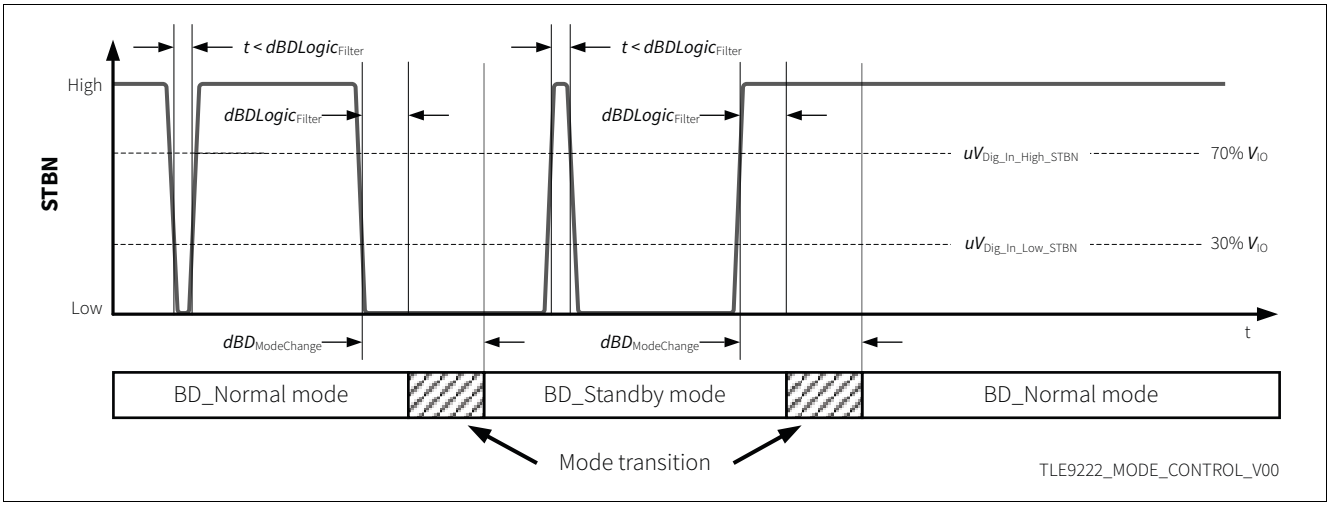


Figure 5 Mode control with the STBN input

The ERRN output is used to signal events detected by the TLE9222 to the host controller. Depending on the provided host command, the ERRN output indicates errors or wake-up events, see **Table 4**. The TLE9222 reacts on and signals these events on the ERRN output within the time $dReactionTime_{ERRN}$. Detailed information about the detected events as given in **Table 4** can be read out from the status register with the SPI interface as described in **Chapter 4.8**.

Table 4 Signalling on the ERRN and RxD pins

STBN	ERRN	RxD	Cause / Comment	Effect
BD_Normal mode				
High	High	High / Low[1)]	Default condition for BD_Normal mode	–
High	Low	High / Low[1)]	Bus error detected	–
			Transmitter time-out detected	Transmitter disabled
			Overtemperature event detected	Transmitter disabled
			BGE input “low”	Transmitter disabled
			SPI error detected	–
BD_Standby mode				
Low	High	High	Default condition for BD_Standby mode	–
Low	Low	Low	Bus wake-up detected	–
High	Low	High	V_{CC} undervoltage detected	Forced BD_Standby mode
X[2)]	Low	Low	V_{IO} undervoltage detected	Forced BD_Standby mode, logic inputs follow default states (see **Table 2**) SDO “high impedance”
BD_OFF condition				
X[2)]	Low	Low	uV_{CC} below $uBDPDV_{CC}$	–

1) Depending on bus state; RxD “low” when Data_0 is detected, RxD “high” when Data_1 is detected or when bus is Idle

2) X = “Don’t care”

A “low” output level on the ERRN pin is latched. To reset the ERRN event and the status register either a correct read-out of the status register or a mode change by the host command is required, given that the error condition has been resolved.

4.5 Power Supply Interface

The TLE9222 is powered by the V_{CC} pin which shall be connected to a voltage supply with nominal 5 V. Additionally, the TLE9222 provides the V_{IO} reference voltage pin for all digital inputs and outputs. The voltages at the V_{CC} and V_{IO} pins are monitored for detection of undervoltage events.

4.5.1 V_{CC} Undervoltage Detection

The TLE9222 detects undervoltage events on the V_{CC} pin if the voltage uV_{CC} falls below the undervoltage detection threshold $uBDUVV_{CC}$ for a time $t > dBDUVV_{CC\_blk}$. Upon detection the V_{CC}-undervoltage flag and the error flag are set. In case the TLE9222 is in BD_Normal mode, the transmitter will be disabled and the ERRN output will go “low” after the time $dReactionTime_{ERRN}$. After the time $dBDUVV_{CC}$ the TLE9222 will force a transition to BD_Standby, regardless of the host command (see **Figure 6**).

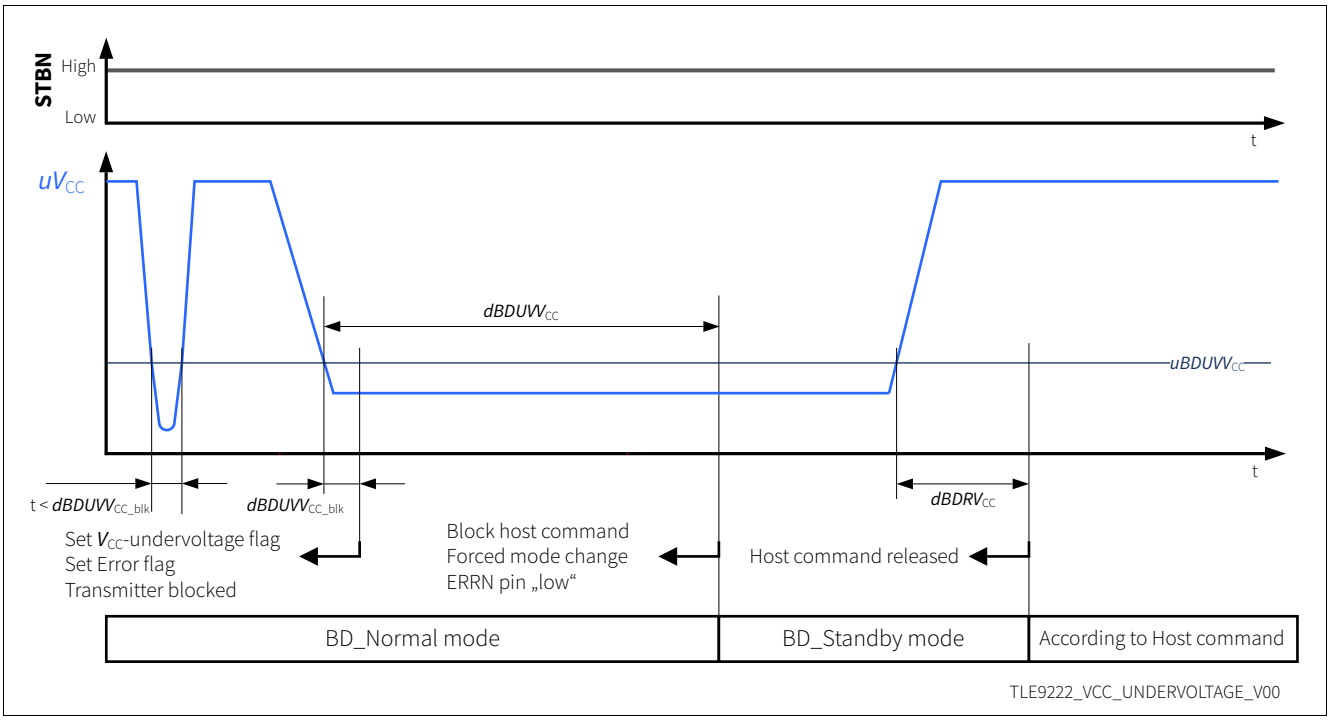


Figure 6 V_{CC} undervoltage detection

The TLE9222 recovers from a V_{CC} undervoltage event after the time $t > dBDRV_{CC}$ following the voltage uV_{CC} rise above the undervoltage detection threshold $uBDUVV_{CC}$. This will release the host command and change operation mode accordingly.

4.5.2 V_{IO} Undervoltage Detection

The V_{IO} undervoltage detection is similar to that on the V_{CC} supply. Undervoltage events on the V_{IO} pin are detected if the voltage uV_{IO} falls below the undervoltage detection threshold uUV_{IO} for a time $t > dBDUVV_{IO\_blk}$. Upon detection the V_{IO}-undervoltage flag and the error flag are set. While an undervoltage event is present on the V_{IO} pin, the reference threshold levels of all digital input and output pins are invalid. Therefore, the

TLE9222 blocks the host interface, communication controller interface, SPI interface and the bus guardian interface. The digital outputs RxD and ERRN are set “low” and all digital input pins follow their default levels (see **Table 2**). The SDO output is set to high impedance state. After the time $dBDUVV_{IO}$ the TLE9222 will force a transition to BD_Standby mode.

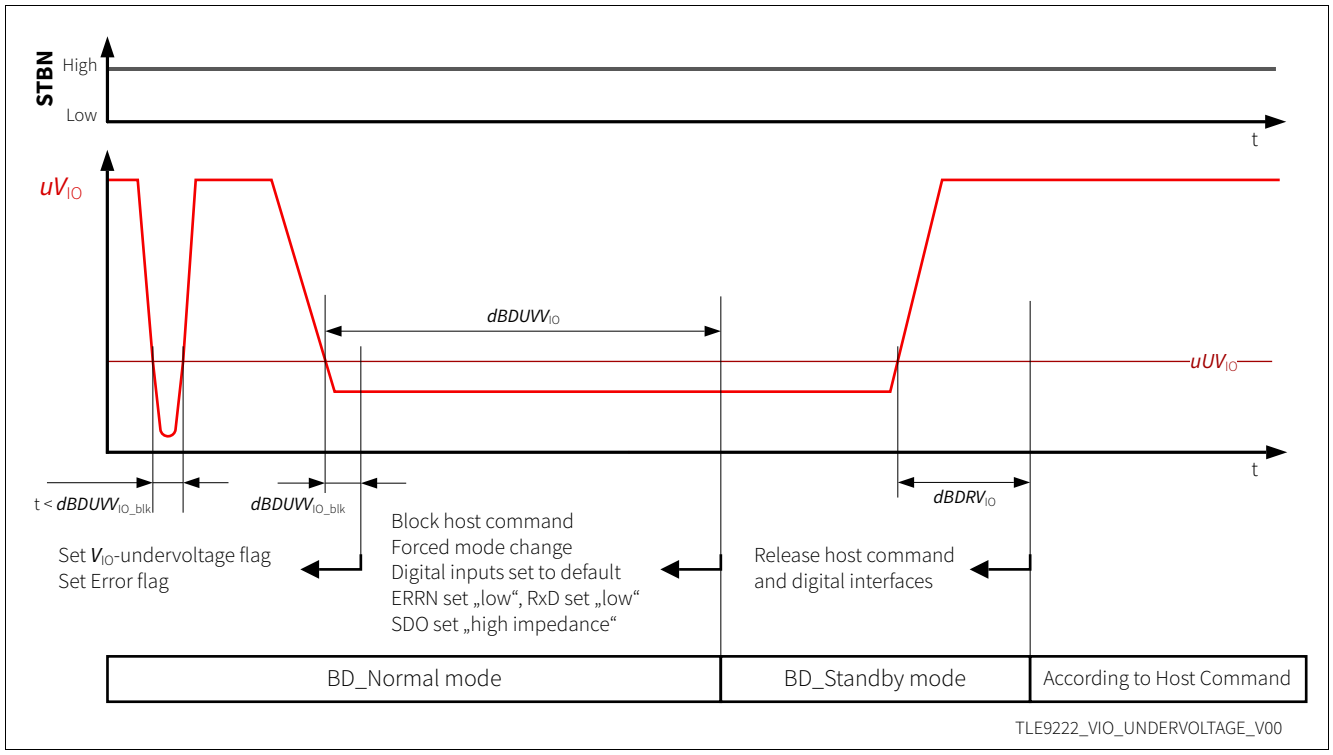


Figure 7 V_{IO} undervoltage detection

The TLE9222 will recover from a V_{IO} undervoltage event after the time $t > dBDRV_{IO}$ following the voltage uV_{IO} rise above the undervoltage detection threshold uUV_{IO}. This will release the SPI interface and host command, and change mode accordingly (see **Figure 7**).

4.5.3 Power-up and Power-down

The TLE9222 will remain in BD_Off condition as long as the voltage on the V_{CC} supply pin, uV_{CC}, is below the power-down threshold $uBDPDV_{CC}$. When uV_{CC} is ramped up higher than $uBDPDV_{CC}$ the TLE9222 powers up and begins initialization of the BD_Standby mode within the time dBD_{Power}. After both voltages uV_{CC} and uV_{IO} have risen above their respective undervoltage detection thresholds ($uBDUVV_{CC}$ and uUV_{IO}, respectively), the digital interfaces will be released and the full functionality of the device will be available. The power-on event can be identified with the corresponding flag in the status register and mode change according to the host command will then be initiated (see **Figure 8**).

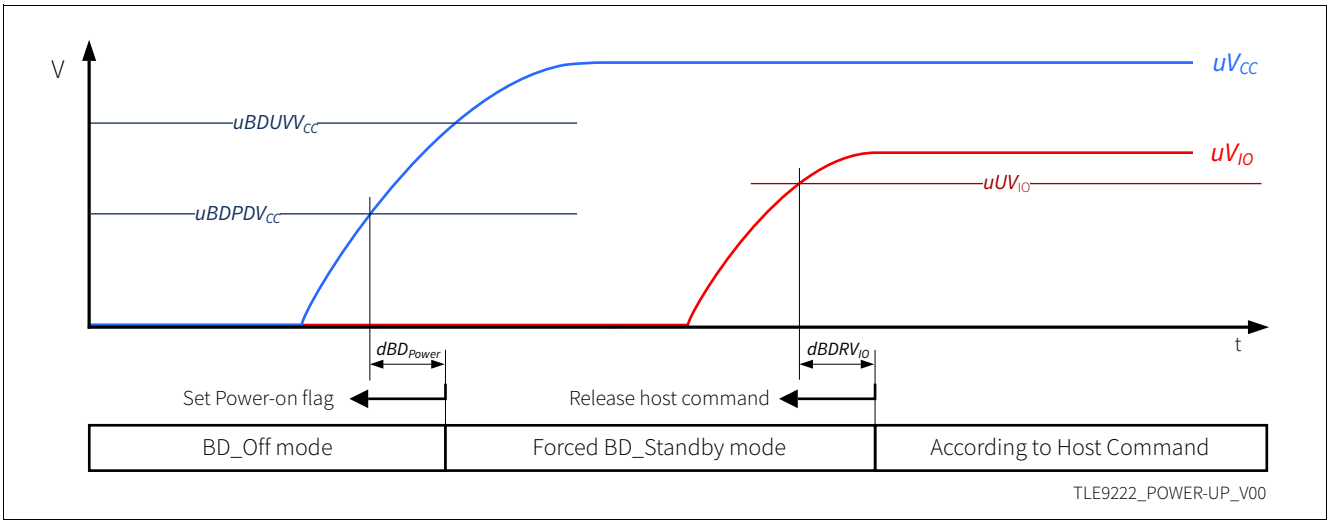


Figure 8 Power-up behavior

The power-down sequence of the TLE9222 is shown in **Figure 9**. As the voltage at the V_{CC} supply pin, uV_{CC}, falls below the undervoltage threshold the V_{CC}-undervoltage flag and the error flag are set. After the detection time for V_{CC} undervoltage $dBDUVV_{CC}$ the TLE9222 blocks the host command and automatically enters BD_Standby mode.

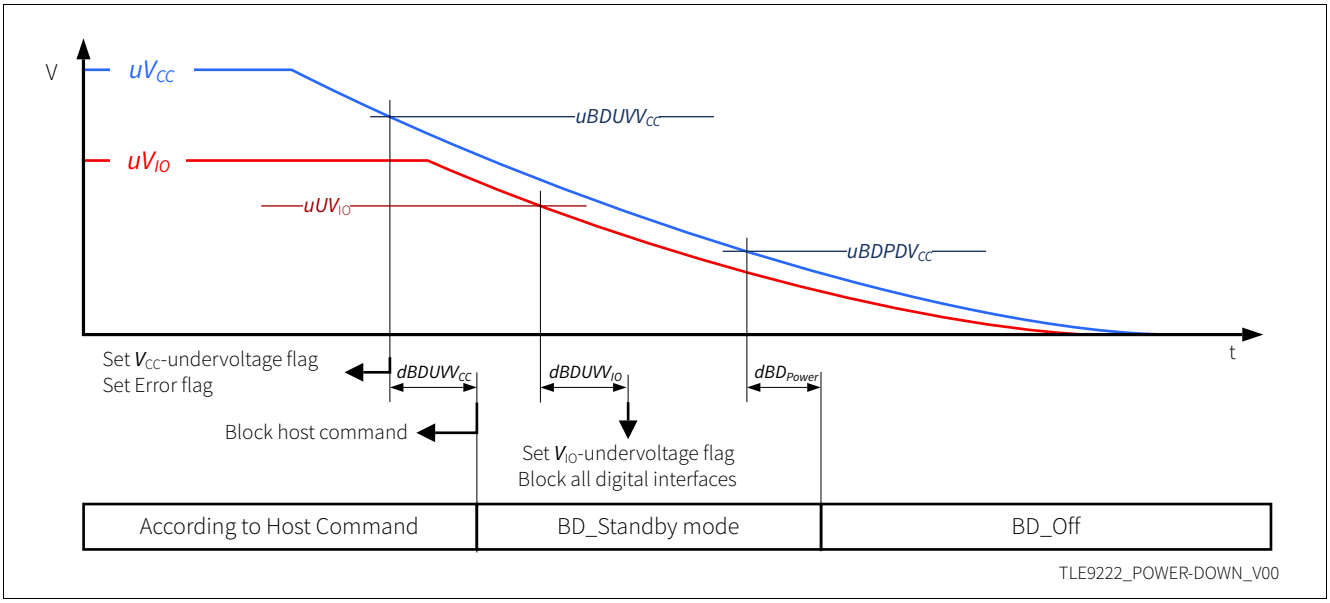


Figure 9 Power-down behavior

While the TLE9222 is being powered down, the behavior on the digital interface level shift reference pin V_{IO} is very similar to the V_{CC} supply pin. As uV_{IO} falls below the undervoltage threshold the undervoltage timer is started and the V_{IO}-undervoltage flag is set. If V_{CC} is not already in undervoltage condition, the error flag is also set. After the detection time for V_{IO} undervoltage, $dBDUVV_{IO}$, the TLE9222 blocks the host command (if not already blocked because of V_{CC} undervoltage) and all digital interfaces and enters BD_Standby mode.

When the voltage at the V_{CC} supply pin, uV_{CC}, falls below the power-on threshold $uBDPDV_{CC}$ the TLE9222 enters BD_Off condition within the time dBD_{Power}.

4.6 Remote Wake-up

The TLE9222 detects and signals a remote wake-up request after correct reception of a bus wake-up pattern or wake-up payload in a FlexRay data frame while operating in BD_Standby mode. When the valid wake-up pattern or wake-up payload is detected, the TLE9222 signals the request with the remote wake-up flag in the status register and on the RxD and ERRN outputs within the time $dBDWakeupReaction_{Remote}$.

The wake-up detector is also active in BD_Normal mode, but wake-up requests are only flagged when the TLE9222 is in BD_Standby mode.

4.6.1 Bus Wake-up Patterns

A wake-up pattern consists of at least two wake-up symbols. A wake-up symbol on the FlexRay bus is defined as either a phase of Data_0 followed by a phase of Idle, or alternatively as a phase of Data_0 followed by a phase of Data_1. A valid remote wake-up event is detected with the reception of at least two consecutive wake-up symbols on the bus within the time $dWU_{Timeout}$ (see **Figure 10** and **Figure 11**).

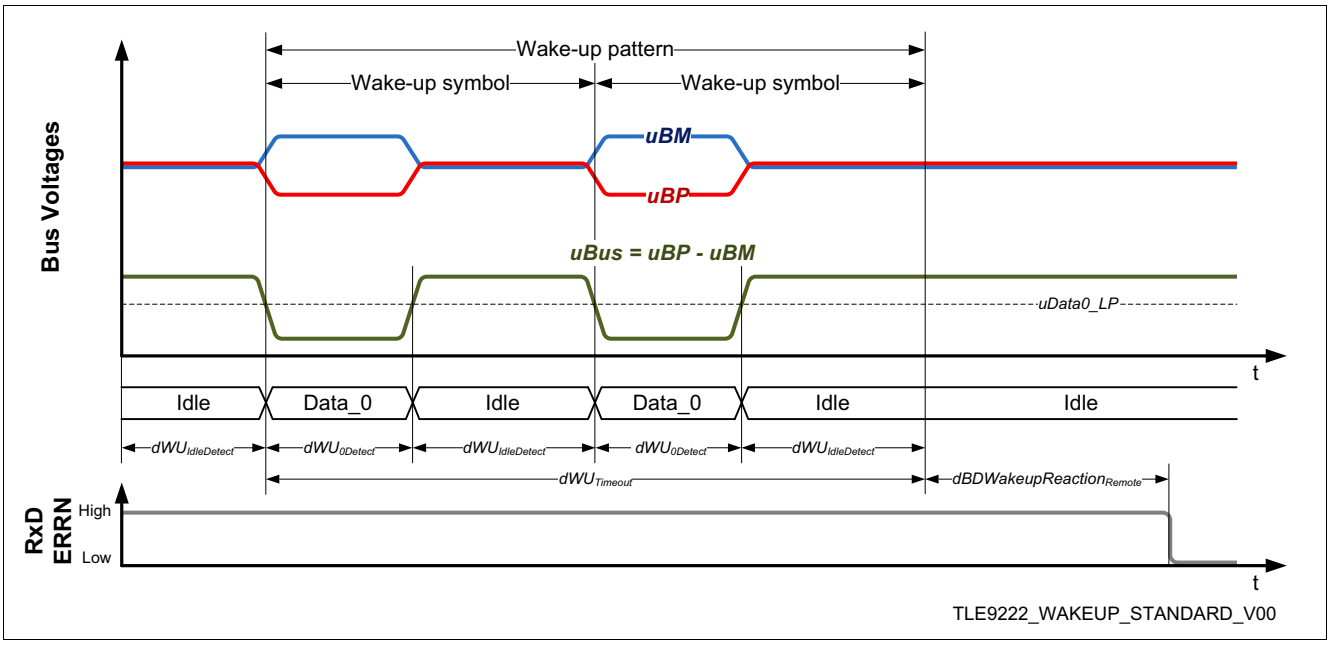


Figure 10 Standard wake-up pattern

The Data_0 phases have to be longer than the time $dWU_{0Detect}$ while the Idle or Data_1 (alternative wake-up pattern) phases have to be longer than the time $dWU_{IdleDetect}$. The TLE9222 detects and signals both the standard and the alternative wake-up patterns without any behavioral differences.

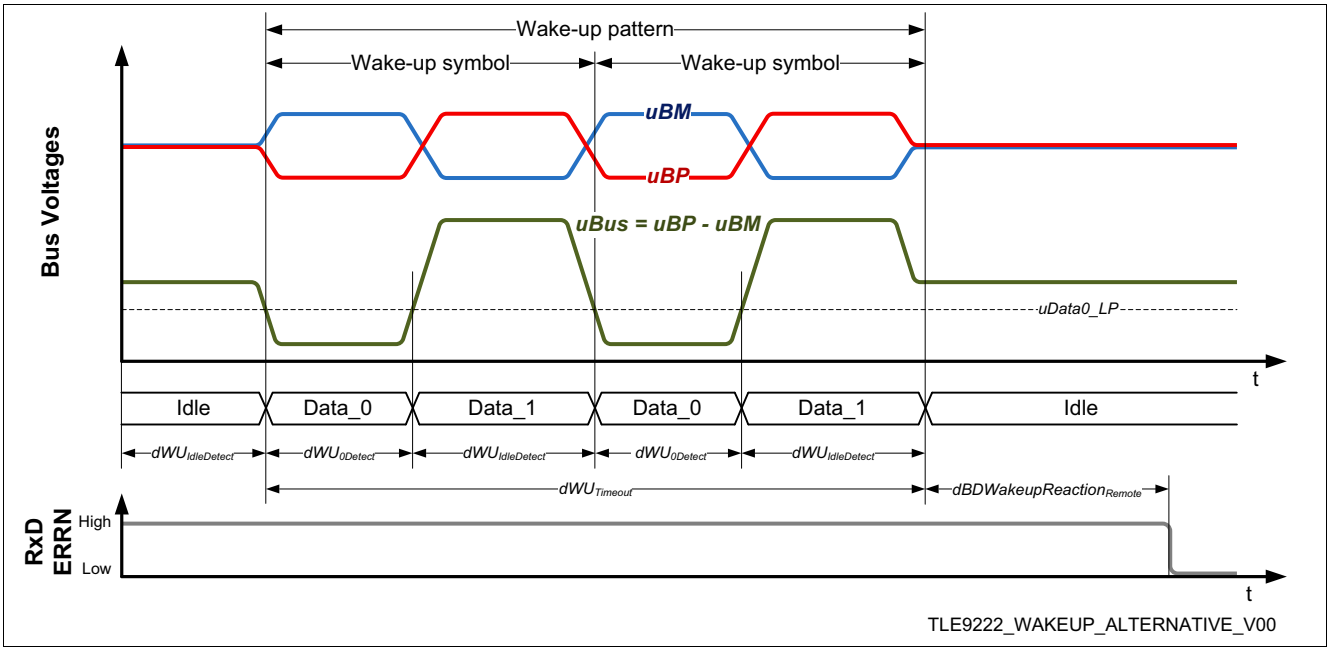


Figure 11 Alternative wake-up pattern

4.6.2 Wake-up by Payload

In addition to wake-up detection by wake-up patterns, the TLE9222 also supports wake-up requests by a specific payload within the data field of a FlexRay communication frame with data transmission rate of 10 Mbit/s.

A dedicated Byte Start Sequence (BSS) is transmitted before each byte of the payload within the FlexRay data frame. The BSS consists of one “high” bit followed by one “low” bit. For transmitting a “Data_0” byte on the FlexRay bus, the FlexRay controller sends 10 bits, the “high” bit and the “low” bit as part of the BSS followed by the eight “low” data bits (HL= BSS; LLLLLLLL= “Data_0”). For sending a “Data_1” byte the FlexRay controller sends the “high” bit and the “low” bit, followed by the eight consecutive “high” data bits (HL = BSS; HHHHHHHH = “Data_1”) (see **Figure 12**).

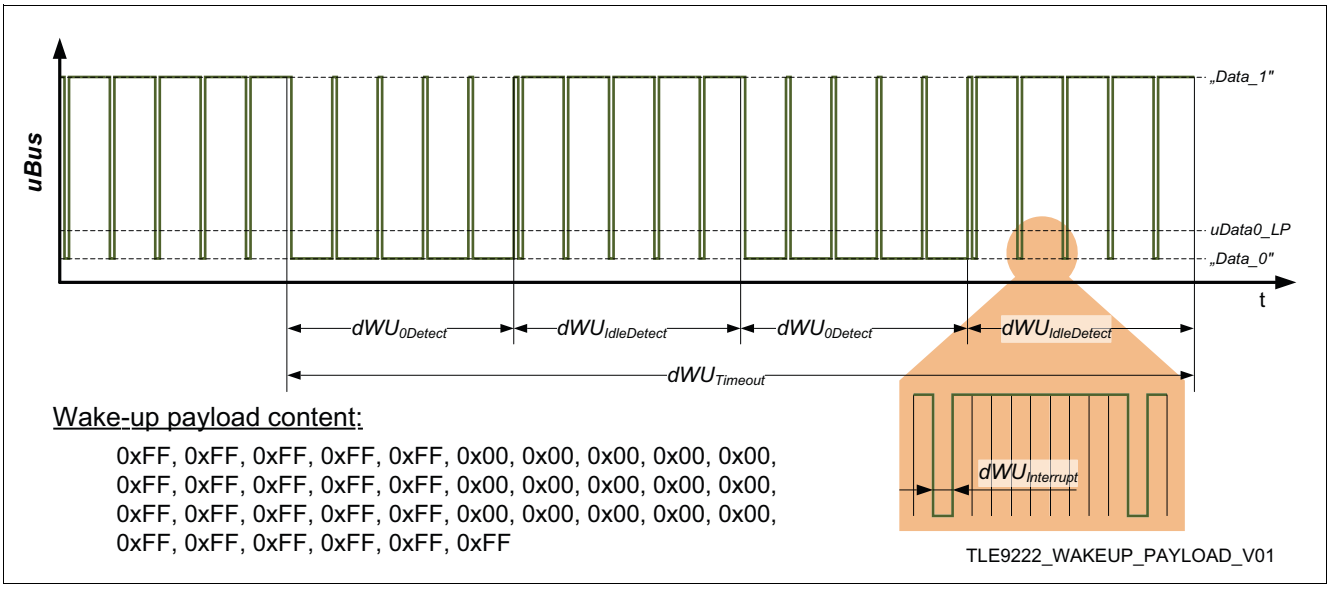


Figure 12 Wake-up by payload

4.7 Fail Safe Functions and Flags

In addition to power supply undervoltage detection, the TLE9222 provides several functions for detection of local or remote failures with corresponding status flags. These errors are signalled with the ERRN output and can be read out from the status register. When local errors are detected, the TLE9222 initiates fail safe procedures for device self protection and prevention of communication channel interruption.

4.7.1 Overtemperature detection

The transmitter of the TLE9222 is protected against overtemperature events when active in BD_Normal mode. If the junction temperature rises above the $T_{J(warning)}$ threshold the temperature-warning flag in the status register is set. If the junction temperature continues to rise and exceeds the $T_{J(Shut\_Down)}$ threshold, the transmitter will be disabled and the overtemperature event will be flagged by the temperature-high flag in the status register and signalled with the ERRN output.

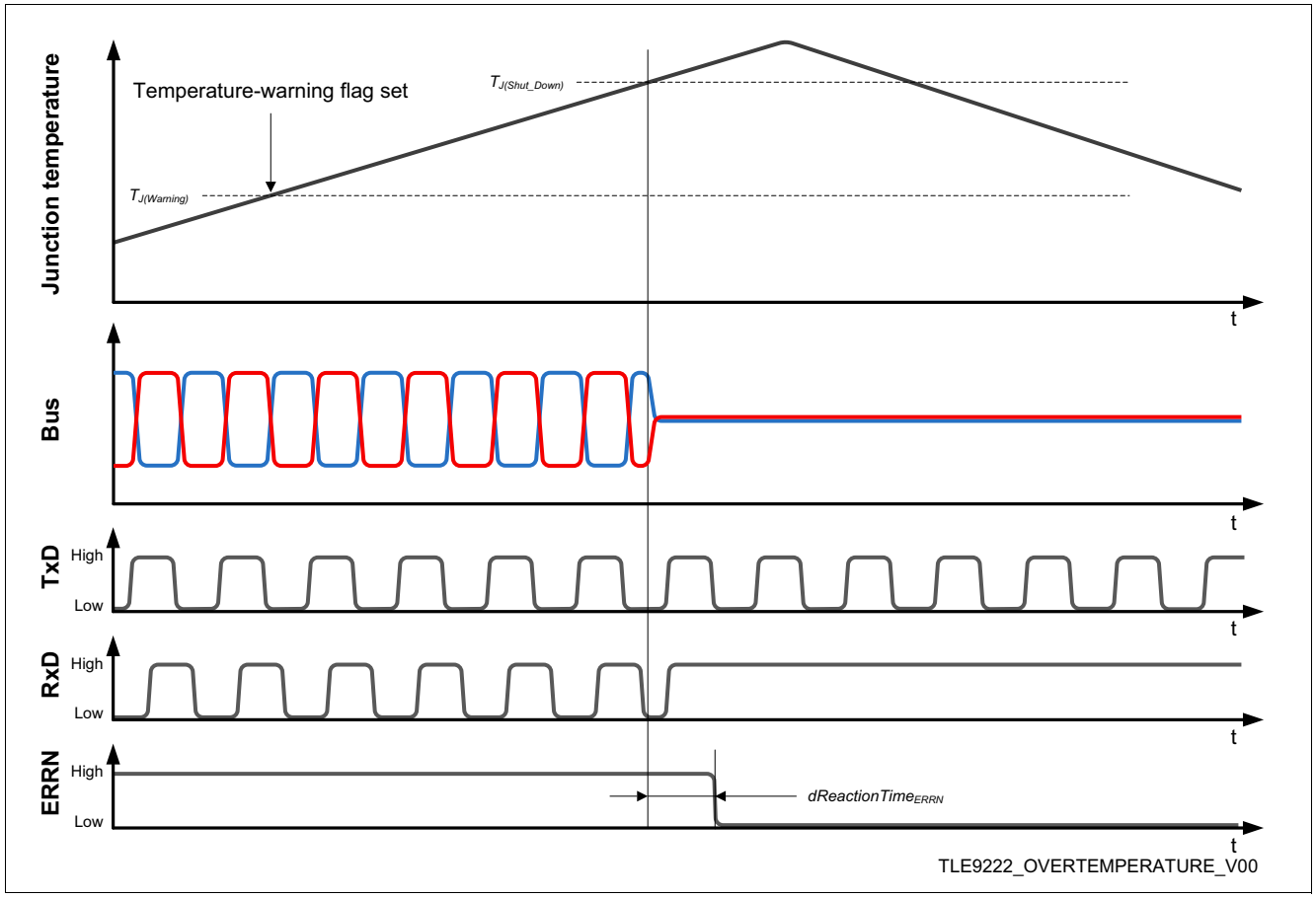


Figure 13 Overtemperature protection

4.7.2 Bus Error Detector

The bus error detector monitors the FlexRay bus for identifying external failures which may lead to corrupt data transmission and reception. With the RxD-TxD compare function and the bus overcurrent monitoring, bus errors are detected and signalled with the bus error flag. The bus error detector is only enabled in BD_Normal mode while the transmitter is active.

4.7.2.1 RxD-TxD Compare

When the TLE9222 transmits data on the bus (TxEN “low” and BGE “high”), the digital input data on TxD is compared with the received data on the RxD output. If the data is not identical, a failure condition is identified.

Both the positive and the negative edges on the TxD input signal triggers an internal comparator to compare the TxD signal with the RxD signal. The results are stored in an internal error counter. When the internal error counter exceeds 10 reported comparison failures, the bus error flag will be set. The error counter is reset when the transmitter is deactivated.

4.7.2.2 Bus Overcurrent

The BP and BM bus pins have implemented current sensors for detection of overcurrent conditions in the direction in or out of the pins. Detection of overcurrent is the typical signature of a short circuit of one of the bus lines to the ground or a supply line.

4.7.3 Transmitter Time-Out

For avoiding unintentional blocking of the FlexRay bus in case of e.g. a malfunctioning microcontroller or short circuits on the PCB, the transmitter is protected with a time-out function. When the transmitter is activated for bus transmission while in BD_Normal mode, with a “low” signal on TxEN and “high” on BGE, a timer is started. In case a time-out occurs, the transmitter will automatically be disabled and the failure will be signaled on the ERRN output and in the status register.

The transmitter timer is reset when the transmitter is deactivated with either TxEN or BGE.

4.7.4 V_{IO} Undervoltage-flag

During V_{IO} undervoltage events, the SPI register is blocked and can not be read out. After undervoltage recovery, depending on host command and the status of other register flags, the V_{IO}-undervoltage flag may or may not be set. Please refer to **Chapter 4.7.6**.

4.7.5 SPI-error flag

The SPI-error flag is used for indication of incorrect SPI read-out procedure, please find detailed description in **Chapter 4.8.1**.

4.7.6 Error flag

If any local errors or bus errors are detected, the respective bit in the status register is flagged together with the error flag (bit 12). If the error flag is set, but no other error contributing flags in the status register set, then this indicates that a V_{IO} undervoltage event has occurred in the past but recovery has already taken place.

While the error flag is set and the host command on the STBN input is “high”, the ERRN output is “low”.

4.7.7 Mode Flags

The mode flag in the status register indicates the current operating mode of the TLE9222, regardless of the applied host command. If the TLE9222 is in BD_Standby mode, bit 1 will be “low”. If the current operation mode is BD_Normal, bit 1 will be “high”. The mode flag will only toggle during an operation mode change, i.e. not be reset by SPI register read-out. The mode indication can be beneficial for the host when the TLE9222 is forced to a different mode than requested with the host command during V_{CC} undervoltage events.

4.8 SPI Interface and Status Register

The TLE9222 has a 16-bit SPI interface for reading out the internal status register. The bits in the register reflects detailed flags regarding external events such as wake-up and power-on recognition, detection of errors / warnings and operation mode indication, see **Table 5**.

Table 5 Bit definition of the status register

Bit	Name	Indication	Comment
Bit 0	Remote wake-up flag	“Low”: Remote wake-up detected	–
		“High”: –	–
Bit 1	Mode flag	”Low”: BD_Standby mode	–
		“High”: BD_Normal mode	–
Bit 2	BGE flag	“Low”: Transmitter disabled by Bus Guardian, BGE input “low” in BD_Normal mode	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 3	RxEN flag	“Low”: Bus activity ongoing	Not latched
		“High”: Bus idle	–
Bit 4	Power-on flag	“Low”: Power-on detected	–
		“High”: –	–
Bit 5	Bus-error flag	“Low”: Bus error detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 6	Temperature-high flag	“Low”: Overtemperature detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 7	Transmitter time-out flag	“Low”: Transmitter activation time-out	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 8	V_{CC}-undervoltage flag	“Low”: V_{CC} Undervoltage detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 9	V_{IO}-undervoltage flag	“Low”: V_{IO} Undervoltage detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 10	SPI-error flag	“Low”: SPI error detected	Error, will trigger Bit 12 → “low”
		“High”: –	–
Bit 11	Temperature-warning flag	“Low”: High temperature warning	–
		“High”: –	–
Bit 12	Error flag	“Low”: Error(s) detected	Error, will trigger ERRN output “low” if signal on STBN is “high”
		“High”: No errors detected	–
Bit 13	Reserved	Always ”High”	–
Bit 14	Reserved	Always “Low”	–
Bit 15	Even parity bit	“Low”: Odd parity of Bit 0 to Bit 14	–
		“High”: Even parity of Bit 0 to Bit 14	–

All the flags in the status register are “active low”, the default level is “high”.

The RxEN flag indicates ongoing bus transmission. As soon as the bus state returns to idle, this flag is set “high”.

The wake-up, power-on and error flags and their corresponding status register bits are latched “low”. A mode change by host command or a correct SPI status bit register read-out will reset these flags, given that the error condition has been resolved.

4.8.1 Read-out procedure

The SPI interface of the TLE9222 is enabled by the SCSN (SPI Chip Select Not) input. While SCSN is “high”, the SDO (SPI Data Output) output is in a high impedance state and clock signals on the SCLK input are ignored. The read-out procedure is initiated with a “low” signal on SCSN, which will cause the SDO output to be set “low” (see **Figure 13**). After the time $dSPI_{Lead}$ the status register data can be shifted out on the SDO output synchronized with the rising edge of a clock signal on the SCLK input. With a clock signal period of $dSPI_{Clk}$, the TLE9222 supports SPI data rates in the range 10 kbit/s to 4 Mbit/sIf a transition on SCSN from “high” to “low” is detected while SCLK is “high”, this would be identified as a SPI error.

Within the SCSN period, the time $dSPI_{SCSN\_Low}$ while the signal on SCSN is “low”, exactly 16 clock cycles are expected for a correct read-out procedure. Incorrect SPI access, with more or less than 16 SCLK cycles or wrong timing, is protected by the SPI timer. If the read-out time $dSPI_{SCSN\_Low}$ expires, the SDO output is set to “high impedance” within the time $dSPI_{SDOZ}$. Additionally the error flag and SPI-error flag in the status register will be set, while the state of all other latched bits are left unchanged.

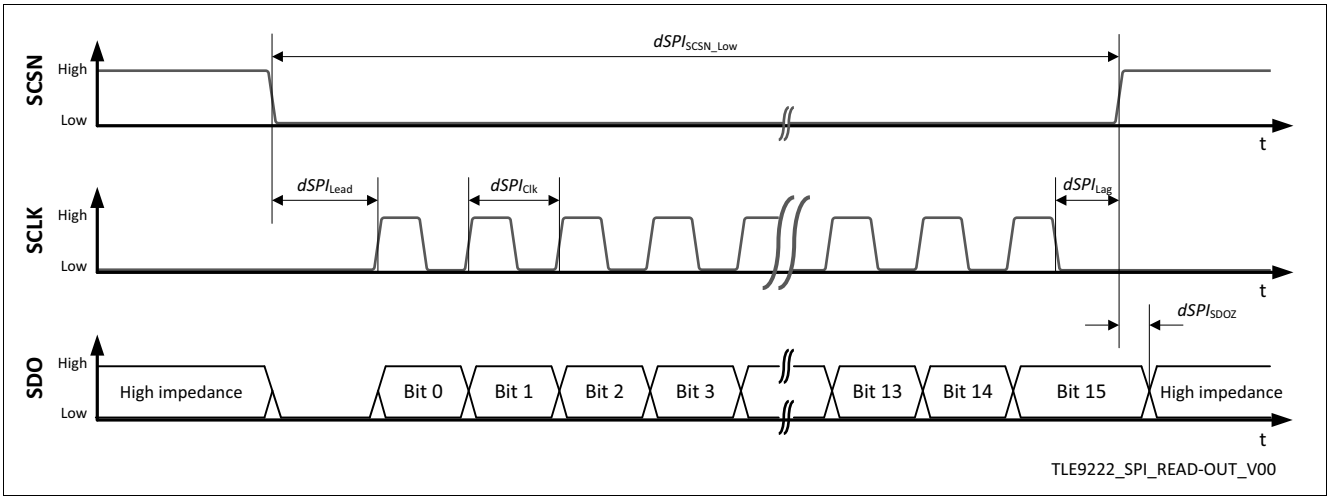


Figure 14 SPI read-out

After a correct SPI read-out process, the information on the ERRN output and the flags in the status register are refreshed. Next SPI read-out can be initiated after SCSN is set “high” for the time $dSPI_{Interframe}$.

The SPI interface is available in both BD_Normal mode and BD_Standby mode, but SPI readout should not occur at the same time as a mode change with the host interface, the time $dBD_{ModeChange}$ must be respected. The SPI register is also blocked during undervoltage conditions on V_{IO}.

While the TLE9222 is set in BD_Standby with host command (pin STBN = “low”) and no wake-up or errors have been detected, the SPI interface requires an enable time of $dSPI_{LeadStbOK}$ from SCSN goes “low” until the first rising edge on the clock signal on the SCLK input can be applied.

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings [1)]

All voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Voltage V_{CC}	uV_{CC}	-0.3	–	6.0	V	–	P_5.1.1
Digital Reference Voltage V_{IO}	uV_{IO}	-0.3	–	6.0	V	–	P_5.1.2
DC voltage on pin BP	*uBP*	-40	–	40	V	–	P_5.1.3
DC voltage on pin BM	*uBM*	-40	–	40	V	–	P_5.1.4
DC voltage on logic input pins TxD, TxEN, BGE, STBN, SCSN, SCLK	uV_{Logic_in}	-0.3	–	6.0	V	–	P_5.1.5
DC voltage on logic output pins RxD, ERRN, SDO	uV_{Logic_out}	-0.3	–	uV_{IO} + 0.3	V	–	P_5.1.6
Currents							
Output Current on pin RxD	*iRxD*	-40	–	40	mA	–	P_5.1.7
Output Current on pin ERRN	*iERRN*	-40	–	40	mA	–	P_5.1.8
Output Current on pin SDO	*iSDO*	-40	–	40	mA	–	P_5.1.9
Temperature							
Junction Temperature	T_j	-40	–	150	°C	–	P_5.1.10
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_5.1.11
ESD Susceptibility							
ESD Susceptibility to GND on BP and BM	$uESD_{Ext}$	-8	–	8	kV	HBM[2)]	P_5.1.12
ESD Susceptibility to GND all other pins	$uESD_{Int}$	-2	–	2	kV	HBM[2)]	P_5.1.13
ESD Susceptibility to GND all pins	$uESD_{CDM}$	-750	–	750	V	CDM[3)]	P_5.1.14

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF).

3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

5.2 Functional Range

Table 7 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage V_{CC}	uV_{CC}	4.75	–	5.25	V	–	P_5.2.1
Digital Reference Voltage V_{IO}	uV_{IO}	3.0	–	5.25	V	–	P_5.2.2
Junction Temperature	T_J	-40	–	150	°C	–	P_5.2.3

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

5.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 8 Thermal Resistance [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance							
Junction to Ambient	R_{thJA}	–	120	–	K/W	[2)]	P_5.3.1
Thermal Shutdown Junction Temperature							
Thermal warning temp.	$T_{J(warning)}$	150	160	170	°C	–	P_5.3.2
Thermal shut-down temp.	$T_{J(Shut\_Down)}$	170	180	190	°C	–	P_5.3.3
Thermal shutdown hysteresis	ΔT	–	6	–	K	–	P_5.3.4

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The TLE9222 (PG-TSSOP-14) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6 Electrical Characteristics

6.1 Functional Device Characteristics

Table 9 Electrical Characteristics

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption V_{CC} Power Supply							
Current Consumption in BD_Normal mode	iV_{CC}	–	33	40	mA	Transmitter active	P_6.1.1
Current Consumption in BD_Normal mode	iV_{CC_idle}	–	6	15	mA	Transmitter idle;	P_6.1.2
Current Consumption in BD_Standby mode	$iV_{CC\_Stb\_150}$	–	30	40	µA	$T_J \leq 150°C$; No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.3
Current Consumption in BD_Standby mode	$iV_{CC\_Stb\_85}$	–	17	25	µA	$T_J \leq 85°C$; No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.4
Current Consumption in BD_Off condition	iV_{CC_Off}	–	–	35	µA	Logic inputs in default states;	P_6.1.5
Current Consumption V_{IO} Reference							
Current Consumption in BD_Normal mode	iV_{IO}	–	0.15	0.5	mA	–	P_6.1.6
Current Consumption in BD_Standby mode	iV_{IO_Stb}	–	1	5	µA	No bus activity or local errors detected; Logic inputs in default states; ERRN = “high”	P_6.1.7
Current Consumption in BD_Off condition	iV_{IO_Off}	–	–	5	µA	Logic inputs in default states	P_6.1.8
Undervoltage Detection V_{CC} Power Supply							
Undervoltage detection threshold on V_{CC}	$uBDUVV_{CC}$	4.0	4.25	4.75	V	–	P_6.1.9
Undervoltage detection hysteresis on V_{CC}	$uBDUVV_{CC\_Hys}$	–	100	–	mV	–	P_6.1.10

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power-on reset threshold	$uBDPDV_{CC}$	1.5	2.5	3.5	V	–	P_6.1.11
Transition time to BD_Standby mode after power-up	dBD_{Power}	–	50	100	µs	$V_{CC} > uBDPDV_{CC}$	P_6.1.12
Undervoltage filter time	$dBDUVV_{CC\_blk}$	3	–	10	µs	1)	P_6.1.13
Undervoltage detection time	$dBDUVV_{CC}$	3	40	100	µs	Time between under-voltage event and forced mode change	P_6.1.14
Undervoltage recovery time	$dBDRV_{CC}$	3	40	100	µs	Time between under-voltage recovery and forced mode change	P_6.1.15
Undervoltage Detection V_{IO} Reference							
Undervoltage detection threshold on V_{IO}	uUV_{IO}	2.5	2.7	3.0	V	–	P_6.1.16
Undervoltage detection hysteresis on V_{IO}	$uBDUVV_{IO\_Hys}$	–	30	–	mV	–	P_6.1.17
Undervoltage filter time	$dBDUVV_{IO\_blk}$	1	–	10	µs	1)	P_6.1.18
Undervoltage detection time	$dBDUVV_{IO}$	1	40	100	µs	Time between under-voltage event and forced mode change	P_6.1.19
Undervoltage recovery time	$dBDRV_{IO}$	1	40	100	µs	Time from recovery until possible mode change	P_6.1.20
Digital Output RxD							
High level output voltage	$uV_{Dig\_Out\_High\_RxD}$	80	–	100	%	Relative to uV_{IO}; 2); $iRxD_H$ = -2 mA;	P_6.1.21
Low level output voltage	$uV_{Dig\_Out\_Low\_RxD}$	–	–	20	%	Relative to uV_{IO}; 2); $iRxD_L$ = 2 mA;	P_6.1.22
Output voltage while uV_{IO} is in undervoltage condition	$uV_{Dig\_Out\_UV\_RxD}$	–	–	250	mV	$uV_{IO} < uUV_{IO}$; 100 kΩ load to GND;	P_6.1.23
Output voltage while in BD_Off condition	$uV_{Dig\_Out\_Off\_RxD}$	–	–	100	mV	100 kΩ load to GND;	P_6.1.24
Rise time on the RxD output	$dBDRxD_{R15}$	–	2	6	ns	20 % → 80% of uV_{IO}; C_{BDRxD} = 15 pF	P_6.1.25
Fall time on the RxD output	$dBDRxD_{F15}$	–	2	6	ns	80 % → 20% of uV_{IO}; C_{BDRxD} = 15 pF	P_6.1.26
Rise time on the RxD output	$dBDRxD_{R25}$	–	3	8	ns	20 % → 80% of uV_{IO}; C_{BDRxD} = 25 pF	P_6.1.27

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fall time on the RxD output	$dBDRxD_{F25}$	–	3	8	ns	80 % → 20% of uV_{IO}; C_{BDRxD} = 25 pF	P_6.1.28
Sum of rise and fall time on the RxD output	$dBDRxD_{R15}$ + $dBDRxD_{F15}$	–	4	12	ns	C_{BDRxD} = 15 pF;	P_6.1.29
Difference of rise and fall time on the RxD output	$\lvert dBDRxD_{R15}$ - $dBDRxD_{F15}\rvert$	–	1	2.5	ns	C_{BDRxD} = 15 pF;	P_6.1.30
Sum of rise and fall time on the RxD output	$dBDRxD_{R25}$ + $dBDRxD_{F25}$	–	6	13	ns	C_{BDRxD} = 25 pF;	P_6.1.31
Difference of rise and fall time on the RxD output	$\lvert dBDRxD_{R25}$ - $dBDRxD_{F25}\rvert$	–	1	2.5	ns	C_{BDRxD} = 25 pF;	P_6.1.32
Digital Output ERRN							
High level output voltage	$uV_{Dig\_Out\_High\_ERRN}$	80	–	100	%	Relative to uV_{IO}; [2]; $iERRN_H$ = -2 mA;	P_6.1.33
Low level output voltage	$uV_{Dig\_Out\_Low\_ERRN}$	–	–	20	%	Relative to uV_{IO}; [2]; $iERRN_L$ = 2 mA;	P_6.1.34
Output voltage while uV_{IO} is in undervoltage condition	$uV_{Dig\_Out\_UV\_ERRN}$	–	–	250	mV	uV_{IO} < uUV_{IO}; 100 kΩ load to GND;	P_6.1.35
Output voltage while in BD_Off condition	$uV_{Dig\_Out\_UFF\_ERRN}$	–	–	100	mV	100 kΩ load to GND;	P_6.1.36
Rise time on the ERRN output	$dBDERRN_{R25}$	–	3	8	ns	[1]; 20 % → 80% of uV_{IO}; C_{BDERRN} = 25 pF	P_6.1.37
Fall time on the ERRN output	$dBDERRN_{F25}$	–	3	8	ns	[1]; 80 % → 20% of uV_{IO}; C_{BDERRN} = 25 pF	P_6.1.38
Reaction time on the ERRN pin	$dReactionTime_{ERRN}$	–	5	30	µs	–	P_6.1.39
Digital Output SDO							
High level output voltage	$uV_{Dig\_Out\_High\_SDO}$	80	–	100	%	Relative to uV_{IO}; [2]; $iSDO_H$ = -2 mA;	P_6.1.40
Low level output voltage	$uV_{Dig\_Out\_Low\_SDO}$	–	–	20	%	Relative to uV_{IO}; [2]; $iSDO_L$ = 2 mA;	P_6.1.41
Leakage current while in high impedance state	$iBDSDO_Z$	-1	–	1	µA	0V < $uSDO$ < uV_{IO}; SCSN = "high"	P_6.1.42
Rise time on the SDO output	$dBDSDO_{R25}$	–	3	8	ns	[1]; 20 % → 80% of uV_{IO}; C_{BDSDO} = 25 pF	P_6.1.43
Fall time on the SDO output	$dBDSDO_{F25}$	–	3	8	ns	[1]; 80 % → 20% of uV_{IO}; C_{BDSDO} = 25 pF	P_6.1.44

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reaction time for setting SDO output to "high impedance"	$dSPI_{SDOZ}$	–	–	250	ns	[1]	P_6.1.45
Digital Input TxD							
Threshold for detecting logical "high"	*uBDLogic_1*	–	–	60	%	Relative to uV_{IO};	P_6.1.46
Threshold for detecting logical "low"	*uBDLogic_0*	40	–	–	%	Relative to uV_{IO};	P_6.1.47
High level input current	*iBDLogic_1*	20	–	200	µA	–	P_6.1.48
Low level input current	*iBDLogic_0*	-1	–	1	µA	–	P_6.1.49
Input capacitance on pin TxD	*C_BDTxD*	–	–	5	pF	[1]	P_6.1.50
Digital Input TxEN							
Threshold for detecting logical "high"	$uV_{Dig\_In\_High\_TxEN}$	–	–	70	%	Relative to uV_{IO};	P_6.1.51
Threshold for detecting logical "low"	$uV_{Dig\_In\_Low\_TxEN}$	30	–	–	%	Relative to uV_{IO};	P_6.1.52
High level input current	$i_{Dig\_In\_High\_TxEN}$	-1	–	1	µA	–	P_6.1.53
Low level input current	$i_{Dig\_In\_Low\_TxEN}$	-200	–	-20	µA	–	P_6.1.54
Input capacitance on pin TxEN	*C_BDTxEN*	–	–	5	pF	[1]	P_6.1.55
Maximum transmitter activation time	*dBDTxActiveMax*	1500	–	2600	µs	–	P_6.1.56
Digital Input BGE							
Threshold for detecting logical "high"	$uV_{Dig\_In\_High\_BGE}$	–	–	70	%	Relative to uV_{IO};	P_6.1.57
Threshold for detecting logical "low"	$uV_{Dig\_In\_Low\_BGE}$	30	–	–	%	Relative to uV_{IO};	P_6.1.58
High level input current	$i_{Dig\_In\_High\_BGE}$	20	–	200	µA	–	P_6.1.59
Low level input current	$i_{Dig\_In\_Low\_BGE}$	-1	–	1	µA	–	P_6.1.60
Transmitter activation delay BGE, Idle → active	*dBDBGEia*	–	50	75	ns	R_{DCLOAD} = 40 Ω	P_6.1.61
Transmitter deactivation delay BGE, Active → idle	*dBDBGEai*	–	50	75	ns	R_{DCLOAD} = 40 Ω	P_6.1.62
Input capacitance on pin BGE	*C_BDBGE*	–	–	5	pF	[1]	P_6.1.63
Digital Input STBN							

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Threshold for detecting logical "high"	$uV_{Dig\_In\_High\_STBN}$	–	–	70	%	Relative to uV_{IO};	P_6.1.64
Threshold for detecting logical "low"	$uV_{Dig\_In\_Low\_STBN}$	30	–	–	%	Relative to uV_{IO};	P_6.1.65
High level input current	$i_{Dig\_In\_High\_STBN}$	20	–	200	µA	–	P_6.1.66
Low level input current	$i_{Dig\_In\_Low\_STBN}$	-1	–	1	µA	–	P_6.1.67
Mode transition time after applying host command	$dBD_{ModeChange}$	–	–	100	µs	–	P_6.1.68
Filter time for detection of host commands	$dBDLogic_{Filter}$	2	–	6	µs	–	P_6.1.69
Input capacitance on pin STBN	*C_BDSTBN*	–	–	5	pF	1)	P_6.1.70
Digital Input SCLK							
Threshold for detecting logical "high"	$uV_{Dig\_In\_High\_SCLK}$	–	–	70	%	Relative to uV_{IO};	P_6.1.71
Threshold for detecting logical "low"	$uV_{Dig\_In\_Low\_SCLK}$	30	–	–	%	Relative to uV_{IO};	P_6.1.72
High level input current	$i_{Dig\_In\_High\_SCLK}$	20	–	200	µA	–	P_6.1.73
Low level input current	$i_{Dig\_In\_Low\_SCLK}$	-1	–	1	µA	–	P_6.1.74
SPI clock period	$dSPI_{Clock}$	0.25	–	100	µs	–	P_6.1.75
SPI enable time	$dSPI_{Lead}$	250	–	–	ns	–	P_6.1.76
SPI enable time	$dSPI_{LeadStbOK}$	4	–	–	µs	BD_Standby mode; No Wake or errors detected; STBN = "low"; ERRN = "high"	P_6.1.77
SPI disable time	$dSPI_{Lag}$	250	–	–	ns	C_{BDSDO} = 25 pF	P_6.1.78
Input capacitance on pin SCLK	*C_BDSCLK*	–	–	5	pF	1)	P_6.1.79
Digital Input SCSN							
Threshold for detecting logical "high"	$uV_{Dig\_In\_High\_SCSN}$	–	–	70	%	Relative to uV_{IO};	P_6.1.80
Threshold for detecting logical "low"	$uV_{Dig\_In\_Low\_SCSN}$	30	–	–	%	Relative to uV_{IO};	P_6.1.81

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High level input current	$i_{Dig\_In\_High\_SCSN}$	-1	–	1	µA	–	P_6.1.82
Low level input current	$i_{Dig\_In\_Low\_SCSN}$	-200	–	-20	µA	–	P_6.1.83
SPI timeout	$dSPI_{Timeout}$	2.1	–	4	ms	–	P_6.1.84
SPI Interframe space	$dSPI_{Interframe}$	10	–	–	µs	Break between consecutive SPI read-outs	P_6.1.85
Input capacitance on pin SCSN	*C_BDSCSN*	–	–	5	pF	[1]	P_6.1.86
Bus Transmitter, BP and BM							
Absolute differential output voltage while sending; Data_0 and Data_1	$uBDTx_{active}$	0.9	–	2.0	V	40 Ω < R_{DCLOAD} < 55 Ω; [4]	P_6.1.87
BP short circuit current Short to GND, Absolute value	$iBP_{GNDShortMax}$	–	20	60	mA	–	P_6.1.88
BP short circuit current Short to -5 V, Absolute value	$iBP_{-5ShortMax}$	–	40	60	mA	–	P_6.1.89
BP short circuit current Short to 27 V, Absolute value	$iBP_{BAT27ShortMax}$	–	25	60	mA	–	P_6.1.90
BP short circuit current Short to BM, Absolute value	$iBP_{BMShortMax}$	–	35	60	mA	–	P_6.1.91
BM short circuit current Short to GND, Absolute value	$iBM_{GNDShortMax}$	–	20	60	mA	–	P_6.1.92
BM short circuit current Short to -5 V, Absolute value	$iBM_{-5ShortMax}$	–	40	60	mA	–	P_6.1.93
BM short circuit current Short to 27 V, Absolute value	$iBM_{BAT27ShortMax}$	–	25	60	mA	–	P_6.1.94
BM short circuit current Short to BP, Absolute value	$iBM_{BPShortMax}$	–	35	60	mA	–	P_6.1.95
Transmitter delay negative voltage	*dBDTx10*	–	35	50	ns	R_{DCLOAD} = 40 Ω; [3]; [4]	P_6.1.96
Transmitter delay positive voltage	*dBDTx01*	–	35	50	ns	R_{DCLOAD} = 40 Ω; [3]; [4]	P_6.1.97
Transmitter delay mismatch *dBDTxAsym* = |*dBDTx10 - dBDTx01*|	*dBDTxAsym*	–	–	4	ns	R_{DCLOAD} = 40 Ω; [3]; [4]; [7]	P_6.1.98

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fall time differential bus voltage (80% → 20%)	*dBusTx10*	6	13	18.75	ns	R_{DCLOAD} = 40 Ω; [4]	P_6.1.99
Rise time differential bus voltage (20% → 80%)	*dBusTx01*	6	13	18.75	ns	R_{DCLOAD} = 40 Ω; [4]	P_6.1.100
Difference between differential bus voltage rise time and fall time *dBusTxDiff* = |*dBusTx01* - *dBusTx10*|	*dBusTxDiff*	–	–	3	ns	R_{DCLOAD} = 40 Ω;	P_6.1.101
Transmitter delay Idle → active	*dBDTxia*	–	40	75	ns	R_{DCLOAD} = 40 Ω;	P_6.1.102
Transmitter delay Active → idle	*dBDTxai*	–	45	75	ns	R_{DCLOAD} = 40 Ω;	P_6.1.103
Transmitter delay mismatch *dBDTxDM* = *dBDTxai* - *dBDTxia*	*dBDTxDM*	-30	–	30	ns	R_{DCLOAD} = 40 Ω;	P_6.1.104
Transition time Idle → active	*dBusTxia*	–	10	30	ns	R_{DCLOAD} = 40 Ω;	P_6.1.105
Transition time Active → idle	*dBusTxai*	–	10	30	ns	R_{DCLOAD} = 40 Ω;	P_6.1.106
Bus Receiver, BP and BM							
Receiver threshold for detecting Data_1	*uData1*	150	–	300	mV	-10 V < *uCM* < 15 V;	P_6.1.107
Receiver threshold for detecting Data_0	*uData0*	-300	–	-150	mV	-10 V < *uCM* < 15 V;	P_6.1.108
Mismatch of receiver thresholds	*uData0* - |*uData1*|	-30	–	30	mV	(*uBP* + *uBM*) / 2 = 2.5 V;	P_6.1.109
Common mode voltage range *uCM* = (*uBP* + *uBM*) /2	*uCM*	-10	–	15	V	[5];	P_6.1.110
Filter time for bus idle detection	*dBDIdleDetection*	50	–	200	ns	*uBus* = 900 mV → 30 mV;	P_6.1.111
Filter time for bus active detection	*dBDActivityDetection*	100	–	250	ns	*uBus* = 30 mV → 900 mV;	P_6.1.112
Receiver common mode input resistance	R_{CM1}, R_{CM2}	10	–	40	kΩ	Bus idle; open load;	P_6.1.113
Receiver differential input resistance	R_{CM1} + R_{CM2}	20	–	80	kΩ	Bus idle; open load;	P_6.1.114

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Absolute differential bus idle voltage	$uBDTx_{Idle}$	0	–	30	mV	TxEN = "high"; 40 Ω < R_{DCLOAD} < 55 Ω;	P_6.1.115
Idle voltage at BP and BM BD_Normal mode	$uBias_{Non-LowPower}$	1.8	2.5	3.2	V	TxEN = "high"; [6]; 40 Ω < R_{DCLOAD} < 55 Ω;	P_6.1.116
Idle voltage at BP and BM BD_Standby mode	$uBias_{LowPower}$	-100	0	100	mV	40 Ω < R_{DCLOAD} < 55 Ω; [6];	P_6.1.117
Absolute leakage current on BP when in BD_Off condition	iBP_{Leak}	–	7	15	µA	*uBP* = *uBM* = 5 V; All other pins connected to GND. GND pin connected directly to 0 V;	P_6.1.118
Absolute leakage current on BM when in BD_Off condition	iBM_{Leak}	–	7	15	µA	*uBP* = *uBM* = 5 V; All other pins connected to GND. GND pin connected directly to 0 V;	P_6.1.119
Absolute BP leakage current loss of GND	$iBP_{LeakGND}$	–	500	1600	µA	*uBP* = *uBM* = 0 V; All other pins connected via 0 Ω to 16 V;	P_6.1.120
Absolute BM leakage current loss of GND	$iBM_{LeakGND}$	–	500	1600	µA	*uBP* = *uBM* = 0 V; All other pins connected via 0 Ω to 16 V;	P_6.1.121
Receiver delay, negative edge	*dBDRx10*	–	60	75	ns	C_{BDRxD} = 25 pF; (see **Figure 18**);	P_6.1.122
Receiver delay, positive edge	*dBDRx01*	–	60	75	ns	C_{BDRxD} = 25 pF; (see **Figure 18**);	P_6.1.123
Receiver delay mismatch *dBDRxAsym* = |*dBDRx10* - *dBDRx01*|	*dBDRxAsym*	–	–	5	ns	(*uBP* + *uBM*) / 2 = 2.5 V; C_{BDRxD} = 25 pF; [7]; (see **Figure 18**);	P_6.1.124
Idle reaction time	*dBDRxai*	50	–	250	ns	(see **Figure 19**);	P_6.1.125
Activity reaction time	*dBDRxia*	100	–	300	ns	(see **Figure 19**);	P_6.1.126
Idle Loop Delay *dBDTxRxai* = *dBDTxai* + *dBDRxai*	*dBDTxRxai*	–	–	325	ns	–	P_6.1.127
BP output current, Bus idle	iBP_{Idle}	-5.0	–	5.0	mA	-27 V < *uBP* < 27 V;	P_6.1.128
BM output current, Bus idle	iBM_{Idle}	-5.0	–	5.0	mA	-27 V < *uBM* < 27 V;	P_6.1.129
Input capacitance on pin BP	*C_BDBP*	–	–	30	pF	[1]; *uBP* = 100 mV; f_{Test} = 5 MHz;	P_6.1.130

Table 9 Electrical Characteristics (cont'd)

uV_{CC} = 4.75 V to 5.25 V; uV_{IO} = 3.0 V to 5.25 V; R_{DCLOAD} = 45 Ohm; C_{DCLOAD} = 100 pF; T_j = -40°C to +150°C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input capacitance on pin BM	*C_BDBM*	–	–	30	pF	[1]; *uBM* = 100 mV; f_{Test} = 5 MHz;	P_6.1.131
Differential bus input capacitance	*C_BDBus*	–	–	20	pF	[1]; *uBP* - *uBM* = 100 mV; f_{Test} = 5 MHz;	P_6.1.132
Remote Wake-up Detection, BP and BM							
Low-power receiver threshold for detecting Data_0	*uData0_LP*	-400	–	-100	mV	–	P_6.1.133
Acceptance time-out of a Data_0 phase in wake-up pattern	$dWU_{0Detect}$	1	–	4	µs	–	P_6.1.134
Acceptance time-out of an Idle or Data_1 phase in wake-up pattern	$dWU_{IdleDetect}$	1	–	4	µs	–	P_6.1.135
Acceptance time-out for wake-up pattern recognition	$dWU_{Timeout}$	48	–	140	µs	–	P_6.1.136
Acceptance time-out for interruptions	$dWU_{Interruptt}$	0.13	–	1	µs	[8]	P_6.1.137
Reaction time after wake-up	$dBDWakeup Reaction_{Remote}$	–	–	100	µs	–	P_6.1.138

1) Not subject to production test, specified by design.
2) No undervoltage on V_{IO}. V_{CC} supplied.
3) For all TxD signals with a sum of rise and fall time (20% - 80% uV_{IO}) of up to 9ns.
4) The TxD signal is constant for 100 ns ... 4400 ns before the first edge and also in case the test is performed with the opposite polarity.
5) Tested on a receiving bus driver. Sending bus driver has a ground offset voltage in the range of [-12.5 V to +12.5 V] and sends a 50 / 50 pattern.
6) Bus Driver connected to GND and uV_{CC} = 5 V.
7) For ±300 mV as well as ±150 mV levels of *uBUS*.
8) When the phase that is interrupted was continuously present for at least 870 ns.

6.2 Diagrams

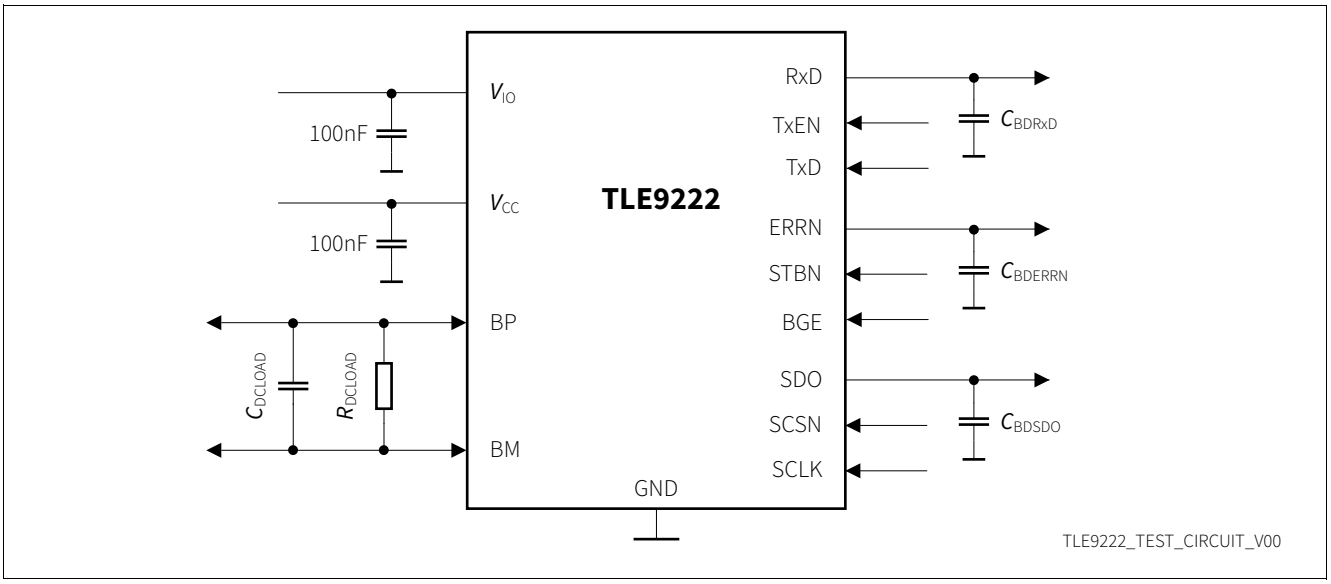


Figure 15 Simplified test circuit

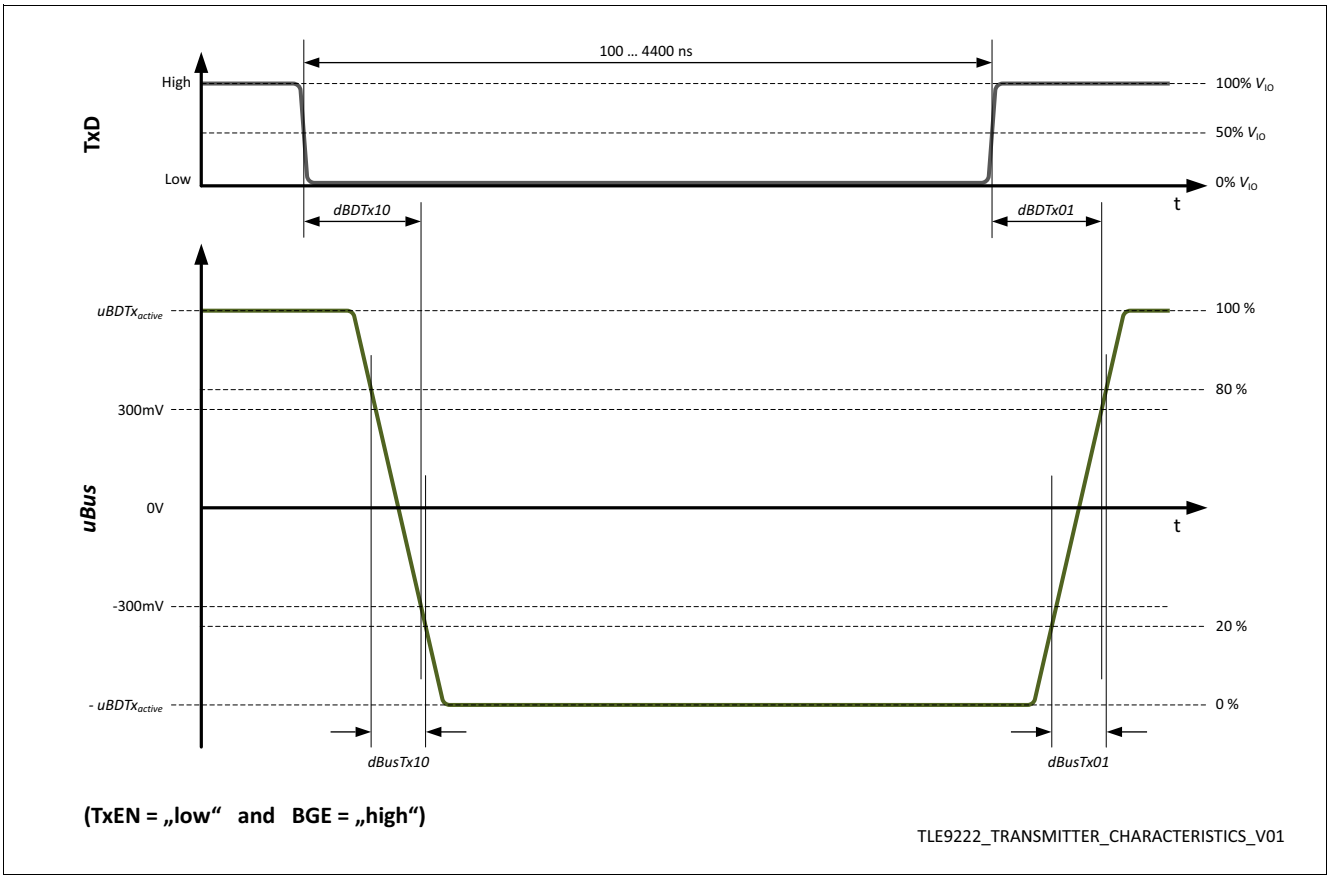


Figure 16 Transmitter characteristics

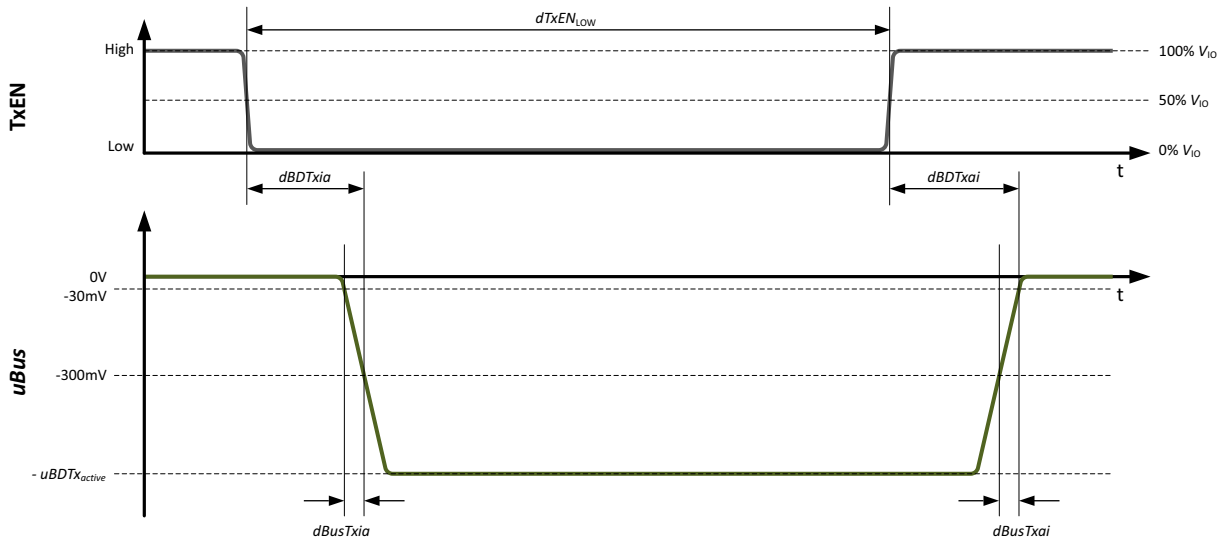


Figure 17 Transmitter characteristics from “idle” to “active” and vice versa

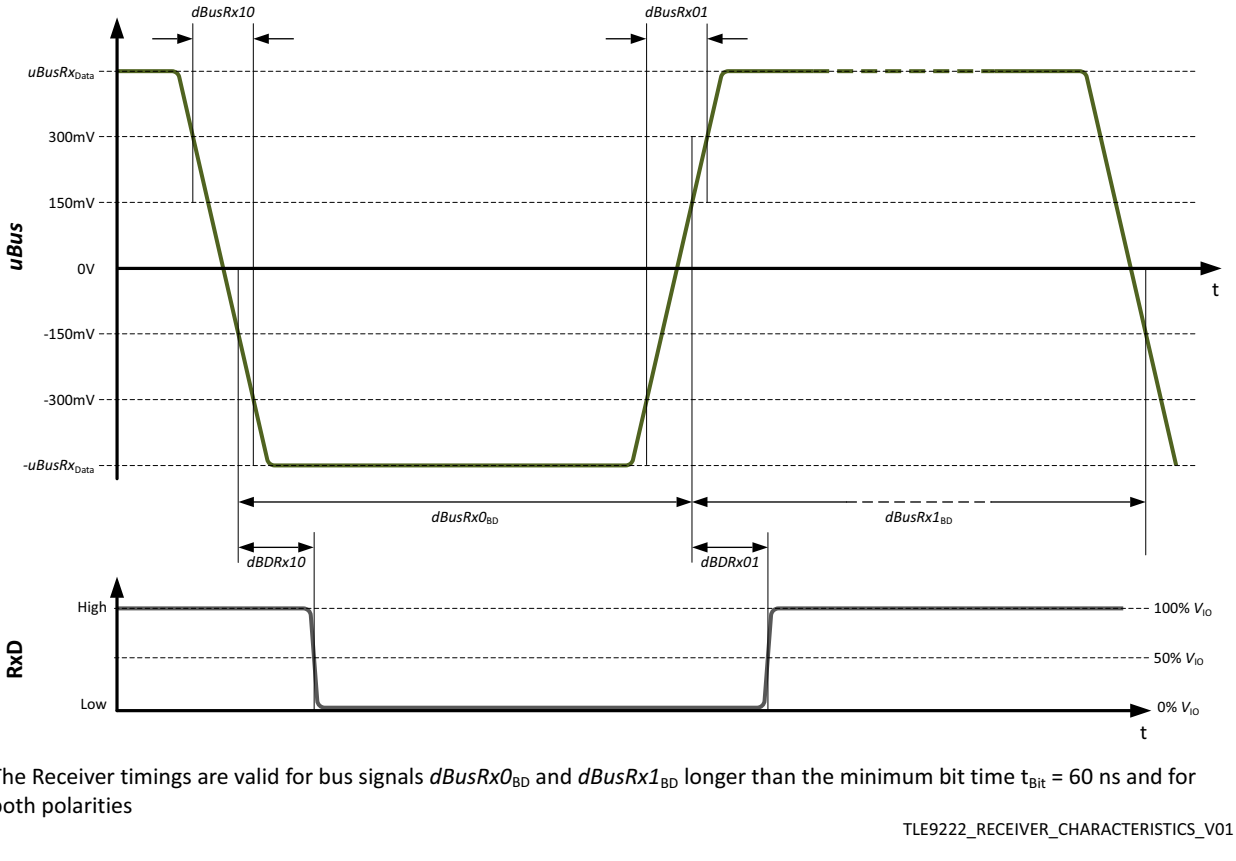


Figure 18 Receiver timing characteristics

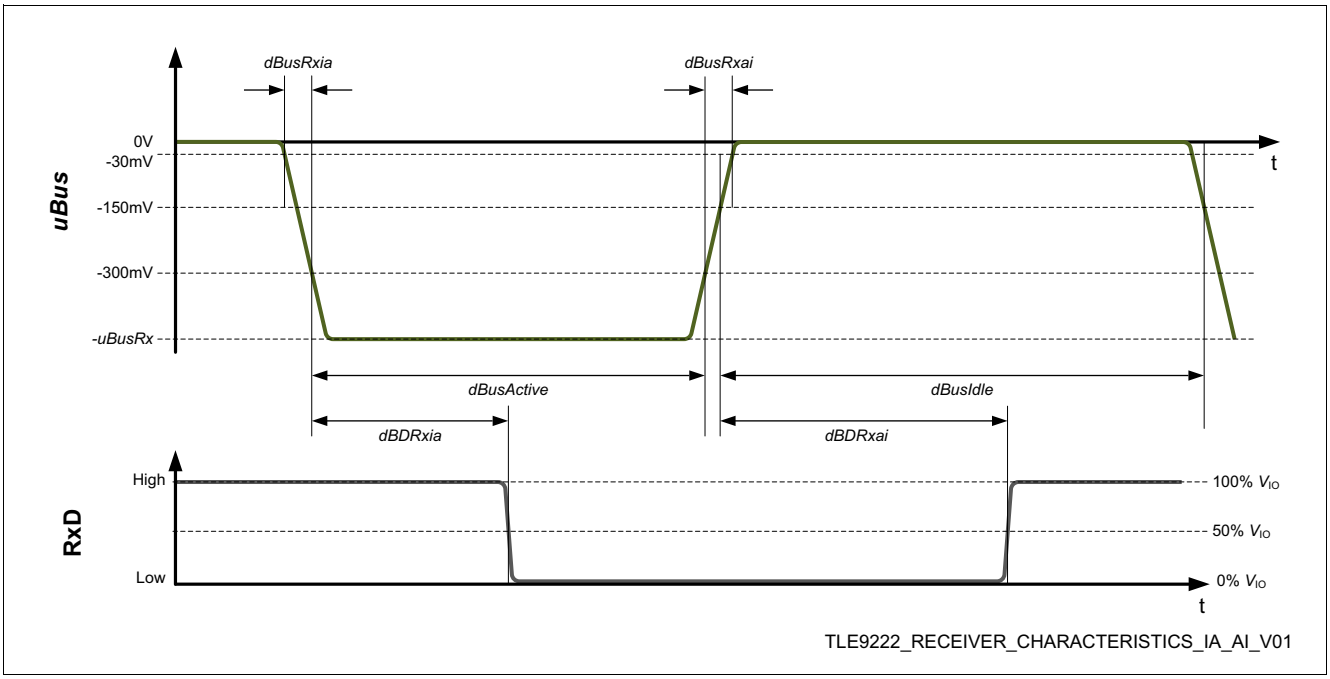


Figure 19 Receiver characteristics from “idle” to “active” and vice versa

7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 ESD Robustness according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 10 ESD Robustness according to IEC61000-4-2

Performed Test	Symbol	Result	Unit	Comment
Electrostatic discharge voltage at pin BM and BP versus GND	$uESD_{IEC}$	≥ 8	kV	Positive pulse
Electrostatic discharge voltage at pin BM and BP versus GND	$uESD_{IEC}$	≤ -8	kV	Negative pulse

7.2 Bus Interface Simulation Model Parameter

The simulated value $R_{BDTransmitter}$ describes the equivalent bus driver output impedance.

$$R_{BDTransmitter} = 50\Omega \times (uBus_{100} - uBus_{40}) / (2.5 \times uBus_{40} - uBus_{100})$$

$uBus_{100}$ = differential output voltage on a 100Ω || 100pF load, while driving “Data_1” to the bus. Value based on simulation.

$uBus_{40}$ = differential output voltage on a 40Ω || 100pF load, while driving “Data_1” to the bus. Value based on simulation.

TLE9222_SIMULATION_V00

Figure 20 Bus Driver output resistance

Table 11 Simulation Parameters [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bus interface simulation resistor	$R_{BDTransmitter}$	30	100	500	Ω	–
RxD signal difference of rise and fall time at TP4_CC	–	–	–	5	ns	–

1) Simulated value for reference purposes only.

7.3 Application Example

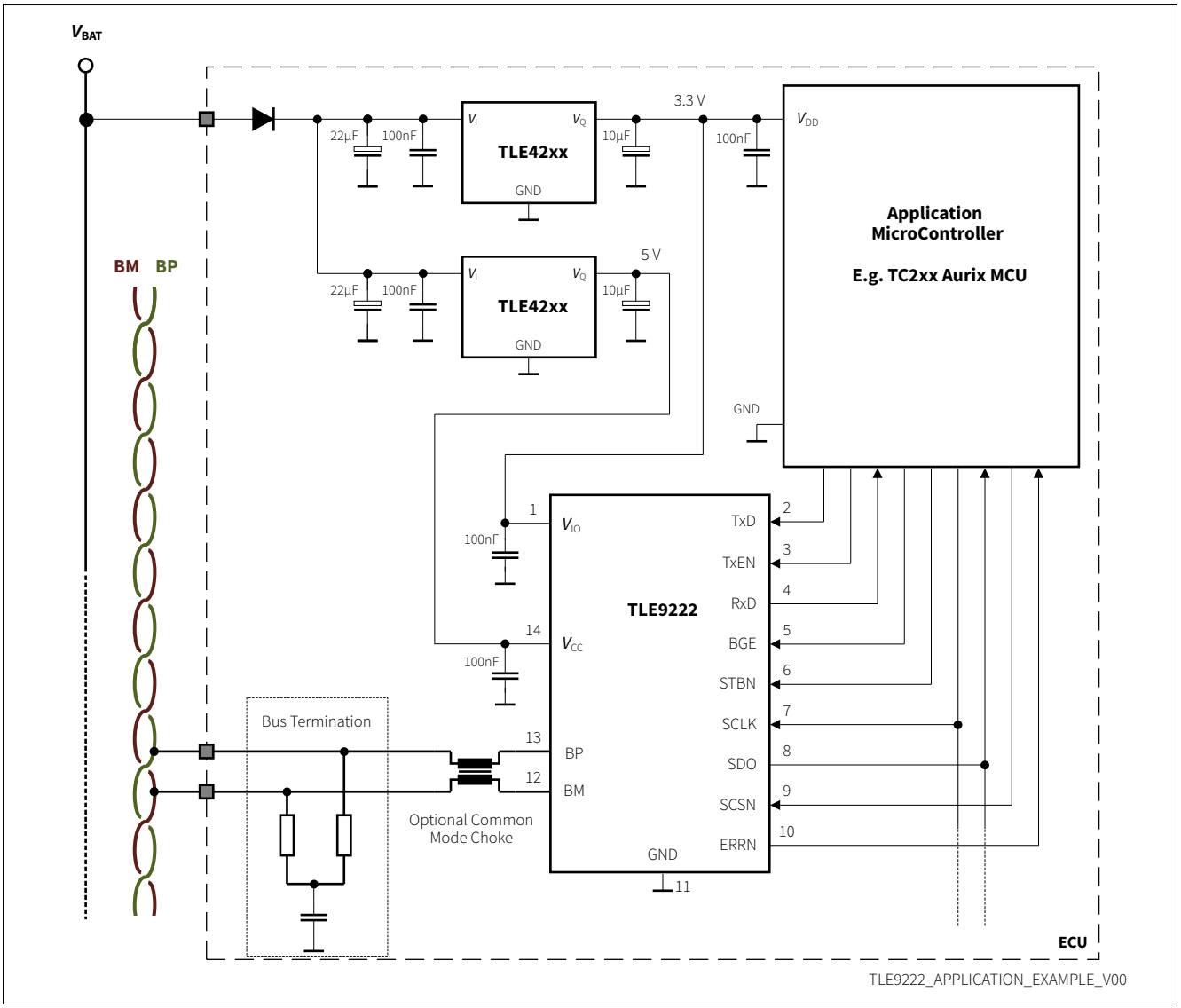


Figure 21 Simplified Application example

7.4 Implementation of ECU Functional Safety concepts

The TLE9222 has been implemented with features for alleviating the development of functional safety requirements on a system level. The top level objective is to ensure a malfunctioning ECU is put in a safe state, which for the FlexRay transceiver means no bus disturbance.

This is realized by the Bus Guardian interface, which controls the bus transmitter directly at the driver stages. The TLE9222 is also implemented with a redundant diagnostic path for detecting the true state of the bus transmitter. This status is multiplexed back to the ERRN output, which is set “low” when the transmitter is reliably disabled. By taking advantage of this safety feature, the ECU diagnostic coverage can be increased.

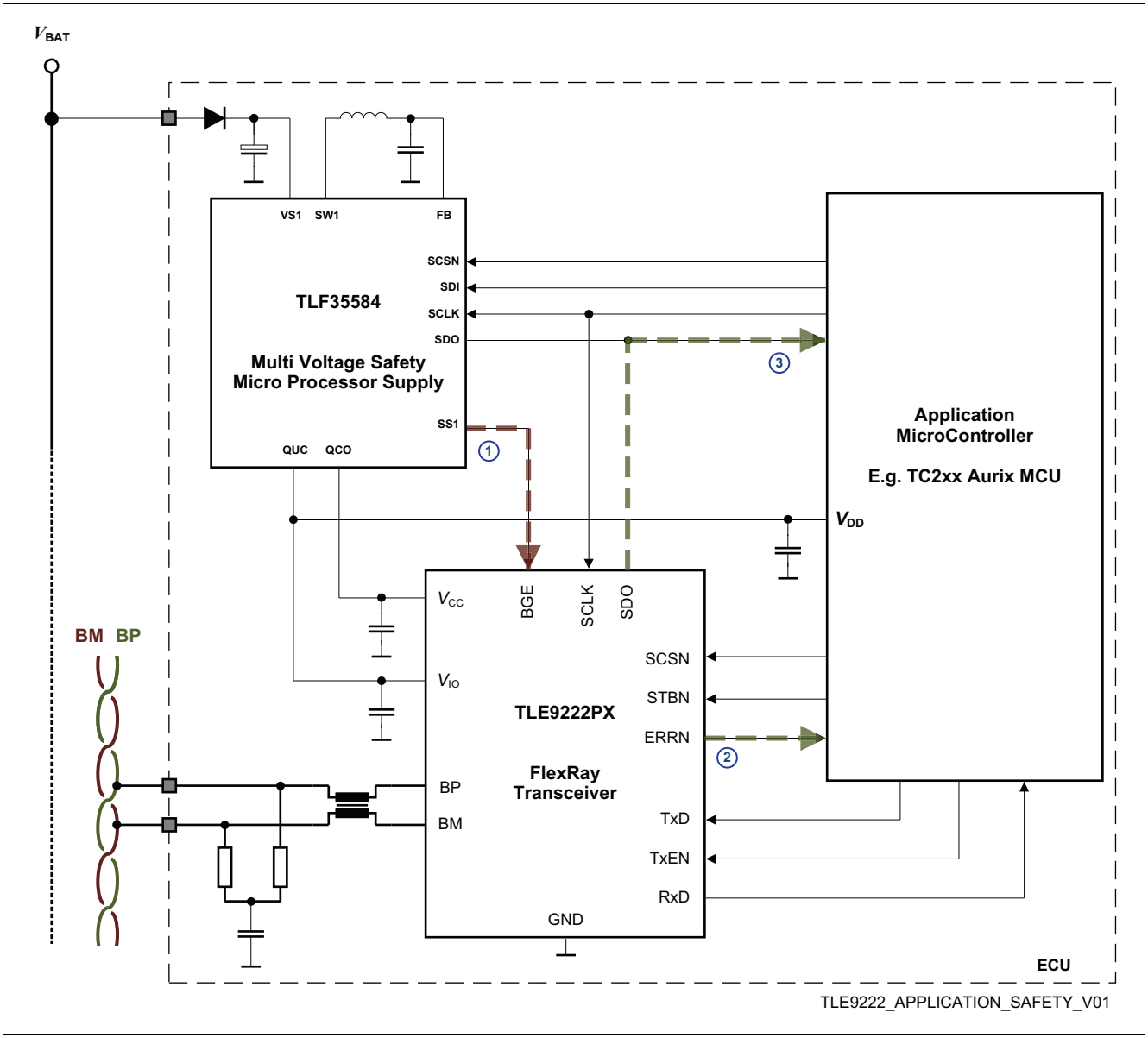


Figure 22 Application diagram

In **Figure 22** an application example of an Automotive ECU for safety critical applications is shown. Together with a Safety MCU Supply IC, e.g. the Infineon TLF35584, that incorporates safe state control functionality, the BGE input of the TLE9222 is connected to the safe state output. If the Safety Supply IC detects unexpected behavior at the supply voltages or incorrect MCU behavior through the functional watchdog, the TLE9222

makes sure there is no influence to the FlexRay bus after the BGE input is set “low”. Additionally, the microcontroller can detect the true state of the transceiver output drivers from the ERRN out, which should trigger a SPI readout of the status register. By observing the BGE flag being set “low”, the MCU has verified that the TLE9222 has been safely disconnected from the bus by the Safety Supply IC.

It is recommended to follow these steps for the ECU software implementation. After ECU power-up, the MCU should test and verify the correct behavior of the fail safe state as a part of its initialization routine, before releasing the transceiver for bus access and transmission.

7.5 Minimizing ECU current consumption through BD_Standby mode

The very low current consumption of $iV_{CC\_Stb\_85}$ and $iV_{CC\_Stb\_150}$ of the TLE9222 can only be reached with the correct system implementation and software control. While operating in ECU low power mode with the TLE9222 in BD_Standby mode, the logic inputs should be in their default states (See **Table 2**). This prevents current to flow through the implemented pull-up / pull-down circuits. Secondly, the logic outputs, RxD and ERRN, should be in their default condition “high” for BD_Standby mode (See **Table 4**). After the TLE9222 is set to BD_Standby mode, it is recommended to perform a SPI readout for verifying correct state transition and to clear pending diagnosis flags.

A MCU in low-power mode should continuously (by interrupt) or periodically (by polling) monitor the ERRN output for wake-up information. Even if the wake-up function is not being used, the MCU should clear the flags of the status register by SPI readout. For simpler ECU implementations, not using the SPI interface, a mode change cycle to BD_Normal mode and back to BD_Standby mode again has the same effect.

7.6 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

8 Package Outlines

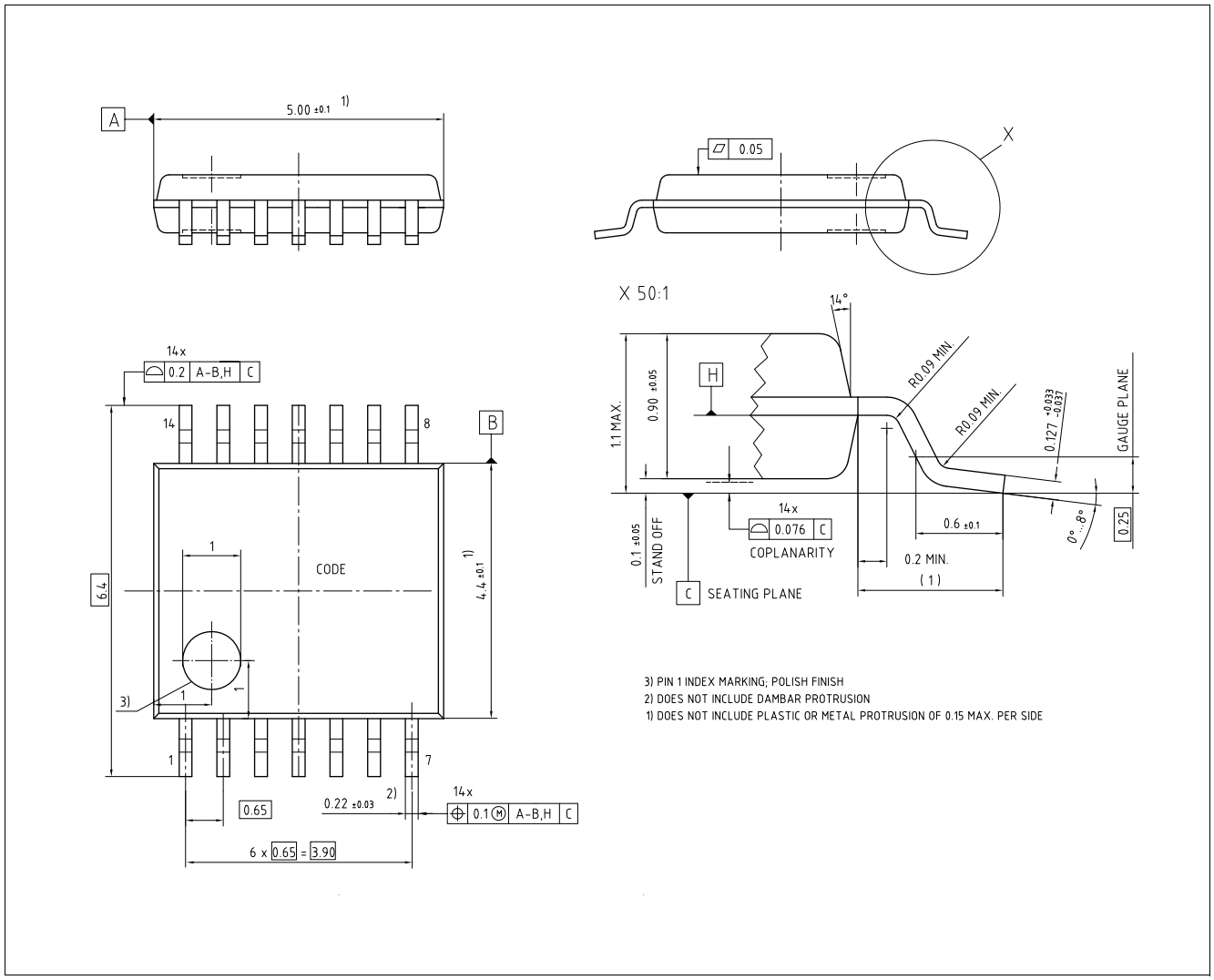


Figure 23 PG-TSSOP-14 (PG-TSSOP-14-1)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.0	2015-06-12	Initial release

www.infineon.com

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Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

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