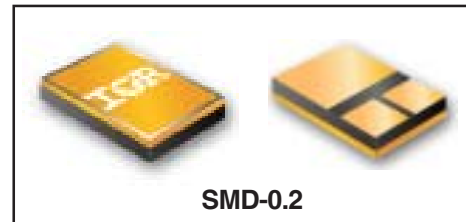


**RADIATION HARDENED  
 LOGIC LEVEL POWER MOSFET  
 SURFACE MOUNT (SMD-0.2)**

**2N7609U8  
 IRHLMN77110  
 100V, N-CHANNEL  
 R7 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	R <sub>DS(on)</sub>	I <sub>D</sub>
IRHLMN77110	100K Rads (Si)	0.29Ω	6.5A
IRHLMN73110	300K Rads (Si)	0.29Ω	6.5A



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

**Features:**

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

**Absolute Maximum Ratings**

**Pre-Irradiation**

	Parameter		Units
I <sub>D</sub> @ V <sub>GS</sub> = 4.5V, T <sub>C</sub> = 25°C	Continuous Drain Current	6.5	A
I <sub>D</sub> @ V <sub>GS</sub> = 4.5V, T <sub>C</sub> = 100°C	Continuous Drain Current	4.1	
I <sub>DM</sub>	Pulsed Drain Current ①	26	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	23.2	W
	Linear Derating Factor	0.18	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	21	mJ
I <sub>AR</sub>	Avalanche Current ①	6.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	2.32	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.3	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	0.25 (Typical)	g

For footnotes refer to the last page

**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBVDSS/ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.105	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.29	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.1A <sup>④</sup>
VGS(th)	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔVGS(th)/ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-6.0	—	mV/°C	
gfs	Forward Transconductance	3.5	—	—	S	V <sub>DS</sub> = 15V, I <sub>DS</sub> = 4.1A <sup>④</sup>
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	1.0	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
		—	—	10		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>g</sub>	Total Gate Charge	—	—	11	nC	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.5A V <sub>DS</sub> = 50V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.0		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	6.0		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	18	ns	V <sub>DD</sub> = 50V, I <sub>D</sub> = 6.5A, V <sub>GS</sub> = 5.0V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	75		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	50		
t <sub>f</sub>	Fall Time	—	—	12		
LS + LD	Total Inductance	—	6.8	—	nH	Measured from the center of drain pad to center of source pad
C <sub>iss</sub>	Input Capacitance	—	572	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	124	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1.6	—		
R <sub>g</sub>	Gate Resistance	—	10.5	—	Ω	f = 1.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	6.5	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.5A, V <sub>GS</sub> = 0V <sup>④</sup>
I <sub>SM</sub>	Pulse Source Current (Body Diode) <sup>①</sup>	—	—	26		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.5A, di/dt ≤ 100A/μs
t <sub>rr</sub>	Reverse Recovery Time	—	—	215	ns	V <sub>DD</sub> ≤ 25V <sup>④</sup>
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	1.05	μC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	5.4	°C/W	

**Note:** Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

## Radiation Characteristics

## IRHLNM77110, 2N7609U8

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

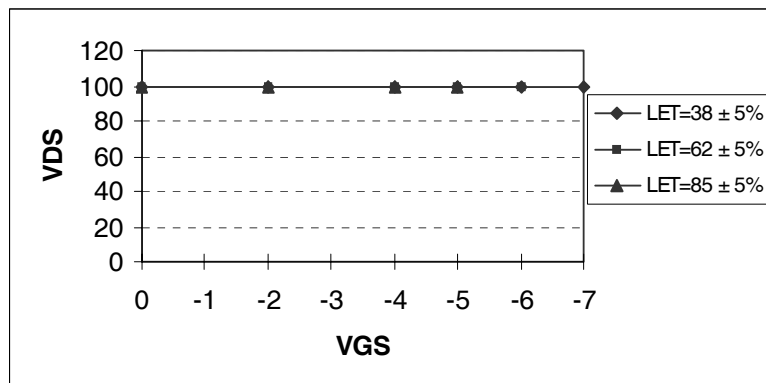
	Parameter	Upto 300K Rads (Si) <sup>1</sup>		Units	Test Conditions
		Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	2.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100		V <sub>GS</sub> = -10V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	1.0	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (TO-3) ④	—	0.32	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.1A
R <sub>DS(on)</sub>	Static Drain-to-Source On-state Resistance (SMD-0.2) ④	—	0.29	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.1A
V <sub>SD</sub>	Diode Forward Voltage④	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 6.5A

1. Part numbers IRHLNM77110, IRHLNM73110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS=0V	@VGS=-2V	@VGS=-4V	@VGS=-5V	@VGS=-6V	@VGS=-7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100	100
62 ± 5%	355 ± 7.5%	33 ± 7.5%	100	100	100	100	100	-
85 ± 5%	380 ± 10%	29 ± 7.5%	100	100	100	100	-	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

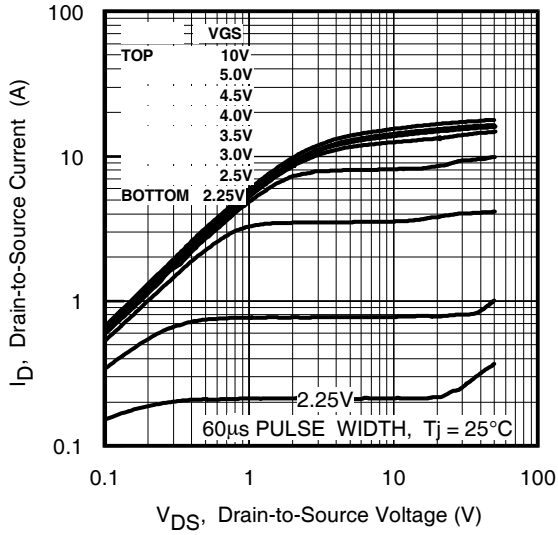


Fig 1. Typical Output Characteristics

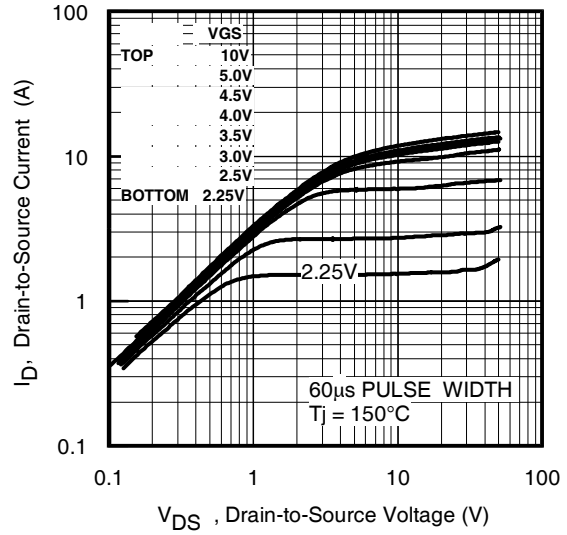


Fig 2. Typical Output Characteristics

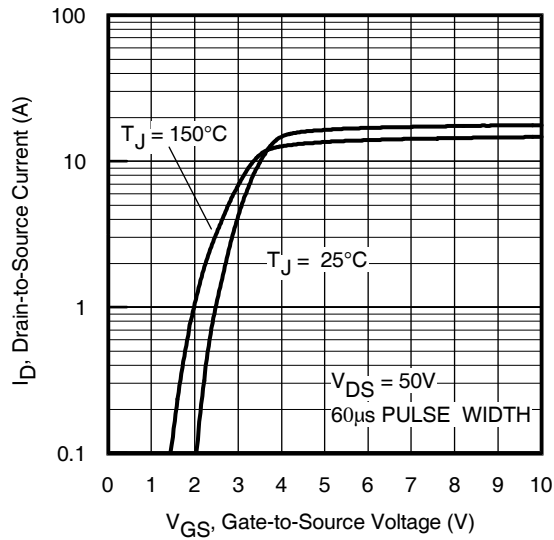


Fig 3. Typical Transfer Characteristics

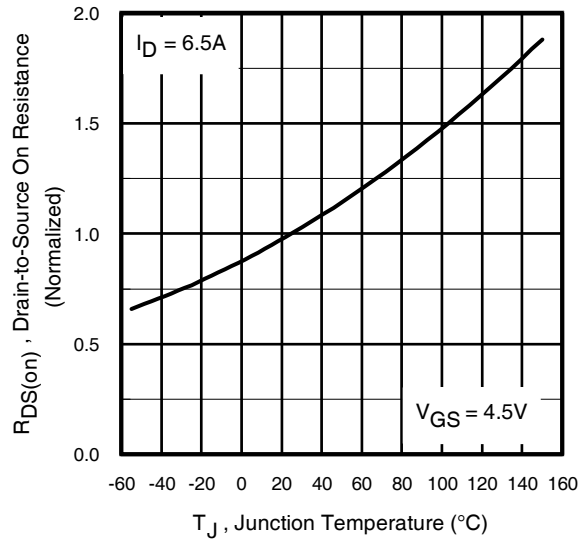


Fig 4. Normalized On-Resistance Vs. Temperature

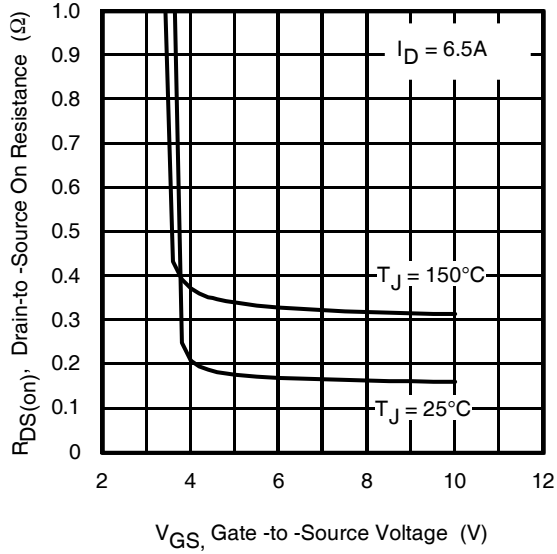


Fig 5. Typical On-Resistance Vs Gate Voltage

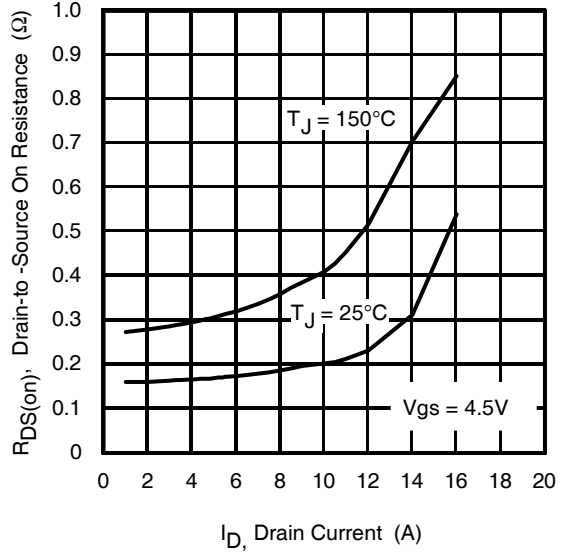


Fig 6. Typical On-Resistance Vs Drain Current

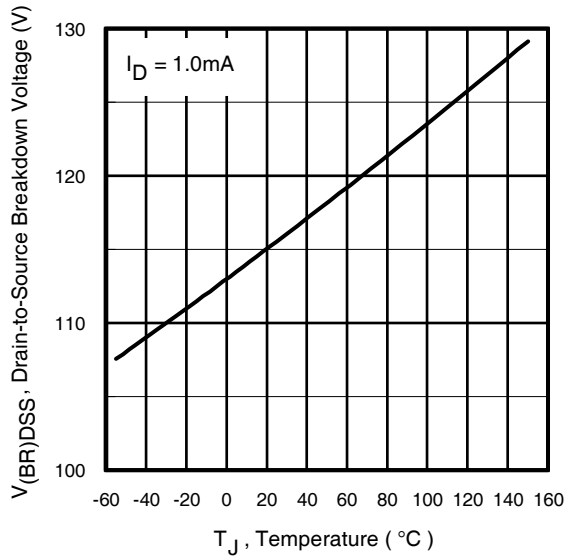


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

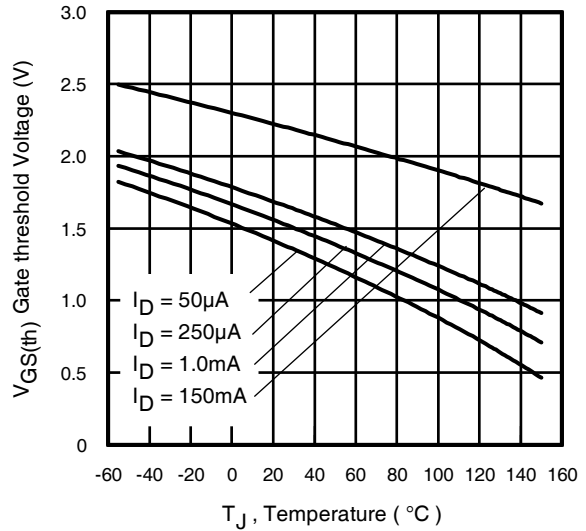
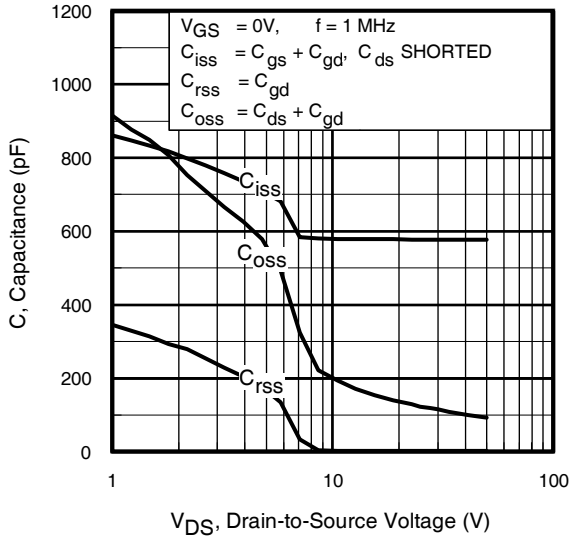
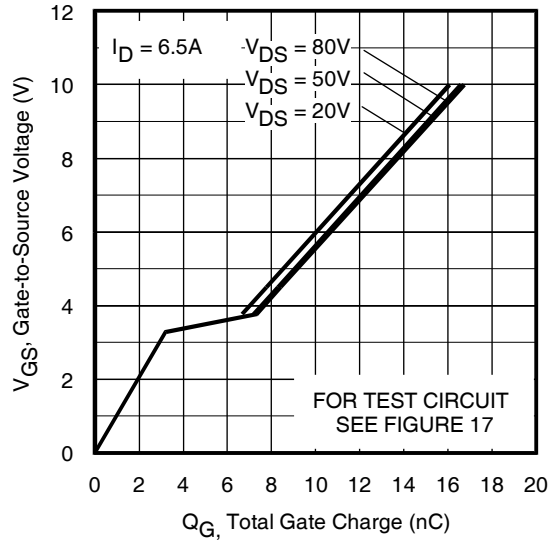


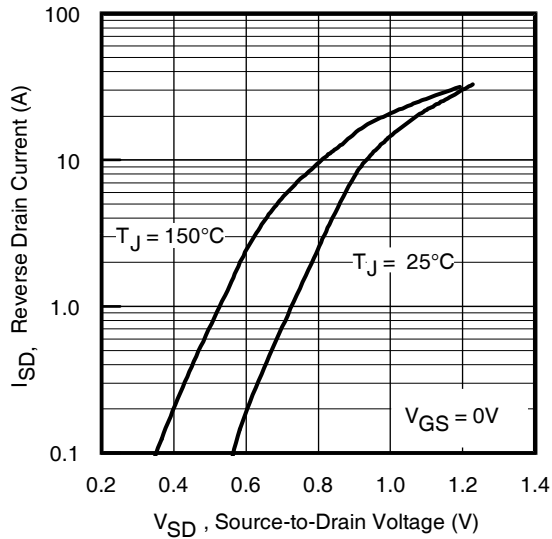
Fig 8. Typical Threshold Voltage Vs Temperature



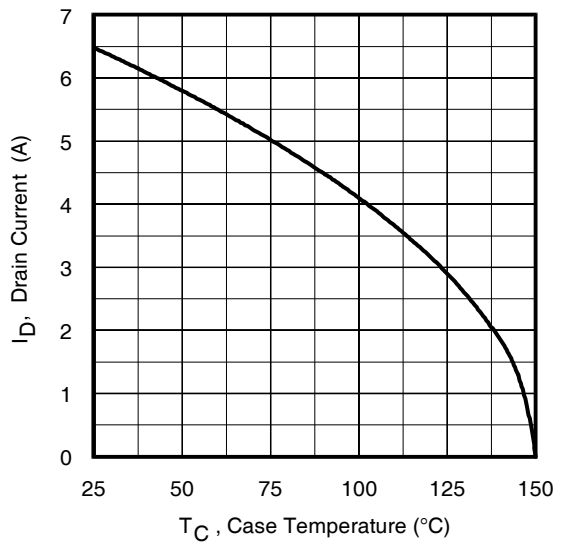
**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 11.** Typical Source-to-Drain Diode Forward Voltage



**Fig 12.** Maximum Drain Current Vs. Case Temperature

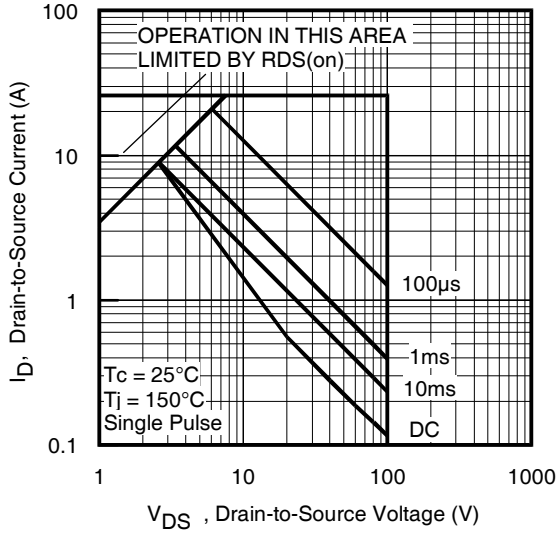


Fig 13. Maximum Safe Operating Area

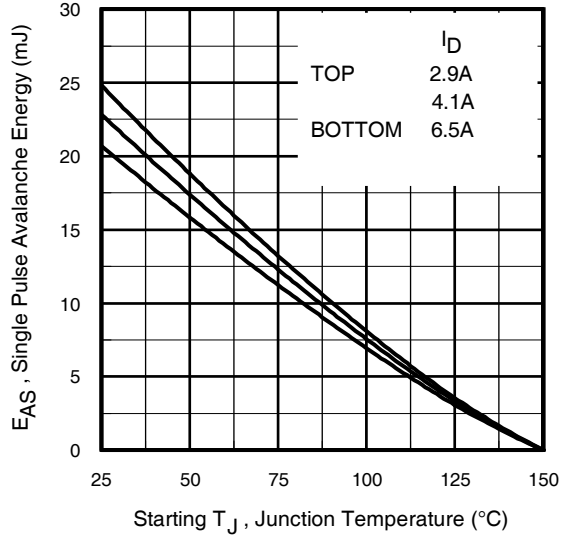


Fig 14. Maximum Avalanche Energy Vs. Drain Current

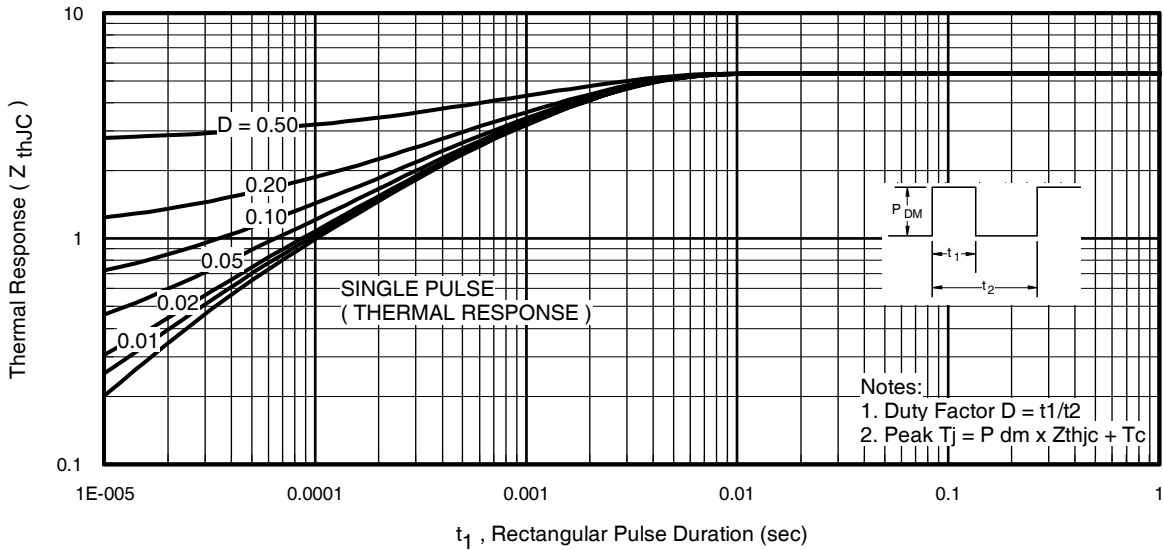


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

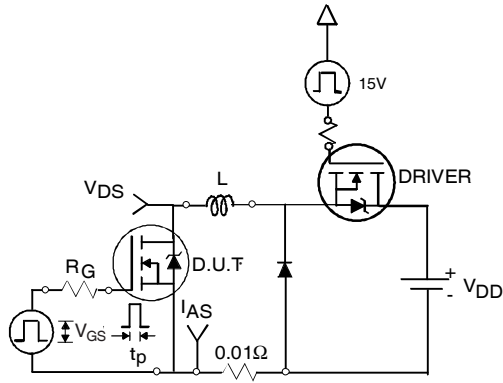


Fig 16a. Unclamped Inductive Test Circuit

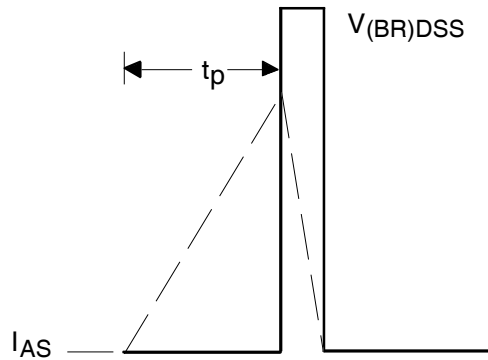


Fig 16b. Unclamped Inductive Waveforms

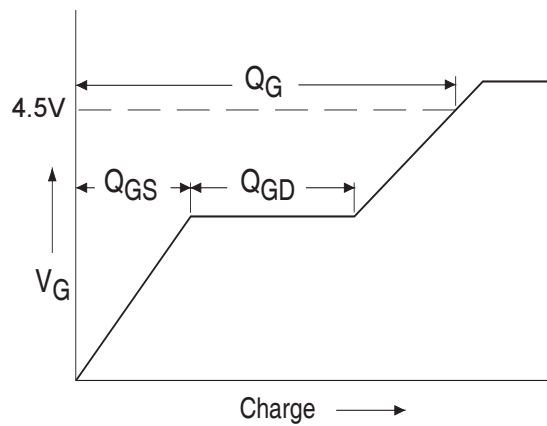


Fig 17a. Basic Gate Charge Waveform

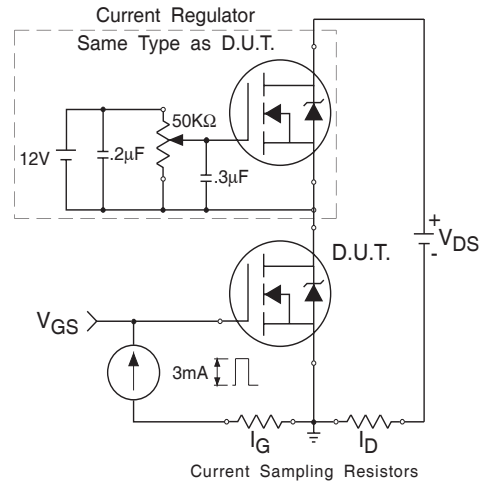


Fig 17b. Gate Charge Test Circuit

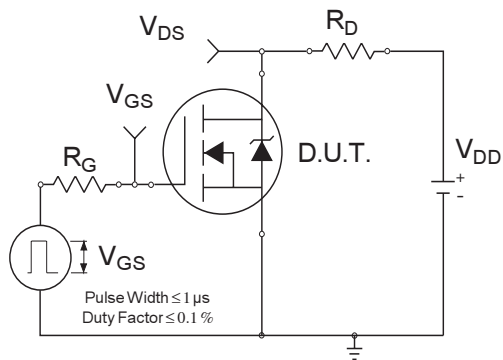


Fig 18a. Switching Time Test Circuit

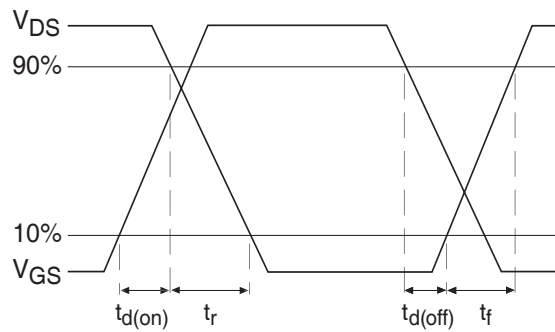


Fig 18b. Switching Time Waveforms



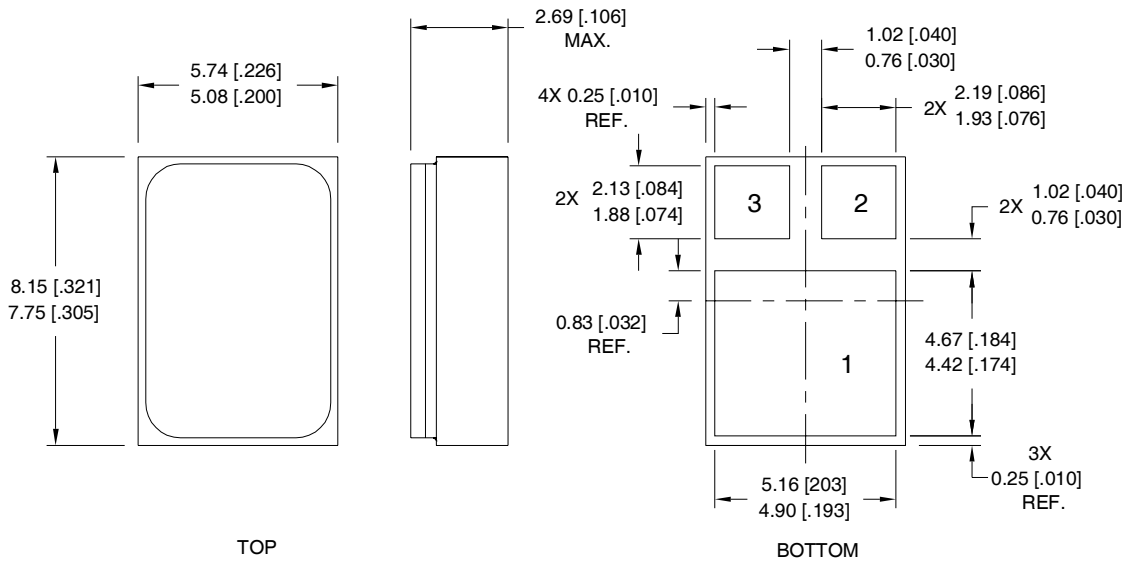
**Pre-Irradiation**

**IRHLNM77110, 2N7609U8**

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ C$ ,  $L = 0.98mH$   
Peak  $I_L = 6.5A$ ,  $V_{GS} = 10V$
- ③  $I_{SD} \leq 6.5A$ ,  $di/dt \leq 490A/\mu s$ ,  
 $V_{DD} \leq 100V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
10 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
80 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.

**Case Outline and Dimensions — SMD-0.2**



**NOTES:**

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

**PAD ASSIGNMENT**

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE

International  
**IOR** Rectifier

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*Data and specifications subject to change without notice. 02/2012*