

KS54AHCT 664/665
KS74AHCT

Octal Bus Transceivers
with Parity T-52-31

Preliminary Specifications

FEATURES

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (IOL = 24 mA @ VOL = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

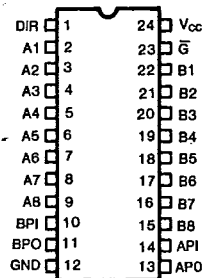
These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, \bar{G} , can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

PIN CONFIGURATION



FUNCTION TABLE

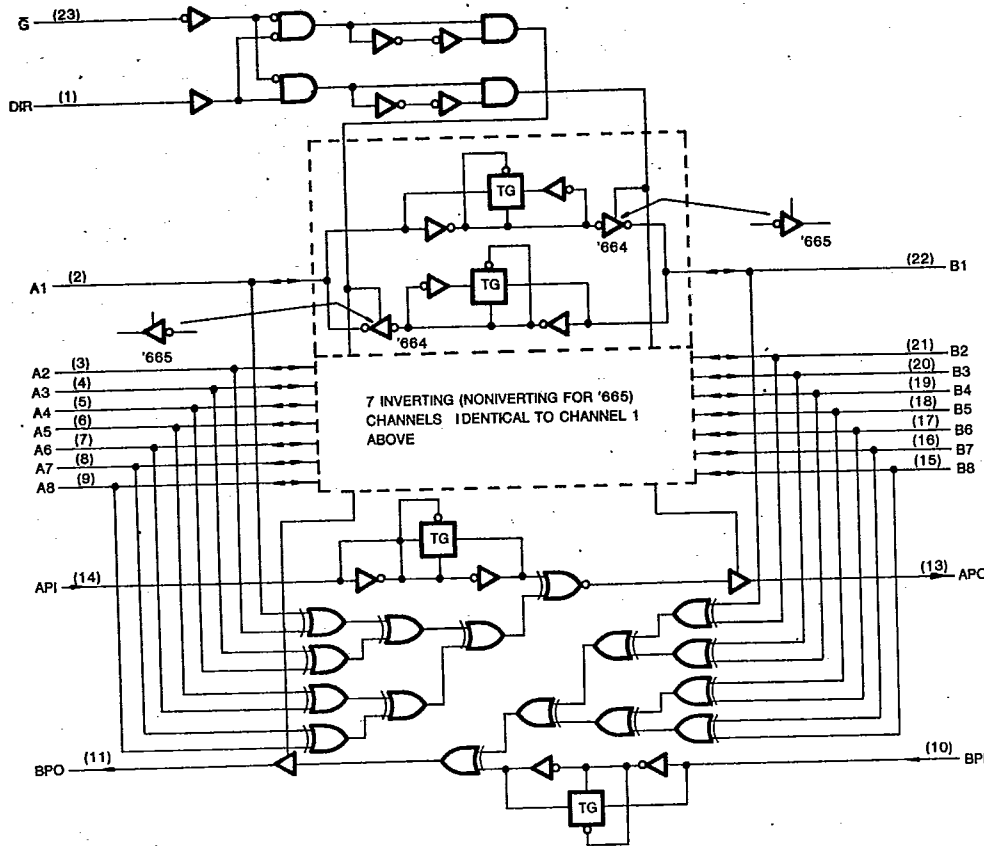
| CONTROL INPUTS | | NUMBER OF HIGH INPUTS ON A BUS AND API | NUMBER OF HIGH INPUTS ON B BUS AND BPI | OUTPUTS | | OPERATION | |
|----------------|-----|--|--|---------|-----|-------------------------|-----------------|
| \bar{G} | DIR | | | APO | BPO | '664 | '665 |
| L | L | X | 0, 2, 4, 6, 8 | Z | H | \bar{B} Data to A Bus | B Data to A Bus |
| L | L | X | 1, 3, 5, 7, 9 | Z | L | \bar{A} Data to B Bus | A Data to B Bus |
| L | H | 0, 2, 4, 6, 8 | X | H | Z | \bar{A} Data to B Bus | A Data to B Bus |
| L | H | 1, 3, 5, 7, 9 | X | L | Z | \bar{A} Data to B Bus | A Data to B Bus |
| H | X | X | X | Z | Z | Isolation | Isolation |

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LOGIC DIAGRAM



Absolute Maximum Ratings*

- Supply Voltage Range V_{cc} -0.5V to +7V
- DC Input Diode Current, I_{IK}
 $(V_i < -0.5V \text{ or } V_i > V_{cc} + 0.5V)$ ± 20 mA
- DC Output Diode Current, I_{OK}
 $(V_o < -0.5V \text{ or } V_o > V_{cc} + 0.5V)$ ± 20 mA
- Continuous Output Current Per Pin, I_o
 $(-0.5V < V_o < V_{cc} + 0.5V)$ ± 70 mA
- Continuous Current Through
 V_{cc} or GND pins ± 250 mA
- Storage Temperature Range, T_{stg} -65°C to +150°C
- Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

- Supply Voltage, V_{cc} 4.5V to 5.5V
- DC Input & Output Voltages*, V_{in}, V_{out} . . . 0V to V_{cc}
- Operating Temperature
 Range
 KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times, t_r, t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{cc} or GND)

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DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

| Characteristic | Symbol | Test Conditions | $T_a = 25^\circ\text{C}$ | | | Unit | |
|--------------------------------------|-----------------|---|--------------------------|---|--|---------------------|---------------|
| | | | Typ | KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ | KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ | | |
| Minimum High-Level Input Voltage | V_{IH} | | | 2.0 | 2.0 | 2.0 | V |
| Maximum Low-Level Input Voltage | V_{IL} | | | 0.8 | 0.8 | 0.8 | V |
| Minimum High-Level Output Voltage | V_{OH} | $V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$ | V_{CC} 4.2 | $V_{CC}-0.1$ 3.98 | $V_{CC}-0.1$ 3.84 | $V_{CC}-0.1$ 3.7 | V |
| Maximum Low-Level Output Voltage | V_{OL} | $V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$ | 0 | 0.1 0.26 0.39 | 0.1 0.33 0.5 | 0.1 0.4 | V |
| Maximum Input Current | I_{IN} | $V_{IN}=V_{CC}$ or GND | | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| Maximum 3-State Leakage Current | I_{OZ} | Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND | | ± 0.5 | ± 5.0 | ± 10.0 | μA |
| Maximum Quiescent Supply Current | I_{CC} | $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$ | | 8.0 | 80.0 | 160.0 | μA |
| Additional Worst Case Supply Current | ΔI_{CC} | per input pin $V_I=2.4\text{V}$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$ | | 2.7 | 2.9 | 3.0 | mA |

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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT664, AHCT665

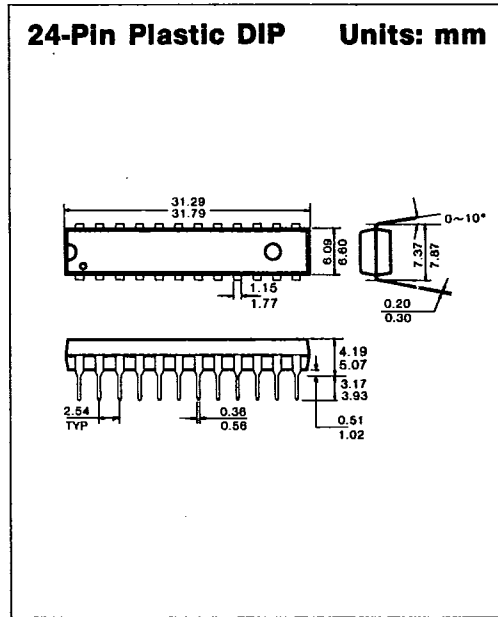
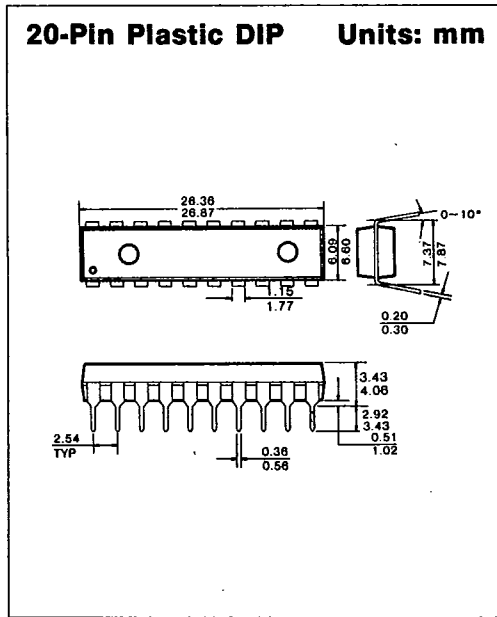
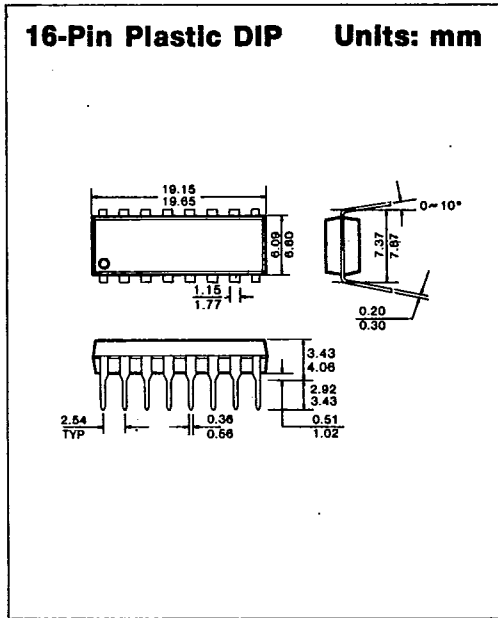
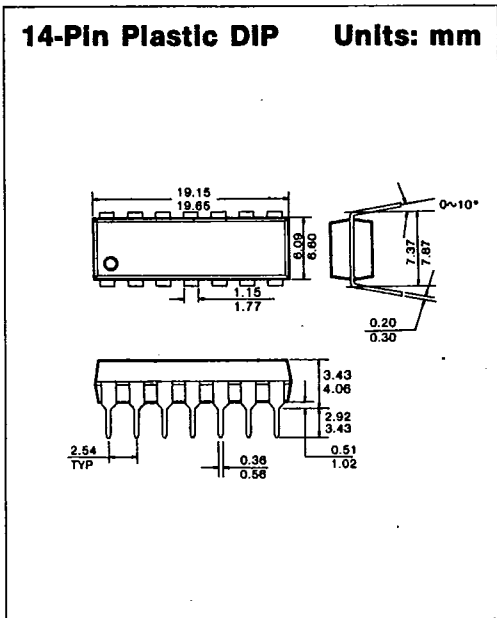
| Characteristic | Symbol | Conditions† | $T_a = 25^\circ\text{C}$ | KS74AHCT | | KS54AHCT | | Unit |
|--|-----------|---|---|---|----------|--|----------|------|
| | | | $V_{CC} = 5.0\text{V}$ | $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ | | $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ | | |
| | | | Typ | $V_{CC} = 5.0\text{V} \pm 10\%$ | | $V_{CC} = 5.0\text{V} \pm 10\%$ | | |
| | | | Min | Max | Min | Max | | |
| Propagation Delay, A or B to B or A | t_{PLH} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 11 14 | | 18 23 | | 22 28 | ns |
| | t_{PHL} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 11 14 | | 18 23 | | 22 28 | ns |
| Propagation Delay, A or B to APO or BPO | t_{PLH} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | | 27 32 | | 32 38 | ns |
| | t_{PHL} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | | 27 32 | | 32 38 | ns |
| Propagation Delay, API or BPI to APO or BPO | t_{PLH} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 11 14 | | 18 23 | | 22 28 | ns |
| | t_{PHL} | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 11 14 | | 18 23 | | 22 28 | ns |
| Output Enable Time, G to A or B | t_{PZH} | $R_L = 1\text{k}\Omega$ | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | 27 32 | | 32 38 | ns |
| | t_{PZL} | | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | 27 32 | | 32 38 | ns |
| Output Disable Time, G to A or B | t_{PHZ} | $R_L = 1\text{k}\Omega$ | | 16 | 27 | | 32 | ns |
| | t_{PLZ} | | $C_L = 50\text{pF}$ | 16 | 27 | | 32 | ns |
| Output Enable Time, DIR to A or B | t_{PZH} | $R_L = 1\text{k}\Omega$ | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | 27 32 | | 32 38 | ns |
| | t_{PZL} | | $C_L = 50\text{pF}$ $C_L = 150\text{pF}$ | 16 19 | 27 32 | | 32 38 | ns |
| Output Disable Time, DIR to A or B | t_{PHZ} | $R_L = 1\text{k}\Omega$ | | 16 | 27 | | 32 | ns |
| | t_{PLZ} | | $C_L = 50\text{pF}$ | 16 | 27 | | 32 | ns |
| Input Capacitance | C_{IN} | | 5 | | | | pF | |
| Output Capacitance | C_{OUT} | Output Disabled | | | | | pF | |
| Power Dissipation Capacitance* | C_{PD} | | | | | | pF | |

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
 † For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES

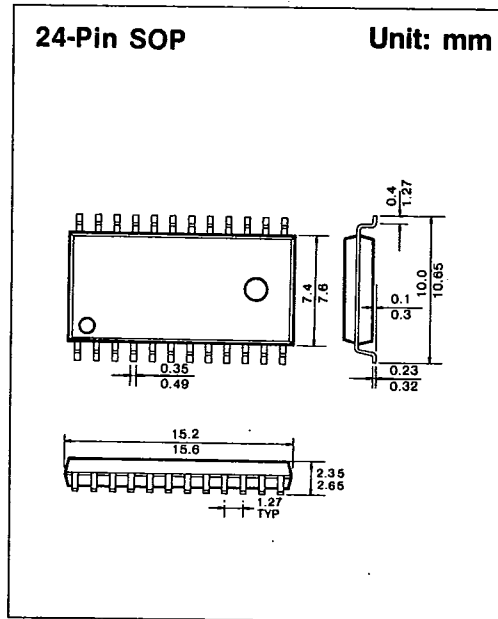
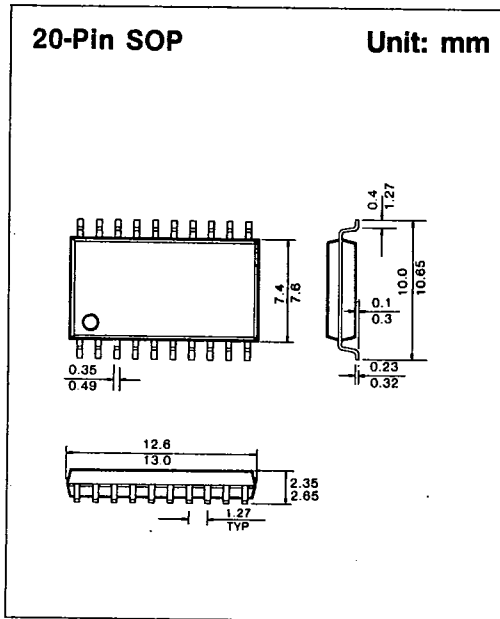
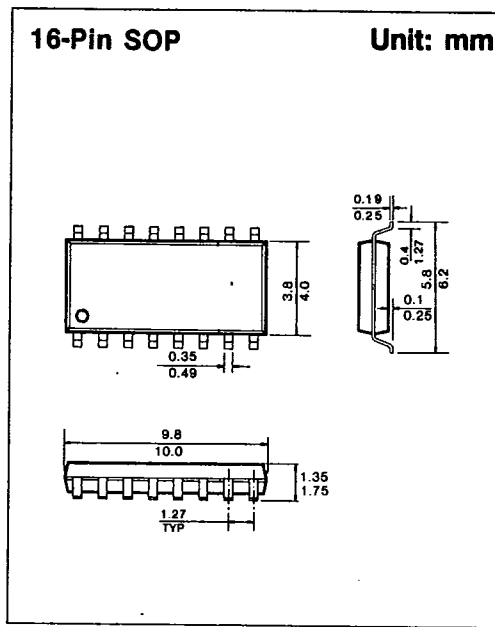
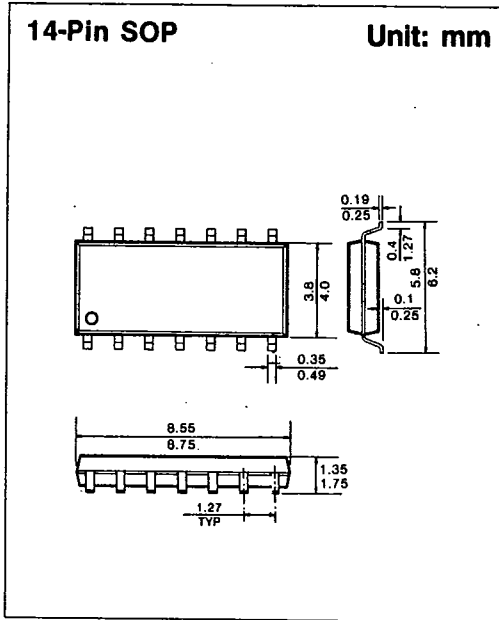


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PACKAGE DIMENSIONS

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2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm

| Dim | Millimeters | |
|----------------|-------------|-------|
| | Min | Max |
| A | — | 5.08 |
| B | 0.38 | 0.58 |
| B ₁ | 1.40 | 1.78 |
| C | 0.20 | 0.38 |
| D | 18.16 | 19.58 |
| E | 8.10 | 7.49 |
| E ₁ | 7.62 | 10.03 |
| F | 2.54 | |
| L | 3.18 | 4.19 |
| Q | 0.51 | 1.02 |
| S | 1.91 | 2.29 |

16-Pin Ceramic DIP Units: mm

| Dim | Millimeters | |
|----------------|-------------|-------|
| | Min | Max |
| A | — | 5.08 |
| B | 0.38 | 0.58 |
| B ₁ | 1.40 | 1.78 |
| C | 0.20 | 0.38 |
| D | 19.05 | 19.94 |
| E | 8.10 | 7.49 |
| E ₁ | 7.62 | 10.03 |
| F | 2.54 | |
| L | 3.18 | 4.19 |
| Q | 0.51 | 1.02 |
| S | 0.51 | 1.14 |

20-Pin Ceramic DIP Units: mm

| Dim | Millimeters | |
|----------------|-------------|-------|
| | Min | Max |
| A | 4.06 | 5.08 |
| B | 0.38 | 0.53 |
| B ₁ | 1.14 | 1.52 |
| C | 0.20 | 0.38 |
| D | 25.78 | 26.93 |
| E | 8.10 | 8.60 |
| E ₁ | 7.77 | 7.88 |
| F | 2.54 | |
| L | 3.73 | 4.01 |
| Q | 0.38 | 0.89 |
| S | 0.51 | 1.14 |

24-Pin Ceramic DIP Units: mm

| Dim | Millimeters | |
|----------------|-------------|-------|
| | Min | Max |
| A | 4.06 | 5.08 |
| B | 0.38 | 0.53 |
| B ₁ | 1.14 | 1.52 |
| C | 0.20 | 0.38 |
| D | 31.50 | 32.84 |
| E | 7.24 | 7.75 |
| E ₁ | 7.77 | 7.98 |
| F | 2.54 | |
| L | 3.73 | 4.01 |
| Q | 0.508 | 1.778 |
| S | 1.85 | 1.93 |

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