P4M644YL, P8M648YL

SDRAM MODULE 4M, 8M x 64 DIMM

Features:

- JEDEC - Standard 168-pin (gold), dual in-line memory module (DIMM).
- TSOP components.
- Single 3.3v ±.3v power supply.
- Nonbuffered fully synchronous; all signals measured on positive edge of system clock.
- Internal pipelined operation; column address can be changed every clock cycle.
- Quad internal banks for hiding row access/precharge.
- 64ms 4096 cycle refresh.
- All inputs, outputs, clocks LVTTL compatible.

Options: Part Number:

4 - 4Mx16 SDRAM TSOP P4M644YL-XX
8 - 4Mx16 SDRAM TSOP P8M648YL-XX

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Freq	CAS Latency
-66CL2	-10/-12	66MHZ	2 or 3
-100CL3A	-8A	100MHZ	3

GENERAL DESCRIPTION

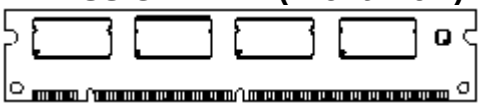
The S4M644YL and S8M648YL are high performance dynamic random-access 32MB and 64MB modules respectively. These modules are organized in a x64 configuration, and utilize dual bank architecture with a synchronous interface. All signals are registered on the positive edge of the clock signals CK0 through CK3. Read and write accesses to the SDRAM are burst oriented; accesses start at a location and continue for a programmed number of locations in a sequence. Accesses begin with an ACTIVE command, which is followed by a READ or WRITE command.

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vcc Supply relative to Vss.....-1 to +4.6V
Operating Temperature T_A (Ambient) .....25 ° to +70 °C
Storage Temperature.....-55 to +125 °C
Power Dissipation……4 or 8 W
Short Circuit Output Current……50 mA

Stresses beyond these may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect reliability.

PIN ASSIGNMENT (Front View)



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	DU	90	Vcc	132	RFU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	QQMB1	71	DQ26	113	DQMB5	155	DQ58
30	SO#	72	DQ27	114	S1#	156	DQ59
31	DU	73	Vcc	115	RAS#	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	RFU	168	Vcc

CAPACITANCE: (This parameter is sampled. VCC = +3.3V m 0.3V; f = 1 MHz)

Parameter	Symbol	Max		Units
		32MB	64MB	
Input Capacitance: A0 - A11, BAO-BA1, RAS#, CAS#, WE#,	C_{I1}	25	45	pF
Input Capacitance: S0#-S3#, CK0-CK3	C_{I2}	15	25	pF
Input Capacitance: CKE0, CKE1,	C_{I3}	25	45	pF
Input Capacitance: DQMB0#, DQMB7	C_{I4}	8	15	pF
Input Capacitance: SQL, SA0-SA2	C_{I5}	6	6	pF
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	10	15	pF

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter	Symbol	Min	Max	Units
Supply Voltage	Vcc/Vccq	3.0	3.6	V
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.0	Vcc + .3	V
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.3	0.8	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vcc All other pins not under test = 0V	I_I I_2 I_3	-10 -20 -30	10 20 30	uA
Output Leakage Current DQs are disabled; 0V ≤ VOUT ≤ VccQ	I_{OZ}	-20	20	uA
Output High Voltage (I_{OUT} = -4 mA)	V_{OH}	2.4		V
Output Low Voltage (I_{OUT} = 4 mA)	V_{OL}		0.4	V

ICC OPERATING CONDITIONS AND MAXIMUM LIMITS: Vcc = 3.3V ± 10%V, Temp. = 25° to 70 °C

Supply Current		Symbol		-8A	-10	Units	Notes
OPERATING CURRENT: ACTIVE mode, burst = 1, READ or WRITE, tRC > tRC (MIN), one bank active,	CL = 2	Icc1	32MB 64MB	N/A	380 730	mA	1, 2, 3
	CL = 3	Icc1	32MB 64MB	440 890	420 850	mA	1, 2, 3
STANDBY CURRENT: POWER-DOWN mode, CKE = LOW, no accesses in progress	tCK = 15ns	Icc2	32MB 64MB	20 40	16 32	mA	
	CLK = LOW	Icc2	32MB 64MB	20 40	8 16	mA	
STANDBY CURRENT: CS# = HIGH, CKE = HIGH, tCK = 15ns, both banks idle		Icc3	32MB 64MB	200 400	200 400	mA	3, 4
STANDBY CURRENT: CS# = HIGH, CKE = HIGH, tCK = 15ns, both banks active after tRCD met, no accesses in progress.		Icc4	32MB 64MB	200 400	200 400	mA	3, 4
OPERATING CURRENT: BURST mode after tRCD met, continuous burst, READ, WRITE, tCK ≥ tCK. MIN, other bank active	CL = 2	Icc5	32MB 64MB	N/A	680 880	mA	1, 2, 3
	CL = 3	Icc5	32MB 64MB	780 980	740 960	mA	1, 2, 3
AUTO REFRESH CURRENT tRC ≥ tRC (MIN)	CL = 2	Icc6	32MB6 4MB	N/A	780 1560	mA	1, 2, 3
	CL = 3	Icc6	32MB 64MB	1000 2000	960 1920	mA	1, 2, 3

NOTES:

1. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
2. The Icc current will decrease as the CAS latency is reduced. This is because maximum cycle rate is slower as CAS latency is reduced.
3. Address transitions average one transition every 30ns.
4. Other input signals are allowed to transition no more than once in any 30ns period.

AC ELECTRICAL CHARACTERISTICS: Vcc = 3.3V ± 10%V, Temp. = 25° to 70°C (CL = CAS Latency)

AC CHARACTERISTICS		-8A	-8A	-10	-10		
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CLK (positive edge) CL = 3	tAC		6		7.5	ns	
Access time from CLK (positive edge) CL = 2	tAC		N/A		9	ns	
Address hold time	tAH	1		1		ns	
Address setup time	tAS	2		3		ns	
CLK high level width	tCH	3		3.5		ns	
CLK low level width	tCL	3		3.5		ns	
Clock cycle time CL = 3	tCK	8		10		ns	
Clock cycle time CL = 2	tCK	N/A		15		ns	
CKE hold time	tCKH	1		1		ns	
CKE setup time	tCKS	2		3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time	tCMH	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time	tCMS	2		3		ns	
Data-in hold time	tDH	1		1		ns	
Data-in setup time	tDS	2		3		ns	
Data-out high impedance time	tHZ		9		9	ns	1
Data-out low impedance time	tLZ	2		2		ns	
Data-out hold time	tOH	3		3		ns	
ACTIVE to PRECHARGE command period	tRAS	50	16K	60	16K	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period	tRC	80		96		ns	
ACTIVE to READ or WRITE delay	tRCD	30		30		ns	
Refresh period (4096 cycles) tT = 1ns.	tREF		64		64	ms	
PRECHARGE command period	tRP	30		30		ns	
ACTIVE bank A to ACTIVE bank B command period	tRRD	20		20		ns	
Transition time	tT	3	2	1	2	ns	
Write recovery time	tWR	20		20		ns	
Exit SELF REFRESH to ACTIVE command	tXSR	80		96		ns	

NOTES:

1. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to Voh or Vol. The last valid data element will meet tOH before going high-Z.
2. * See –8 Speed Options Chart on page 2.

AC ELECTRICAL CHARACTERISTICS: Vcc = 3.3V ± 10%V, Temp. = 25° to 70°C (CL = CAS Latency)

PARAMETER	**SYM**	**-8A**	**-10**	**UNITS**	**NOTES**
READ/WRITE command to READ/WRITE command	tCCD	1	1	tCK	1
CKE to clock disable or power down entry mode	tCKED	1	1	tCK	2
CKE to clock enable or power down exit setup mode	tPED	1	1	tCK	2
DQM to input data delay	tDQD	0	0	tCK	1
DQM to data mask during WRITEs	tDQM	0	0	tCK	1
DQM to data high-impedance during READs	tDQZ	2	2	tCK	1
WRITE command to input data delay	tDWD	0	0	tCK	1
Data-in to ACTIVATE command	tDAL	5	5	tCK	3
Data-in tp precharge reference clock minimum cycle rate, tWR Timing	tDPL	2	2	tCK	
Last data-in to burst stop command	tBDL	0	0	tCK	1
Last data-in to new READ/WRITE command	tCDL	1	1	tCK	1
Last data-in to precharge command	tRDL	2	2	tCK	1
LOAD MODE REGISTER command to command	tMRD	2	2	tCK	1
Data-out to high impedance from precharge CL = 3	tROH	3	3	tCK	1
Data-out to high impedance from precharge CL = 2	tROH		2	tCK	1

NOTES:

1. Clocks required specified by JEDEC functionality and not dependent on any timing parameter.
2. Timing actually specified by tCKS, clock(s) specified as a reference only at a minimum cycle rate.
3. Timing actually specified by tWR plus tRP clock(s) specified as a reference only at a minimum cycle rate.

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD) . The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3).

The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ∓ 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	Vcc x .7	Vcc x .5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	Vcc x .3	V	
OUTPUT LOW VOLTAGE, I_{OUT} =3mA	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT, V_{IN} = GND to Vcc	I_{LI}		10	µA	
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to Vcc	I_{LO}		10	µA	
STANDBY CURRENT SCL=SDA=Vcc -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}		30	µA	
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	µA	

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ∓ 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	**Symbol**	**MIN**	**MAX**	**Units**	**Notes**
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
IIdle bus time before a transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	^{T}HD:DAT	0		µs	
Start condition hold time	^{T}HD:STA	4		µs	
Clock HIGH period	^{t}HIGH	4		µs	
Noise suppresssion time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	^{T}SU:DAT	250		ns	
Start condition setup time	^{T}SU:STA	4.7		µs	
Stop condition setup time	^{T}SU:STO	4.7		µs	
WRITE cycle time	^{t}WR		10	ms	1

NOTES:

1. The SPD EEPROM WRITE cycle time (^{t}WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

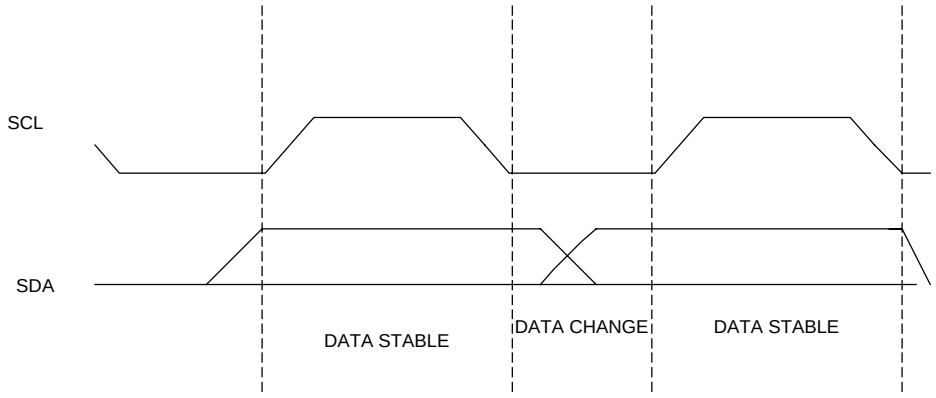


Figure 1
DATA VALIDITY

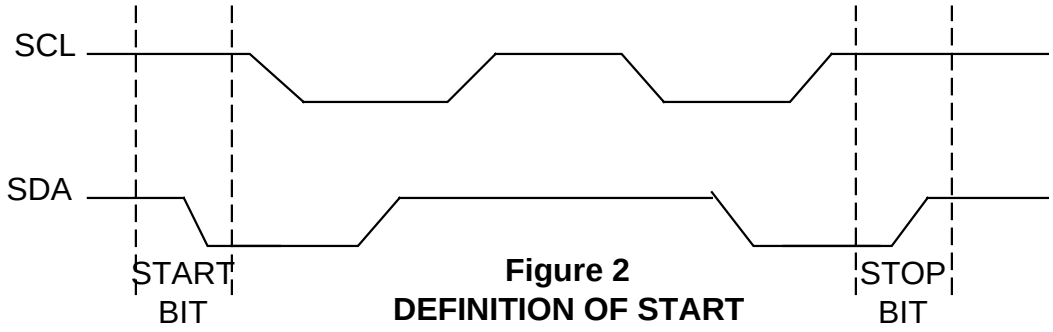


Figure 2
DEFINITION OF START AND STOP

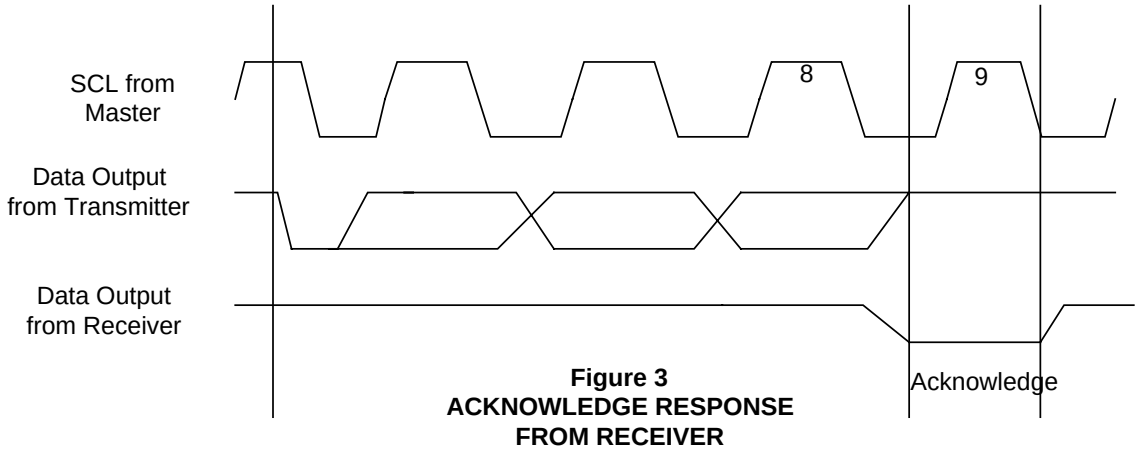


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER