Data Sheet

S6F2002

Preliminary

492 - channel source driver with power circuit
for 16.7M colors ASG TFT-LCD panel

Oct. 26. 2004

Ver. 0.1

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S6F2002 Specification Revision History			
Version	**Content**	**Author**	**Date**
0.0	New release	K.M.Kim S.H.Kim B.H.Han	August 30, 2004
0.1	P.5 Introduction comment revised. P.7 Block diagram revised.	B.H.Han	October 26, 2004

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INTRODUCTION

S6F2002 is a single or dual chip solution for amorphous-Si-gate TFT-LCD panel : source driver, gate-less level shifter and power circuits are integrated on one chip. S6F2002 can display up to 164-RGB x 240-dot graphics on 16.7M-color TFT-LCD panel. Specially, S6F2002 supports amorphous Si TFT-LCD panel.

There are two kinds of interfaces in terms of data type. In case of display data, the S6F2002 offers a flexible 24-/8-bits high speed bus interface for transferring the 16.7M-color display data and supports a serial peripheral interface (SPI) for transferring the control signals to set register value of driver IC.

S6F2002 has various functions for reducing power consumption of LCD system. S6F2002 can be operated as low as 1.8V operating voltage. Internal VCOM signal generator which outputs TFT-LCD counter-electrode driving signals, voltage follower circuits and accurate potentiometer for driving data lines of LCD panel are embedded.

S6F2002 employs display-data digital-signal-processing unit to accomplish a tiny chip size. Display data input via 24-/8-bits bus interface is compressed into 18-/6-bits data by real-time DSP algorithm. As a result, S6F2002 can receive 24-/8-bits display data transferred from MPU or AP and display 16.7M color images without losing color depth or original display information by unique digital-data processing.

S6F2002 is suitable for any small or intermediate-sized mobile display solutions requiring long-term driving capability such as digital still cameras, digital cellular phones and personal multimedia player, etc.

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FEATURES

164-RGB x 240-dot Amorphous Si-Gate TFT-LCD driver IC for 16,777,216 colors (492ch-source driver).

24-/8- bits RGB interface and serial peripheral interface (SPI)

Supporting SYNC mode / DE mode data transfer system

Supporting Delta / Stripe pixel panel

Adjustable color-display control functions

−   16,777,216 colors can be displayed at the same time (gamma adjust included)

Supporting dual / single chip solution (master / slave operation is selectable in 2-driver system)

Supporting low-power operation :

−   Power-save functions such as standby mode, external VCOM mode.
−   Voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
−   Employing equalizing function for the charge-sharing between VCOM circuits and source driver.

Frame/ 1- /2- raster row inversion driving

Structure for TFT-display retention volume (Cst structure)

Internal power supply circuit :

−   Internal VCL / VGOFF generator for VCOM blocks and gate level shifter circuits.
−   Internal power regulator is included for low-power consumption.
−   Adjustable VCOMOUT amplitude: the amplitude of VCOMOUT is determined by VCOMH / VCOML voltages. VCOMH / VCOML voltages are directly designated by VCM4-0 & VDV4-0 register value, respectively. 31-level precise digital potentiometers are also employed to set VCOMH& VCOML.

Operating voltages :

• Applying voltage
−   VDD   to VSS = 1.8 to 2.5 V (non-regulating)   : supply voltage range for logic circuit – non-regulated
  a) VDD3 to VSS = 2.5 to 3.3 V (regulating)   : supply voltage range for logic circuit – regulated
  b) VDD3 to VSS = 1.8 to 3.3 V (logic interface)   : supply voltage range for logic signal interface
−   VCI   to VSS = 2.5 to 3.3 V   : supply voltage range for analog function block
−   AVDD to VSS = 4.0 to 5.0 V   : supply voltage range for liquid crystal driver circuits
−   VGH   to VSS =
−   VGL   to VSS =

• Generated voltage
−   For the analog block: |VCL| = 0.2x|VGL| : generated power for internal analog block.
                           RVDD = 2.0 V fixed   : generated power for internal logic block.
−   For the gate driver: |VGOFF| = 0.7x |VGL| : negative reference for ASG level shifter block.
                           |VGH-VGOFF| $_{(max)}$ = 25.0 V
−   For the TFT-LCD counter electrode: VCOMOUT amplitude $_{(max)}$ = 5.5 V
                           VCOMH to VSS = 3.0 to 4.5 V
                           VCOML to VSS = -1.0 to 1.0 V

Released Package Type : *COG Only*

−   *S6F2002 offers only a COG package type. Film type package such as User-COF is NOT available.*

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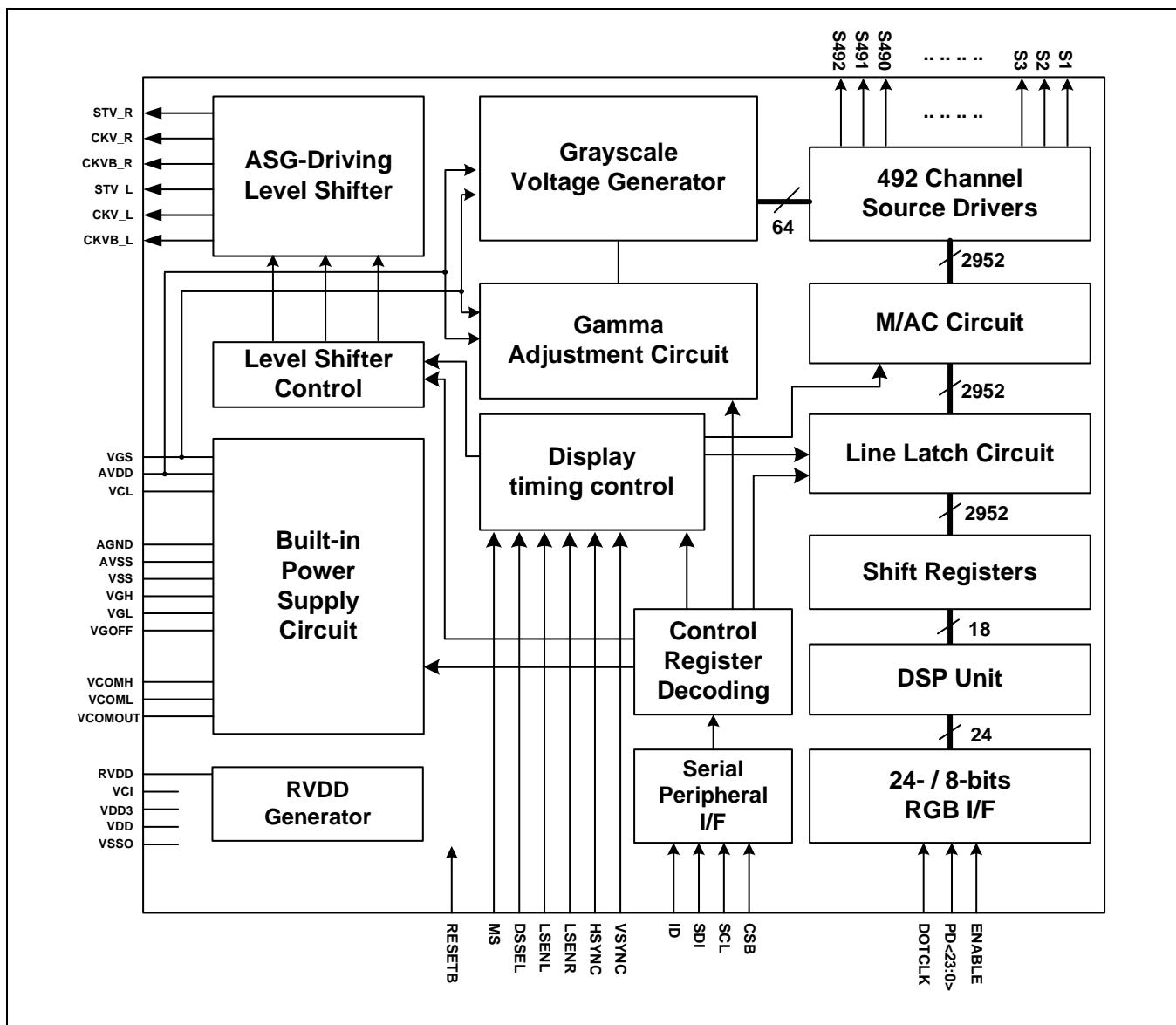
BLOCK DIAGRAM

Figure 1. Block Diagram

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PAD CONFIGURATION
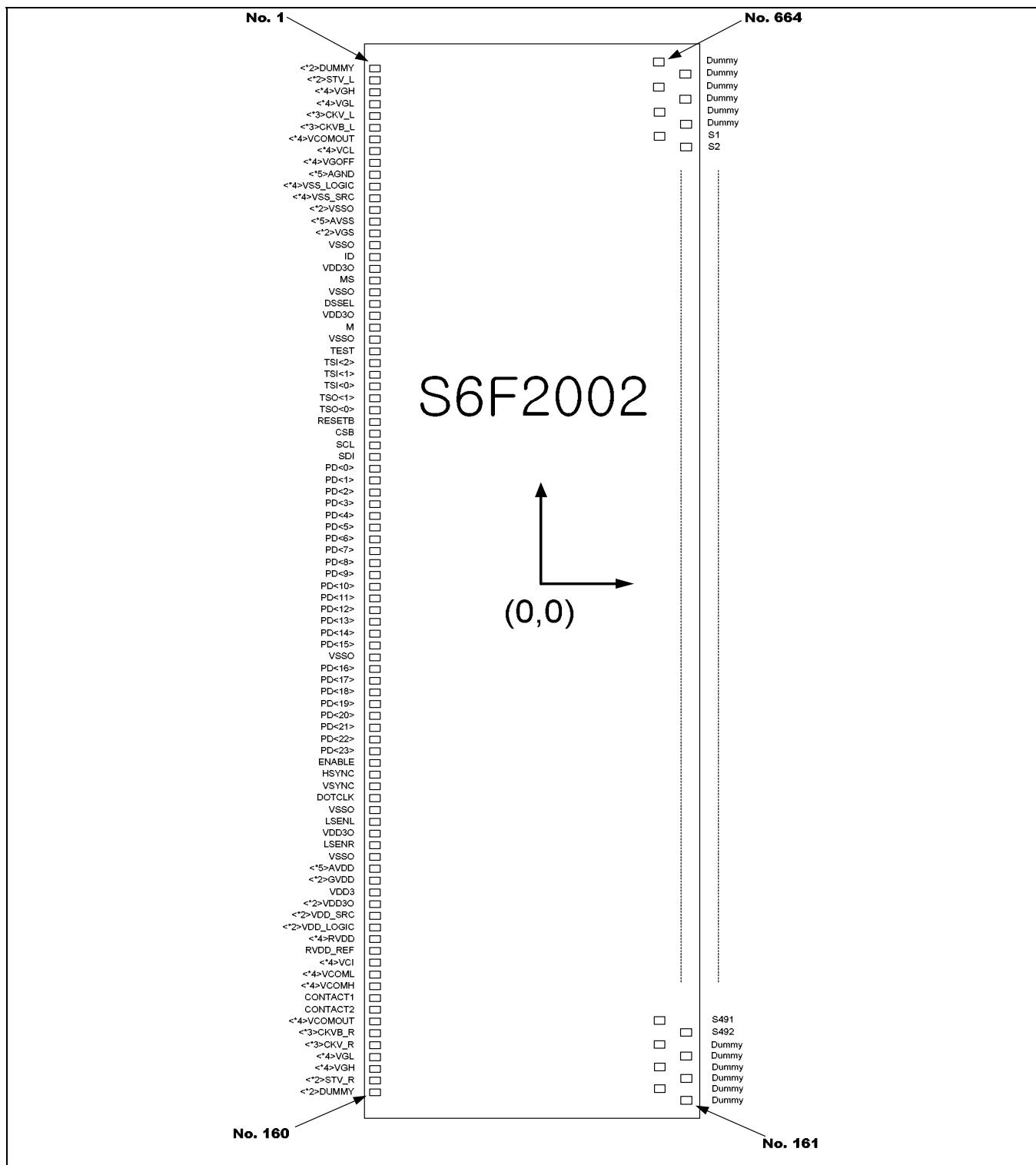
Figure 2. Pad Configuration

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PAD DESIGN INFORMATION
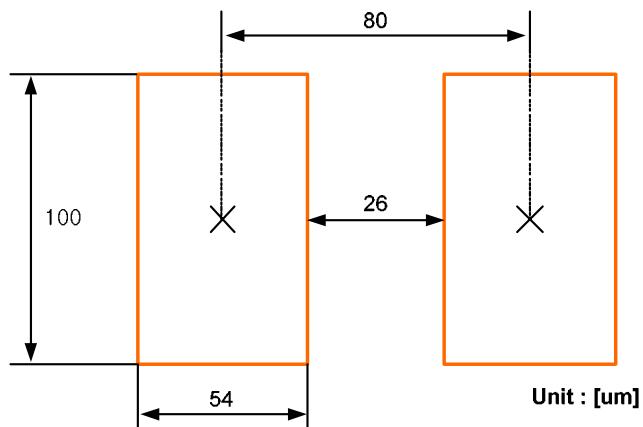
Figure 3. Bump Information – Straight Input Pad
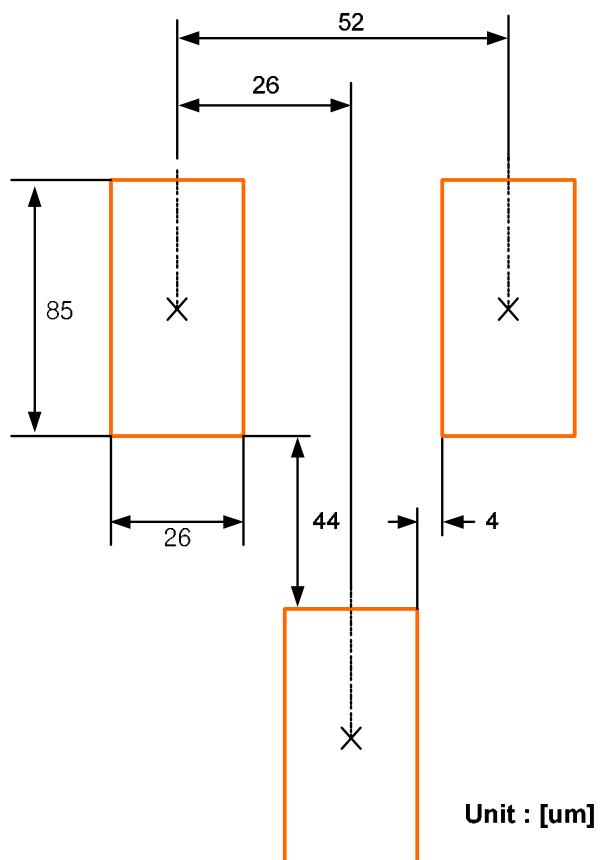
Figure 4. Bump Information – Staggered Output Pad

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Table 1. Mechanical Pad Dimension

Items	Pad Name.	Size		Unit
		X	Y	
Chip size (With scribe lane : 100um)	-	13,600	1,300	um
Chip thickness	-	450+/-10		
Pad pitch	1 to 160 (Input pad)	80		
	161 to 664 (Output pad, Even number)	52		
	161 to 664 (Output pad, Odd number)	52		
Bumped pad size (top)	Input pad	54 +/-3	100 +/-3	
	Output pad	26 +/-3	85 +/-3	
Bumped pad height	All pads	15(typ.) +/-3		

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ALIGN KEY INFORMATION
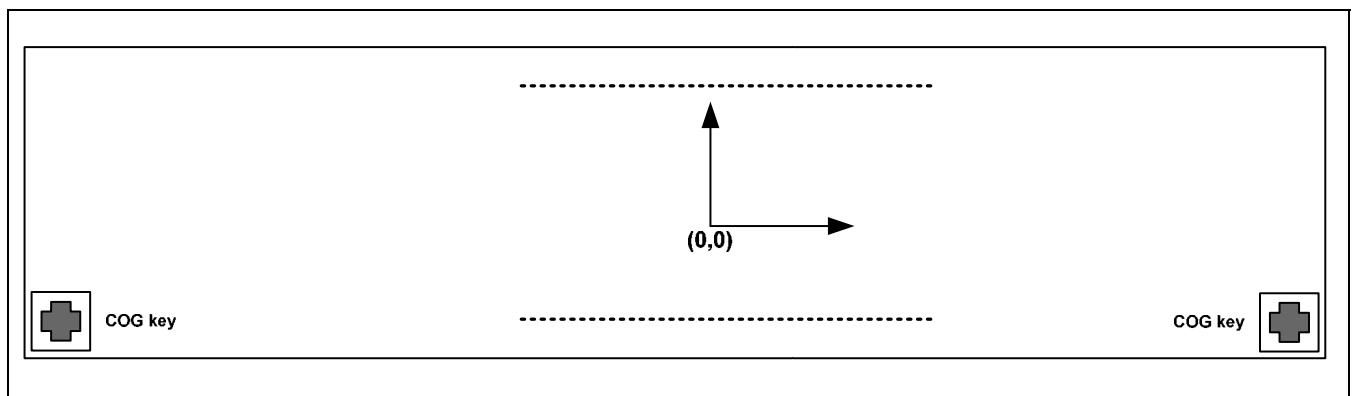
Figure 5. COG Align Key Layout
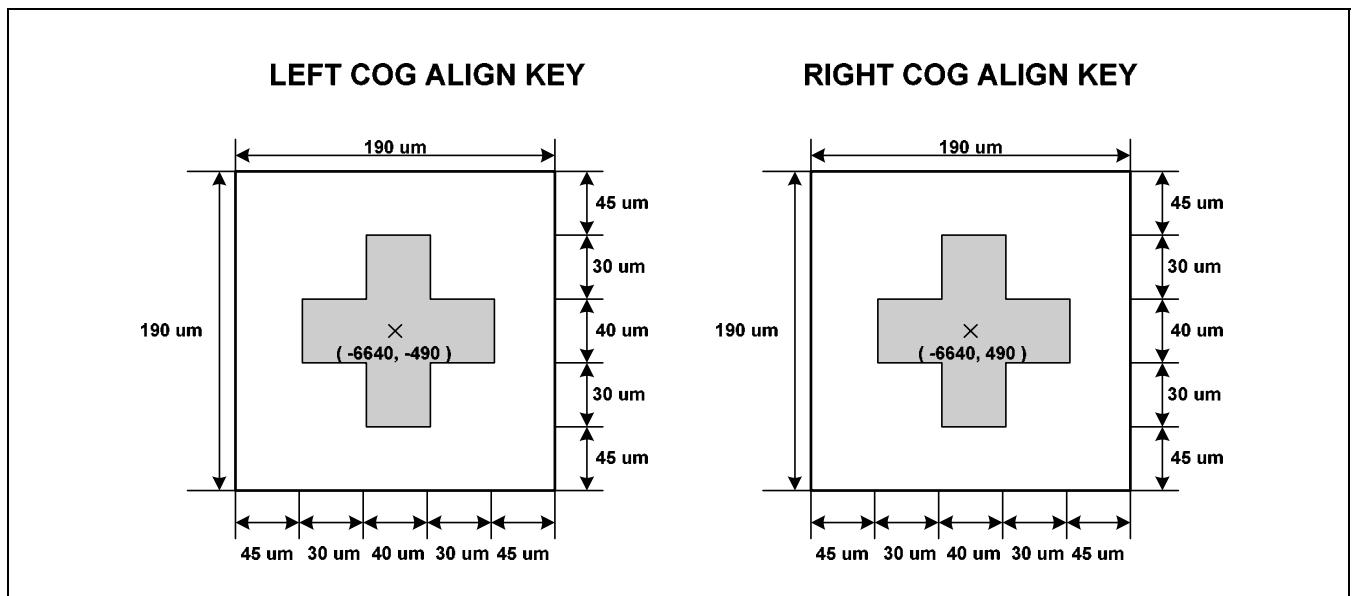
Figure 6. COG Align Key Information

PAD COORDINATES

Table 2. Pad Coordinates

| NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY<1>	-6360	-531	51	VGS	-2360	-531	101	VSS	1640	-531
2	DUMMY<2>	-6280	-531	52	VGS	-2280	-531	102	LSENL	1720	-531
3	STV_L	-6200	-531	53	VSS	-2200	-531	103	VDD3	1800	-531
4	STV_L	-6120	-531	54	ID	-2120	-531	104	LSENR	1880	-531
5	VGH	-6040	-531	55	VDD3	-2040	-531	105	VSS	1960	-531
6	VGH	-5960	-531	56	MS	-1960	-531	106	AVDD	2040	-531
7	VGH	-5880	-531	57	VSS	-1880	-531	107	AVDD	2120	-531
8	VGH	-5800	-531	58	DSSEL	-1800	-531	108	AVDD	2200	-531
9	VGL	-5720	-531	59	VDD3	-1720	-531	109	AVDD	2280	-531
10	VGL	-5640	-531	60	M	-1640	-531	110	AVDD	2360	-531
11	VGL	-5560	-531	61	VSS	-1560	-531	111	GVDD	2440	-531
12	VGL	-5480	-531	62	TEST	-1480	-531	112	GVDD	2520	-531
13	CKV_L	-5400	-531	63	TSI<2>	-1400	-531	113	VDD3	2600	-531
14	CKV_L	-5320	-531	64	TSI<1>	-1320	-531	114	VDD3	2680	-531
15	CKV_L	-5240	-531	65	TSI<0>	-1240	-531	115	VDD3	2760	-531
16	CKVB_L	-5160	-531	66	TSO<1>	-1160	-531	116	VDD	2840	-531
17	CKVB_L	-5080	-531	67	TSO<0>	-1080	-531	117	VDD	2920	-531
18	CKVB_L	-5000	-531	68	RESETB	-1000	-531	118	VDD	3000	-531
19	VCOMOUT	-4920	-531	69	CSB	-920	-531	119	VDD	3080	-531
20	VCOMOUT	-4840	-531	70	SCL	-840	-531	120	RVDD	3160	-531
21	VCOMOUT	-4760	-531	71	SDI	-760	-531	121	RVDD	3240	-531
22	VCOMOUT	-4680	-531	72	PD<0>	-680	-531	122	RVDD	3320	-531
23	VCL	-4600	-531	73	PD<1>	-600	-531	123	RVDD	3400	-531
24	VCL	-4520	-531	74	PD<2>	-520	-531	124	RVDD_REF	3480	-531
25	VCL	-4440	-531	75	PD<3>	-440	-531	125	VCI	3560	-531
26	VCL	-4360	-531	76	PD<4>	-360	-531	126	VCI	3640	-531
27	VGOFF	-4280	-531	77	PD<5>	-280	-531	127	VCI	3720	-531
28	VGOFF	-4200	-531	78	PD<6>	-200	-531	128	VCI	3800	-531
29	VGOFF	-4120	-531	79	PD<7>	-120	-531	129	VCOML	3880	-531
30	VGOFF	-4040	-531	80	PD<8>	-40	-531	130	VCOML	3960	-531
31	AGND	-3960	-531	81	PD<9>	40	-531	131	VCOML	4040	-531
32	AGND	-3880	-531	82	PD<10>	120	-531	132	VCOML	4120	-531
33	AGND	-3800	-531	83	PD<11>	200	-531	133	VCOMH	4200	-531
34	AGND	-3720	-531	84	PD<12>	280	-531	134	VCOMH	4280	-531
35	AGND	-3640	-531	85	PD<13>	360	-531	135	VCOMH	4360	-531
36	VSS	-3560	-531	86	PD<14>	440	-531	136	VCOMH	4440	-531
37	VSS	-3480	-531	87	PD<15>	520	-531	137	CONTACT1	4520	-531
38	VSS	-3400	-531	88	VSS	600	-531	138	CONTACT2	4600	-531
39	VSS	-3320	-531	89	PD<16>	680	-531	139	VCOMOUT	4680	-531
40	VSS	-3240	-531	90	PD<17>	760	-531	140	VCOMOUT	4760	-531
41	VSS	-3160	-531	91	PD<18>	840	-531	141	VCOMOUT	4840	-531
42	VSS	-3080	-531	92	PD<19>	920	-531	142	VCOMOUT	4920	-531
43	VSS	-3000	-531	93	PD<20>	1000	-531	143	CKVB_R	5000	-531
44	VSS	-2920	-531	94	PD<21>	1080	-531	144	CKVB_R	5080	-531
45	VSS	-2840	-531	95	PD<22>	1160	-531	145	CKVB_R	5160	-531
46	AVSS	-2760	-531	96	PD<23>	1240	-531	146	CKV_R	5240	-531
47	AVSS	-2680	-531	97	ENABLE	1320	-531	147	CKV_R	5320	-531
48	AVSS	-2600	-531	98	HSYNC	1400	-531	148	CKV_R	5400	-531
49	AVSS	-2520	-531	99	VSYNC	1480	-531	149	VGL	5480	-531
50	AVSS	-2440	-531	100	DOTCLK	1560	-531	150	VGL	5560	-531

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Table 3. Pad Coordinates (Continued)

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	VGL	5640	-531	201	S<458>	5499	538	251	S<408>	4199	538
152	VGL	5720	-531	202	S<457>	5473	413	252	S<407>	4173	413
153	VGH	5800	-531	203	S<456>	5447	538	253	S<406>	4147	538
154	VGH	5880	-531	204	S<455>	5421	413	254	S<405>	4121	413
155	VGH	5960	-531	205	S<454>	5395	538	255	S<404>	4095	538
156	VGH	6040	-531	206	S<453>	5369	413	256	S<403>	4069	413
157	STV_R	6120	-531	207	S<452>	5343	538	257	S<402>	4043	538
158	STV_R	6200	-531	208	S<451>	5317	413	258	S<401>	4017	413
159	DUMMY<3>	6280	-531	209	S<450>	5291	538	259	S<400>	3991	538
160	DUMMY<4>	6360	-531	210	S<449>	5265	413	260	S<399>	3965	413
161	DUMMY<5>	6591	538	211	S<448>	5239	538	261	S<398>	3939	538
162	DUMMY<6>	6565	413	212	S<447>	5213	413	262	S<397>	3913	413
163	DUMMY<7>	6513	538	213	S<446>	5187	538	263	S<396>	3887	538
164	DUMMY<8>	6487	413	214	S<445>	5161	413	264	S<395>	3861	413
165	DUMMY<9>	6435	538	215	S<444>	5135	538	265	S<394>	3835	538
166	DUMMY<10>	6409	413	216	S<443>	5109	413	266	S<393>	3809	413
167	S<492>	6383	538	217	S<442>	5083	538	267	S<392>	3783	538
168	S<491>	6357	413	218	S<441>	5057	413	268	S<391>	3757	413
169	S<490>	6331	538	219	S<440>	5031	538	269	S<390>	3731	538
170	S<489>	6305	413	220	S<439>	5005	413	270	S<389>	3705	413
171	S<488>	6279	538	221	S<438>	4979	538	271	S<388>	3679	538
172	S<487>	6253	413	222	S<437>	4953	413	272	S<387>	3653	413
173	S<486>	6227	538	223	S<436>	4927	538	273	S<386>	3627	538
174	S<485>	6201	413	224	S<435>	4901	413	274	S<385>	3601	413
175	S<484>	6175	538	225	S<434>	4875	538	275	S<384>	3575	538
176	S<483>	6149	413	226	S<433>	4849	413	276	S<383>	3549	413
177	S<482>	6123	538	227	S<432>	4823	538	277	S<382>	3523	538
178	S<481>	6097	413	228	S<431>	4797	413	278	S<381>	3497	413
179	S<480>	6071	538	229	S<430>	4771	538	279	S<380>	3471	538
180	S<479>	6045	413	230	S<429>	4745	413	280	S<379>	3445	413
181	S<478>	6019	538	231	S<428>	4719	538	281	S<378>	3419	538
182	S<477>	5993	413	232	S<427>	4693	413	282	S<377>	3393	413
183	S<476>	5967	538	233	S<426>	4667	538	283	S<376>	3367	538
184	S<475>	5941	413	234	S<425>	4641	413	284	S<375>	3341	413
185	S<474>	5915	538	235	S<424>	4615	538	285	S<374>	3315	538
186	S<473>	5889	413	236	S<423>	4589	413	286	S<373>	3289	413
187	S<472>	5863	538	237	S<422>	4563	538	287	S<372>	3263	538
188	S<471>	5837	413	238	S<421>	4537	413	288	S<371>	3237	413
189	S<470>	5811	538	239	S<420>	4511	538	289	S<370>	3211	538
190	S<469>	5785	413	240	S<419>	4485	413	290	S<369>	3185	413
191	S<468>	5759	538	241	S<418>	4459	538	291	S<368>	3159	538
192	S<467>	5733	413	242	S<417>	4433	413	292	S<367>	3133	413
193	S<466>	5707	538	243	S<416>	4407	538	293	S<366>	3107	538
194	S<465>	5681	413	244	S<415>	4381	413	294	S<365>	3081	413
195	S<464>	5655	538	245	S<414>	4355	538	295	S<364>	3055	538
196	S<463>	5629	413	246	S<413>	4329	413	296	S<363>	3029	413
197	S<462>	5603	538	247	S<412>	4303	538	297	S<362>	3003	538
198	S<461>	5577	413	248	S<411>	4277	413	298	S<361>	2977	413
199	S<460>	5551	538	249	S<410>	4251	538	299	S<360>	2951	538
200	S<459>	5525	413	250	S<409>	4225	413	300	S<359>	2925	413

Table 4. Pad Coordinates (Continued)

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	S<358>	2899	538	351	S<308>	1599	538	401	S<258>	299	538
302	S<357>	2873	413	352	S<307>	1573	413	402	S<257>	273	413
303	S<356>	2847	538	353	S<306>	1547	538	403	S<256>	247	538
304	S<355>	2821	413	354	S<305>	1521	413	404	S<255>	221	413
305	S<354>	2795	538	355	S<304>	1495	538	405	S<254>	195	538
306	S<353>	2769	413	356	S<303>	1469	413	406	S<253>	169	413
307	S<352>	2743	538	357	S<302>	1443	538	407	S<252>	143	538
308	S<351>	2717	413	358	S<301>	1417	413	408	S<251>	117	413
309	S<350>	2691	538	359	S<300>	1391	538	409	S<250>	91	538
310	S<349>	2665	413	360	S<299>	1365	413	410	S<249>	65	413
311	S<348>	2639	538	361	S<298>	1339	538	411	S<248>	39	538
312	S<347>	2613	413	362	S<297>	1313	413	412	S<247>	13	413
313	S<346>	2587	538	363	S<296>	1287	538	413	S<246>	-13	538
314	S<345>	2561	413	364	S<295>	1261	413	414	S<245>	-39	413
315	S<344>	2535	538	365	S<294>	1235	538	415	S<244>	-65	538
316	S<343>	2509	413	366	S<293>	1209	413	416	S<243>	-91	413
317	S<342>	2483	538	367	S<292>	1183	538	417	S<242>	-117	538
318	S<341>	2457	413	368	S<291>	1157	413	418	S<241>	-143	413
319	S<340>	2431	538	369	S<290>	1131	538	419	S<240>	-169	538
320	S<339>	2405	413	370	S<289>	1105	413	420	S<239>	-195	413
321	S<338>	2379	538	371	S<288>	1079	538	421	S<238>	-221	538
322	S<337>	2353	413	372	S<287>	1053	413	422	S<237>	-247	413
323	S<336>	2327	538	373	S<286>	1027	538	423	S<236>	-273	538
324	S<335>	2301	413	374	S<285>	1001	413	424	S<235>	-299	413
325	S<334>	2275	538	375	S<284>	975	538	425	S<234>	-325	538
326	S<333>	2249	413	376	S<283>	949	413	426	S<233>	-351	413
327	S<332>	2223	538	377	S<282>	923	538	427	S<232>	-377	538
328	S<331>	2197	413	378	S<281>	897	413	428	S<231>	-403	413
329	S<330>	2171	538	379	S<280>	871	538	429	S<230>	-429	538
330	S<329>	2145	413	380	S<279>	845	413	430	S<229>	-455	413
331	S<328>	2119	538	381	S<278>	819	538	431	S<228>	-481	538
332	S<327>	2093	413	382	S<277>	793	413	432	S<227>	-507	413
333	S<326>	2067	538	383	S<276>	767	538	433	S<226>	-533	538
334	S<325>	2041	413	384	S<275>	741	413	434	S<225>	-559	413
335	S<324>	2015	538	385	S<274>	715	538	435	S<224>	-585	538
336	S<323>	1989	413	386	S<273>	689	413	436	S<223>	-611	413
337	S<322>	1963	538	387	S<272>	663	538	437	S<222>	-637	538
338	S<321>	1937	413	388	S<271>	637	413	438	S<221>	-663	413
339	S<320>	1911	538	389	S<270>	611	538	439	S<220>	-689	538
340	S<319>	1885	413	390	S<269>	585	413	440	S<219>	-715	413
341	S<318>	1859	538	391	S<268>	559	538	441	S<218>	-741	538
342	S<317>	1833	413	392	S<267>	533	413	442	S<217>	-767	413
343	S<316>	1807	538	393	S<266>	507	538	443	S<216>	-793	538
344	S<315>	1781	413	394	S<265>	481	413	444	S<215>	-819	413
345	S<314>	1755	538	395	S<264>	455	538	445	S<214>	-845	538
346	S<313>	1729	413	396	S<263>	429	413	446	S<213>	-871	413
347	S<312>	1703	538	397	S<262>	403	538	447	S<212>	-897	538
348	S<311>	1677	413	398	S<261>	377	413	448	S<211>	-923	413
349	S<310>	1651	538	399	S<260>	351	538	449	S<210>	-949	538
350	S<309>	1625	413	400	S<259>	325	413	450	S<209>	-975	413

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Table 5. Pad Coordinates (Continued)

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	S<208>	-1001	538	501	S<158>	-2301	538	551	S<108>	-3601	538
452	S<207>	-1027	413	502	S<157>	-2327	413	552	S<107>	-3627	413
453	S<206>	-1053	538	503	S<156>	-2353	538	553	S<106>	-3653	538
454	S<205>	-1079	413	504	S<155>	-2379	413	554	S<105>	-3679	413
455	S<204>	-1105	538	505	S<154>	-2405	538	555	S<104>	-3705	538
456	S<203>	-1131	413	506	S<153>	-2431	413	556	S<103>	-3731	413
457	S<202>	-1157	538	507	S<152>	-2457	538	557	S<102>	-3757	538
458	S<201>	-1183	413	508	S<151>	-2483	413	558	S<101>	-3783	413
459	S<200>	-1209	538	509	S<150>	-2509	538	559	S<100>	-3809	538
460	S<199>	-1235	413	510	S<149>	-2535	413	560	S<99>	-3835	413
461	S<198>	-1261	538	511	S<148>	-2561	538	561	S<98>	-3861	538
462	S<197>	-1287	413	512	S<147>	-2587	413	562	S<97>	-3887	413
463	S<196>	-1313	538	513	S<146>	-2613	538	563	S<96>	-3913	538
464	S<195>	-1339	413	514	S<145>	-2639	413	564	S<95>	-3939	413
465	S<194>	-1365	538	515	S<144>	-2665	538	565	S<94>	-3965	538
466	S<193>	-1391	413	516	S<143>	-2691	413	566	S<93>	-3991	413
467	S<192>	-1417	538	517	S<142>	-2717	538	567	S<92>	-4017	538
468	S<191>	-1443	413	518	S<141>	-2743	413	568	S<91>	-4043	413
469	S<190>	-1469	538	519	S<140>	-2769	538	569	S<90>	-4069	538
470	S<189>	-1495	413	520	S<139>	-2795	413	570	S<89>	-4095	413
471	S<188>	-1521	538	521	S<138>	-2821	538	571	S<88>	-4121	538
472	S<187>	-1547	413	522	S<137>	-2847	413	572	S<87>	-4147	413
473	S<186>	-1573	538	523	S<136>	-2873	538	573	S<86>	-4173	538
474	S<185>	-1599	413	524	S<135>	-2899	413	574	S<85>	-4199	413
475	S<184>	-1625	538	525	S<134>	-2925	538	575	S<84>	-4225	538
476	S<183>	-1651	413	526	S<133>	-2951	413	576	S<83>	-4251	413
477	S<182>	-1677	538	527	S<132>	-2977	538	577	S<82>	-4277	538
478	S<181>	-1703	413	528	S<131>	-3003	413	578	S<81>	-4303	413
479	S<180>	-1729	538	529	S<130>	-3029	538	579	S<80>	-4329	538
480	S<179>	-1755	413	530	S<129>	-3055	413	580	S<79>	-4355	413
481	S<178>	-1781	538	531	S<128>	-3081	538	581	S<78>	-4381	538
482	S<177>	-1807	413	532	S<127>	-3107	413	582	S<77>	-4407	413
483	S<176>	-1833	538	533	S<126>	-3133	538	583	S<76>	-4433	538
484	S<175>	-1859	413	534	S<125>	-3159	413	584	S<75>	-4459	413
485	S<174>	-1885	538	535	S<124>	-3185	538	585	S<74>	-4485	538
486	S<173>	-1911	413	536	S<123>	-3211	413	586	S<73>	-4511	413
487	S<172>	-1937	538	537	S<122>	-3237	538	587	S<72>	-4537	538
488	S<171>	-1963	413	538	S<121>	-3263	413	588	S<71>	-4563	413
489	S<170>	-1989	538	539	S<120>	-3289	538	589	S<70>	-4589	538
490	S<169>	-2015	413	540	S<119>	-3315	413	590	S<69>	-4615	413
491	S<168>	-2041	538	541	S<118>	-3341	538	591	S<68>	-4641	538
492	S<167>	-2067	413	542	S<117>	-3367	413	592	S<67>	-4667	413
493	S<166>	-2093	538	543	S<116>	-3393	538	593	S<66>	-4693	538
494	S<165>	-2119	413	544	S<115>	-3419	413	594	S<65>	-4719	413
495	S<164>	-2145	538	545	S<114>	-3445	538	595	S<64>	-4745	538
496	S<163>	-2171	413	546	S<113>	-3471	413	596	S<63>	-4771	413
497	S<162>	-2197	538	547	S<112>	-3497	538	597	S<62>	-4797	538
498	S<161>	-2223	413	548	S<111>	-3523	413	598	S<61>	-4823	413
499	S<160>	-2249	538	549	S<110>	-3549	538	599	S<60>	-4849	538
500	S<159>	-2275	413	550	S<109>	-3575	413	600	S<59>	-4875	413

Table 6. Pad Coordinates (Continued)

NO	NAME	X	Y	NO	NAME	X	Y
601	S<58>	-4901	538	651	S<8>	-6201	538
602	S<57>	-4927	413	652	S<7>	-6227	413
603	S<56>	-4953	538	653	S<6>	-6253	538
604	S<55>	-4979	413	654	S<5>	-6279	413
605	S<54>	-5005	538	655	S<4>	-6305	538
606	S<53>	-5031	413	656	S<3>	-6331	413
607	S<52>	-5057	538	657	S<2>	-6357	538
608	S<51>	-5083	413	658	S<1>	-6383	413
609	S<50>	-5109	538	659	DUMMY<11>	-6409	538
610	S<49>	-5135	413	660	DUMMY<12>	-6435	413
611	S<48>	-5161	538	661	DUMMY<13>	-6487	538
612	S<47>	-5187	413	662	DUMMY<14>	-6513	413
613	S<46>	-5213	538	663	DUMMY<15>	-6565	538
614	S<45>	-5239	413	664	DUMMY<16>	-6591	413
615	S<44>	-5265	538				
616	S<43>	-5291	413				
617	S<42>	-5317	538				
618	S<41>	-5343	413				
619	S<40>	-5369	538				
620	S<39>	-5395	413				
621	S<38>	-5421	538				
622	S<37>	-5447	413				
623	S<36>	-5473	538				
624	S<35>	-5499	413				
625	S<34>	-5525	538				
626	S<33>	-5551	413				
627	S<32>	-5577	538				
628	S<31>	-5603	413				
629	S<30>	-5629	538				
630	S<29>	-5655	413				
631	S<28>	-5681	538				
632	S<27>	-5707	413				
633	S<26>	-5733	538				
634	S<25>	-5759	413				
635	S<24>	-5785	538				
636	S<23>	-5811	413				
637	S<22>	-5837	538				
638	S<21>	-5863	413				
639	S<20>	-5889	538				
640	S<19>	-5915	413				
641	S<18>	-5941	538				
642	S<17>	-5967	413				
643	S<16>	-5993	538				
644	S<15>	-6019	413				
645	S<14>	-6045	538				
646	S<13>	-6071	413				
647	S<12>	-6097	538				
648	S<11>	-6123	413				
649	S<10>	-6149	538				
650	S<9>	-6175	413				

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PIN DESCRIPTION

Table 7. Power Supply Pin Description

Symbol	I/O	Description
VDD	Power	System power supply for logic circuit block. As S6F2002 has internal power regulator, VDD range varies with each mode. Non-regulated : +1.8 ~ +2.5 V Regulated : +2.0 V fixed. (connecting RVDD)
VDD3	Power	System power supply for logic interface signal. (VDD3: +1.8V~3.3V)
VSS	Power	System ground level. (0V)
AGND	Power	System ground level for power circuit block. (0V)
AVSS	Power	System ground level for source driver circuit block. (0V)
VCI	Power	System power supply for internal power generation circuit block.
AVDD	Power	System power supply for source driver circuit block.
GVDD	I	Reference voltage for grayscale voltage generator, high level. Connect this pin at AVDD when in usual case.
VGS	I	Reference voltage for grayscale voltage generator, low level. Connect this pin at AVSS when in usual case.

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Table 8. Power Supply Pin Description (Continued)

Symbol	I/O	Description
VCOMOUT	O	A power supply for the TFT- LCD panel counter electrode. Connect this pin to the TFT-LCD panel counter electrode. This output also contributes for equalizing function: When EQ = "High" period, all outputs of source driver (S1 to S492) are shorted to VCOMOUT level (Hi-Z).
VCOMH	O	High level output voltage of VCOMOUT signal. Output voltage level can be established directly by VCM4-0 register setting. Attach a capacitor to this pin for stabilization.
VCOML	O	Low level output voltage of VCOMOUT signal. Output voltage level can be established directly by VDV4-0 register setting. Attach a capacitor to this pin for stabilization.
VGH	Power	A positive power supply for level shifter circuit blocks which output amorphous-silicon gate driving signals such as CKV_L/R, CKVB_L/R, STV_L/R.
VGL	Power	A negative power supply for level shifter circuit blocks which output amorphous-silicon gate driving signals such as CKV_L/R, CKVB_L/R, STV_L/R. It is also used as a power supply for VCL & VGOFF generation circuit block.
VGOFF	O	A voltage output pin for amorphous-silicon gate driver signals which comes from integrated gate level shifter circuits. VGOFF indicates a negative voltage level for the gate-off signal. Connect a capacitor for stabilization.
VCL	O	A voltage output pin for VCOML generation circuit block. VCL is used as a negative power supply pin for VCOML generator. Connect a capacitor for stabilization.

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Table 9. Interface Pin Description

Symbol	I/O	Description
ID	I	ID setting pin for a device code.
CSB	I	Selects the S6F2002: Low: S6F2002 is selected and can be accessed High: S6F2002 is not selected and cannot be accessed Must be tied to VSS level when not in use.
SCL	I	Serial clock input pin for a clock-synchronous serial interface.
SDI	I	Serial data input pin for a clock-synchronous serial interface.
DSSEL	I	Select Dual- / Single- chip operation mode. Low: Operates in the single-chip configuration. High: Operates in the dual-chip configuration.
MS	I	Select Master / Slave operation mode in dual-chip configuration. Low: Operates as a master driver High: Operates as a slave driver Note. In the single-chip configuration, MS should be fixed at 'L', selected as a master driver.
LSENL	I	Output enable signal of ASG level shifters on the left side. Low: CKV_L / CKVB_L / STV_L outputs gate-off (VGOFF) level. High: CKV_L / CKVB_L / STV_L outputs gate control signal traveling from VGH to VGOFF.
LSENR	I	Output enable signal of ASG level shifters on the right side. Low: CKV_R / CKVB_R / STV_R outputs gate-off (VGOFF) level. High: CKV_R / CKVB_R / STV_R outputs gate control signal traveling from VGH to VGOFF.
ENABLE	I	Data enabling signal for using DE Mode.
VSYNC	I	Synchronous signal of frame for using SYNC Mode.
HSYNC	I	Synchronous signal of line for using SYNC Mode.
DOTCLK	I	Dot clock signal.
PD [23:0]	I	Serves as a 24-bit data bus. 8-bit interface: PD [23:16] 24-bit interface: PD [23:0] Unused pins must be connected to VDD3 or VSS level.

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Table 10. Interface Pin Description (Continued)

Symbol	I/O	Description
TEST	I	TEST mode entry pin. This pin is used only for test purpose at vendor-side. Fixed at GND level in user-configuration.
TSI [2:0]	I	Test mode selection pins. These pins are used only for test purpose at vendor-side. Fixed at GND level in user-configuration.
TSO [1:0]	O	Test signal output pins. Leave floating in user-configuration.
VDD3O	Power	VDD3 level used only for I/O pads: Should be connected to VDD3.
VSSO	Power	VSS level used only for I/O pads: Should be connected to VSS.
RESETB	I	Reset pins. Initializes the LSI when low. Must be reset after power-on.
CONTACT1 CONTACT2	-	Pass-through pins. Identical pins at input and output part that is connected without any internal circuitry.

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Table 11. Display Pin Description

Symbol	I/O	Description
S1 – S492	O	Source driver output pins. S1, S4, S7, ... S(3n-2) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-1) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
STV_L STV_R	O	TFT-LCD gate shift start pulse for amorphous-silicon gate panel.
CKV_L CKV_R	O	TFT-LCD gate shift clock for amorphous-silicon gate panel.
CKVB_L CKVB_R	O	TFT-LCD gate shift clock for amorphous-silicon gate panel.
M	O	Output pin for AC-cycle signal

Table 12. Internal Power Regulator Pin Description

Symbol	I/O	Description
RVDD	O	Internal generated power supply output so called Regulated-VDD. When VDD3 exceeds 2.5V, VDD should be connected to RVDD instead of external VDD3 to protect internal logic circuit and to obtain low-power condition. Attach a capacitor to this pin for stabilization.
RVDD_REF	I	Reference voltage input pin for generating VCOMH / VCOML level. This pin should be connected to RVDD outputs.

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POWER SUPPLY CONFIGURATION

S6F2002 has internal power regulator named RVDD circuit. Regulated voltage output is 2.0V. By use of this circuit block, damage on internal logic circuit by excessive power supply can be prohibited. Furthermore, lower power consumption can be obtained either. Detailed power connection example and application setup are depicted from figure.7 to figure.9 with various power levels which are applied.

CASE 1. DUAL POWER SUPPLY SYSTEM 1
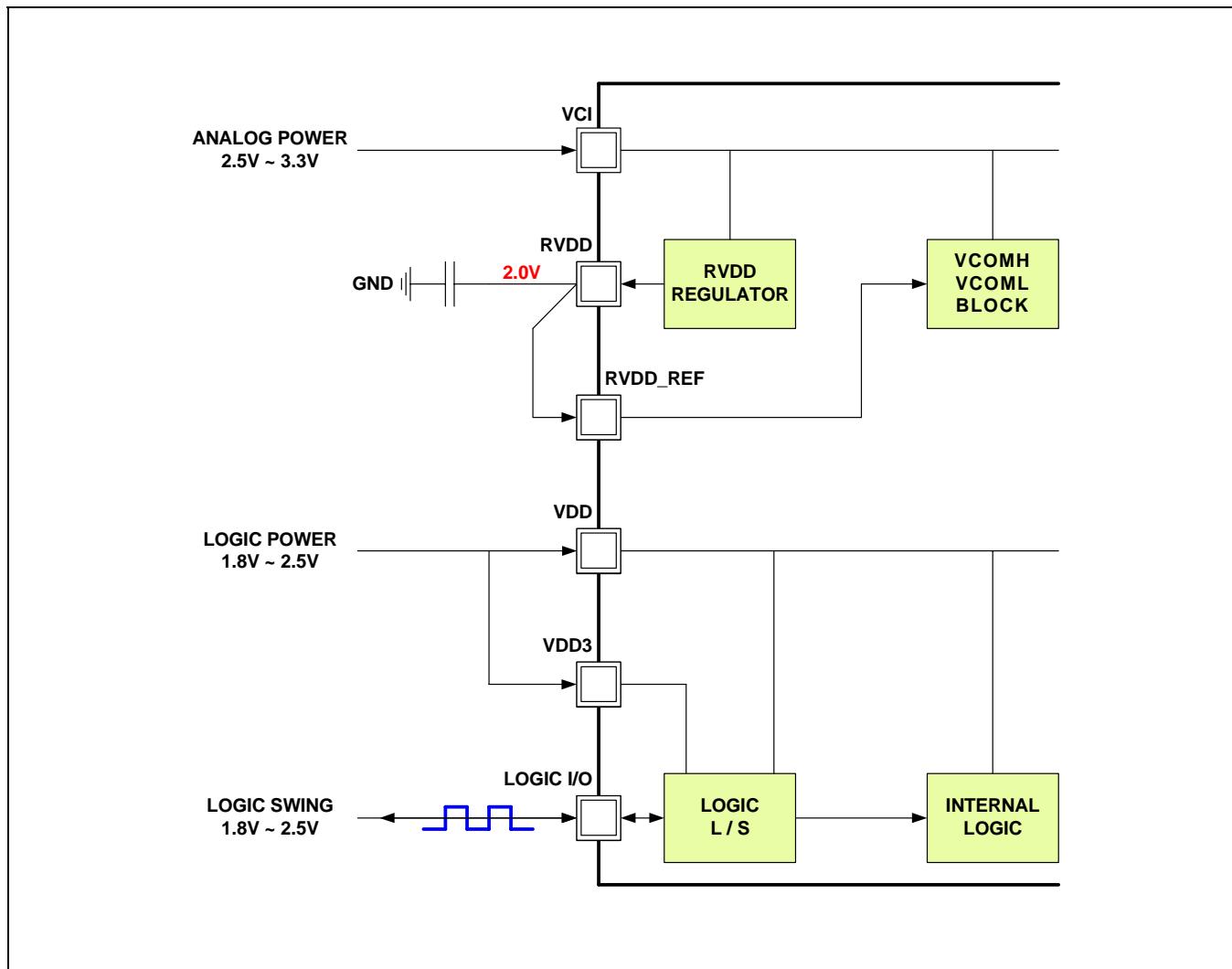
Figure 7. Dual Power Supply System : VDD < 2.5V

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CASE 2. DUAL POWER SUPPLY SYSTEM 2
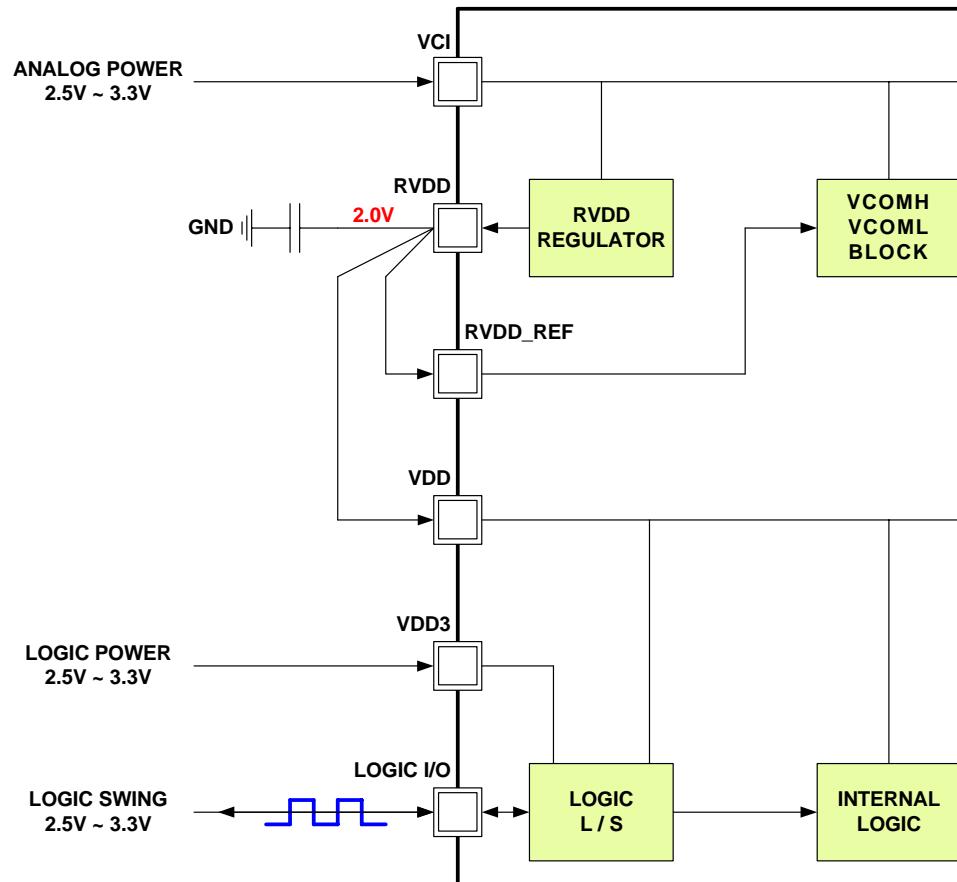
Figure 8. Dual Power Supply System : VDD > 2.5V

CASE 3. SINGLE POWER SUPPLY SYSTEM
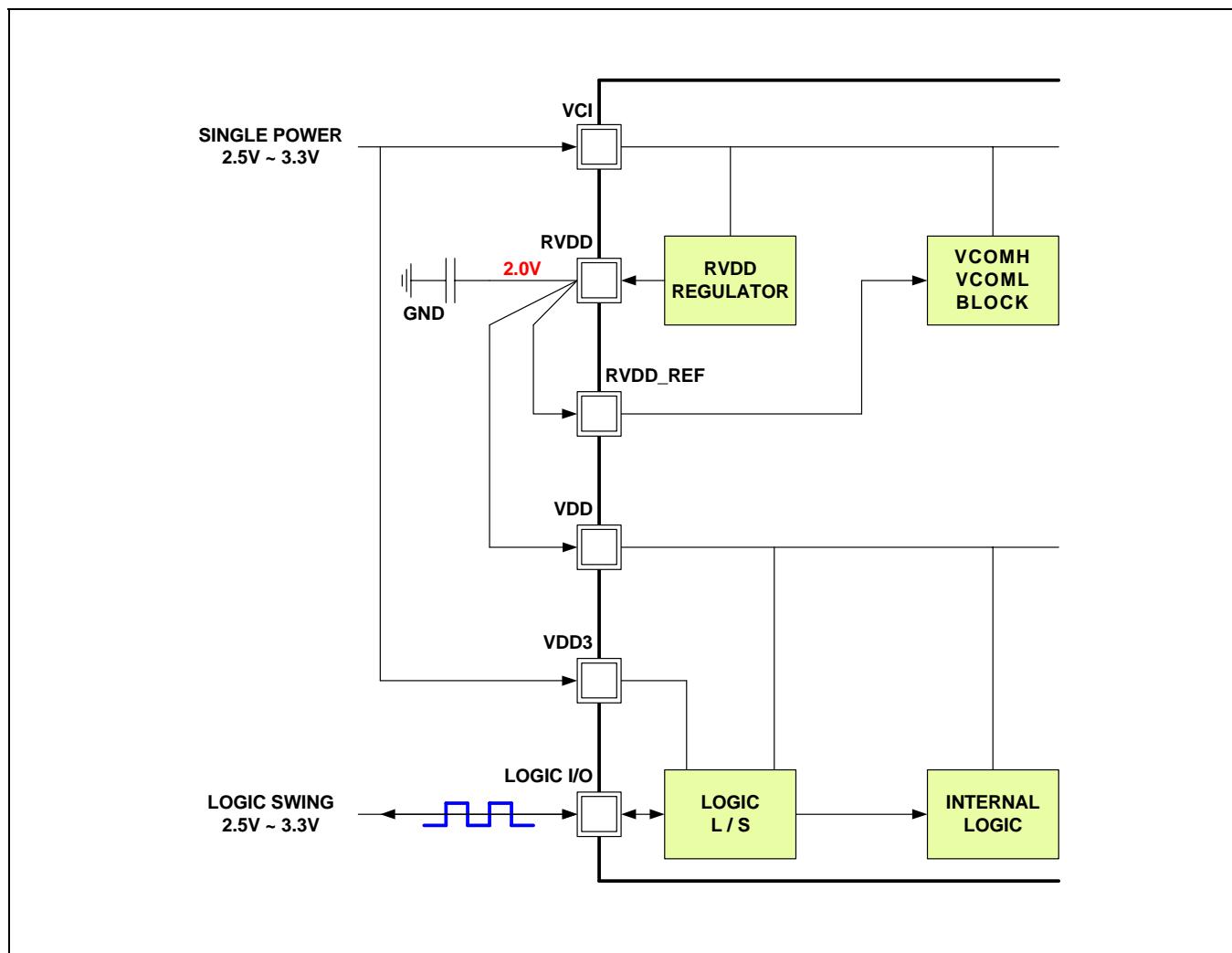
Figure 9. Single Power Supply System

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FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

The S6F2002 has a Serial Peripheral Interface port (SPI).
This block receives instructions and transfers the data to the internal control register for power control, display control, gamma adjustment. (to control the power circuit, display circuit and gamma adjustment circuit.).

Table 13. Register Selection (Serial Peripheral Interface)

R/W Bit	RS Bit	Operations
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers
1	1	Reads Instructions

EXTERNAL INTERFACE (RGB-I/F)

The S6F2002 supports RGB interface as an external interface for motion picture display.
RGB display data of one line(from S1 to S492) are latched to the data latch register through parallel data bus PD in orderly. If one line data is latched, data is transferred to the source driver amp and then the data of data latch register is displayed.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates LCD driver voltages which correspond to the grayscale levels as specified in the grayscale Υ-adjusting resistor. 262,144 possible colors can be displayed at the same time. For details, see the Υ-adjusting resistor.

DISPLAY TIMING CONTROL

The timing generator generates the interface signals such as STV, CKV, CKVB through the embedded level shifter for amorphous-silicon gate driver.

LIQUID CRYSTAL DISPLAY DRIVER CIRCUIT

The liquid crystal display driver circuit consists of 492 source drivers (S1 to S492).
Display pattern data are latched when 492-bit data have arrived. The latched data then enable the source drivers to generate drive waveform outputs. The SS bit can change the shift direction of 492-bit data by selecting an appropriate direction for the device-mounted configuration.

POWER GENERATION CIRCUIT

Power generation circuit generates VCL, VGOFF, VcomH, VcomL and VCOMOUT voltages which are related to display the TFT-LCD panel.

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DESCRIPTION OF POWER GENERATION CIRCUIT

Figure.10 shows a block diagram of reference power generating circuit of S6F2002.

The Vcom generation circuit consists of VcomH generation circuit, VcomL generation circuit and VCOMOUT switching stage which drives counter-electrode of TFT-LCD panel directly. VcomH generation circuit produces high level of Vcom output by embedded voltage-adjustment circuit & voltage follower as an output stage. Voltage level of VcomH is set by VCM4-0 register and is ranging from 3.0V to 4.5V. VcomL generation circuit produces low level of Vcom output by embedded voltage-adjustment circuit & voltage follower as an output stage. Voltage level of VcomL is set by VDV4-0 register and is ranging from -1.0V to 1.0V. There's no relationship bewean set values of VcomH & VcomL because they're set by independent analog circuits.

VCL & VGOFF are generated from VGL voltage with some equations as follows: $|VGOFF| = 0.7 \times |VGL|$, $|VCL| = 0.2 \times |VGL|$. VCL provides negative power supply for VcomL circuit. VGOFF serves as a negative voltage reference for ASG level shifter.
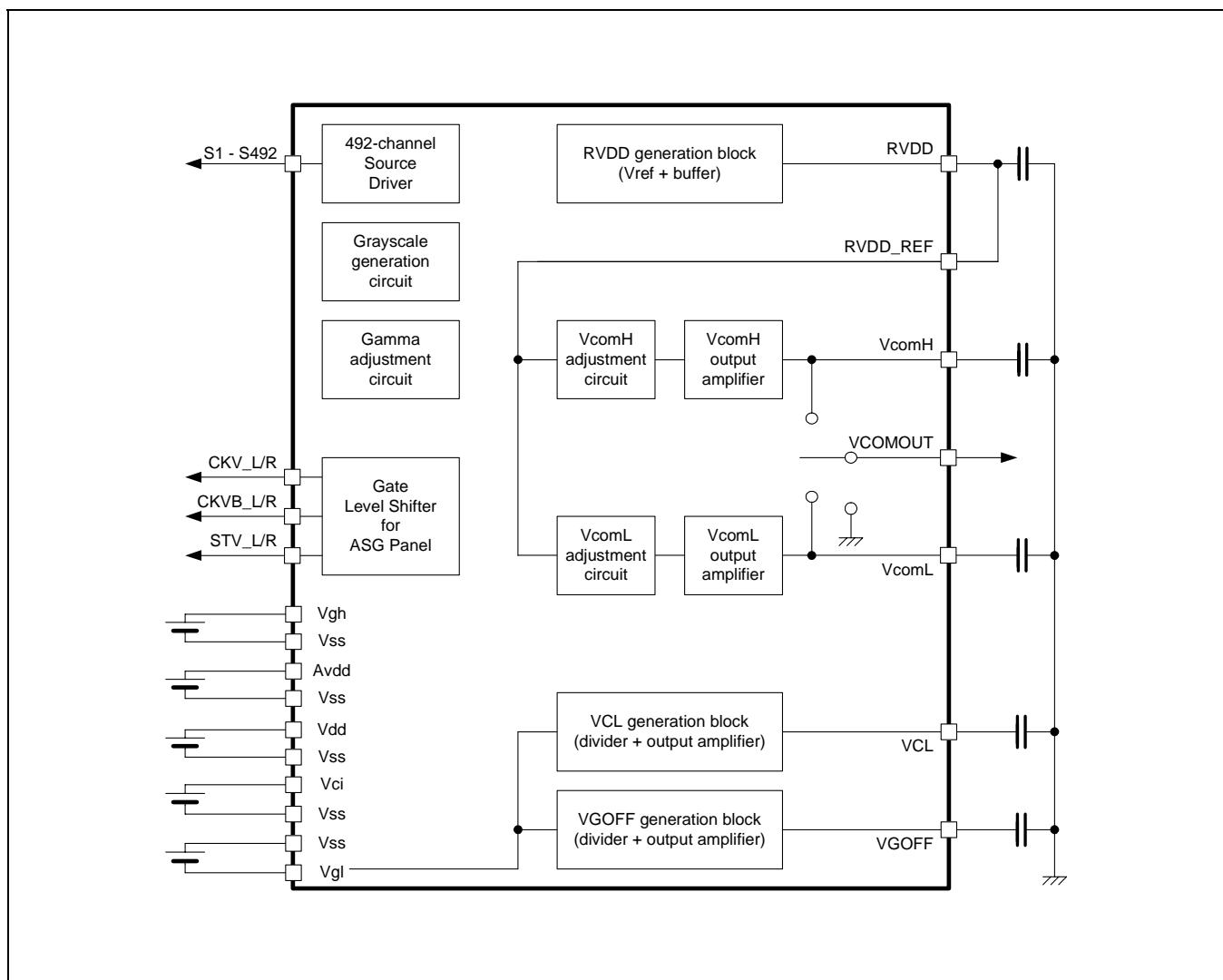

Figure 10. Reference Power Generation Block Diagram

Notes: Use the 1uF capacitor.

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PATTERN DIAGRAM OF THE VOLTAGE SETTING

The following figure shows a pattern diagram of the voltage settings.
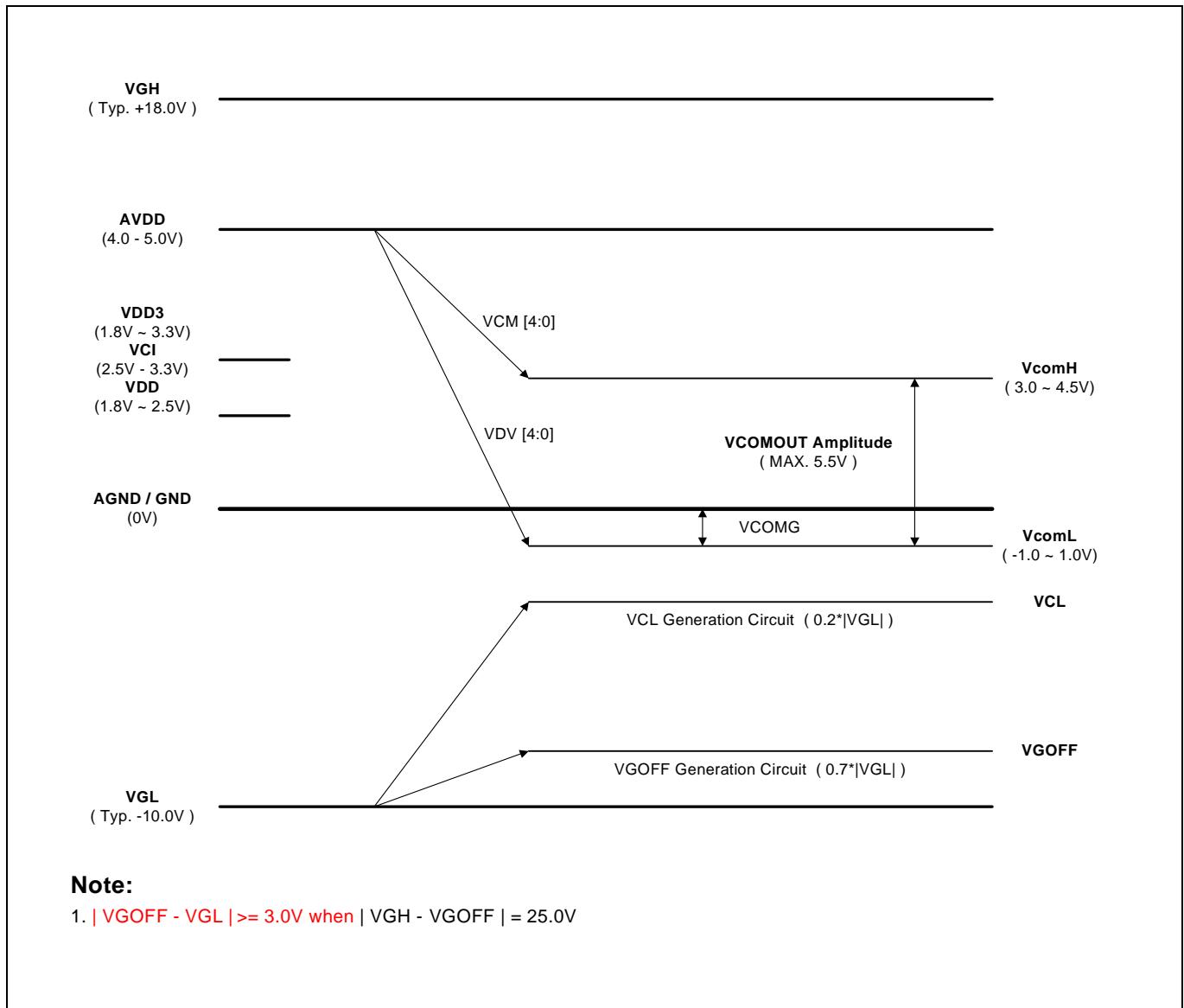
Figure 11. Pattern Diagram Of Internal Voltage Setting

INSTRUCTIONS

OUTLINE

The operation of the S6F2002 is determined by signals sent through Serial Peripheral Interface. These signals include the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0), make up the S6F2002 instructions.

There are five categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Set grayscale level for the internal grayscale palette table

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INSTRUCTION TABLE

Reg No.	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
-										ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
01h	IM	NMD	SSMD	0	0	0	0	0	REV	0	0	NL4	NL3	NL2	NL1	NL0
02h	0	0	DS1	DS0	0	CHS1	CHS0	0	DF1	DF0	0	0	RGB1	RGB0	0	0
03h	VPL	HPL	DPL	EPL	0	0	0	SS	0	0	0	0	0	0	STB	0
04h	0	CLW2	CLW1	CLW0	0	0	0	0	0	0	GAON	0	SDR	0	0	0
05h	NW1	NW0	0	DSC	0	0	0	GIF	FHN	0	FTN1	FTN0	0	0	FWI1	FWI0
06h	0	0	0	0	0	0	0	VBP8	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
07h	0	0	0	0	0	0	HBP9	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
08h	0	0	0	SDT2	SDT1	SDT0	0	0	0	0	0	EQ2	EQ1	EQ0	0	0
09h	0	EXM	0	0	GON	0	POC	0	0	SAP2	SAP1	SAP0	0	AP2	AP1	AP0
0ah	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
10h	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
11h	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
12h	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
13h	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
14h	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
15h	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
16h	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
17h	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
18h	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
19h	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40

INSTRUCTION DESCRIPTIONS

Ensure that you are aware of the assignments of instruction bits (IB15-0) for each interface that are illustrated below.

INDEX (IR)

The index instruction specifies the control register indexes (R00h to R4Fh). It sets the register number in the range of 0000000 to 1111111 in binary form. However, do not access to index register and instruction bit that is not allocated in index register.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 12. Index Instruction

STATUS READ (SR)

The status read instruction reads the internal status of the S6F2002.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 13. Status Read Instruction

ID READ (R00H)

The ID read instruction reads the device index of S6F2002 : when perform this instruction, 2002H is read.

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	O	O	1	O	O	O	O	O	O	O	O	O	O	O	1	O

Figure 14. ID Read Instruction

DISPLAY INTERFACE CONTROL (R01H)

RW	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		IM	NMD	SSMD	O	O	O	O	O	REV	O	O	NL4	NL3	NL2	NL1	NL1

Figure 15. Display Interface Control Instruction

IM : Specify the PD data weight.
        IM = "0" : 24bits interface
        IM = "1" : 8bits interface

NMD : Specify the ASG format.
        NMD = "0" : Normal ASG
        NMD = "1" : Double ASG

SSMD : Specify the interface mode.
        SSMD = "0" : SYNC Mode
        SSMD = "1" : DE Mode

REV : Reverses all character and graphics display sections .
        REV = "0" : Normally White Panel
        REV = "1" : Normally Black Panel

Table 14. REV Bit And Source Output Level Of Displayed Area

REV	Data	Source Output Level of Displayed Area	
		Positive Polarity	**Negative Polarity**
0	6'b000000 ⋮ 6'b111111	V0 ⋮ V63	V63 ⋮ V0
1	6'b000000 ⋮ 6'b111111	V63 ⋮ V0	V0 ⋮ V63

Preliminary

NL4–0 : Specify number of lines for the LCD drive. Number of lines for the LCD drive can be adjusted for every eight raster-rows. The selected size should be larger than or equal to the panel size to be driven.

Table 15. NL Bits And Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster Rows	Gate- Lines Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	176RGB X 16	16	G1 to G16
0	0	0	1	0	176RGB X 24	24	G1 to G24
0	0	0	1	1	176RGB X 32	32	G1 to G32
0	0	1	0	0	176RGB X 40	40	G1 to G40
0	0	1	0	1	176RGB X 48	48	G1 to G48
0	0	1	1	0	176RGB X 56	56	G1 to G56
0	0	1	1	1	176RGB X 64	64	G1 to G64
0	1	0	0	0	176RGB X 72	72	G1 to G72
0	1	0	0	1	176RGB X 80	80	G1 to G80
0	1	0	1	0	176RGB X 88	88	G1 to G88
0	1	0	1	1	176RGB X 96	96	G1 to G96
0	1	1	0	0	176RGB X 104	104	G1 to G104
0	1	1	0	1	176RGB X 112	112	G1 to G112
0	1	1	1	0	176RGB X 120	120	G1 to G120
0	1	1	1	1	176RGB X 128	128	G1 to G128
1	0	0	0	0	176RGB X 136	136	G1 to G136
1	0	0	0	1	176RGB X 144	144	G1 to G144
1	0	0	1	0	176RGB X 152	152	G1 to G152
1	0	0	1	1	176RGB X 160	160	G1 to G160
1	0	1	0	0	176RGB X 168	168	G1 to G168
1	0	1	0	1	176RGB X 176	176	G1 to G176
1	0	1	1	0	176RGB X 184	184	G1 to G184
1	0	1	1	1	176RGB X 192	192	G1 to G192
1	1	0	0	0	176RGB X 200	200	G1 to G200
1	1	0	0	1	176RGB X 208	208	G1 to G208
1	1	0	1	0	176RGB X 216	216	G1 to G216
1	1	0	1	1	176RGB X 224	224	G1 to G224
1	1	1	0	0	176RGB X 232	232	G1 to G232
1	1	1	0	1	176RGB X 240	240	G1 to G240

DISPLAY DATA CONTROL (R02H)

RW	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	DS1	DS0	0	CHS1	CHS0	0	DF1	DF0	0	0	RGB1	RGB2	0	0

Figure 16. Display Data Control Instruction

DS1-0 : Select relationship between input data type and output data type.

Table 16. DS Bits Setting

DS1	DS0	Input	Output
0	0	Stripe / Delta	Stripe / Delta
0	1	Delta	Stripe
1	0	Stripe	Delta
1	1	Setting Inhibited	

CHS1-0 : Select channel length.

Table 17. CHS Bits Setting

CHS1	CHS0	Channel Length
0	0	384 (128 RGB)
0	1	480 (160 RGB)
1	0	492 (164 RGB)
1	1	Setting Inhibited

DF1-0 : Select data format when 8-bit interface (IM=1).

Table 18. DF Bits Setting

DF1	DF0	Data Format
0	0	RGB RGB
0	1	RGBX RGBX
1	0	XRGB XRGB
1	1	Setting Inhibited

Note : RGBX (X: Dummy Data)

RGB1-0 : Select RGB data format.

Table 19. RGB Bits Setting

RGB1	RGB0	Source Output (n=0~163)		
		S(3n+1)	S(3n+2)	S(3n+3)
0	0	R	G	B
0	1	B	G	R
1	0	G	R	B
1	1	R	B	G

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ENTRY MODE (R03H)

RW	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		VPL	HPL	DPL	EPL	O	O	O	SS	O	O	O	O	O	O	STB	O

Figure 17. Entry Mode Instruction

VSPL : Reverses the polarity of the VSYNC signal.
     VSPL= "0": VSYNC is low active.
     VSPL= "1": VSYNC is high active.

HSPL : Reverses the polarity of the HSYNC signal.
     HSPL= "0": HSYNC is low active.
     HSPL= "1": HSYNC is high active.

DPL : Reverses the polarity of the DOTCLK signal.
     DPL= "0": Display data is fetched at rising edge of DOTCLK.
     DPL= "1": Display data is fetched at falling edge of DOTCLK.

EPL : Set the polarity of ENABLE pin while using DE interface mode.
     EPL = "0": ENABLE = "Low" / write data of PD23-0
             ENABLE = "High" / don't write data of PD23-0
     EPL = "1": ENABLE = "High" / write data of PD23-0
             ENABLE = "Low" / don't write data of PD23-0

SS : Selects the output shift direction of the source driver.
     SS= "0": S1~S3   S490~S492
     SS= "1": S490~S492   S1~S3

STB : When STB = 1, S6F2002 enters 'stand-by' mode, where display operation completely stops with halting all the internal operations. Further, all the external clock pulses are blocked to prevent unnecessary power consumption. For more information, please refer to the Stand-by Mode section. Only the following instructions can be executed during the stand-by mode.

   - Standby mode cancel (STB = "0")

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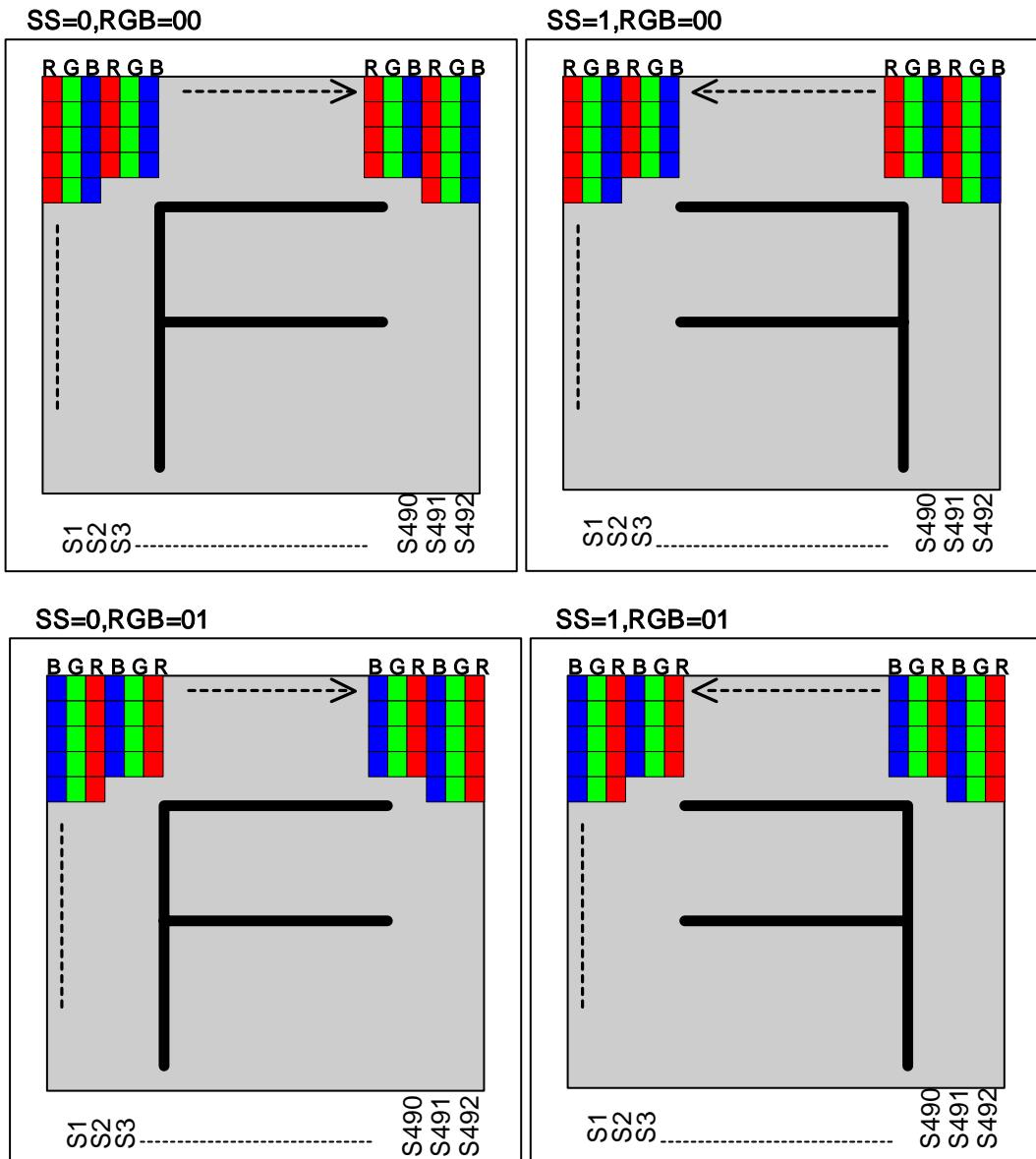
Figure 18. Display Direction According To SS, RGB

GATE CONTROL 1 (R04H)

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	O	CLW2	CLW1	CLW0	O	O	O	O	O	O	GAON	O	SDR	O	O	O

Figure 19. Gate Control1 Instruction
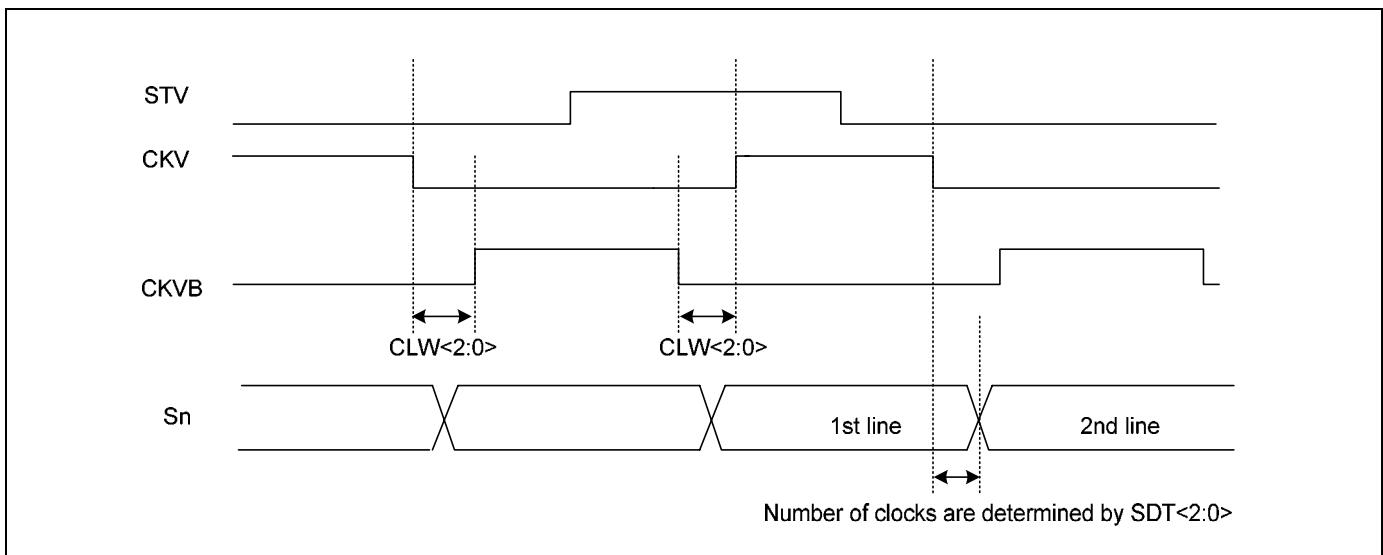
Figure 20. CLW bits

CLW2-0 : Specify the pulse output timing of the CKV and CKVB signal.

Table 20. CLW Bits Setting

CLW2	CLW1	CLW0	Pulse Output Timing of CKVB (DOTCLK)	
			24 Bit Interface (IM=0)	8 Bit Interface (IM=1)
0	0	0	0 clock	0 clock
0	0	1	8 clock	24 clock
0	1	0	16 clock	48 clock
0	1	1	24 clock	72 clock
1	0	0	32 clock	96 clock
1	0	1	40 clock	120 clock
1	1	0	48 clock	144 clock
1	1	1	56 clock	168 clock

NOTE: The values indicate the number of clocks after the falling edge of CKV & CKVB.

GAON : Gate all on.

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SDR : Select odd or even line by STV_L/R, CKV_L/R and CKVB_L/R when Double ASG(NMD="1")

  SDR = "0" : STV_R, CKV_R, CKVB_R drive odd line

    STV_L, CKV_L, CKVB_L drive even line

  SDR = "1" : STV_L, CKV_L, CKVB_L drive odd line

    STV_R, CKV_R, CKVB_R drive even line

GATE CONTROL2 (R05H)

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NW1	NW0	O	DSC	O	O	O	GIF	FHN	O	FTI1	FTI0	O	O	FWI1	FWI0

Figure 21. Gate Control2 Instruction

NW1-0 : Specify the number of raster-rows that will alternate in the line inversion waveform.

Table 21. NW Bits Setting

NW1	NW0	Line Inversion
0	0	Frame Inversion
0	1	1-Line Inversion
1	0	2-Line Inversion
1	1	Setting Inhibited
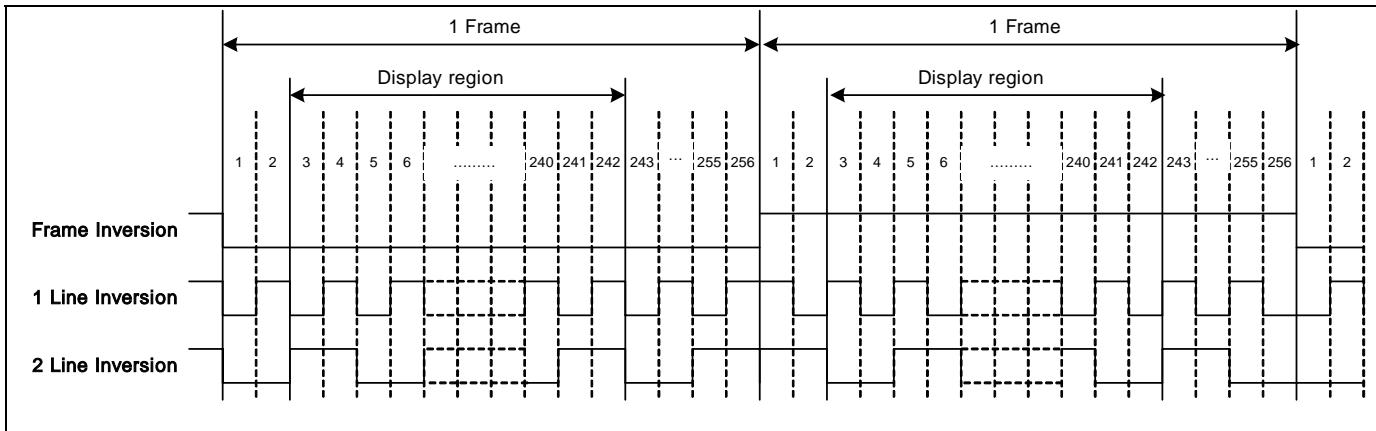
Figure 22. Frame / Line Inversion Timing

DSC : Specify state of gate control signals (STV_L/R, CKV_L/R, CKVB_L/R).

  DSC = "0" : Gate control signals are disable. (fixed to VGOFF level)

  DSC = "1" : Gate control signals are enable. (either VGH or VGOFF)

GIF : Specify type of gate control signals.

  GIF = "0" : STV is fixed by FWI, FTI and FHN when SYNC Mode (SSMD=0).

    STV is fixed as width as 2 horizontal period when DE Mode (SSMD=1).

  GIF = "1" : STV is fixed as width as 1 horizontal period.
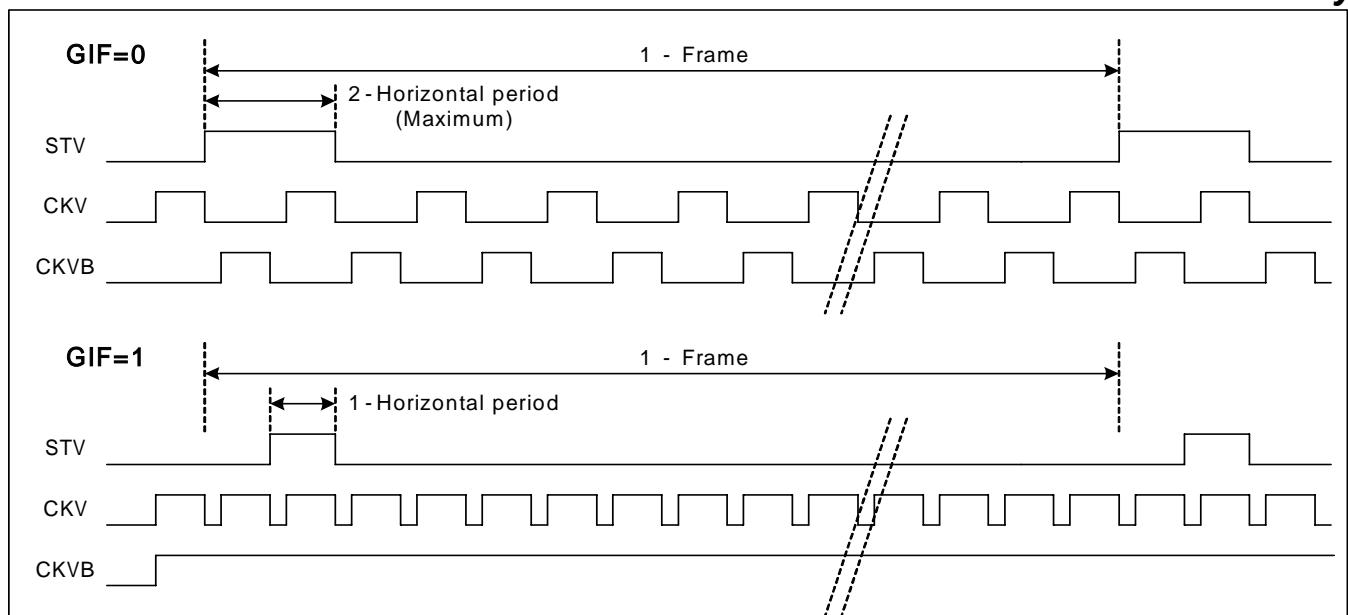
Figure 23. Gate Output Control Waveform1

FHN : Specify period of STV when SYNC Mode(SSMD=0).

       FHN = "0" : The width of STV is fixed by FWI.

       FHN = "1" : The width of STV is fixed as delayed 1H by FTI and next 1H.

FTI1-0 : Specify start point of STV when SYNC Mode(SSMD=0).

Table 22. FTI Bits Setting

FTI1	FTI0	Delay amount	
		24 bit I/F	**8 bit I/F**
0	0	0 clock	0 clock
0	1	7 clock	21 clock
1	0	17 clock	51 clock
1	1	37 clock	111 clock

FWI1-0 : Specify width of STV when SYNC Mode(SSMD=0).

Table 23. FWI Bits Setting

FWI1	FWI0	Width of STV	
		24 bit I/F	**8 bit I/F**
0	0	10 clock	30 clock
0	1	40 clock	120 clock
1	0	80 clock	240 clock
1	1	1 H Period	

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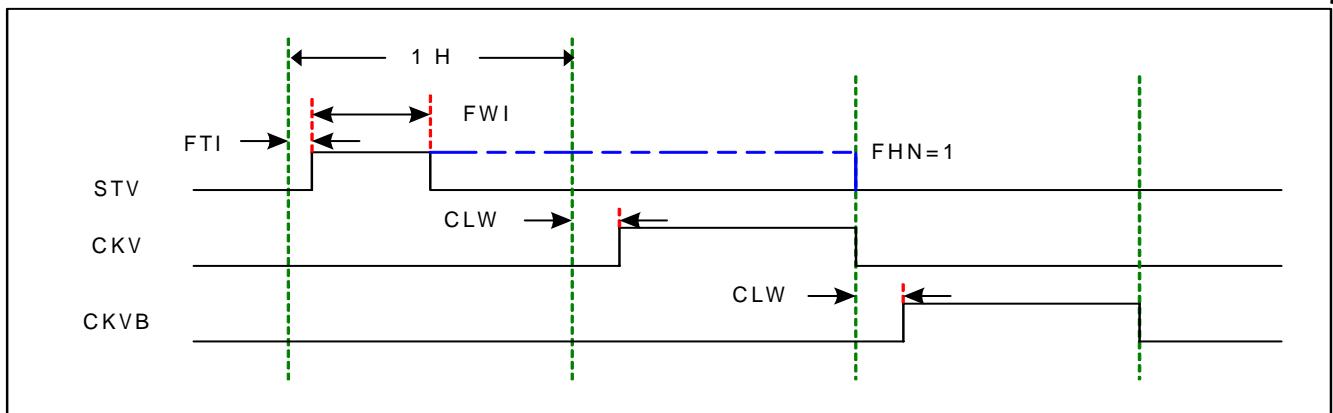
Figure 24. Gate Output Control Waveform2

DISPLAY CONTROL1 (R06H)

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	O	O	O	O	O	O	O	VBP8	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 25. Display Control1 Instruction

VBP8-0 : Vertical back porch. (3H < VBP < 512H)

DISPLAY CONTROL2 (R07H)

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	O	O	O	O	O	O	HBP9	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 26. Display Control2 Instruction

HBP9-0 : Horizontal back porch. (7clock < HBP < 1024clock)

Preliminary

SOURCE OUTPUT TIMING CONTROL (R08H)

RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SDT2	SDT1	SDT0	0	0	0	0	0	EQ2	EQ1	EQ0	0	0

Figure 27. Source Output Timing Control Instruction

SDT1-0 : Specify the timing on which a source signal is output after falling edge of a gate signal.

Table 24. SDT Bits Setting

SDT2	SDT1	SDT0	Delay amount of the source output (DOTCLK)	
			24 Bit Interface (IM=0)	8 Bit Interface (IM=1)
0	0	0	0 clock	0 clock
0	0	1	8 clock	24 clock
0	1	0	16 clock	48 clock
0	1	1	24 clock	72 clock
1	0	0	32 clock	96 clock
1	0	1	40 clock	120 clock
1	1	0	48 clock	144 clock
1	1	1	56 clock	168 clock

EQ2-0 : Equalized period is added as specified by bits of EQ2-0. The equalization signal is output for AC raster-rows.

Table 25. EQ Bits Setting

EQ2	EQ1	EQ0	Equalizing Period (DOTCLK)	
			24 Bit Interface (IM=0)	8 Bit Interface (IM=1)
0	0	0	Not equalized	Not equalized
0	0	1	16 clock	48 clock
0	1	0	32 clock	96 clock
0	1	1	48 clock	144 clock
1	0	0	64 clock	192 clock
1	0	1	80 clock	240 clock
1	1	0	96 clock	288 clock
1	1	1	112 clock	336 clock

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POWER CONTROL 1 (R09H)

RW	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	EXM	0	0	GON	0	POC	0	0	SAP2	SAP1	SAP0	0	AP2	AP1	AP0

Figure 28. Power Control1 Instruction

EXM : Disable all the internal VCOM generation circuits such as VcomH / VcomL amplifiers, bias circuits, bleeder resistors, VCOMOUT switching circuit, etc. 'EXM' instruction is useful to suppress additional power consumption when S6F2002 works in an external-VCOM driving configuration.

Table 26. EXM Bit And Power Block Status

EXM	STATUS		
0	Normal Operation		
1	Disabled the internal VCOM generation circuits.		
	Blocks	Status	
	VcomH	Not generated (OPA disabled, Hi-Z)	
	VcomL	Not generated (OPA disabled, Hi-Z)	
	VCOMOUT	Stop switchig (M signal blocked, VCOMOUT: GND)	

GON : VCOMOUT level is GND when GON = 0.

Table 27. GON Bit and VCOMOUT

GON	VCOMOUT
0	GND fixed
1	Normal Operation

POC: power control.
　　　POC = "0" : White Display
　　　POC = "1" : Normal Display

Preliminary

SAP2-0: The amount of fixed current from the fixed current source in the operational amplifier for the source driver is adjusted. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when SAP2-0 = "000", the current consumption can be reduced by ending the operational amplifier operation.

Table 28. SAP Bits Setting

SAP2	SAP1	SAP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier stops.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

AP2–0: The amount of fixed current in the operational amplifier for the power supply can be adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = "000", the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

Table 29. AP Bits Setting

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Stop operation of the operational amplifiers.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

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POWER CONTROL 2 (R0AH)

R W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		O	O	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	O	O	O	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 29. Power Control2 Instruction

VCOMG : When VCOMG=0, VcomL voltage is fixed to GND and internal circuits which make VcomL are disabled. Therefore, low power consumption is accomplished. When VCOMG = 0, VDV4-0 register setting is invalid. In this case, adjustment of VCOMOUT amplitude is determined only to VcomH by VCM4-0 setting.

Table 30. VCOMG Bit And VcomL

VCOMG	VcomL
0	GND fixed
1	Voltage level set by VDV4-0

VDV4-0 : Set VcomL voltage which is a lower level voltage of VCOMOUT. VcomL voltage is designated directly by VDV4-0 register value ranging from -1.0V to 1.0V in 32 steps. Unit step voltage is around 32mV.

Table 31. VDV4-0 vs VcomL Voltage

VDV4	VDV3	VDV2	VDV1	VDV0	VcomL	VDV4	VDV3	VDV2	VDV1	VDV0	VcomL
0	0	0	0	0	1.000 V	1	0	0	0	0	-0.032 V
0	0	0	0	1	0.935 V	1	0	0	0	1	-0.097 V
0	0	0	1	0	0.871 V	1	0	0	1	0	-0.161 V
0	0	0	1	1	0.806 V	1	0	0	1	1	-0.226 V
0	0	1	0	0	0.742 V	1	0	1	0	0	-0.290 V
0	0	1	0	1	0.677 V	1	0	1	0	1	-0.355 V
0	0	1	1	0	0.613 V	1	0	1	1	0	-0.419 V
0	0	1	1	1	0.548 V	1	0	1	1	1	-0.484 V
0	1	0	0	0	0.484 V	1	1	0	0	0	-0.548 V
0	1	0	0	1	0.419 V	1	1	0	0	1	-0.613 V
0	1	0	1	0	0.355 V	1	1	0	1	0	-0.677 V
0	1	0	1	1	0.290 V	1	1	0	1	1	-0.742 V
0	1	1	0	0	0.226 V	1	1	1	0	0	-0.806 V
0	1	1	0	1	0.161 V	1	1	1	0	1	-0.871 V
0	1	1	1	0	0.097 V	1	1	1	1	0	-0.935 V
0	1	1	1	1	0.032 V	1	1	1	1	1	-1.000 V

VCM4-0 : Set VcomH voltage which is a upper level voltage of VCOMOUT. VcomH voltage is designated directly by VCM4-0 register value ranging from 3.0V to 4.5V in 32 steps. Unit step voltage is about 16mV.

Table 32. VCM4-0 vs VcomH Voltage

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	3.000 V	1	0	0	0	0	3.774 V
0	0	0	0	1	3.048 V	1	0	0	0	1	3.823 V
0	0	0	1	0	3.097 V	1	0	0	1	0	3.871 V
0	0	0	1	1	3.145 V	1	0	0	1	1	3.919 V
0	0	1	0	0	3.194 V	1	0	1	0	0	3.968 V
0	0	1	0	1	3.242 V	1	0	1	0	1	4.016 V
0	0	1	1	0	3.290 V	1	0	1	1	0	4.065 V
0	0	1	1	1	3.339 V	1	0	1	1	1	4.113 V
0	1	0	0	0	3.387 V	1	1	0	0	0	4.161 V
0	1	0	0	1	3.435 V	1	1	0	0	1	4.210 V
0	1	0	1	0	3.484 V	1	1	0	1	0	4.258 V
0	1	0	1	1	3.532 V	1	1	0	1	1	4.306 V
0	1	1	0	0	3.581 V	1	1	1	0	0	4.355 V
0	1	1	0	1	3.629 V	1	1	1	0	1	4.403 V
0	1	1	1	0	3.677 V	1	1	1	1	0	4.452 V
0	1	1	1	1	3.726 V	1	1	1	1	1	4.500 V

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GAMMA CONTROL (R10H TO R19H)

	RW	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R10	W	1	O	O	O	O	O	PRP12	PRP11	PRP10	O	O	O	O	O	PRP02	PRP01	PRP00
R11	W	1	O	O	O	O	O	PRN12	PRN11	PRN10	O	O	O	O	O	PRN02	PRN01	PRN00
R12	W	1	O	O	O	VRP14	VRP13	VRP12	VRP11	VRP10	O	O	O	O	VRP03	VRP02	VRP01	VRP00
R13	W	1	O	O	O	VRN14	VRN13	VRN12	VRN11	VRN10	O	O	O	O	VRN03	VRN02	VRN01	VRN00
R14	W	1	O	O	O	O	O	PKP12	PKP11	PKP10	O	O	O	O	O	PKP02	PKP01	PKP00
R15	W	1	O	O	O	O	O	PKP32	PKP31	PKP30	O	O	O	O	O	PKP22	PKP21	PKP20
R16	W	1	O	O	O	O	O	PKP52	PKP51	PKP50	O	O	O	O	O	PKP52	PKP51	PKP50
R17	W	1	O	O	O	O	O	PKN12	PKN11	PKN10	O	O	O	O	O	PKN02	PKN01	PKN00
R18	W	1	O	O	O	O	O	PKN32	PKN31	PKN30	O	O	O	O	O	PKN22	PKN21	PKN20
R19	W	1	O	O	O	O	O	PKN52	PKN51	PKN50	O	O	O	O	O	PKN52	PKN51	PKN50

Figure 30. Gamma Control Instruction

PRP12-00: Gradient adjusting register for the positive polarity output.
PRN12-00: Gradient adjusting register for the negative polarity output.
VRP14-00: Reference / Amplitude adjustment register for the positive polarity output.
VRN14-00: Reference / Amplitude adjustment register for the negative polarity output.
PKP52–00: Gamma micro adjusting register for the positive polarity output.
PKN52-00: Gamma micro adjusting register for the negative polarity output.

RESET FUNCTION

The S6F2002 is initialized by RESET input. The reset input must be held for at least 1 ms.

INSTRUCTION SET INITIALIZATION

1. NOP
2. Driver output control (IM=0, NMD=0, SSMD=0, REV=0, NL4-0=11101)
3. LCD driving waveform control (DS1-0=00, CHS1-0=00, DF1-0=00, RGB1-0=00)
4. Entry mode set (VPL=0, HPL=0, DPL=0, EPL=0, SS=0, STB=0)
5. Display control (1) (CLW2-0=000, GAON=0, SDR=0)
6. Display control (2) (NW1-0=01, DSC=1, GIF=0, FHN=1, FTI1-0=10, FWI1-0=11)
7. Source Output Timing control (VBP8-0=000H)
8. External display interface (HBP9-0=000H)
9. Panel interface control (SDT2-0=000, EQ2-0=000)
10. Power control 1 (EXM=0, GON=0, POC=0, SAP2-0=000, AP2-0=000)
11. Power control 2 (VCOMG=0, VDV4-0=00000, VCM4-0=00000)
12. Gamma control
     (PRP02-00=000, PRP12-10=000, PRN02-00=000, PRN12-10=000,
      VRP03-00=0000, VRP14-10=00000, VRN03-00=0000, VRN14-10=00000,
      PKP02–00=000, PKP12–10=000, PKP22–20=000, PKP32–30=000,
      PKP42–40=000, PKP52–50=000, PKN02–00=000, PKN12–10=000,
      PKN22–20=000, PKN32–30=000, PKN42–40=000, PKN52–50=000)

OUTPUT PIN INITIALIZATION

1. LCD driver output pins (Source output): Output High-Z level.

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INTERFACE SPECIFICATION

SYSTEM INTERFACE : SERIAL DATA TRANSFER

The S6F2002 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

The S6F2002 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the S6F2002. The S6F2002, when selected, receives the subsequent data string. The ID pin can determine the least significant bit of the identification code. The five upper bits must be 01110. Two different chip addresses must be assigned to a single S6F2002 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the S6F2002 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All S6F2002 instructions are 16 bits. Two bytes are received with the MSB first, and then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Table 33. Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

NOTE: ID pin selects ID bit.

Table 34. RS and R/W Bit Function

RS	RW	Function
0	0	Set index register
0	1	Status read
1	0	Write instruction
1	1	ID read
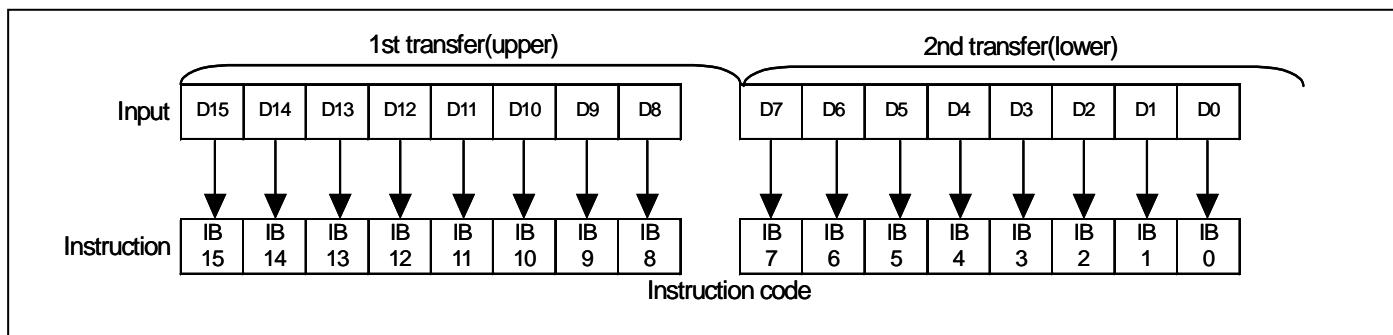
Figure 31. Instruction of Serial Data Transfer

PROCEDURE FOR TRANSFER ON CLOCK SYNCHRONIZED SERIAL BUS INTERFACE
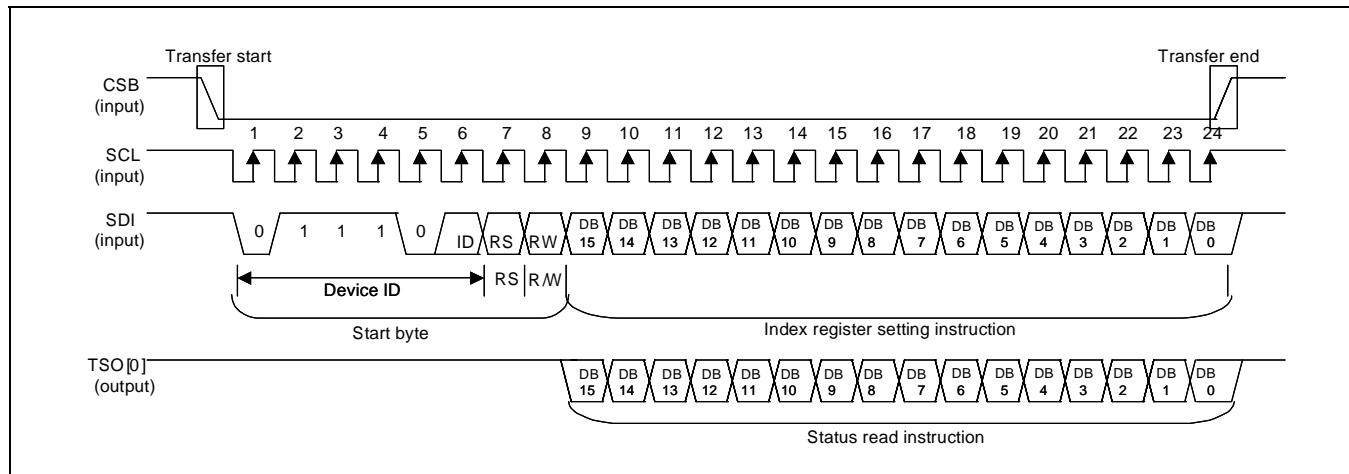
Figure 32. Timing of Basic Data Transfer through Clock-Synchronized Serial Bus Interface

NOTE: The first byte after the start byte is always the upper eight bits.
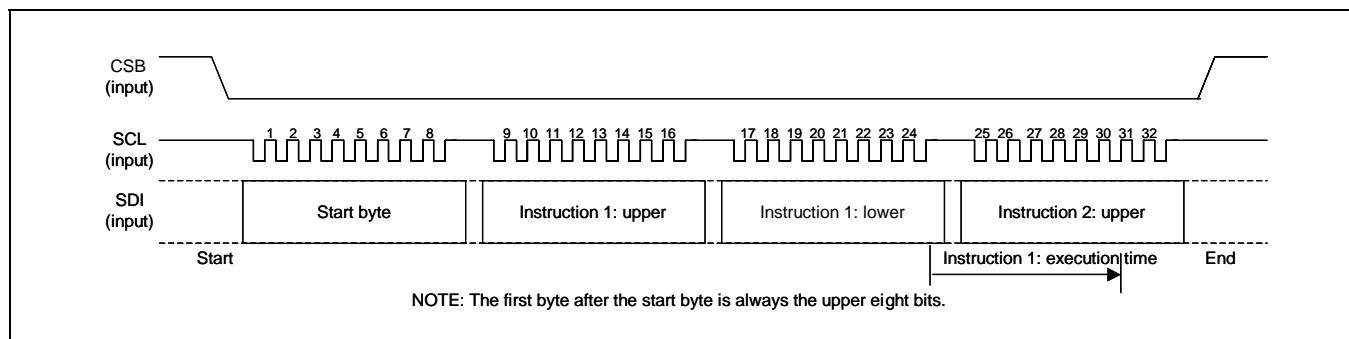
Figure 33. Timing of Consecutive Data-Transfer through Clock-synchronized Serial Bus Interface
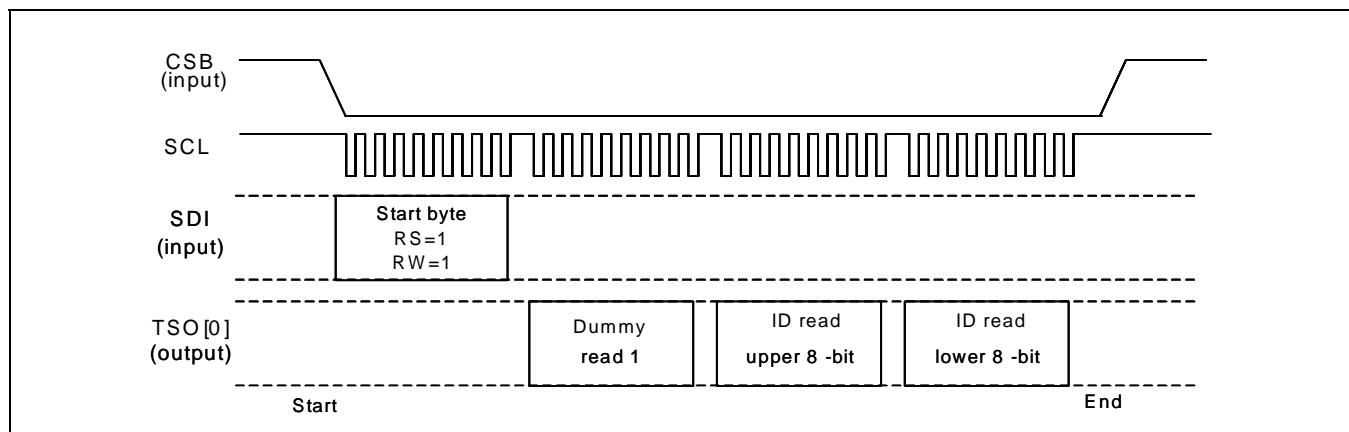
Figure 34. ID Read Timing

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24-BIT INTERFACE

24-bit RGB interface can be used by setting IM to 0. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred via 24-bit RGB data bus (PD23-0).

Input	PD 23	PD 22	PD 21	PD 20	PD 19	PD 18	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
RGB Arrange	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

1-pixel *16,777,216-color display is possible using the 24-bit RGB interface
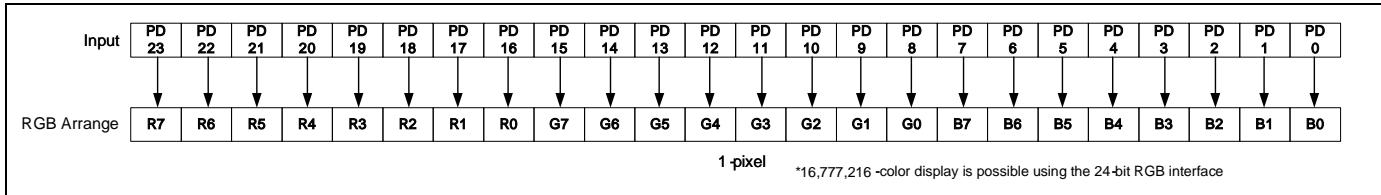
Figure 35. RGB Data Arrangement in the 24-bit Interface Mode

8-BIT INTERFACE

8-bit RGB interface can be used by setting IM to 1. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred via 8-bit RGB data bus (PD23 to 16) Unused pins must be fixed to the GND level.

	1st Transfer								2nd Transfer								3rd Transfer							
Input	PD 23	PD 22	PD 21	PD 20	PD 19	PD 18	PD 17	PD 16	PD 23	PD 22	PD 21	PD 20	PD 19	PD 18	PD 17	PD 16	PD 23	PD 22	PD 21	PD 20	PD 19	PD 18	PD 17	PD 16
RGB Arrange	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

1-pixel *16,777,216-color display is possible using the 8-bit RGB interface
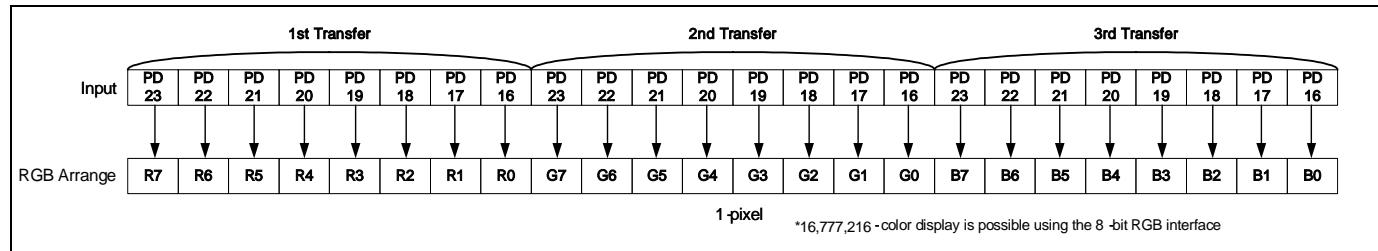
Figure 36. RGB Data Arrangement in the 8-bit Interface Mode

SYNC MODE INTERFACE [24-BIT]

Note : 1. Polarity register setting : VPL=0, HPL=0, DPL=0.
        2. The rising edge of DOTCLK is used to fetch display data PD bus.
        3. Channel length : 164RGB (CHS[1:0]=10).
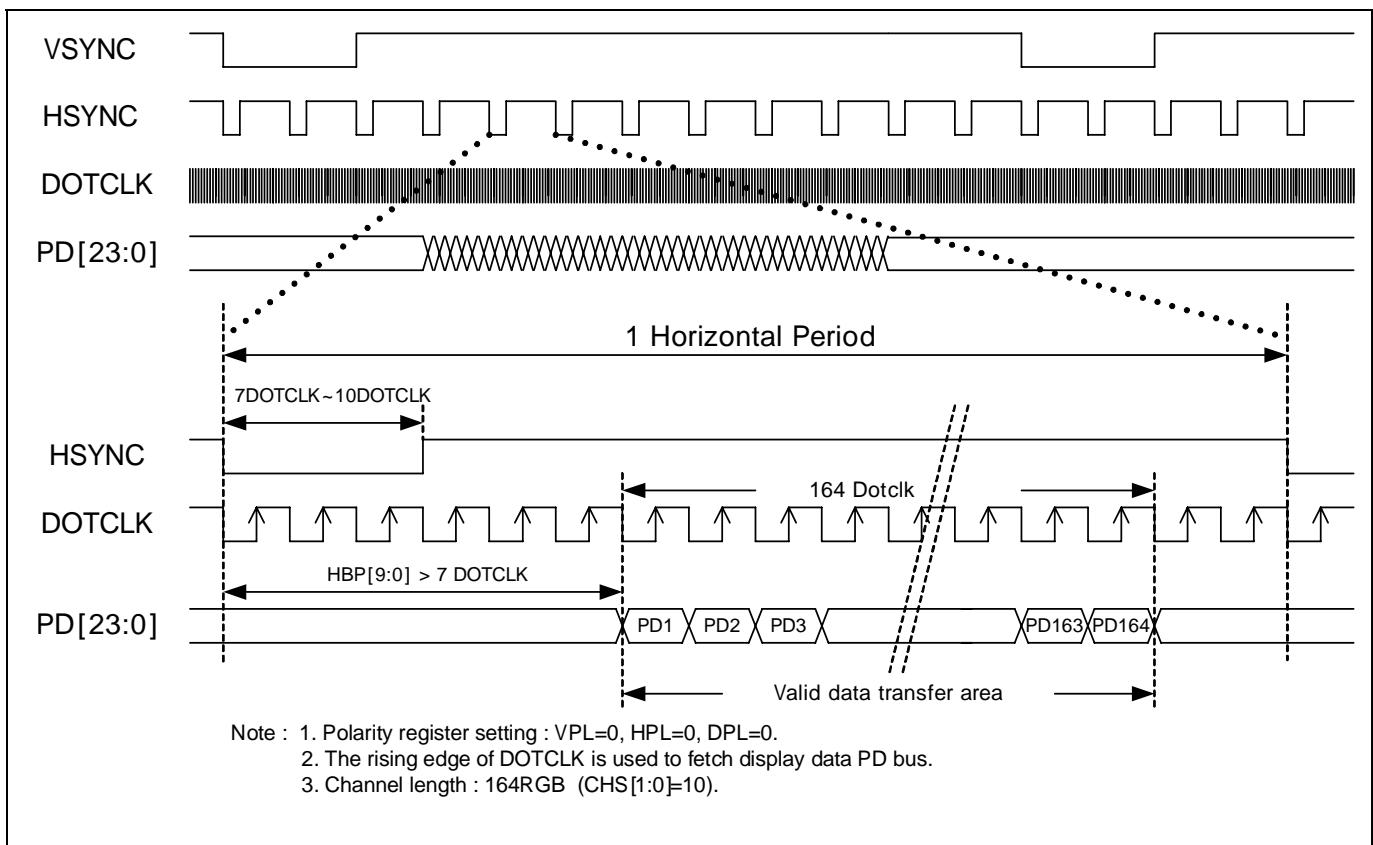
Figure 37. 24-bit SYNC Mode Interface Timing

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SYNC MODE INTERFACE [8-BIT]
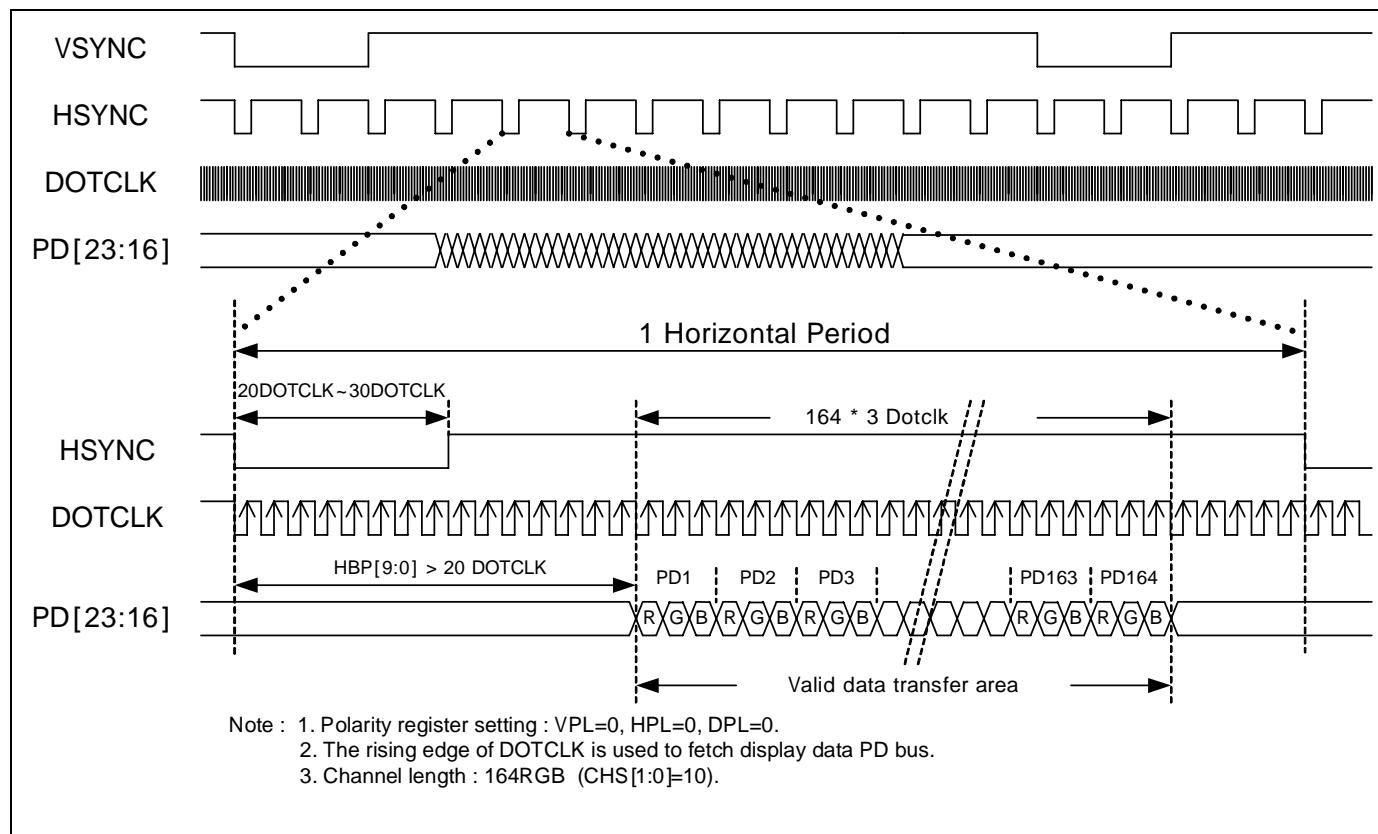
Figure 38. 8-bit SYNC Mode Interface Timing

NOTES: 1. Three clocks are regarded as one clock for transfer when data is transferred in 8-bit interface.
              2. VSYNC, HSYNC, DOTCLK, and PD23-16 should be transferred in units of three clocks.

DE MODE INTERFACE [24-BIT]
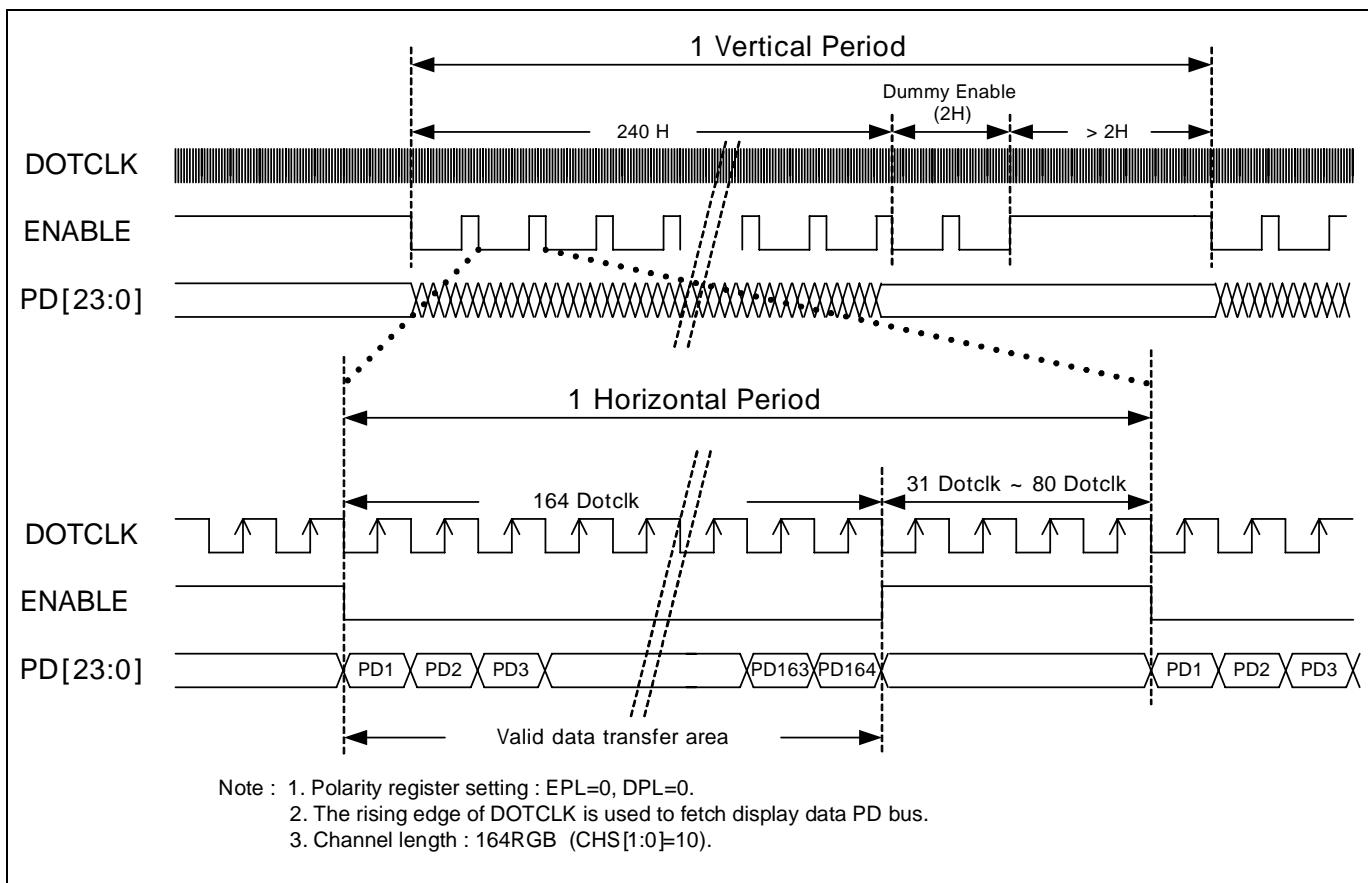
Figure 39. 24-bit DE Mode Interface Timing

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DE MODE INTERFACE [8-BIT]
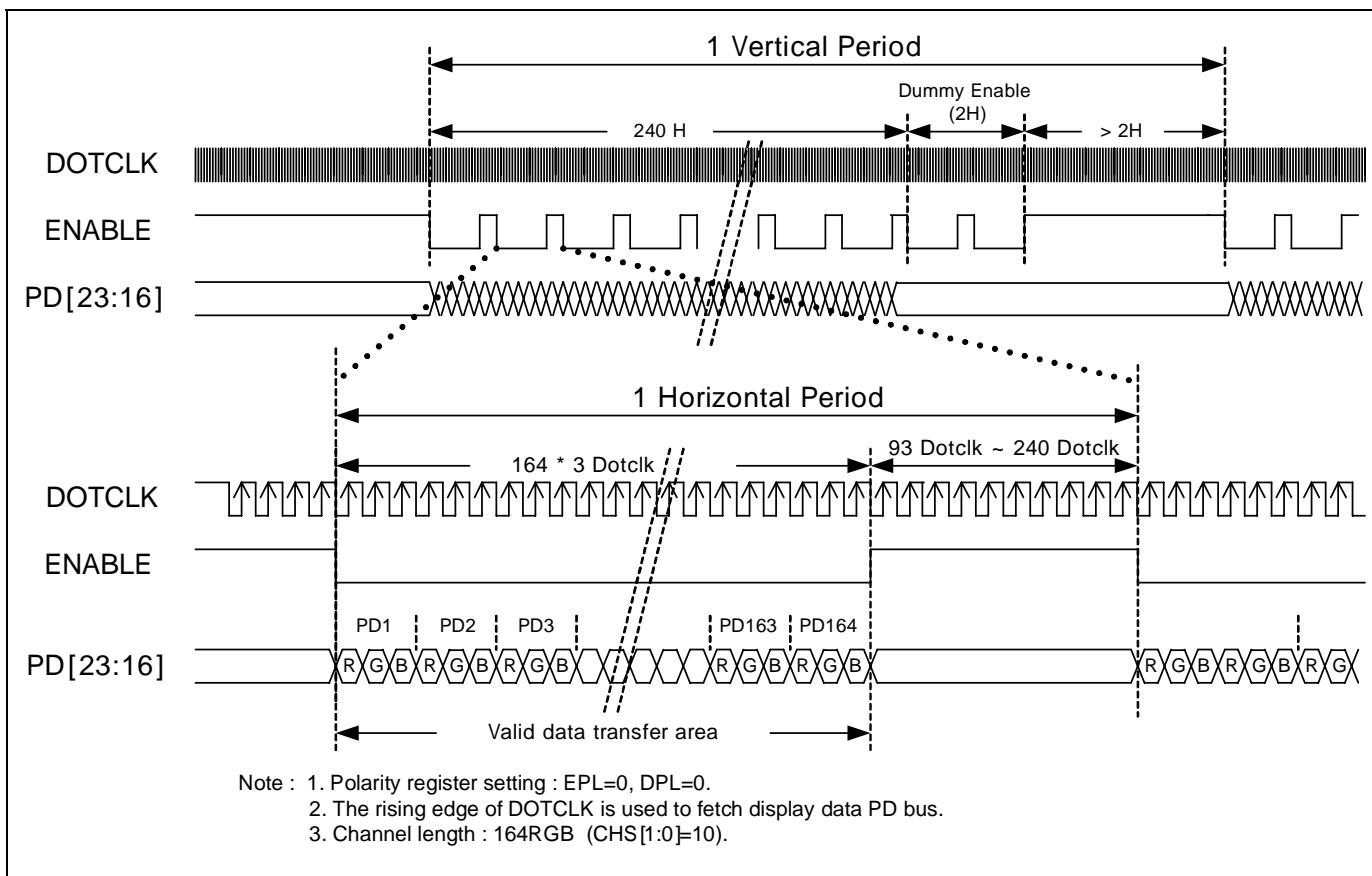
Figure 40. 8-bit DE Mode Interface Timing

DISPLAY SIGNAL TIMING

DISPLAY TIMING IN 1 FRAME
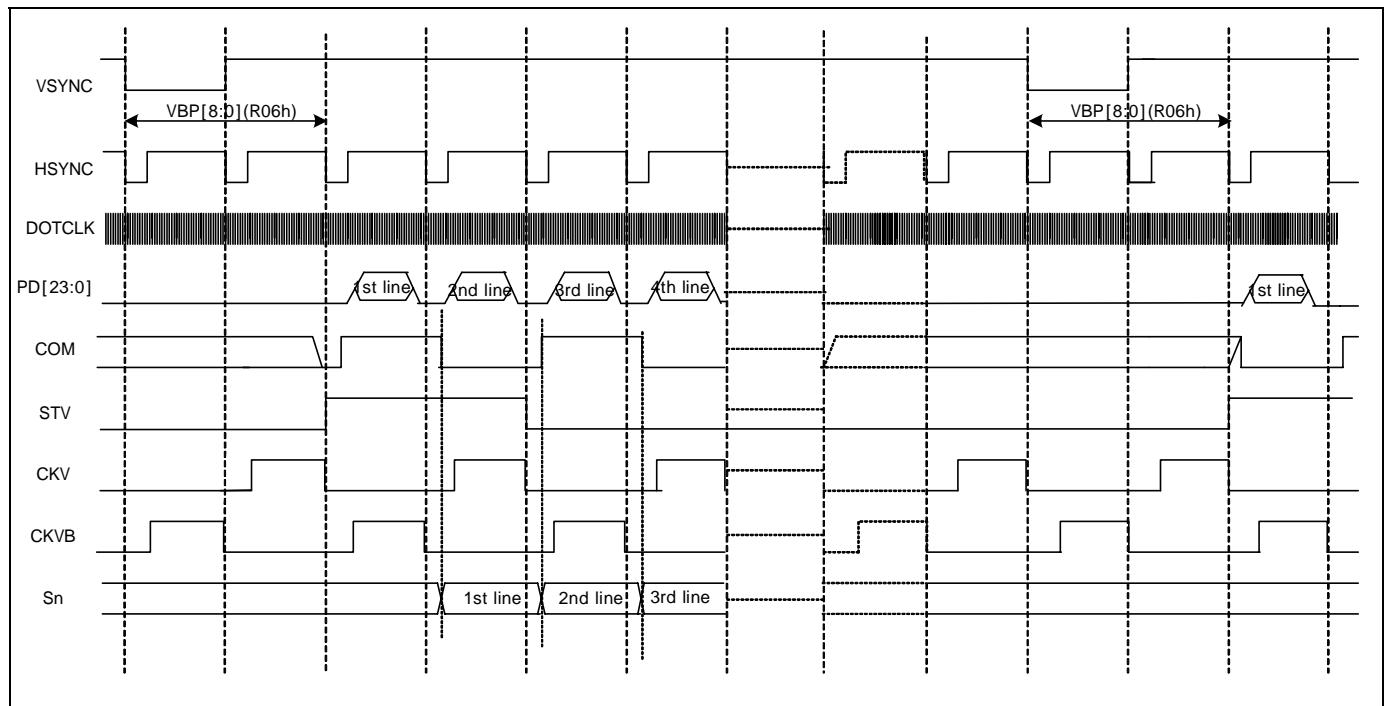
Figure 41. Display Timing in 1 Frame

DISPLAY TIMING IN 1 HORIZONTAL LINE
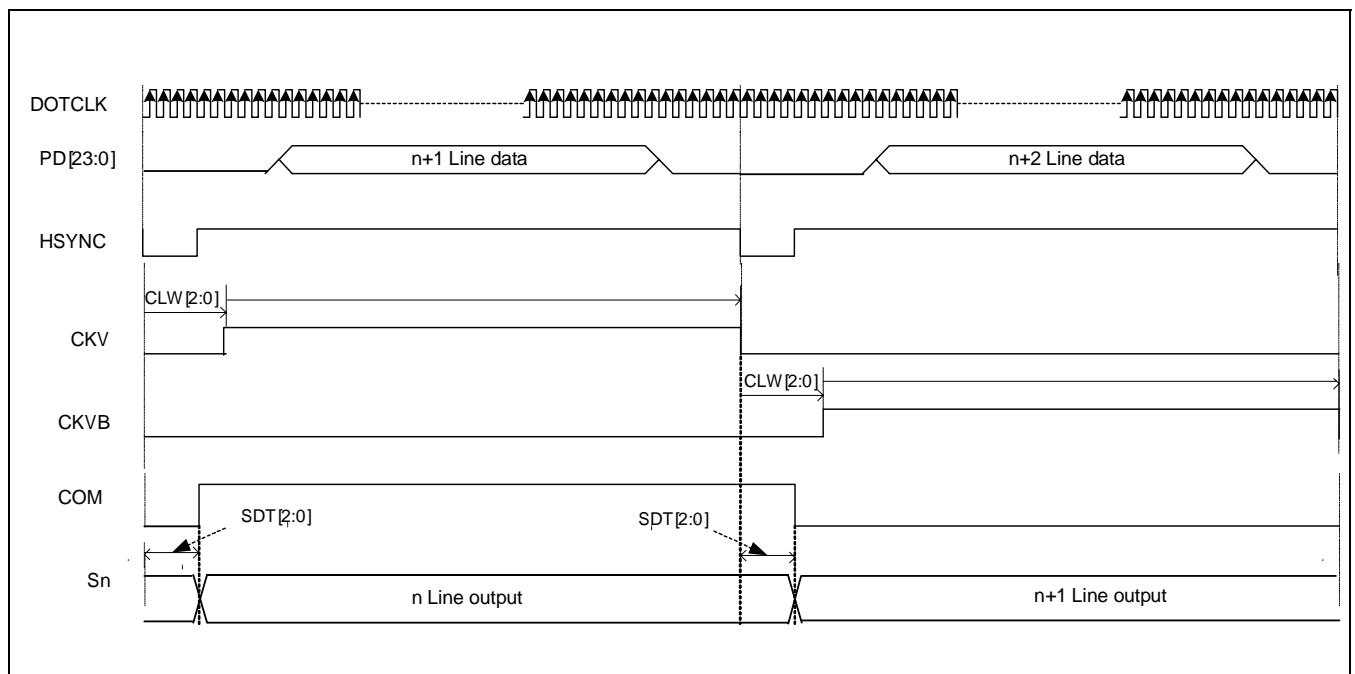
Figure 42. Display Timing in 1 Horizontal Line

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AMORPHOUS-SILICON GATE TFT–LCD PANEL CONTROL

S6F2002 generates timing signals (STV_L/R, CKV_L/R, and CKVB_L/R) for controlling an amorphous -silicon TFT LCD panel with built-in gate driver circuits. S6F2002 also has built-in level shifters for an amorphous-silicon TFT LCD panel.

OUTPUT SIGNALS

Table 35. Output Signals

Level Shifter Output Signals	Remarks
STV_L/R (Output for the frame-start pulse)	-
CKV_L/R (Output for the one-raster-row-cycle pulse)	The output timing varies by bits of CLW2-0.
CKVB_L/R (Output for the one-raster-row-cycle pulse)	
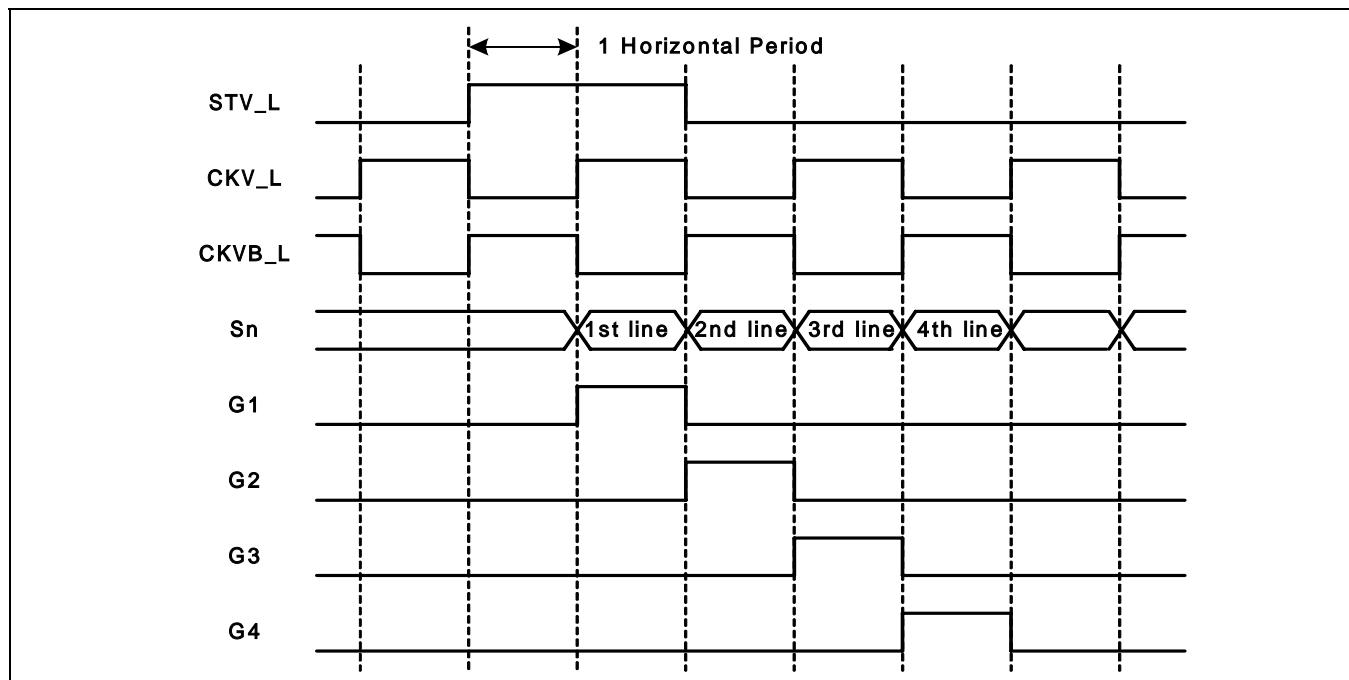
NORMAL ASG (NMD=0)

Figure 43. Gate Control Signal Timing in Normal ASG Mode

NOTE: LSENL=1, LSENR=0.

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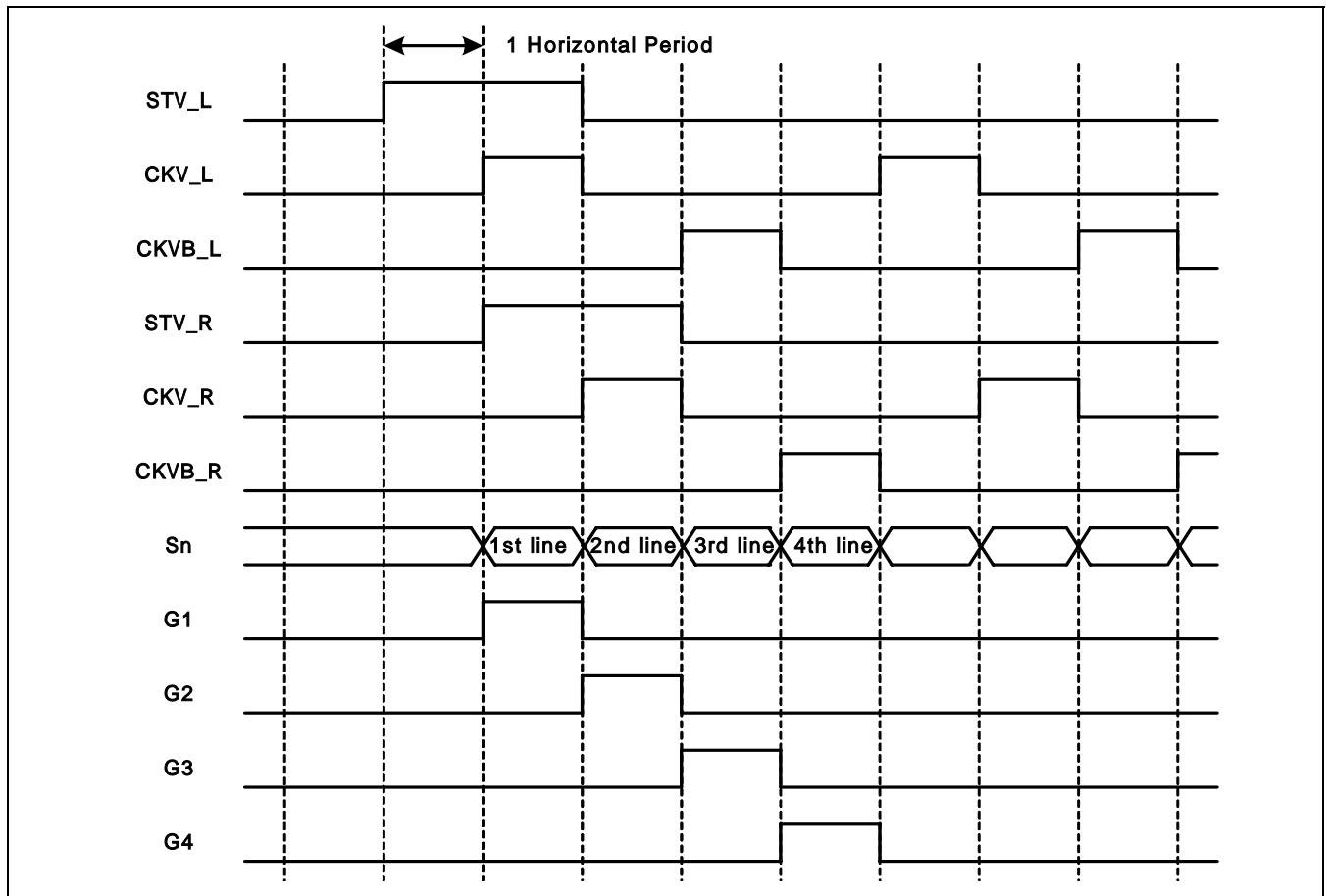
DOUBLE ASG (NMD=1)

Figure 44. Gate Control Signal Timing in Double ASG Mode

NOTE: LSENL=1, LSENR=1.

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GAMMA ADJUSTMENT FUNCTION

S6F2002 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment is executed by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register that determine the 8 grayscale levels. Furthermore, since these registers have the positive polarities and negative polarities, adjust them to match LCD panel respectively.
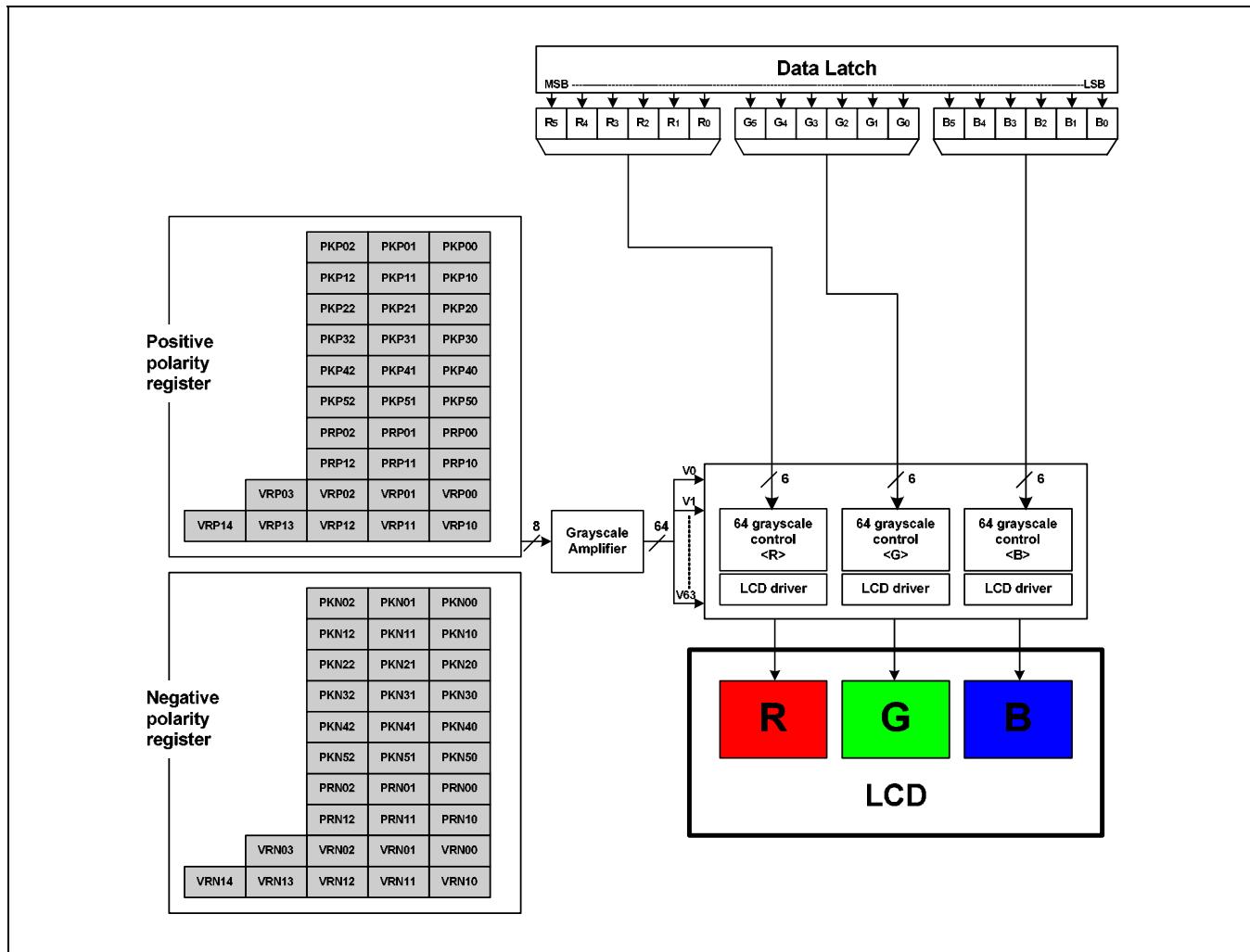
Figure 45. Grayscale Control

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STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. The 8 voltage levels (VIN0-VIN7) between GVDD and VGS are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register. Each level is split into 8 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63.
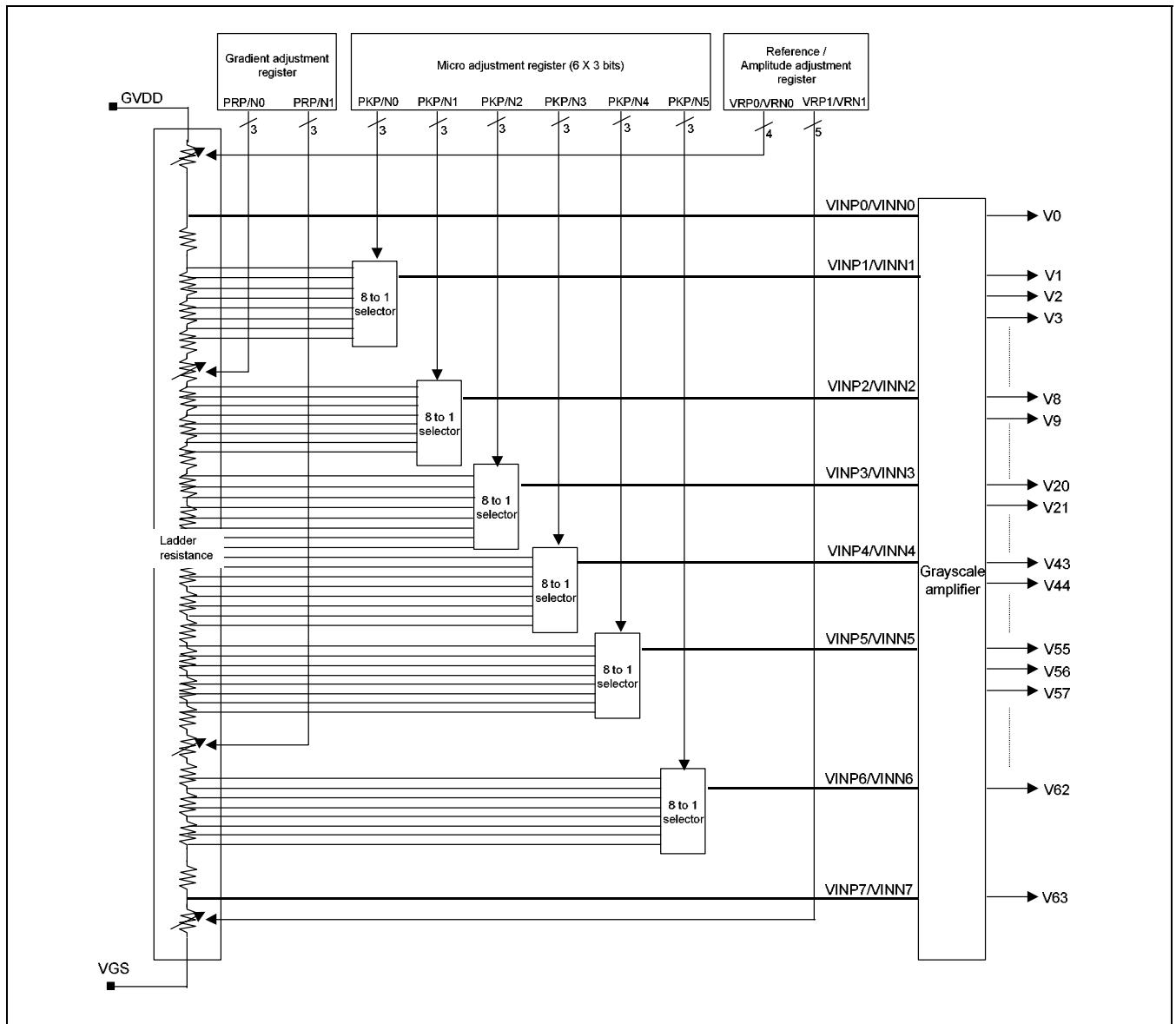
Figure 46. Structure of Grayscale Amplifier

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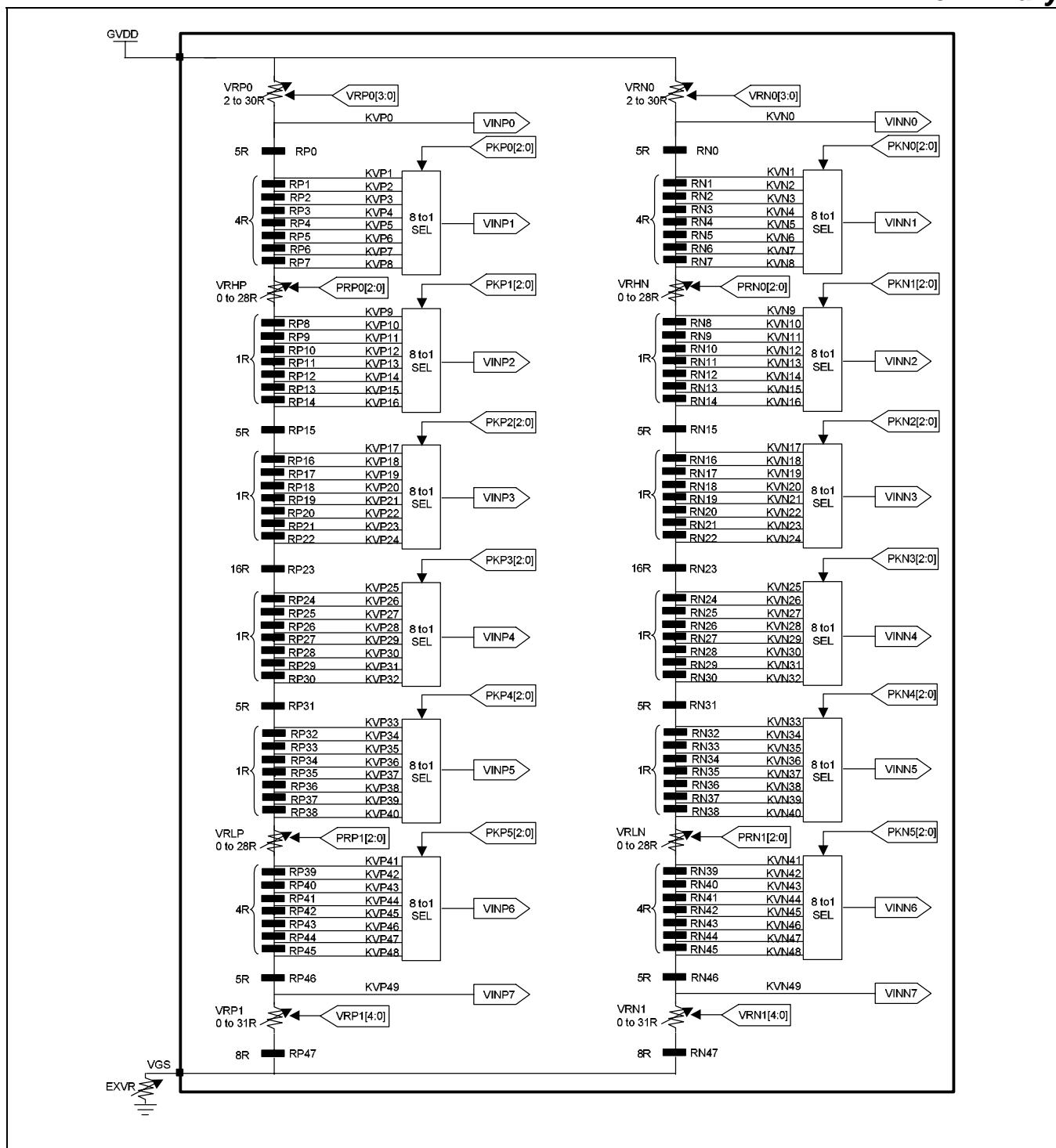
Figure 47. Structure of Resistor Ladder Network / 8 to 1 Selector

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GAMMA ADJUSTMENT REGISTER

This block has registers to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (Average <R><G><B> are common.) The following figure indicates the operation of each adjustment register.
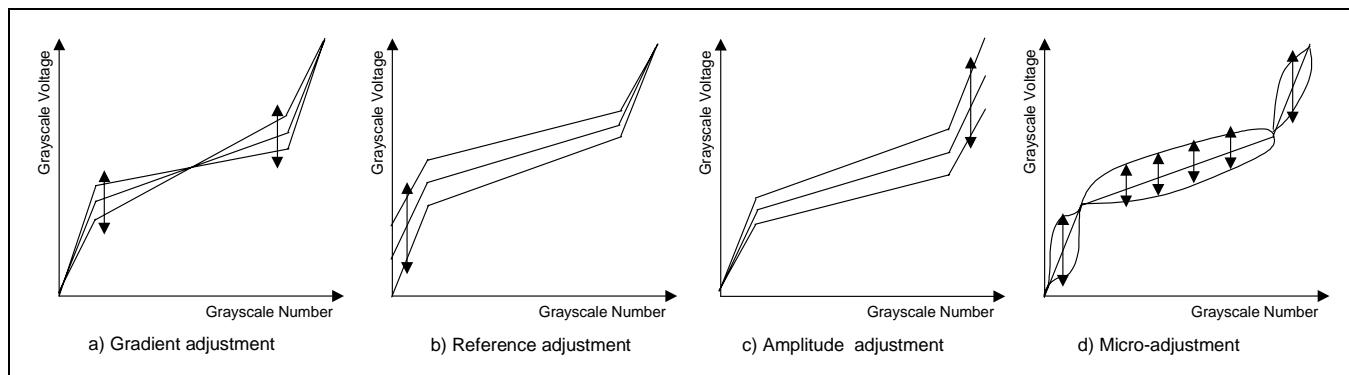
Figure 48. The Operation Of Adjusting Register

GRADIENT ADJUSTING RESISTOR

The gradient adjustment register is to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP(N) / VRLP(N)) of the resistor ladder for the grayscale voltage generator. Also, there is an independent register on the positive/negative polarities in order for corresponding to asymmetry drive.

REFERENCE ADJUSTING RESISTOR

The Reference adjustment register is to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)1) of the ladder resistor for the grayscale voltage generator located at the lower side of the resistor ladder.

AMPLITUDE ADJUSTING RESISTOR

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at the upper side of the resistor ladder.

MICRO-ADJUSTING RESISTOR

The Micro adjustment register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

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Table 36. Gamma Adjustment Register

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Reference adjustment	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
Micro adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

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LADDER RESISTOR NETWORK / 8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

VARIABLE RESISTOR

There are 4 types of the variable resistors that are for the gradient adjustment (VRHP(N) / VRLP(N)) and for the reference / amplitude adjustment (VRP(N)1 / VRP(N)0). The resistance value is set by the gradient adjustment register and the reference / amplitude adjustment registers as below.

Table 37. Gradient Adjustment (1)

Register value PRP(N)0 [2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 38. Gradient Adjustment (2)

Register value PRP(N)1 [2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 39. Reference Adjustment

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
.	.
.	.
.	.
11101	29R
11110	30R
11111	31R

Table 40. Amplitude Adjustment

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
.	.
.	.
.	.
1101	26R
1110	28R
1111	30R

THE 8 TO 1 SELECTOR

In the 8-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the six types of the reference voltage, VIN1 to VIN6.
Following figure explains the relationship between the micro-adjustment register and the selected voltage.

Table 41. Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels are determined by the following formulas listed in the next pages.

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Table 42. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD-ΔV*VRP0/SUMRP	-	VINP0
KVP1	GVDD-ΔV*(VRP0+5R)/SUMRP	PKP0[2:0] = "000"	VINP1
KVP2	GVDD-ΔV*(VRP0+9R)/SUMRP	PKP0[2:0] = "001"	
KVP3	GVDD-ΔV*(VRP0+13R)/SUMRP	PKP0[2:0] = "010"	
KVP4	GVDD-ΔV*(VRP0+17R)/SUMRP	PKP0[2:0] = "011"	
KVP5	GVDD-ΔV*(VRP0+21R)/SUMRP	PKP0[2:0] = "100"	
KVP6	GVDD-ΔV*(VRP0+25R)/SUMRP	PKP0[2:0] = "101"	
KVP7	GVDD-ΔV*(VRP0+29R)/SUMRP	PKP0[2:0] = "110"	
KVP8	GVDD-ΔV*(VRP0+33R)/SUMRP	PKP0[2:0] = "111"	
KVP9	GVDD-ΔV*(VRP0+33R+VRHP)/SUMRP	PKP1[2:0] = "000"	VINP2
KVP10	GVDD-ΔV*(VRP0+34R+VRHP)/SUMRP	PKP1[2:0] = "001"	
KVP11	GVDD-ΔV*(VRP0+35R+VRHP)/SUMRP	PKP1[2:0] = "010"	
KVP12	GVDD-ΔV*(VRP0+36R+VRHP)/SUMRP	PKP1[2:0] = "011"	
KVP13	GVDD-ΔV*(VRP0+37R+VRHP)/SUMRP	PKP1[2:0] = "100"	
KVP14	GVDD-ΔV*(VRP0+38R+VRHP)/SUMRP	PKP1[2:0] = "101"	
KVP15	GVDD-ΔV*(VRP0+39R+VRHP)/SUMRP	PKP1[2:0] = "110"	
KVP16	GVDD-ΔV*(VRP0+40R+VRHP)/SUMRP	PKP1[2:0] = "111"	
KVP17	GVDD-ΔV*(VRP0+45R+VRHP)/SUMRP	PKP2[2:0] = "000"	VINP3
KVP18	GVDD-ΔV*(VRP0+46R+VRHP)/SUMRP	PKP2[2:0] = "001"	
KVP19	GVDD-ΔV*(VRP0+47R+VRHP)/SUMRP	PKP2[2:0] = "010"	
KVP20	GVDD-ΔV*(VRP0+48R+VRHP)/SUMRP	PKP2[2:0] = "011"	
KVP21	GVDD-ΔV*(VRP0+49R+VRHP)/SUMRP	PKP2[2:0] = "100"	
KVP22	GVDD-ΔV*(VRP0+50R+VRHP)/SUMRP	PKP2[2:0] = "101"	
KVP23	GVDD-ΔV*(VRP0+51R+VRHP)/SUMRP	PKP2[2:0] = "110"	
KVP24	GVDD-ΔV*(VRP0+52R+VRHP)/SUMRP	PKP2[2:0] = "111"	
KVP25	GVDD-ΔV*(VRP0+68R+VRHP)/SUMRP	PKP3[2:0] = "000"	VINP4
KVP26	GVDD-ΔV*(VRP0+69R+VRHP)/SUMRP	PKP3[2:0] = "001"	
KVP27	GVDD-ΔV*(VRP0+70R+VRHP)/SUMRP	PKP3[2:0] = "010"	
KVP28	GVDD-ΔV*(VRP0+71R+VRHP)/SUMRP	PKP3[2:0] = "011"	
KVP29	GVDD-ΔV*(VRP0+72R+VRHP)/SUMRP	PKP3[2:0] = "100"	
KVP30	GVDD-ΔV*(VRP0+73R+VRHP)/SUMRP	PKP3[2:0] = "101"	
KVP31	GVDD-ΔV*(VRP0+74R+VRHP)/SUMRP	PKP3[2:0] = "110"	
KVP32	GVDD-ΔV*(VRP0+75R+VRHP)/SUMRP	PKP3[2:0] = "111"	
KVP33	GVDD-ΔV*(VRP0+80R+VRHP)/SUMRP	PKP4[2:0] = "000"	VINP5
KVP34	GVDD-ΔV*(VRP0+81R+VRHP)/SUMRP	PKP4[2:0] = "001"	
KVP35	GVDD-ΔV*(VRP0+82R+VRHP)/SUMRP	PKP4[2:0] = "010"	
KVP36	GVDD-ΔV*(VRP0+83R+VRHP)/SUMRP	PKP4[2:0] = "011"	
KVP37	GVDD-ΔV*(VRP0+84R+VRHP)/SUMRP	PKP4[2:0] = "100"	
KVP38	GVDD-ΔV*(VRP0+85R+VRHP)/SUMRP	PKP4[2:0] = "101"	
KVP39	GVDD-ΔV*(VRP0+86R+VRHP)/SUMRP	PKP4[2:0] = "110"	
KVP40	GVDD-ΔV*(VRP0+87R+VRHP)/SUMRP	PKP4[2:0] = "111"	
KVP41	GVDD-ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "000"	VINP6
KVP42	GVDD-ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "001"	
KVP43	GVDD-ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "010"	
KVP44	GVDD-ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "011"	
KVP45	GVDD-ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "100"	
KVP46	GVDD-ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "101"	
KVP47	GVDD-ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "110"	
KVP48	GVDD-ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP5[2:0] = "111"	
KVP49	GVDD-ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP1
SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN1
ΔV: Electric potential difference between GVDD and VGS = GVDD*[SUMRP(N)/([SUMRP(N)+EXVR])

Table 43. Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

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Table 44. Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD-ΔV*VRN0/SUMRN	-	VINN0
KVN1	GVDD-ΔV*(VRN0+5R)/SUMRN	PKN0[2:0] = "000"	VINN1
KVN2	GVDD-ΔV*(VRN0+9R)/SUMRN	PKN0[2:0] = "001"	
KVN3	GVDD-ΔV*(VRN0+13R)/SUMRN	PKN0[2:0] = "010"	
KVN4	GVDD-ΔV*(VRN0+17R)/SUMRN	PKN0[2:0] = "011"	
KVN5	GVDD-ΔV*(VRN0+21R)/SUMRN	PKN0[2:0] = "100"	
KVN6	GVDD-ΔV*(VRN0+25R)/SUMRN	PKN0[2:0] = "101"	
KVN7	GVDD-ΔV*(VRN0+29R)/SUMRN	PKN0[2:0] = "110"	
KVN8	GVDD-ΔV*(VRN0+33R)/SUMRN	PKN0[2:0] = "111"	
KVN9	GVDD-ΔV*(VRN0+33R+VRHN)/SUMRN	PKN1[2:0] = "000"	VINN2
KVN10	GVDD-ΔV*(VRN0+34R+VRHN)/SUMRN	PKN1[2:0] = "001"	
KVN11	GVDD-ΔV*(VRN0+35R+VRHN)/SUMRN	PKN1[2:0] = "010"	
KVN12	GVDD-ΔV*(VRN0+36R+VRHN)/SUMRN	PKN1[2:0] = "011"	
KVN13	GVDD-ΔV*(VRN0+37R+VRHN)/SUMRN	PKN1[2:0] = "100"	
KVN14	GVDD-ΔV*(VRN0+38R+VRHN)/SUMRN	PKN1[2:0] = "101"	
KVN15	GVDD-ΔV*(VRN0+39R+VRHN)/SUMRN	PKN1[2:0] = "110"	
KVN16	GVDD-ΔV*(VRN0+40R+VRHN)/SUMRN	PKN1[2:0] = "111"	
KVN17	GVDD-ΔV*(VRN0+45R+VRHN)/SUMRN	PKN2[2:0] = "000"	VINN3
KVN18	GVDD-ΔV*(VRN0+46R+VRHN)/SUMRN	PKN2[2:0] = "001"	
KVN19	GVDD-ΔV*(VRN0+47R+VRHN)/SUMRN	PKN2[2:0] = "010"	
KVN20	GVDD-ΔV*(VRN0+48R+VRHN)/SUMRN	PKN2[2:0] = "011"	
KVN21	GVDD-ΔV*(VRN0+49R+VRHN)/SUMRN	PKN2[2:0] = "100"	
KVN22	GVDD-ΔV*(VRN0+50R+VRHN)/SUMRN	PKN2[2:0] = "101"	
KVN23	GVDD-ΔV*(VRN0+51R+VRHN)/SUMRN	PKN2[2:0] = "110"	
KVN24	GVDD-ΔV*(VRN0+52R+VRHN)/SUMRN	PKN2[2:0] = "111"	
KVN25	GVDD-ΔV*(VRN0+68R+VRHN)/SUMRN	PKN3[2:0] = "000"	VINN4
KVN26	GVDD-ΔV*(VRN0+69R+VRHN)/SUMRN	PKN3[2:0] = "001"	
KVN27	GVDD-ΔV*(VRN0+70R+VRHN)/SUMRN	PKN3[2:0] = "010"	
KVN28	GVDD-ΔV*(VRN0+71R+VRHN)/SUMRN	PKN3[2:0] = "011"	
KVN29	GVDD-ΔV*(VRN0+72R+VRHN)/SUMRN	PKN3[2:0] = "100"	
KVN30	GVDD-ΔV*(VRN0+73R+VRHN)/SUMRN	PKN3[2:0] = "101"	
KVN31	GVDD-ΔV*(VRN0+74R+VRHN)/SUMRN	PKN3[2:0] = "110"	
KVN32	GVDD-ΔV*(VRN0+75R+VRHN)/SUMRN	PKN3[2:0] = "111"	
KVN33	GVDD-ΔV*(VRN0+80R+VRHN)/SUMRN	PKN4[2:0] = "000"	VINN5
KVN34	GVDD-ΔV*(VRN0+81R+VRHN)/SUMRN	PKN4[2:0] = "001"	
KVN35	GVDD-ΔV*(RN0+82R+VRHN)/SUMRN	PKN4[2:0] = "010"	
KVN36	GVDD-ΔV*(VRN0+83R+VRHN)/SUMRN	PKN4[2:0] = "011"	
KVN37	GVDD-ΔV*(VRN0+84R+VRHN)/SUMRN	PKN4[2:0] = "100"	
KVN38	GVDD-ΔV*(VRN0+85R+VRHN)/SUMRN	PKN4[2:0] = "101"	
KVN39	GVDD-ΔV*(VRN0+86R+VRHN)/SUMRN	PKN4[2:0] = "110"	
KVN40	GVDD-ΔV*(VRN0+87R+VRHN)/SUMRN	PKN4[2:0] = "111"	
KVN41	GVDD-ΔV*(VRN0+87R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "000"	VINN6
KVN42	GVDD-ΔV*(VRN0+91R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "001"	
KVN43	GVDD-ΔV*(VRN0+95R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "010"	
KVN44	GVDD-ΔV*(VRN0+99R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "011"	
KVN45	GVDD-ΔV*(VRN0+103R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "100"	
KVN46	GVDD-ΔV*(VRN0+107R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "101"	
KVN47	GVDD-ΔV*(VRN0+111R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "110"	
KVN48	GVDD-ΔV*(VRN0+115R+VRHN+VRLN)/SUMRN	PKN5[2:0] = "111"	
KVN49	GVDD-ΔV*(VRN0+120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + 128R + VRHP + VRLP + VRP1
SUMRN: Total of the negative polarity ladder resistance = VRN0 + 128R + VRHN + VRLN + VRN1
ΔV: Electric potential difference between GVDD and VGS = GVDD*[SUMRP(N)/([SUMRP(N)+EXVR)]

Table 45. Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 2

| Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7
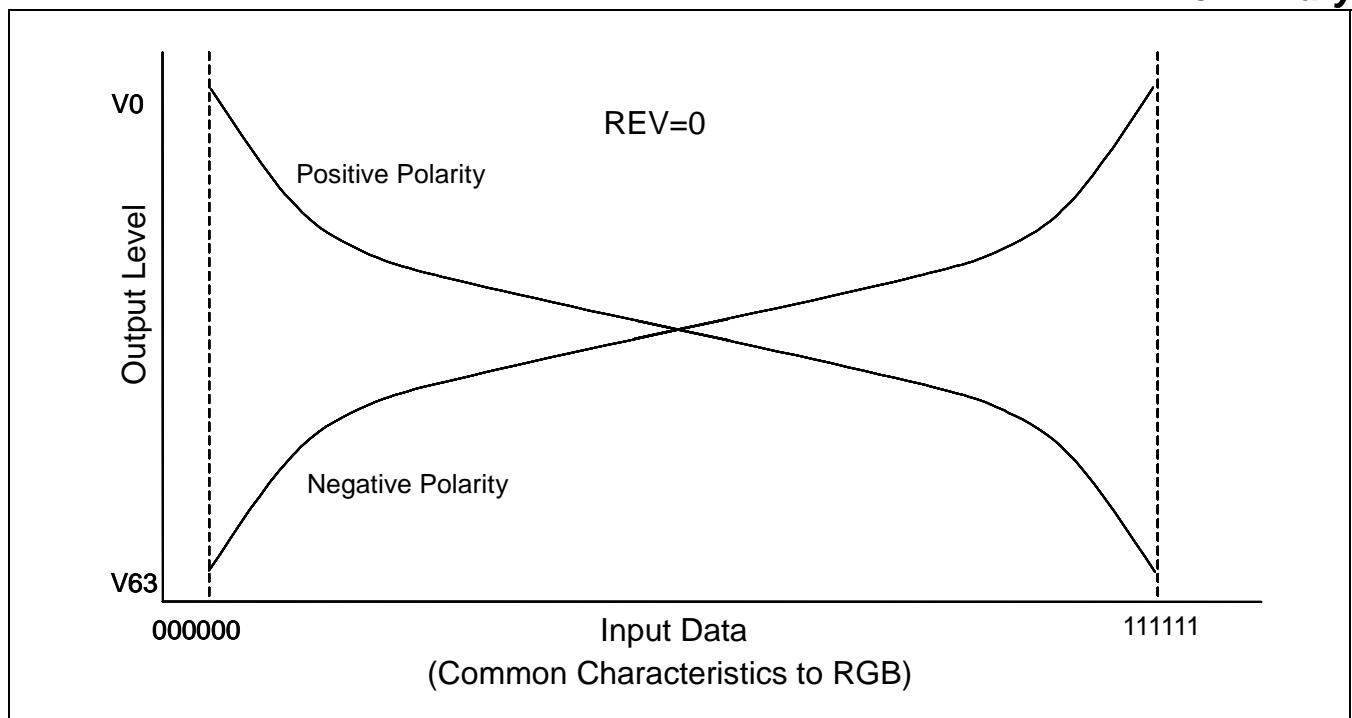
**Figure 49. Relationship between Input Data and Output Voltage**
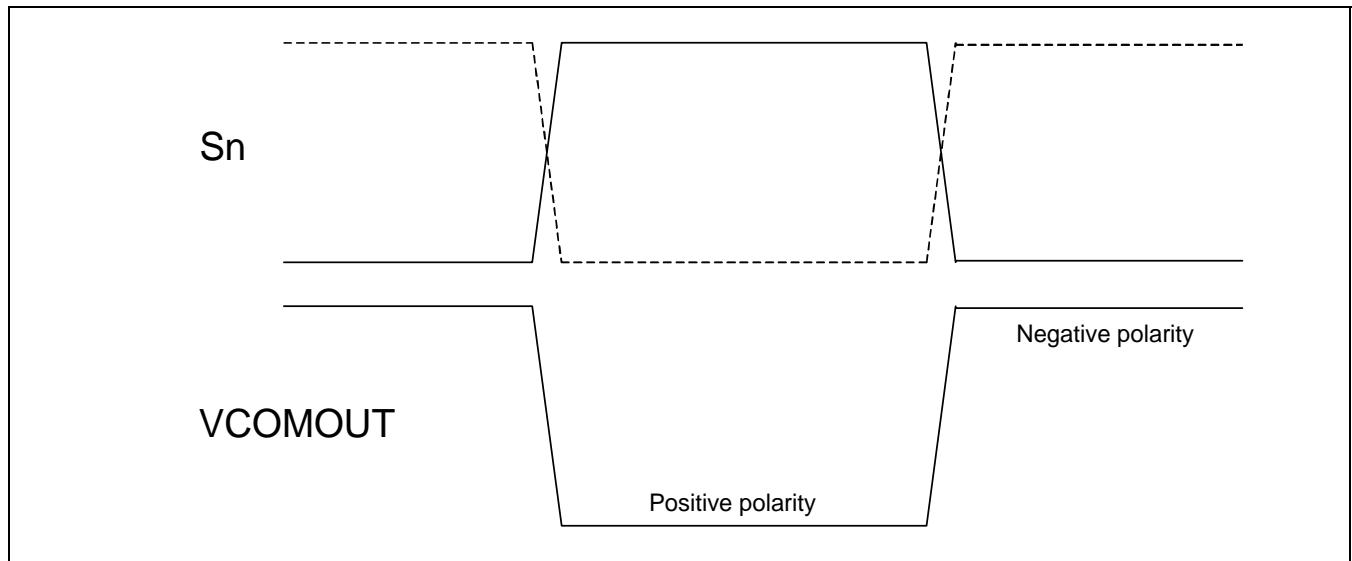
Figure 50. Relationship between Source Driver Output and VCOMOUT

POWER SUPPLY SETUP FLOW

Apply the power in a sequence as shown in Figure 52. The settling time of internally-generated voltage levels and analog circuit block such as operational amplifier depend on the value of external resistor or capacitor.
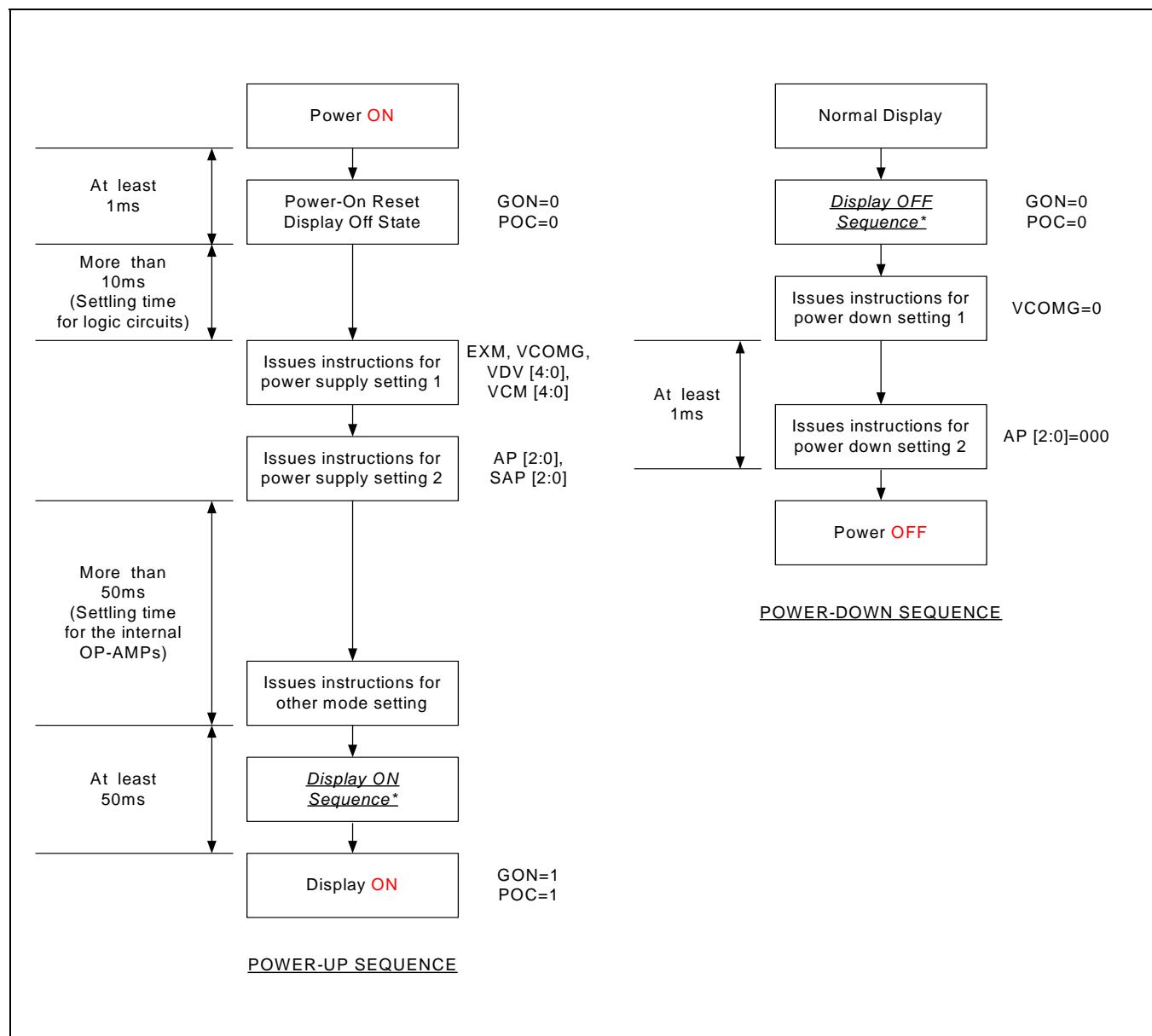

Figure 51. Power Supply Setup Flow

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INSTRUCTION SETUP FLOW

DISPLAY ON / OFF SEQUENCE

```
   ┌─────────────────────┐              ┌─────────────────────┐
   │   Complete          │              │   Normal            │
   │   Power Settings    │              │   Operation State   │
   └─────────────────────┘              └─────────────────────┘
            ┊                                     ┊
   ┌─────────────────────┐              ┌─────────────────────┐
   │  Display Off State  │              │  Display On State   │
   │      GON=0          │              │      GON=1          │
   │      POC=0          │              │      POC=1          │
   │      DSC=0          │              │      DSC=1          │
   └─────────────────────┘              └─────────────────────┘
            │                                     │
   ┌─────────────────────┐              ┌─────────────────────┐
   │      Wait           │              │      Wait           │
   │ (more than 2 frames)│              │ (more than 2 frames)│
   └─────────────────────┘              └─────────────────────┘
            │                                     │
   ┌─────────────────────┐              ┌─────────────────────┐
   │  Display On State   │              │  Display Off State  │
   │      GON=1          │              │      GON=0          │
   │      POC=1          │              │      POC=0          │
   │      DSC=1          │              │      DSC=0          │
   └─────────────────────┘              └─────────────────────┘
            ┊                                     ┊
   ┌─────────────────────┐              ┌─────────────────────┐
   │    Display ON       │              │    Display OFF      │
   └─────────────────────┘              └─────────────────────┘

     DISPLAY-ON SEQUENCE                   DISPLAY-OFF SEQUENCE
```
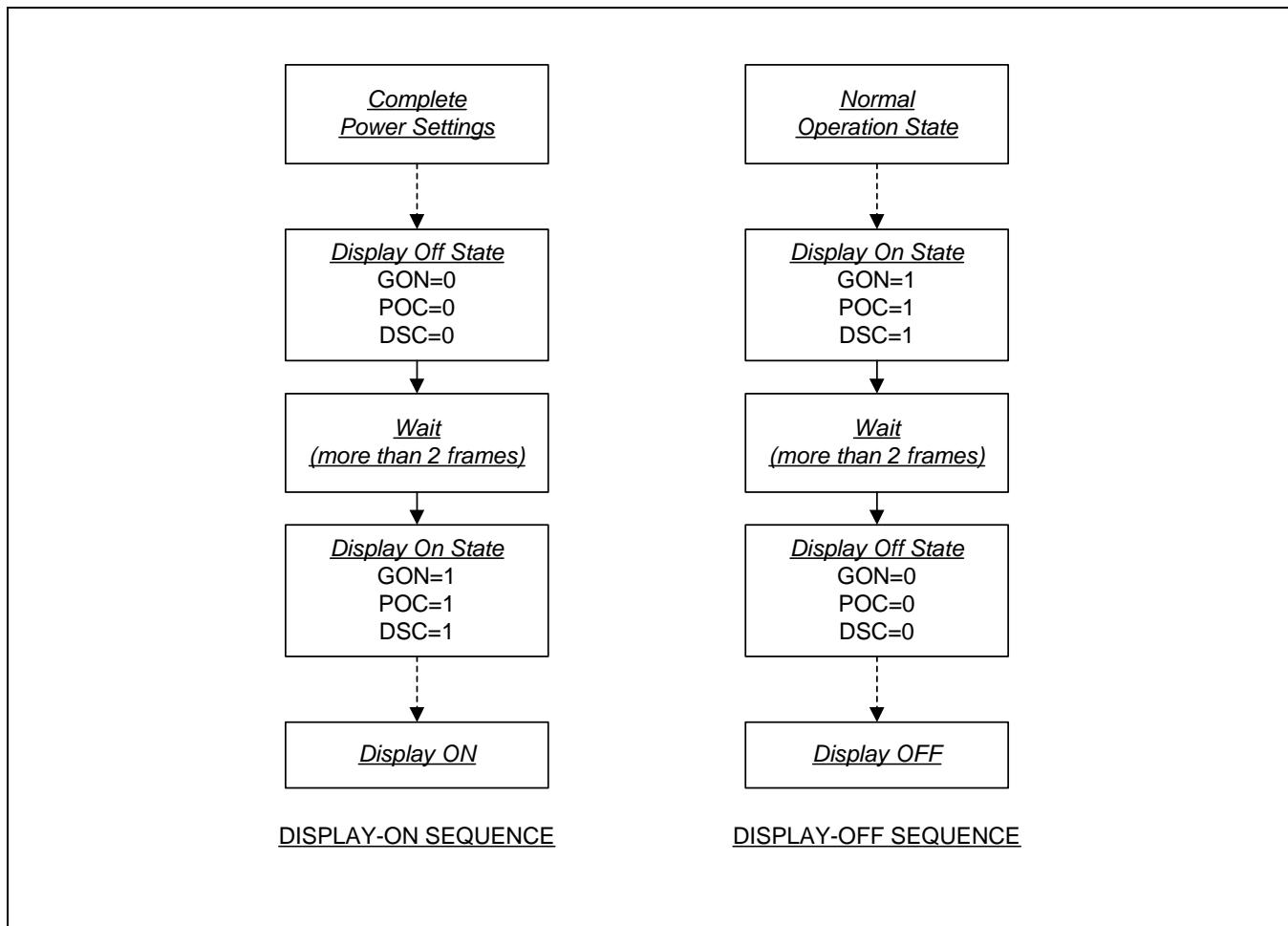
Figure 52. Display On / Off Sequence

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STAND-BY MODE IN / OUT SEQUENCE
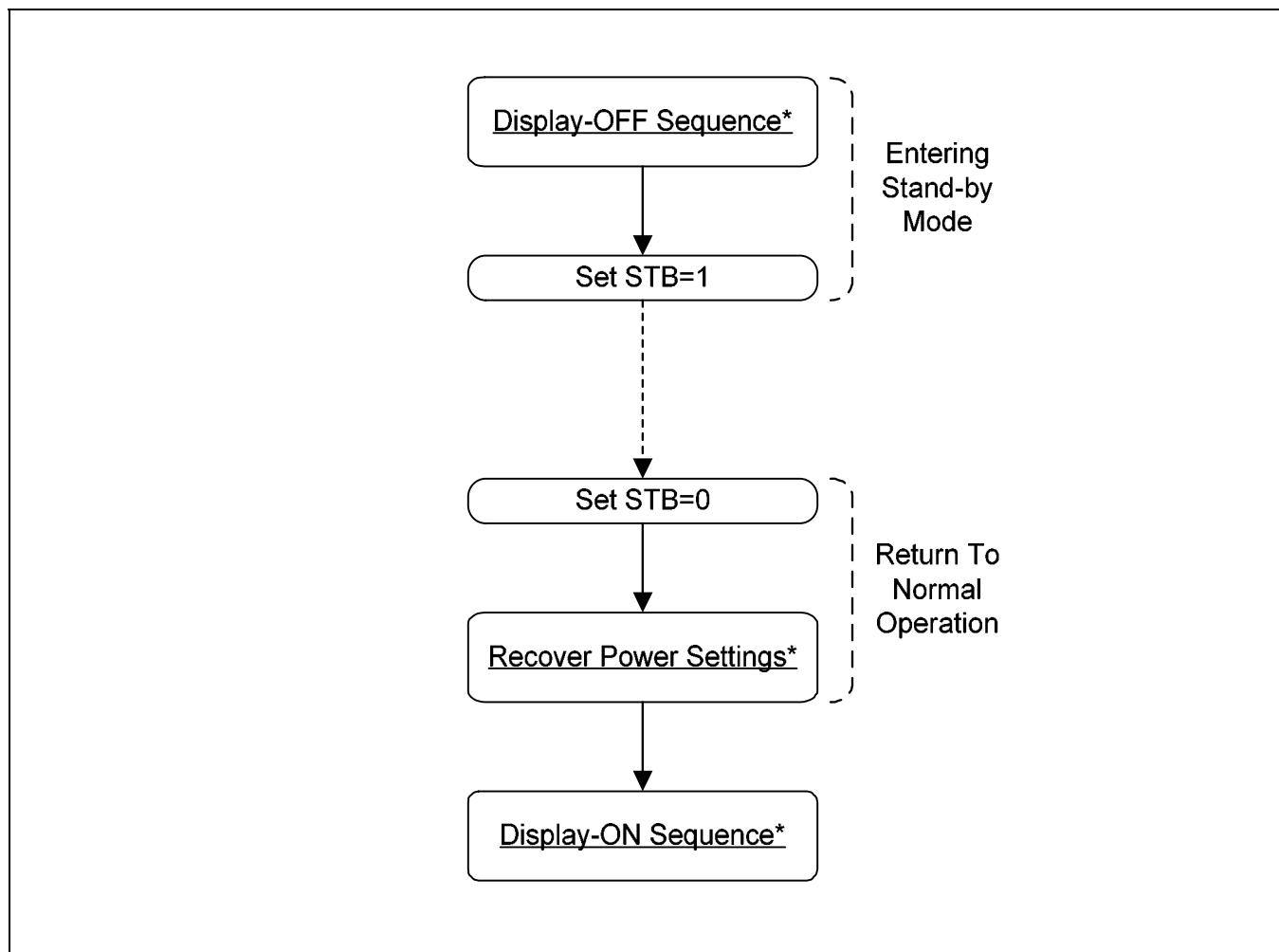
Figure 53. Stand-by Mode In / Out Sequence

N-RASTER-ROW REVERSED AC DRIVE

The S6F2002 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from 1 to 2 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.

Determine the number of the raster-rows n (NW bit set value) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.
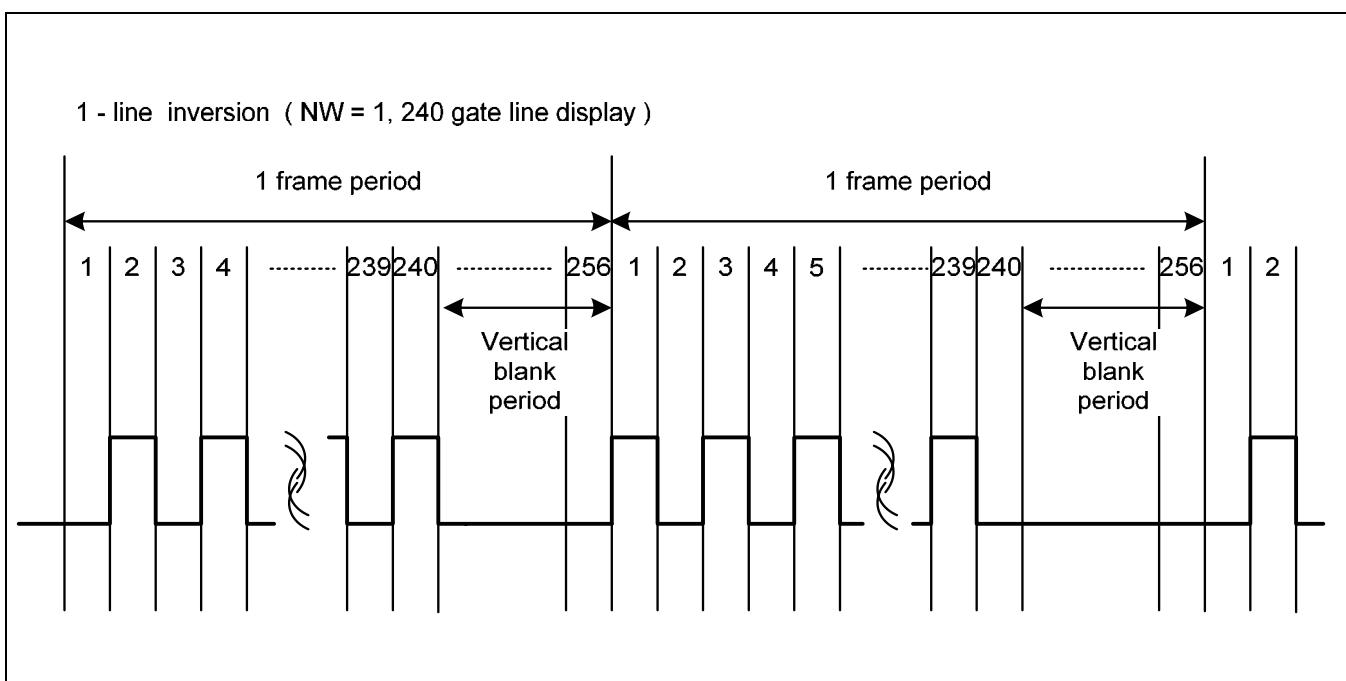
Figure 54. Example of an AC Signal under N-Raster-Row Reversed AC Drive

AC TIMING

Following diagram indicates the AC timing on the each AC drive method. After every 1 drawing, the AC timing is occurred on the reversed frame AC drive. After the AC timing, the blank (all outputs from the gate: VGOFF output) in 16H period is inserted. When the reversed n-raster-row is driving, a blank period of the 16H period is inserted after all screens are drawn.
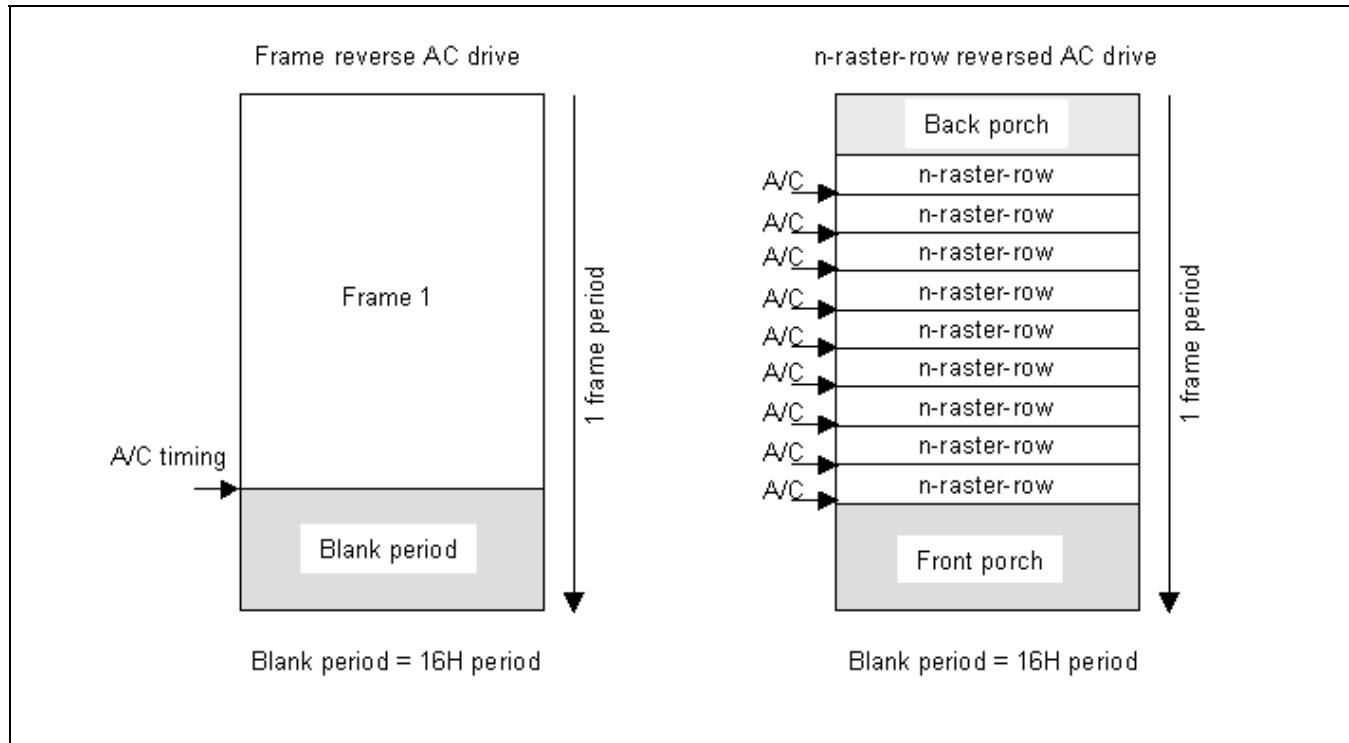
Figure 55. AC Timing

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 46. Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage for logic circuit	VDD	- 0.3 ~ + 5.0	V
Supply voltage for logic I/F circuit	VDD3	- 0.3 ~ + 5.0	V
Supply voltage for internal analog circuit	VCI	- 0.3 ~ + 5.0	V
Supply voltage for LCD driving circuit	AVDD	- 0.3 ~ + 7.0	V
Logic input voltage range	Vin	- 0.3 to VDD +0.5	V
Operating temperature	T_{opr}	-40 ~ +85	°C
Storage temperature	T_{stg}	-55 ~ +110	°C

Notes:

1. Absolute maximum rating is the limit value beyond which the IC may be broken permanently. They do not assure operations.
2. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
3. Absolute maximum rating is guaranteed only when our company's package used.

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DC CHARACTERISTICS

Table 47. DC Characteristics for Power System

(VDD= 2.0V, VDD3= VCI= 3.0V, VSS= 0V, Temp= -40'C ~ +85'C)

Characteristic		Symbol	CONDITION	MIN	TYP	MAX	Unit	Notes
Power supply for internal logic circuit		VDD	-	1.8	-	2.5	V	
Power supply for logic Interface circuit		VDD3	-	1.8	-	3.3	V	
Power supply for internal analog circuit		VCI	-	2.5	-	3.3	V	
Power supply for LCD driving circuit		AVDD	-	4.0	-	5.0	V	
Power supply 1 for ASG level shifter		VGH	"High" Level	-	18.0	-	V	
Power supply 2 for ASG level shifter		VGL	"Low" Level	-	-10.0	-	V	
Generated power for VcomL circuit		VCL	|VCL| = 0.2 x |VGL|	-	-2.0	-	V	
Generated power for ASG level shifter		VGOFF	|VGOFF| = 0.7 x |VGL| |VGH-VGOFF| max = 25V	-	-7.0	-	V	*1
Regulated power for internal logic circuit		RVDD	-	-	2.0	-	V	*2
Logic Input Voltage	High	V_{IH}	-	0.8*VDD3	-	VDD3	V	
	Low	V_{IL}	-	0	-	0.2*VDD3	V	
Logic Output Voltage	High	V_{OH}	I_{OH} = -2.0mA	VDD3-0.5		VDD3	V	
	Low	V_{OL}	I_{OL} = 2.0mA	0.0	-	0.5	V	
Input leakage current		I_{IL}	VIN = VSS or VDD3	-1.0	-	1.0	μA	
Output leakage current		I_{OL}	VIN = VSS or VDD3	-3.0	-	3.0	μA	
Output voltage for VCOMOUT high level		VcomH	Set by VCM4-0 register	3.0	-	4.5	V	
Output voltage for VCOMOUT low level		VcomL	Set by VDV4-0 register	-1.0	-	1.0	V	

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Table 48. DC Characteristics for LCD Driver Outputs

(VDD= 2.0V, VDD3= VCI= 3.0V, VSS= 0V, Temp= -40'C ~ +85'C)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Notes
LCD gate driver output ON resistance	Ron	|VGH-VGOFF| =25V VGH=18V, VGL=-10V	-	-	2		
LCD source driver High-level output current	I_{HOG}	Vso=4.5V Vsx=3.5V	-	-	-100		*3
LCD source driver Low-level output current	I_{LOG}	Vso=0.5V Vsx=1.5V	100	-	-		*3
Output voltage deviation (in single chip)	ΔVo	4.2V $\leq$ Vso	-	±24	±50		*3
		0.8V $<$ Vso $<$ 4.2V	-	±15	±30		*3
		Vso $\leq$ 0.8V	-	±28	±55		*3
Averaged output voltage deviation (between chip to chip)	ΔVd	4.2V $\leq$ Vso	-	±25	±50		*3
		0.8V $<$ Vso $<$ 4.2V	-	±15	±30		*3
		Vso $\leq$ 0.8V	-	±23	±45		*3
LCD source driver output voltage range	Vso	-	AVSS+0.1	-	GVDD-0.1	V	
LCD source driver delay	t_{SD}	AVDD=GVDD=5.0V, SAP="100"	-	-	40		
Current consumption during normal operation	IVDD	No load	-	T.B.D.	T.B.D.		*4
	IVCI		-	T.B.D.	T.B.D.	mA	

Notes:

1. Keep | VGOFF – VGL | greater than or equal to 3.0V when | VGH – VGOFF | = 25.0V
2. RVDD is used in VcomH / VcomL generation block as a reference voltage named RVDD_REF.
3. Vsx is the voltage applied to analog output pins S1 to S492. Vso is the output voltage of analog output pins S1 to S492.
4. VDD3=VCI=3.0V, VDD=2.0V, AVDD= 5.0V, VGH= 18.0V, VGL= -10.0V, NL[4:0]="11101", AP[2:0]="001", SAP[2:0]="001", VCOMG="H", EXM="L", VCM4-0="11000", VDV4-0=11000".

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AC CHARACTERISTICS

Table 49. RGB Data Interface Characteristics

$(T_A = -40 \text{ to } +85 \text{ }^{o}C)$

Characteristic	Symbol	24bit RGB Interface VDD3 = 1.8V to 3.3V		8bit RGB Interface VDD3 = 1.8V to 3.3V		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	t_{DCYC}	100	-	30	-	ns
DOTCLK rise / fall time	t_R, t_F	-	T.B.D	-	T.B.D	
DOTCLK Pulse width high	t_{DCHW}	T.B.D	-	T.B.D	-	
DOTCLK Pulse width low	t_{DCLW}	T.B.D	-	T.B.D	-	
ENABLE setup time	t_{ENS}	T.B.D	-	T.B.D	-	
ENABLE hold time	t_{ENH}	T.B.D	-	T.B.D	-	
PD data setup time	t_{PDS}	T.B.D	-	T.B.D	-	
PD data hold time	t_{PDH}	T.B.D	-	T.B.D	-	
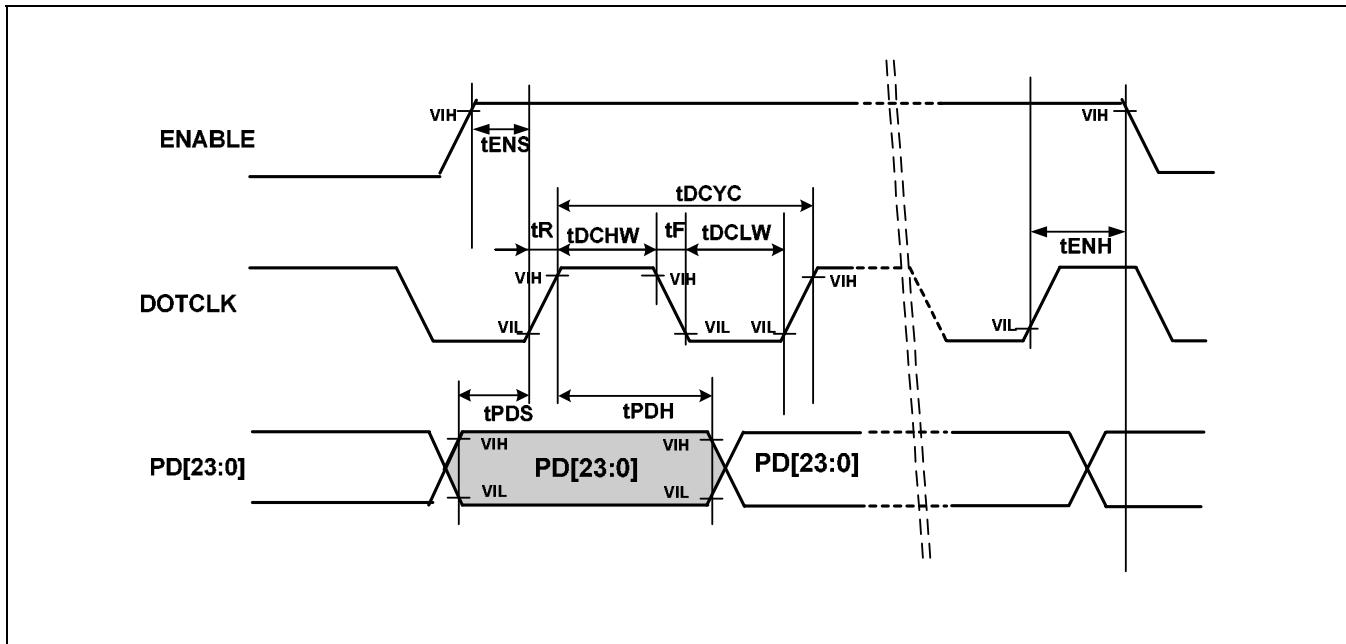
Figure 56. AC Characteristics (DE Mode)

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Table 50. Clock Synchronized Serial Mode Characteristics

$(T_A = -40$ to $+85$ ^{o}C)

Characteristic	Symbol	VDD3 = 1.8V to 3.3V		Unit
		Min.	Max.	
Serial clock cycle time	tscyc	T.B.D.	-	ns
Serial clock rise / fall time	t_R, t_F	-	T.B.D.	
Pulse width high for write	tSCHW	T.B.D.	-	
Pulse width high for read	tSCHR	T.B.D.	-	
Pulse width low for write	tSCLW	T.B.D.	-	
Pulse width low for read	tSCLR	T.B.D.	-	
Chip Select setup time	tCSS	T.B.D.	-	
Chip Select hold time	tCSH	T.B.D.	-	
Serial input data setup time	tSIDS	T.B.D.	-	
Serial input data hold time	tSIDH	T.B.D.	-	
Serial output data delay time	tSODD	-	T.B.D.	
Serial output data hold time	tSODH	T.B.D.	-	

Table 51. Reset Timing Characteristics

$(T_A = -40$ to $+85$ ^{o}C)

Characteristic	Symbol	VDD3 = 1.8V to 3.3V		Unit
		Min.	Max.	
Reset low pulse width	tRES	3*	-	us

*__Note__. Reset low pulse width shorter than 1us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

Table 52. Reset Operation Regarding tRES Pulse Width

tRES Pulse	Action
Shorter than 1 us	No reset
Longer than 3 us	Reset
Between 1 us and 3 us	Not determined
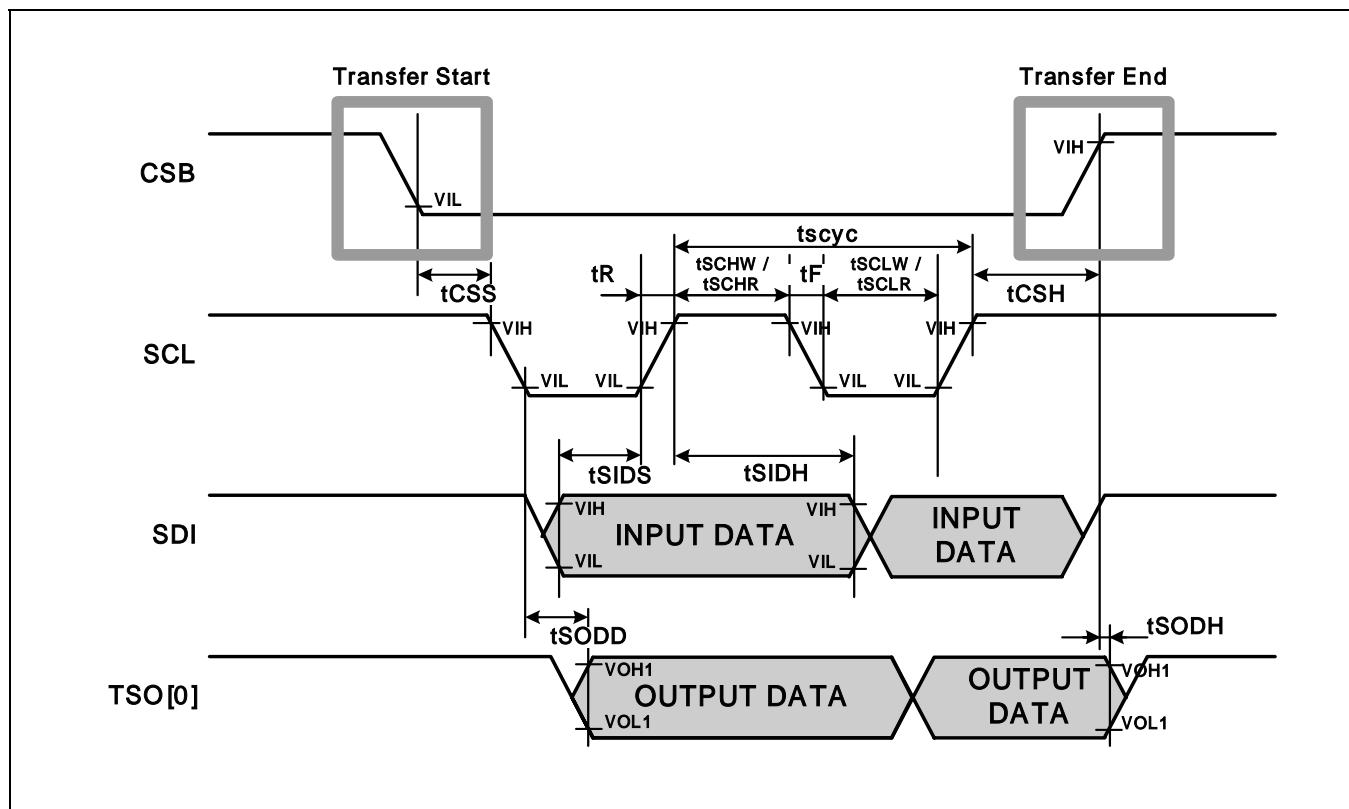
Figure 57. AC Characteristics (SPI Mode)
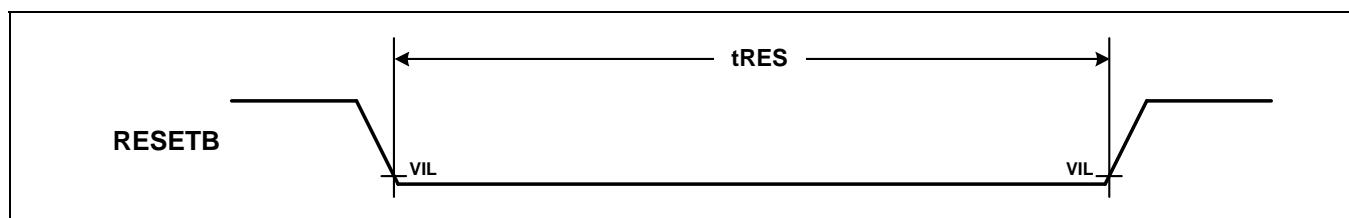
Figure 58. AC Characteristics (RESET timing)

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Table 53. AC Characteristics (STV)

$(T_A = -40 \text{ to } +85 \text{ }^{o}C)$

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Input frequency	fIN	-		-	125	kHz
Propagation delay time	td1 / td2	CL= 50pF	-	240	420	ns
Output rising / falling time	tr / tf	CL= 50pF	-	60	100	ns
Output delay time	td3	CL= 50pF	-	270	470	ns

Table 54. AC Characteristics (CKV, CKVB)

$(T_A = -40 \text{ to } +85 \text{ }^{o}C)$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input frequency	fIN	-		-	125	kHz
Propagation delay time	td1 / td2	CL= 300pF	-	240	420	ns
Output rising / falling time	tr / tf	CL= 300pF	-	240	420	ns
Output delay time	td3	CL= 300pF	-	360	630	ns
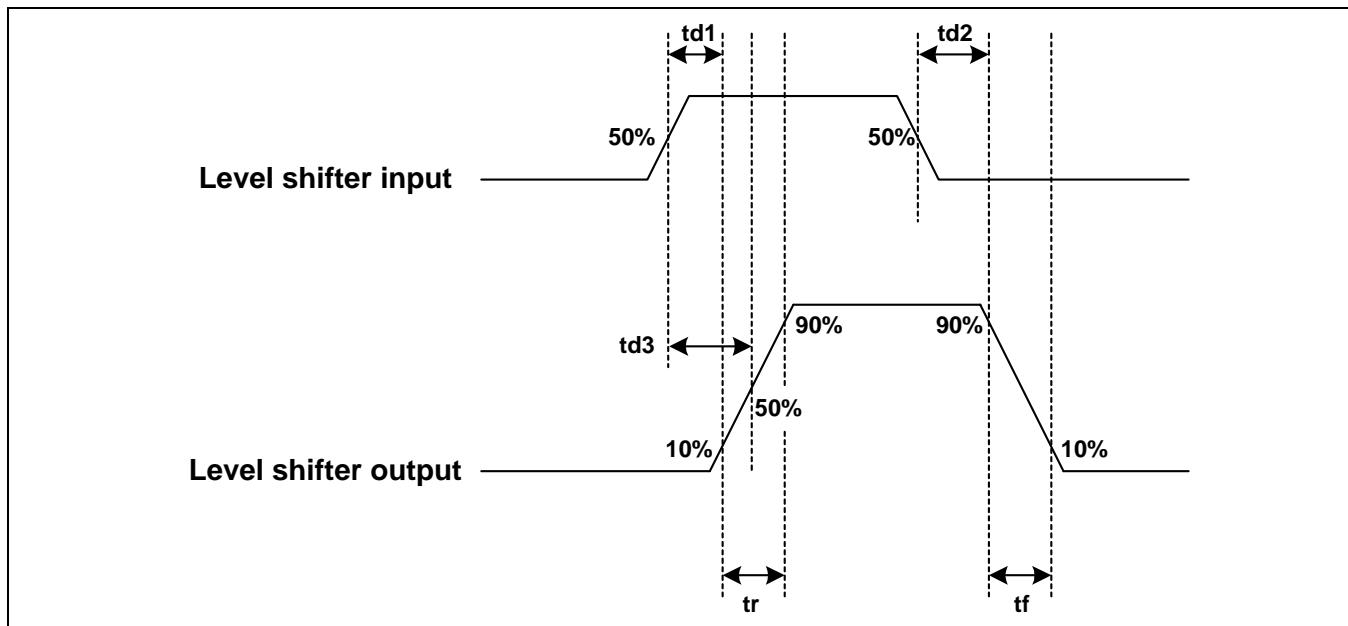
**Figure 59. Level Shifter Input / Output Waveform and AC Timing**

DATA-SHIFT DIRECTION SETTINGS

CHANNEL SELECTION SETTING

Table 55. Panel Application Examples under the Various CHS1-0 Setting

CHS1-0	CONFIGURATIONS	
'00' (128 RGB)	TFT Panel (SS=0) S1 → S384 BUMP VIEW	TFT Panel (SS=1) S1 ← S384 BUMP VIEW
'01' (160 RGB)	TFT Panel (SS=0) S1 → S480 BUMP VIEW	TFT Panel (SS=1) S1 ← S480 BUMP VIEW
'10' (164 RGB)	TFT Panel (SS=0) S1 → S492 BUMP VIEW	TFT Panel (SS=1) S1 ← S492 BUMP VIEW

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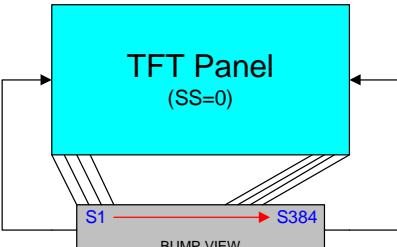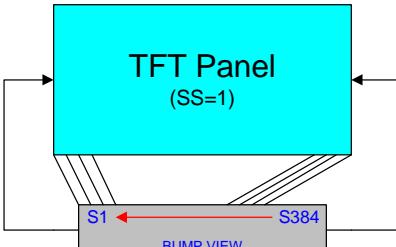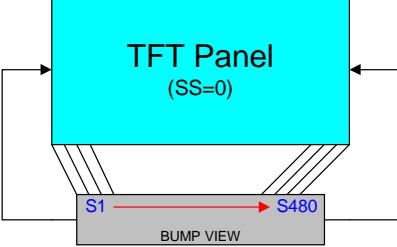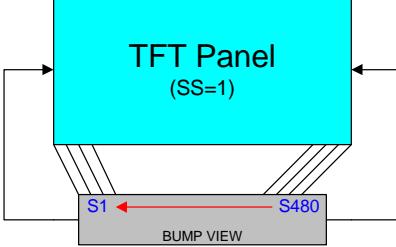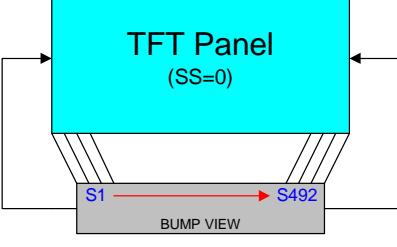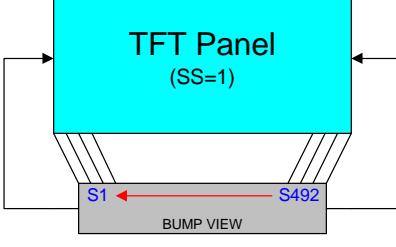
MASTER-SLAVE CONFIGURATION SETTING
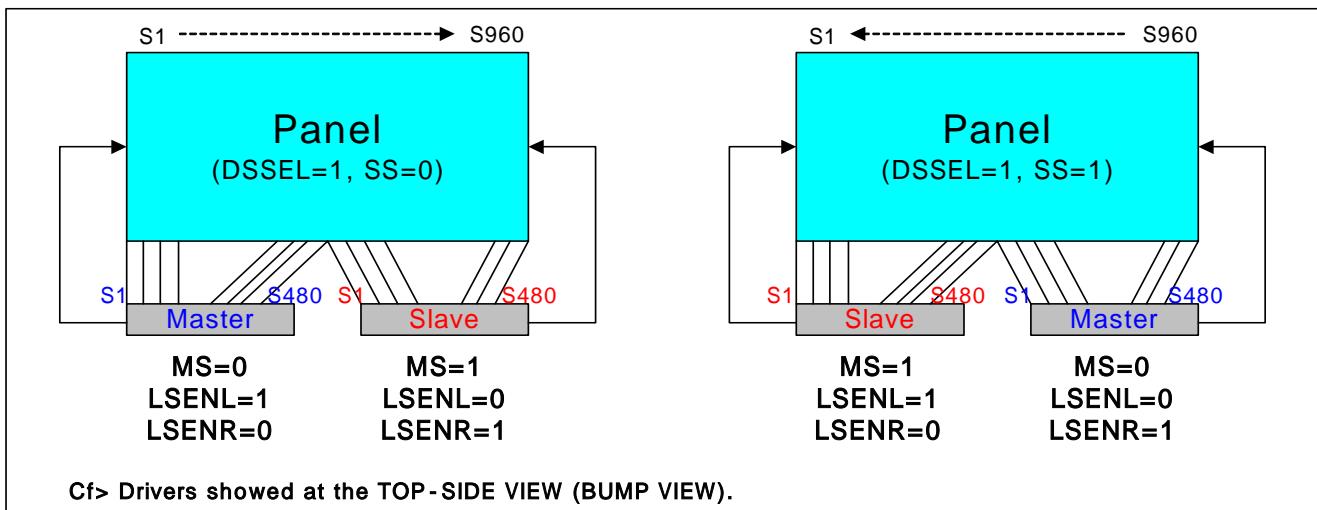
Figure 60 . Master - Slave Application Setting Example

ITO / FPC APPLICATION EXAMPLE
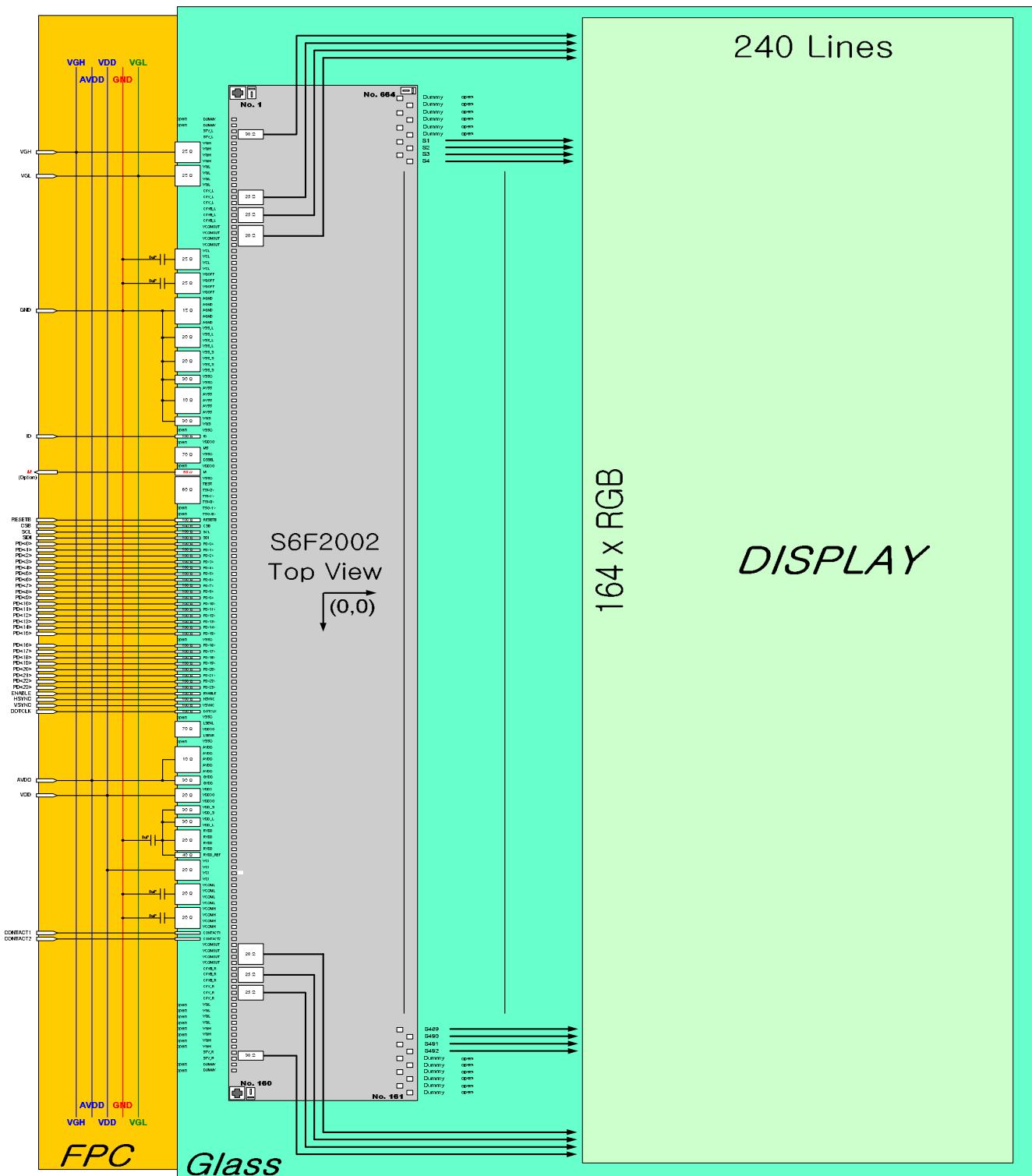
**Figure 61. ITO/FPC Application Schematic**

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CF> Operating conditions of example circuit in previous page are as below :

- Applied Voltage (External)
  - VDD   to VSS   =   3.0 V
  - VCI   to VSS   =   3.0 V
  - AVDD to VSS   =   5.0 V
  - VGH   to VSS   =   18.0 V
  - VGL   to VSS   =   -10.0 V

- Interface Mode
  - Data Width : 24-bit Parallel Mode
  - Resolution : 492-Channel * 240 Line Single Chip Mode
  - Scanning : Double ASG Mode

NOTICE

Precautions for Light
Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

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