TMC

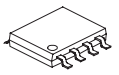
TD3842A/3843A/3844A/3845A

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLERS

DESCRIPTION

The TD3842A/3843A/3844A/3845A are fixed frequency current-mode PWM controller. They are specially designed for Off - Line and DC-to-DC converter applications with minimum external components.

These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier. current sensing comparator, and a high current totempole output Ideally suited for driving a power MOSFET. Protection circuity Includes built in under-voltage lockout and current limiting. The TD3842A and TD3844A have UVLO thresholds of 16V (on) and 10V (off) The TD3843A and TD3845A are 8.4V (on) and 7.6V (off) The TD3842A and TD3843A can operate within 100% duty cycle. The TD3844A and TD3845A can operate with 50% duty cycle.



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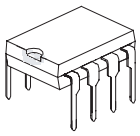

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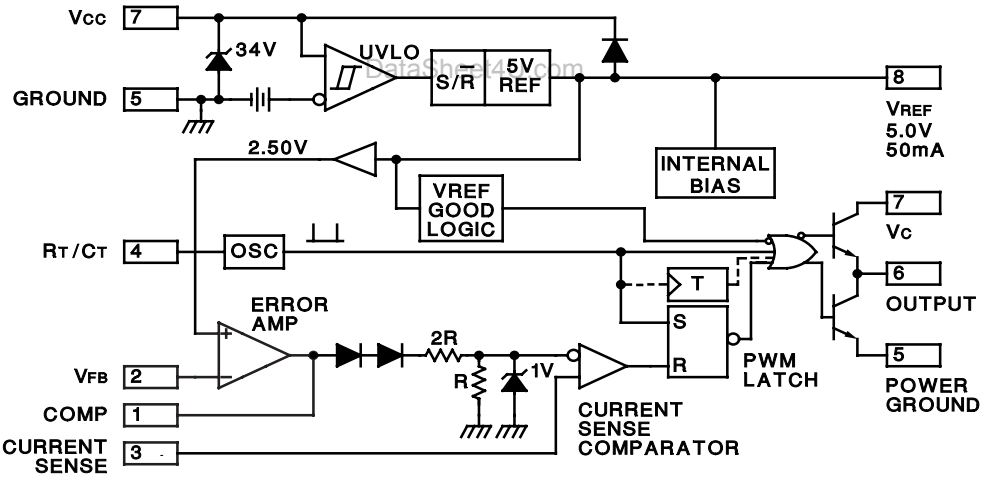
FEATURES

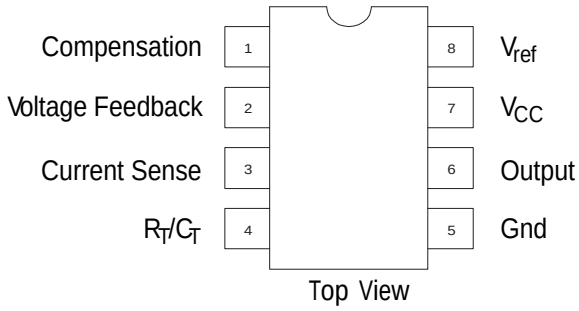
- Low Start Up Current
- Maximum Duty Clamp
- UVLO With Hysteresis
- Operating Frequency Up To 500KHz

BLOCK DIAGRAM



Note 1: Toggle flip flop used only in 3844A and 3845A.

PIN CONNECTIONS



Top View

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	V_{CC}, V_C	30	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	- 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction-to-Air N Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C

1. Maximum Package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	TD3842A/43A/44A/45A Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	-	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	-	3.0	25	mV
Temperature Stability	T_S	-	0.2	-	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.82	-	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	-	50	-	µV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	-	5.0	-	mV
Output Short Circuit Current	I_{SC}	- 30	- 85	- 180	mA
OSCILLATOR SECTION					
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{osc}	 47 46	 52 -	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta_V$	-	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{osc}/\Delta_T$	-	5.0	-	%
Oscillator Voltage Swing (Peak±to±Peak)	V_{osc}	-	1.6	-	V
Discharge Current (V_{osc} = 2.0 V) T_J = 25°C T_A = T_{low} to T_{high}	I_{dischg}	 7.5 7.2	 8.4 -	 9.3 9.5	mA

ERROR AMPLIFIER SECTION

Characteristics	Symbol	TD3842A/43A/44A/45A Min	Typ	Max	Unit
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	-	-0.1	-2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	-	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	-	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	-	dB
Output Current Sink (V_O = 1.1 V, V_{FB} = 2.7 V) Source (V_O = 5.0 V, V_{FB} = 2.3 V)	 I_{Sink} I_{Source}	 2.0 -0.5	 12 -1.0	 - -	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 -	 6.2 0.8	 - 1.1	V

2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for TD3842A/43A/44A/45A T_{high} = +70°C for TD3842A/43A/44A/45A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 4], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 6 & 7)	A_V	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 6)	V_{th}	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 to 25 V (Note 6)	PSRR	-	70	-	dB
Input Bias Current	I_{IB}	-	-2.0	-10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(in/out)}$	-	150	300	ns
OUTPUT SECTION					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA)	 V_{OL} V_{OH} 	 - - 13 12	 0.1 1.6 13.5 13.4	 0.4 2.2 - -	V
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	-	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	-	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	-	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold TD3842A/TD3844A TD 3843A/TD3845A	V_{th}	 14.5 7.8	 16 8.4	 17.5 9.0	V
Minimum Operating Voltage After Turn On TD3842A/TD3844A TD3843A/TD3845A	$V_{CC(min)}$	 8.5 7.0	 10 7.6	 11.5 8.2	V

PWM SECTION

Characteristics		Symbol	Min	Typ	Max	Unit
Duty Cycle						%
Maximum	TD3842A/TDd3843A	DC_{max}	94	96	100	
	TD3844A/TDd3845A		47	48	50	
Minimum		DC_{min}	-	-	0	

TOTAL DEVICE

Power Supply Current (Note 4)	I_{CC}				mA
Startup:					
(V_{CC} = 6.5 V for TD3843A,		-	0.5	1.0	
14 V for TD3842A) Operating		-	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	-	V

4. Adjust V_{CC} above the Startup threshold before setting to 15 V.
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for TD3842A/43A/44A/45A T_{high} = +70°C for TD3842A/43A/44A/45A
6. This parameter is measured at the latch trip point with V_{FB} = 0 V.
7. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

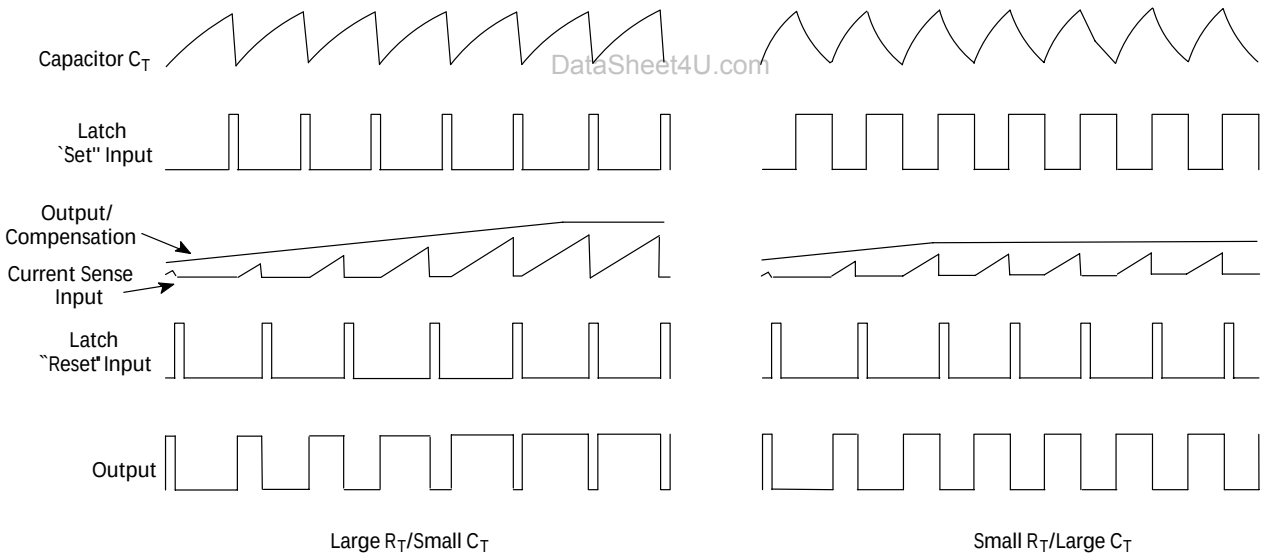
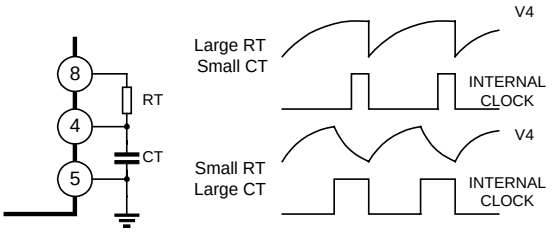
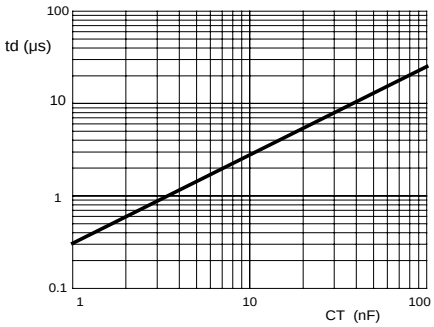


Figure 1. Timing Diagram

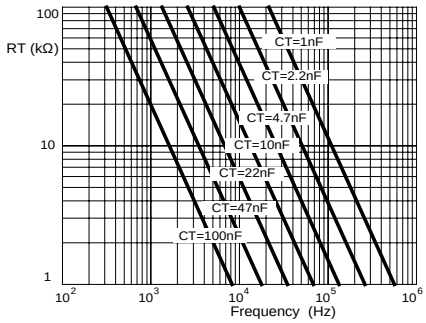
OSCILLATOR SECTION



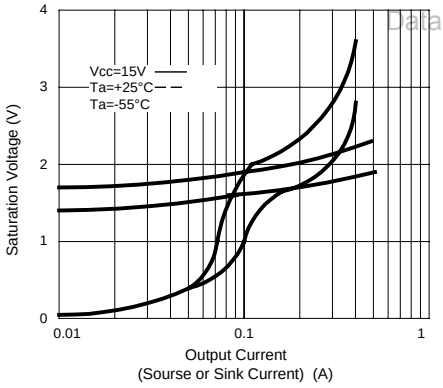
Dead time VS C_T(R_T>5kΩ)



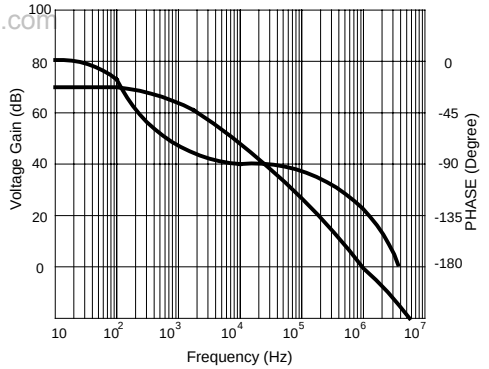
Timing Resistance Vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS



Output Saturation Characteristics

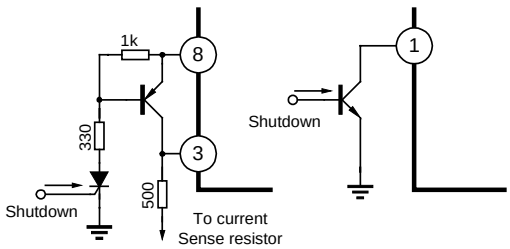


Error Amplifier Open-Loop Frequency Response

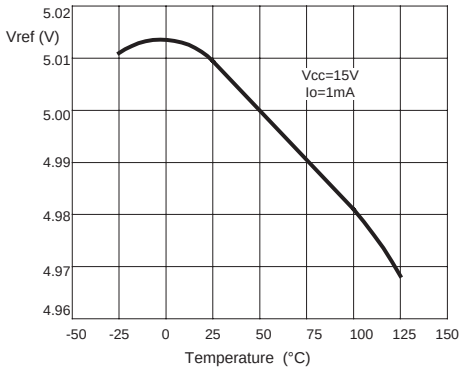
Shutdown TD3842A can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high(refer to block diagram).

The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shut–down may be accomplished by adding an SCR which be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

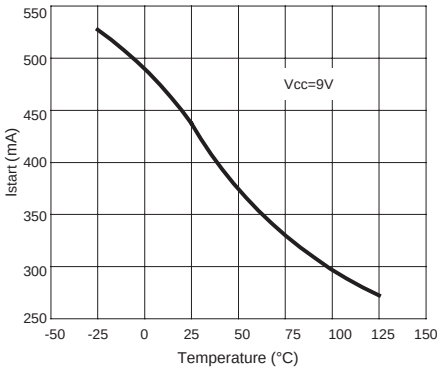
SHUTDOWN TECHNIQUES



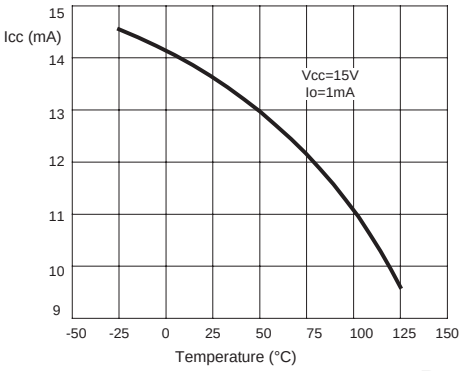
Vref Temperature Drift



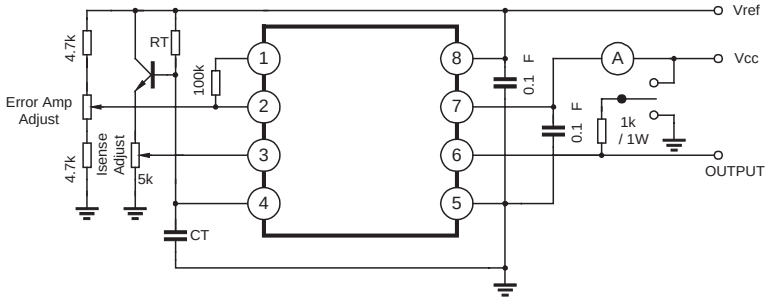
Istart Temperature Drift



Icc Temperature Drift

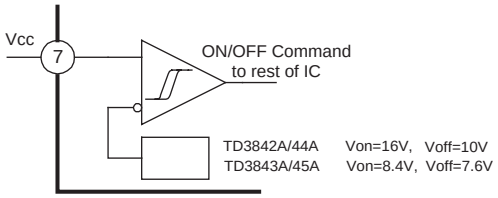


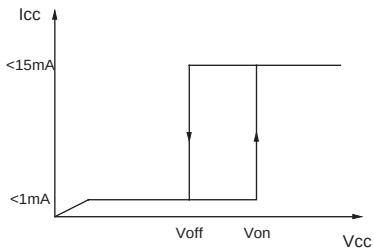
OPEN-LOOP LABORATORY TEST FIXTURE



High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in single point GND. The transistor and 5kΩ potentio-meter are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.

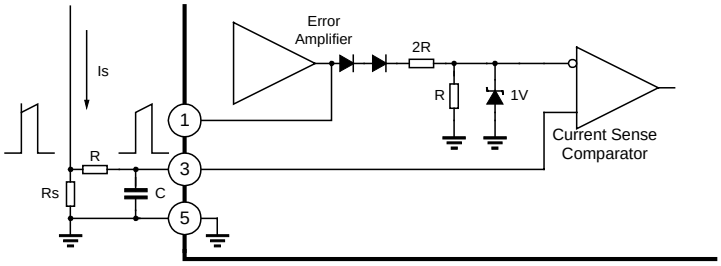
UNDER-VOLTAGE LOCKOUT





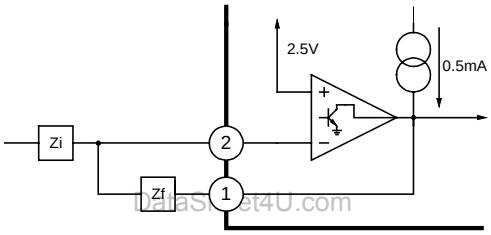
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

CURRENT SENSE CIRCUIT



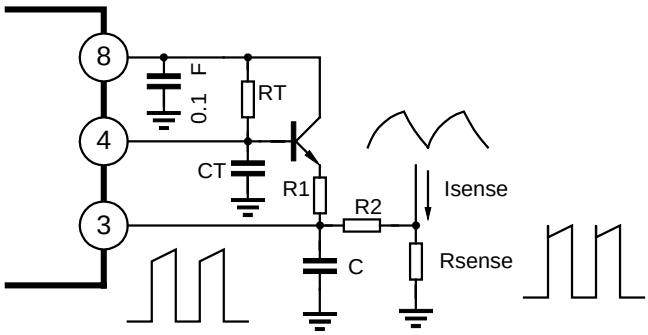
Peak current (Is) determined by the formula:
Is(MAX)=1.0V/Rs.
A small RC filter be required to suppress switch transients.

ERROR AMPLIFIER CONFIGURATION



Error amplifier can source or sink up to 0.5mA

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%.Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.