Standard Products

# UT8R256K16 256K x 16 SRAM

Advanced Data Sheet

October 9, 2002

## FEATURES

- ❑ 15ns maximum access time
- ❑ Asynchronous operation, functionally compatible with industry-standard 256K x 16 SRAMs
- ❑ CMOS compatible inputs and output levels, three-state bidirectional data bus
  - I/O Voltage 2.5 to 3.3 volts, 1.8 volt core
- ❑ Radiation performance
  - Intrinsic total-dose: 100K rad(Si)
  - SEL Immune >100 MeV-cm$^2$/mg
  - Onset LET > 24 MeV-cm$^2$/mg
  - Memory Cell Saturated Cross Section, 1.0 x 10$^{-8}$cm$^2$/bit
    - 1.0E x 10$^{-10}$ errors/bit-day, Adams to 90% geosynchronous heavy ion
  - Neutron Fluence: 3.0E14n/cm$^2$
  - Dose Rate (estimated)
    - Upset 1.0E9 rad(Si)/sec
    - Latchup >1.0E11 rad(Si)/sec
- ❑ Packaging options:
  - TBD
- ❑ Standard Microcircuit Drawing pending
  - QML compliant part

## INTRODUCTION

The UT8R256K16 is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by taking chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 16 I/O pins (DQ0 through DQ15) is then written into the location specified on the address pins (A0 through A17). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 16 input/output pins (DQ0 through DQ15) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).



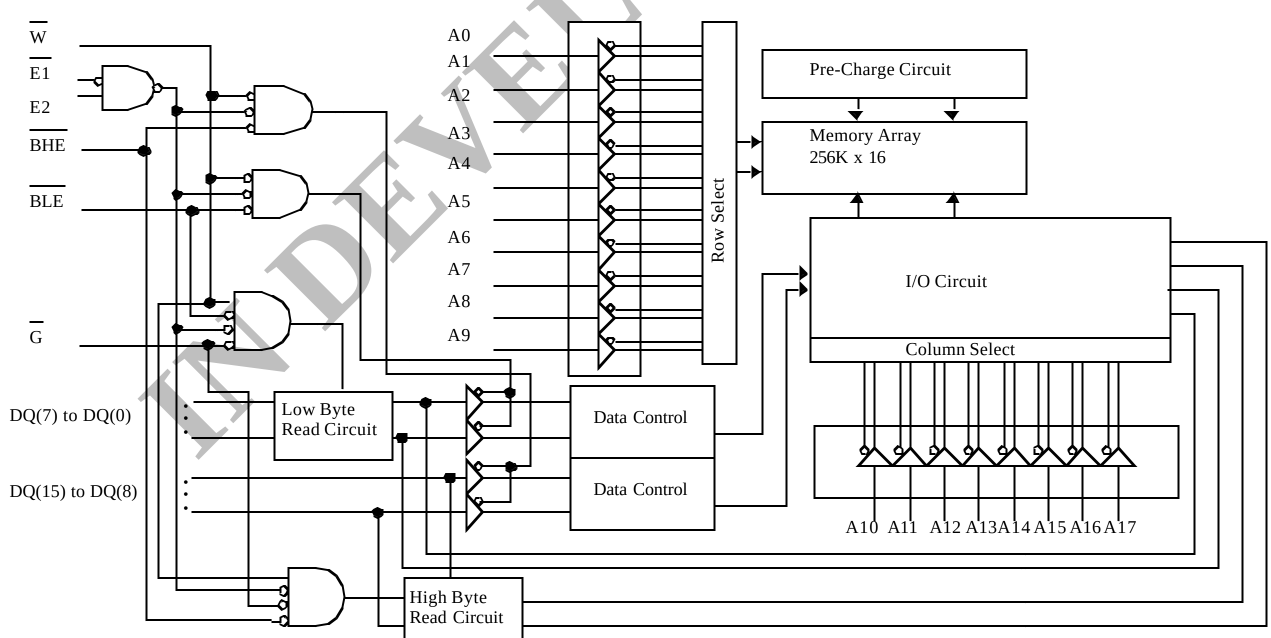



**Figure 1. UT8R256K16 SRAM Block Diagram**

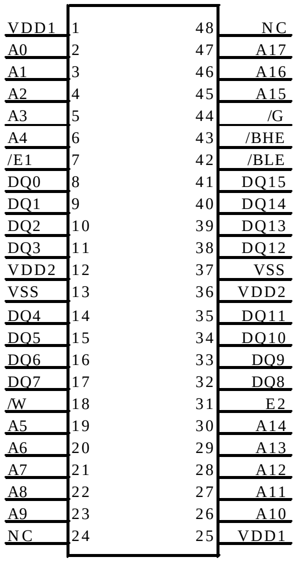



**Figure 2. 15ns SRAM Pinout**

## PIN NAMES

| | | | |
|---|---|---|---|
| A(17:0) | Address Input | $\overline{W}$ | Write Enable |
| DQ(15:0) | Data Input/Output | $\overline{G}$ | Output Enable |
| $\overline{E1}$ | Enable (Active Low) | $V_{DD1}$ | Power (1.8V) |
| E2 | Enable (Active High) | $V_{DD2}$ | Power (2.5V) |
| $\overline{BHE}$ and BLE | Low and high byte enable | $V_{SS}$ | Ground |

# DEVICE OPERATION

The UT8R256K16 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), Half-word Enables ($\overline{BLE}$/$\overline{BHE}$) and Output Enable ($\overline{G}$); 18 address inputs, A(17:0); and 16 bidirectional data lines, DQ(15:0). $\overline{E1}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{E1}$ and E2 enables the device, causes $I_{DD}$ to rise to its active value, and decodes the 18 address inputs to select one of 262,144 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

**Table 1. Device Operation Truth Table**

| $\overline{G}$ | $\overline{W}$ | E2 | $\overline{E1}$ | $\overline{BLE}$ | $\overline{BHE}$ | I/O Mode | Mode |
|---|---|---|---|---|---|---|---|
| X | X | X | H | X | X | DQ(15:8) 3-State DQ(7:0) 3-State | Standby |
| X | X | L | X | X | X | DQ(15:8) 3-State DQ(7:0) 3-State | Standby |
| L | H | H | L | L | H | DQ(15:8) 3-State DQ(7:0) Data Out | Low Byte Read |
| L | H | H | L | H | L | DQ(15:8) Data Out DQ(7:0) 3-State | High Byte Read |
| L | H | H | L | L | L | DQ(15:8) Data Out DQ(7:0) Data Out | Word Read |
| X | L | H | L | L | L | DQ(15:8) Data In DQ(7:0) Data In | Word Write |
| X | L | H | L | L | H | DQ(15:8) 3-State DQ(7:0) Data In | Low Byte Write |
| X | L | H | L | H | L | DQ(15:8) Data In DQ(7:0) 3-State | High Byte Write |
| H | H | H | L | X | X | DQ(15:8) DQ(7:0) All 3-State | 3-State |
| X | X | H | L | H | H | DQ(15:8) DQ(7:0) All 3-State | 3-State |

**Notes:**
1. “X” is defined as a “don’t care” condition.
2. Device active; outputs disabled.

## READ CYCLE

A combination of $\overline{W}$ and E2 greater than $V_{IH}$ (min) and $\overline{E1}$ less than $V_{IL}$ (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(15:0) after the specified $t_{AVQV}$ is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time ($t_{AVAV}$).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified $t_{ETQV}$ is satisfied, the 16-bit word addressed by A(17:0) is accessed and appears at the data outputs DQ(15:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is $t_{GLQV}$ unless $t_{AVQV}$ or $t_{ETQV}$ have not been satisfied.

## Write Cycle

A combination of $\overline{W}$ and $\overline{E1}$ less than $V_{IL}$ (max) and E2 greater than $V_{IH}$(min) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than $V_{IH}$(min), or when $\overline{W}$ is less than $V_{IL}$(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by $t_{WLWH}$ when the write is initiated by $\overline{W}$, and by $t_{ETWH}$ when the write is initiated by $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait user must wait $t_{WLQZ}$ before applying data to the 16 bidirectional pins DQ(15:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by $t_{WLEF}$ when the write is initiated by $\overline{W}$, and by $t_{ETEF}$ when the write is initiated by either $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait $t_{WLQZ}$ before applying data to the sixteen bidirectional pins DQ(15:0) to avoid bus contention.

## BYTE ENABLES

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be accessed. $\overline{BLE}$ controls the lower bits DQ(7:0). $\overline{BHE}$ controls the upper bits DQ(15:8). Writing to the device is performed by asserting $\overline{E1}$, E2 and the byte enables. Reading the device is performed by asserting $\overline{E1}$, E2, $\overline{G}$, and the byte enables while $\overline{W}$ is held inactive (HIGH).

| $\overline{BHE}$ | $\overline{BLE}$ | OPERATION |
|---|---|---|
| 0 | 0 | 16-bit read or write cycle |
| 0 | 1 | 8-bit high byte read or write cycle (low byte bi-direction pins DQ(7:0) are in 3 -state) |
| 1 | 0 | 8-bit low byte read or write cycle (high byte bi-direction pins DQ(15:8) are in 3 -state) |
| 1 | 1 | High and Low byte bi-directional pins remain in 3-state, write function disabled |

## RADIATION HARDNESS

The UT8R256K16 SRAM incorporates special design, layout, and process features which allows operation in a limited radiation environment.

**Table 2. Radiation Hardness Design Specifications[1]**

| | | |
|---|---|---|
| Total Dose | 100K | rad(Si) |
| Heavy Ion Error Rate[2] | 1.0E-10 | Errors/Bit-Day |

**Notes:**

1. The SRAM is immune to latchup to particles of 128MeV-cm$^2$/mg.
2. 10% worst case particle environment, Geosynchronous orbit, 0.025 mils of Aluminum.

## Supply Sequencing

No supply voltage sequencing is required between $V_{DD1}$ and $V_{DD2}$.

**ABSOLUTE MAXIMUM RATINGS**[1]

(Referenced to $V_{SS}$)

| SYMBOL | PARAMETER | LIMITS |
|---|---|---|
| $V_{DD1}$ | DC supply voltage | -0.3 to 2.0V |
| $V_{DD2}$ | DC supply voltage | -0.3 to 3.8V |
| $V_{I/O}$ | Voltage on any pin | -0.3 to 3.8V |
| $T_{STG}$ | Storage temperature | -65 to +150°C |
| $P_D$ | Maximum power dissipation | 1.2W |
| $T_J$ | Maximum junction temperature | +150°C |
| $\Theta_{JC}$ | Thermal resistance, junction-to-case[2] | 5°C/W |
| $I_I$ | DC input current | ±5 mA |

**Notes:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

3. Test per MIL-STD-883, Method 1012.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL | PARAMETER | LIMITS |
|---|---|---|
| $V_{DD1}$ | Positive supply voltage | 1.7 to 1.9V |
| $V_{DD2}$ | Positive supply voltage | 2.25 to 3.6V |
| $T_C$ | Case temperature range | -55 to +125°C |
| $V_{IN}$ | DC input voltage | 0V to $V_{DD2}$ |

**DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)***
(-55°C to +125°C)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | $.7^*V_{DD2}$ | | V |
| $V_{IL}$ | Low-level input voltage | | | $.3^*V_{DD2}$ | V |
| $V_{OL1}$ | Low-level output voltage | $I_{OL}$ = 8mA, $V_{DD2}$ = $V_{DD2}$ (min) | | $.2^*V_{DD2}$ | V |
| $V_{OH1}$ | High-level output voltage | $I_{OH}$ = -4mA, $V_{DD2}$ = $V_{DD2}$ (min) | $.8^*V_{DD2}$ | | V |
| $C_{IN}$ [1] | Input capacitance | $f$ = 1MHz @ 0V | | 7 | pF |
| $C_{IO}$ [1] | Bidirectional I/O capacitance | $f$ = 1MHz @ 0V | | 7 | pF |
| $I_{IN}$ | Input leakage current | $V_{IN}$ = $V_{DD2}$ and $V_{SS}$ | -2 | 2 | µA |
| $I_{OZ}$ | Three-state output leakage current | $V_O$ = $V_{DD2}$ and $V_{SS}$<br>$V_{DD2}$ = $V_{DD2}$ (max), $\overline{G}$ = $V_{DD2}$ (max) | -2 | 2 | µA |
| $I_{OS}$ [2, 3] | Short-circuit output current | $V_{DD2}$ = $V_{DD2}$ (max), $V_O$ = $V_{DD2}$<br>$V_{DD2}$ = $V_{DD2}$ (max), $V_O$ = $V_{SS}$ | -100 | +100 | mA |
| $I_{DD1}(OP_1)$ | Supply current operating @ 1MHz | Inputs : $V_{IL}$ = $V_{SS}$ + 0.2V,<br>$V_{IH}$ = $V_{DD2}$ + 0.2V , $I_{OUT}$ = 0<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | 1 | mA |
| $I_{DD1}(OP_2)$ | Supply current operating @100MHz, | Inputs : $V_{IL}$ = $V_{SS}$ + 0.2V,<br>$V_{IH}$ = $V_{DD2}$ + 0.2V, $I_{OUT}$ = 0<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | 55 | mA |
| $I_{DD2}(OP_1)$ | Supply current operating @ 1MHz | Inputs : $V_{IL}$ = $V_{SS}$ + 0.2V,<br>$V_{IH}$ = $V_{DD2}$ + 0.2V , $I_{OUT}$ = 0<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | TBD | mA |
| $I_{DD2}(OP_2)$ | Supply current operating @100MHz, | Inputs : $V_{IL}$ = $V_{SS}$ + 0.2V,<br>$V_{IH}$ = $V_{DD2}$ + 0.2V, $I_{OUT}$ = 0<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | TBD | mA |
| $I_{DD}(SB)$ [4] | Supply current standby @0Hz | CMOS inputs , $I_{OUT}$ = 0<br>$\overline{E1}$ = $V_{DD2}$, E2 = GND<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | 50 | mA |
| $I_{DD}(SB)$ [4] | Total Supply current standby A(17:0) @ 10MHz | CMOS inputs , $I_{OUT}$ = 0<br>$\overline{E1}$ = $V_{DD2}$ - 0.5, E2 = GND,<br>$V_{DD1}$ = $V_{DD1}$ (max), $V_{DD2}$ = $V_{DD2}$ (max) | | 55 | mA |

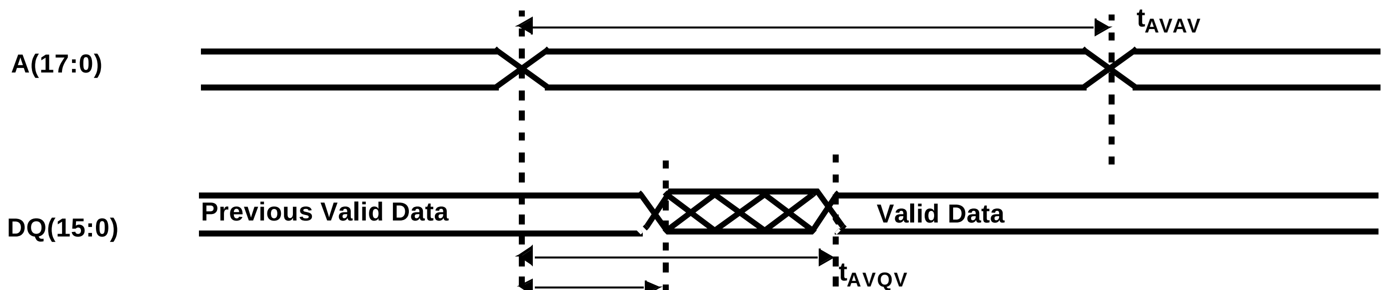
**Notes:**
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E5 rad(Si).
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. $V_{IH}$ = $V_{DD2}$ (max), $V_{IL}$ = 0V.

## AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

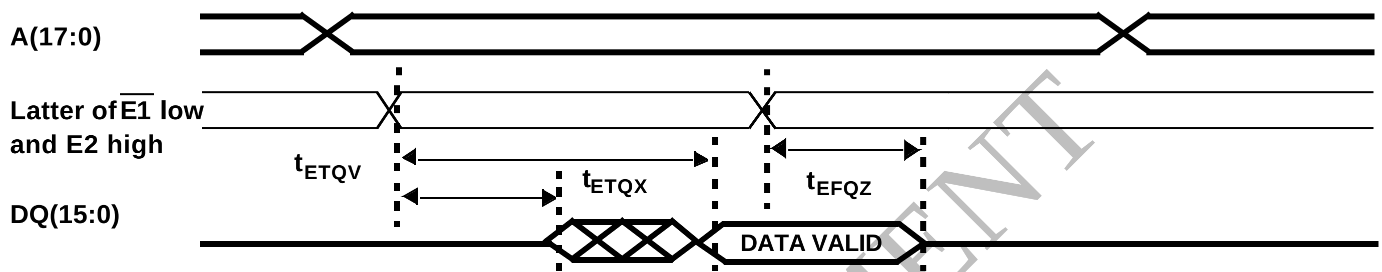
| SYMBOL | PARAMETER | 8R256K16-15 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $t_{AVAV}$[1] | Read cycle time | 15 | | ns |
| $t_{AVQV}$ | Read access time | | 15 | ns |
| $t_{AXQX}$[2] | Output hold time | 5 | | ns |
| $t_{GLQX}$[2] | $\overline{G}$-controlled output enable time | 0 | | ns |
| $t_{GLQV}$ | $\overline{G}$-controlled output enable time | | 7 | ns |
| $t_{GHQZ}$[2] | $\overline{G}$-controlled output three-state time | 0 | 7 | ns |
| $t_{ETQX}$[2,3] | E-controlled output enable time | 5 | | ns |
| $t_{ETQV}$[3] | E-controlled access time | | 15 | ns |
| $t_{EFQZ}$[4] | E-controlled output three-state time[2] | 0 | 7 | ns |
| $t_{BLZ}$ | $\overline{BLE}$, $\overline{BHE}$ Enable to Output in Low-Z | 0 | | ns |
| $t_{BHZ}$ | $\overline{BLE}$, $\overline{BHE}$ Enable to Output in High-Z | | 7 | ns |
| $t_{BA}$ | $\overline{BLE}$, $\overline{BHE}$ Access Time | | 7 | ns |

**Notes:**
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Guaranteed but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.
4. The EF (enable false) notation refers to the latter rising edge of E1 or falling edge of E2.




**Assumptions:**
1. $\overline{E1}$ and $\overline{G} \le V_{IL}$ (max) and E2 and $\overline{W} \ge V_{IH}$ (min)

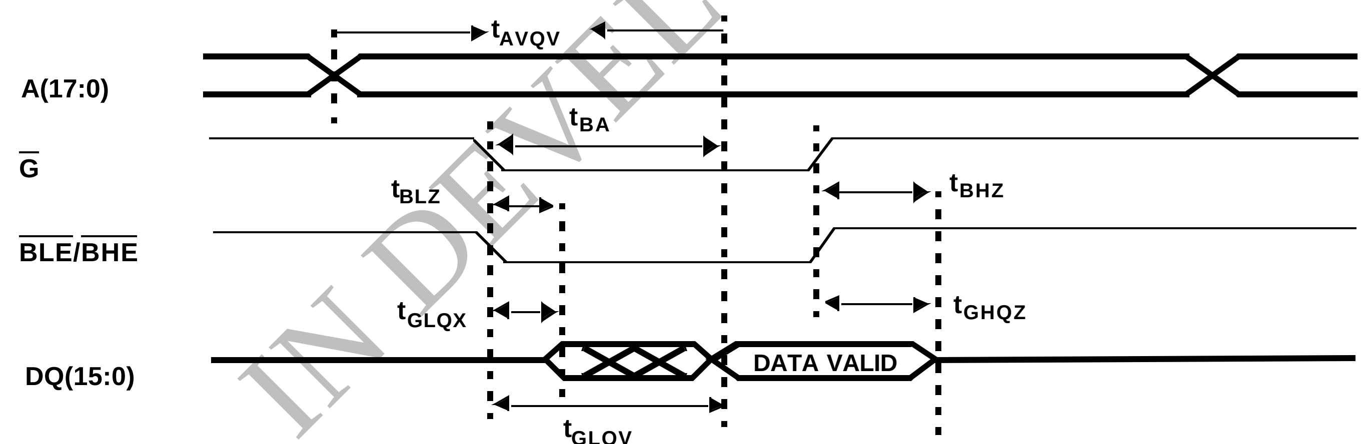
**Figure 3a. SRAM Read Cycle 1: Address Access**




**Assumptions:**
1. $\overline{G}$, $\overline{BHE}$, $\overline{BLE} \le V_{IL}$ (max) and $\overline{W} \ge V_{IH}$ (min)

**Figure 3b. SRAM Read Cycle 2: Chip Enable Access**






**Assumptions:**
1. $\overline{E1} \le V_{IL}$ (max), E2 and $\overline{W} \ge V_{IH}$ (min)

**Figure 3c. SRAM Read Cycle 3: Output Enable Access**

**AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)***

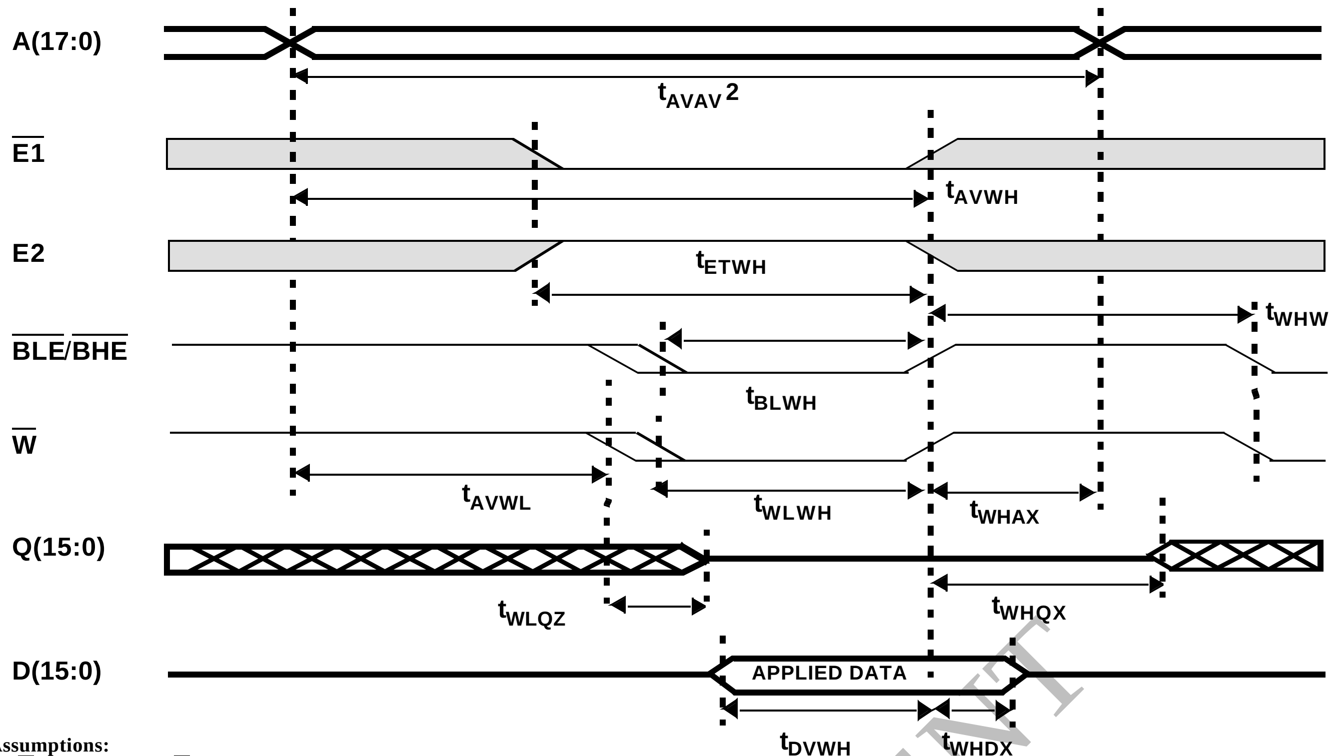
(-55°C to +125°C, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

| SYMBOL | PARAMETER | 8R256K16-15 MIN | 8R256K16-15 MAX | UNIT |
|---|---|---|---|---|
| $t_{AVAV}$[1] | Write cycle time | 15 | | ns |
| $t_{ETWH}$ | Device enable to end of write | 10 | | ns |
| $t_{AVET}$ | Address setup time for write ($\overline{E1}$/E2- controlled) | 0 | | ns |
| $t_{AVWL}$ | Address setup time for write ($\overline{W}$ - controlled) | 0 | | ns |
| $t_{WLWH}$ | Write pulse width | 10 | | ns |
| $t_{WHAX}$ | Address hold time for write ($\overline{W}$ - controlled) | 0 | | ns |
| $t_{EFAX}$ | Address hold time for device enable ($\overline{E1}$/E2- controlled) | 0 | | ns |
| $t_{WLQZ}$[2] | $\overline{W}$ - controlled three-state time | 0 | 7 | ns |
| $t_{WHQX}$[2] | $\overline{W}$ - controlled output enable time | 4 | | ns |
| $t_{ETEF}$ | Device enable pulse width ($\overline{E1}$/E2 - controlled) | 10 | | ns |
| $t_{DVWH}$ | Data setup time | 7 | | ns |
| $t_{WHDX}$ | Data hold time | 0 | | ns |
| $t_{WLEF}$ | Device enable controlled write pulse width | 10 | | ns |
| $t_{DVEF}$ | Data setup time | 7 | | ns |
| $t_{EFDX}$ | Data hold time | 0 | | ns |
| $t_{AVWH}$ | Address valid to end of write | 10 | | ns |
| $t_{WHWL}$ | Write disable time | 4 | | ns |
| $t_{BLWH}$ | $\overline{BLE}$, $\overline{BHE}$ low to write high | 10 | | ns |
| $t_{BLEF}$ | $\overline{BLE}$, $\overline{BHE}$ low to enable high | 10 | | ns |

**Notes**:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

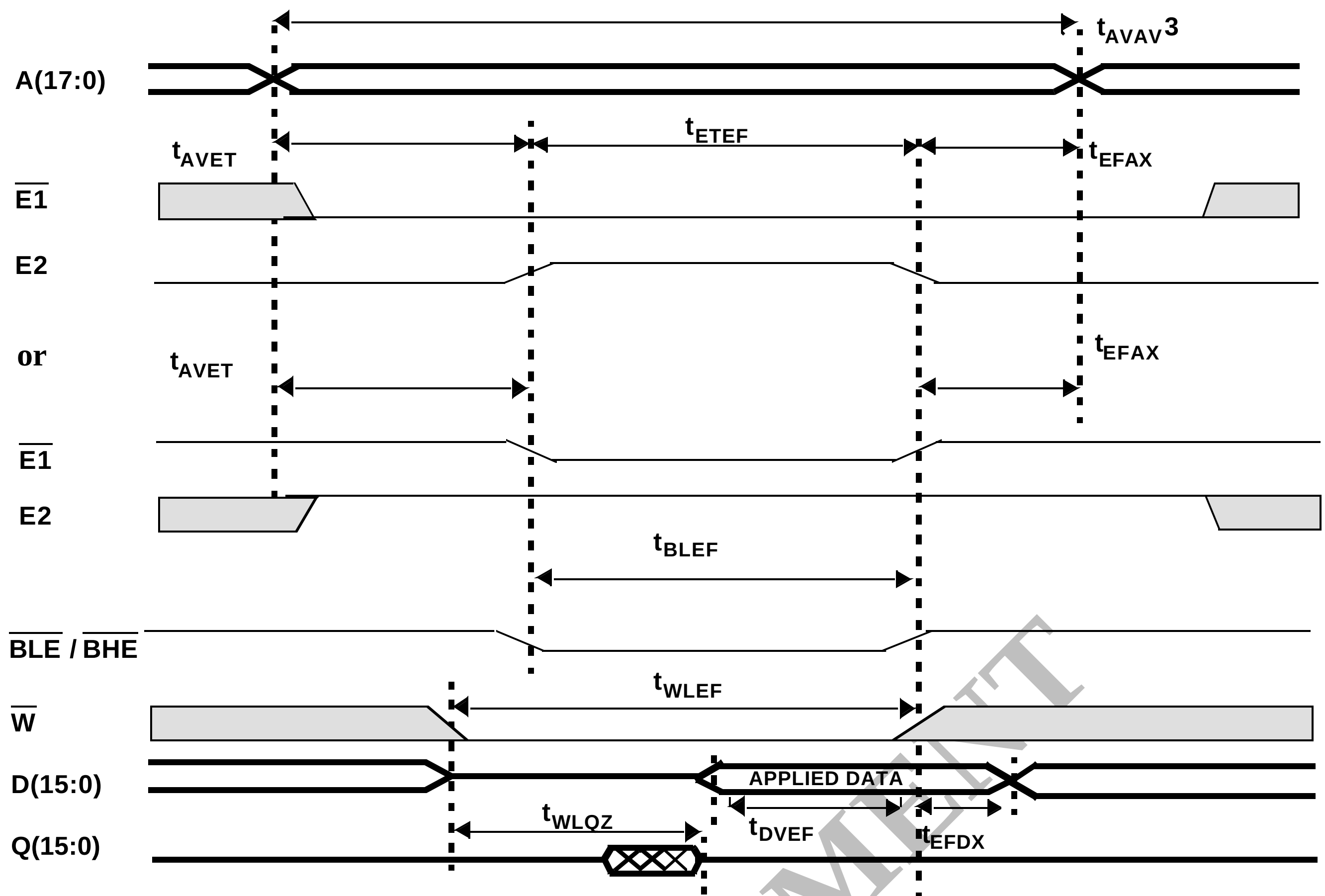
1. Guaranteed but not tested ($\overline{G}$ high).
2. Three-state is defined as 200mV change from steady-state output voltage.




**Assumptions:**

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(15:0) will be in three-state for the entire cycle.
2. G high for $t_{AVAV}$ cycle.

**Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access**




**Assumptions & Notes:**

1. G $\leq$ $V_{IL}$ (max). If G $\geq$ $V_{IH}$ (min) then Q(15:0) will be in three-state for the entire cycle.
2. Either E1 scenario above can occur.
3. G high for $t_{AVAV}$ cycle.

**Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access**

**DATA RETENTION CHARACTERISTICS (Pre and Post-Radiation)**
**($T_C$ = 25°C, $V_{DD2}$ = $V_{DD2}$ (min), 1 Sec DR Pulse)**

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| $V_{DR}$ | $V_{DD1}$ for data retention | 1.0 | -- | V |
| $I_{DDR}$ [1] | Data retention current | -- | 10 | μA |
| $t_{EFR}$ [1,2] | Chip deselect to data retention time | 0 | | ns |
| $t_R$ [1,2] | Operation recovery time | $t_{AVAV}$ | | ns |

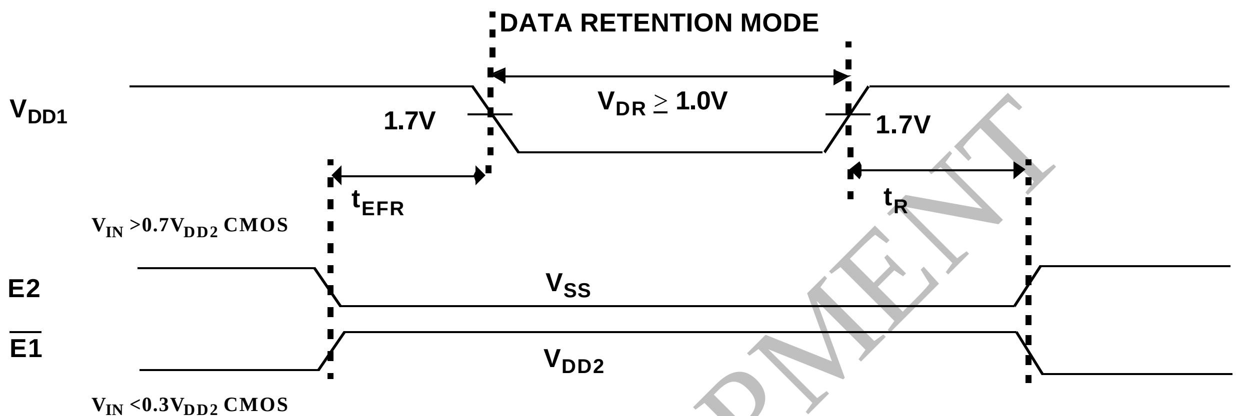
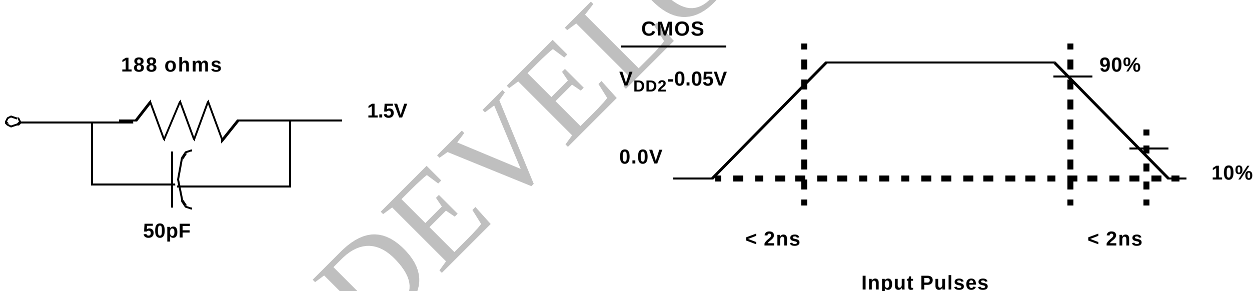



**Figure 5. Low $V_{DD}$ Data Retention Waveform**




**Notes:**
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$).

**Figure 6. AC Test Loads and Input Waveforms**

**PACKAGING**

**TBD**

## ORDERING INFORMATION

### 256K x 16 SRAM

UT **** - * * * * *

Lead Finish:
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option (gold or solder)

Screening:
(C) = Military Temperature Range flow
(P) = Prototype flow

Package Type:
(TBD)

Access Time:
(15) = 15ns access time

Device Type:
(8R256K16) =256K x 16 SRAM



**Notes:**
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55 °C, room temp, and 125°C. Radiation neither tested nor guaranteed.

**256K x 16 SRAM: SMD**

5962 - **TBD** *** * *

Lead Finish:
(A) = Hot solder dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Case Outline:
(TBD)

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type
(01) = 15ns access time, CMOS I/O

Drawing Number: TBD

Total Dose:
(R) = 100K rad(Si)

Federal Stock Class Designator: No options

**Notes:**

1.Lead finish (A,C, or X) must be specified.
2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.