DRA4124E

Silicon PNP epitaxial planar type

For digital circuits
Complementary to DRC4124E
DRA2124E in NS through hole type package

■ Features

- Low collector-emitter saturation voltage $V_{CE(sat)}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

■ Packaging

DRA4124E0A Radial type: 5000 pcs / carton

■ Absolute Maximum Ratings $T_a = 25°C$

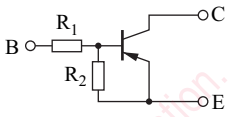
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	–50	V
Collector-emitter voltage (Base open)	V_{CEO}	–50	V
Collector current	I_C	–100	mA
Total power dissipation	P_T	300	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

■ Package

- Code
  NS-B2-B-B
  Package dimension clicks here.→
- Pin Name
  1: Emitter
  2: Collector
  3: Base

■ Marking Symbol: LE

■ Internal Connection



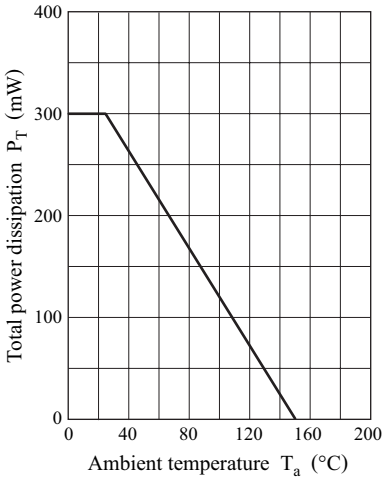
Resistance value	R_1	22	kΩ
	R_2	22	kΩ

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

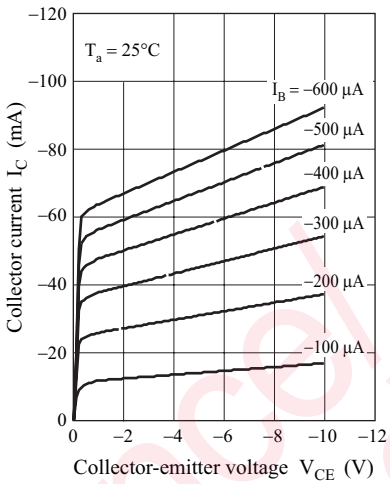
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = –10$ μA, $I_E = 0$	–50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = –2$ mA, $I_B = 0$	–50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = –50$ V, $I_E = 0$			– 0.1	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = –50$ V, $I_B = 0$			– 0.5	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = –6$ V, $I_C = 0$			– 0.2	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = –10$ V, $I_C = –5$ mA	60			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = –10$ mA, $I_B = – 0.5$ mA			– 0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = – 0.2$ V, $I_C = –5$ mA	–2.6			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = –5$ V, $I_C = –100$ μA			– 0.8	V
Input resistance	R_1		–30%	22	+30%	kΩ
Resistance ratio	R_1 / R_2		0.8	1.0	1.2	—

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

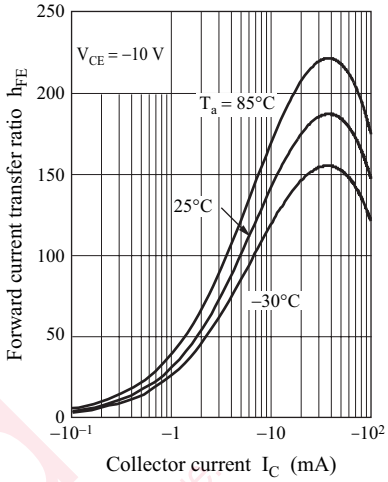
P_T — T_a



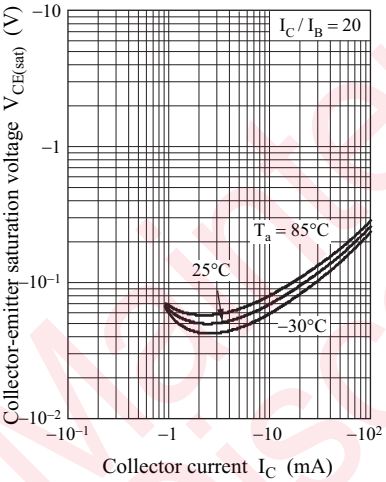
I_C — V_{CE}



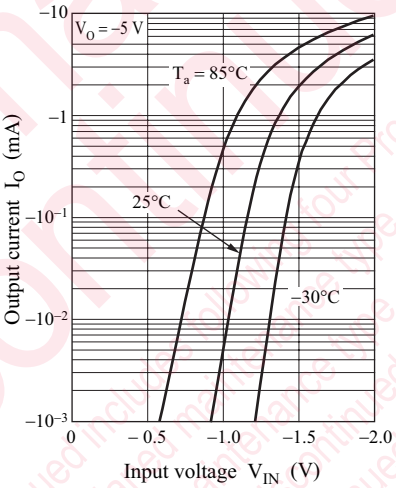
h_{FE} — I_C



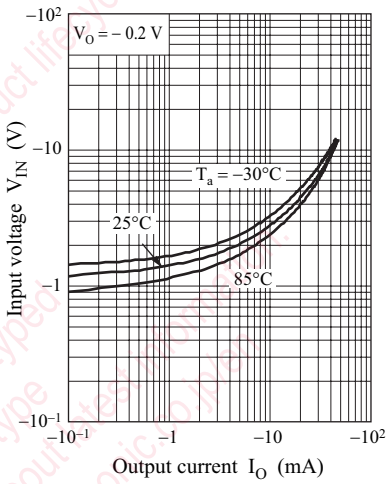
$V_{CE(sat)}$ — I_C



I_O — V_{IN}



V_{IN} — I_O



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