NEC

TFT COLOR LCD MODULE

NL160120AC27-01

54cm (21.3 Type)
UXGA

DATA SHEET

(1st edition)

All information is subject to change without notice.

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INTRODUCTION

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Anti-radioactive design is not implemented in this product.

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1. OUTLINE

1.1 DESCRIPTION

NL160120AC27-01 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL160120AC27-01 has a built-in backlight with an inverter.
The 54cm (21.3 Type) diagonal display area contains 1600 × 1200 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has wide viewing angle and multi-scan function. Therefore, this module calls Super Fine TFT.

1.2 APPLICATIONS

- Desk top PCs, Engineering work stations
- Display terminals for control systems
- Monitors

1.3 FEATURES

- Ultra wide viewing angle (with lateral electric field)
- Multi-scan function: e.g., UXGA, SXGA, XGA, SUN, MAC, SVGA, VGA, VGA-TEXT
- Color control functions (sub-contrast each R, G, B, sub-brightness each R, G, B)
- Wide color gamut (Typ.60%, at center, to NTSC)
- High luminance (200cd/m^2 Typ.) and low reflection
- Analog RGB signals
- Incorporated direct type backlight (twelve lamps, inverter)
- Replaceable backlight unit (part number: 213LHS01)
- Replaceable inverter (part number: 213PW011)
- UL1950 Third Edition (File No.E170632) and CSA-C22.2 No.950-95 (File No.E170632)
- On-Screen Display
  Application with the OSD function might conflict with patents in Europe and/or the U.S.A.
  If you apply the OSD function please do so in accordance with the patent regulations of your location.

VESA: Video Electronics Standards Association
DPMS: Display Power Management Signaling
DDC1: Display Data Channel 1
DDC2B: Display Data Channel 2B

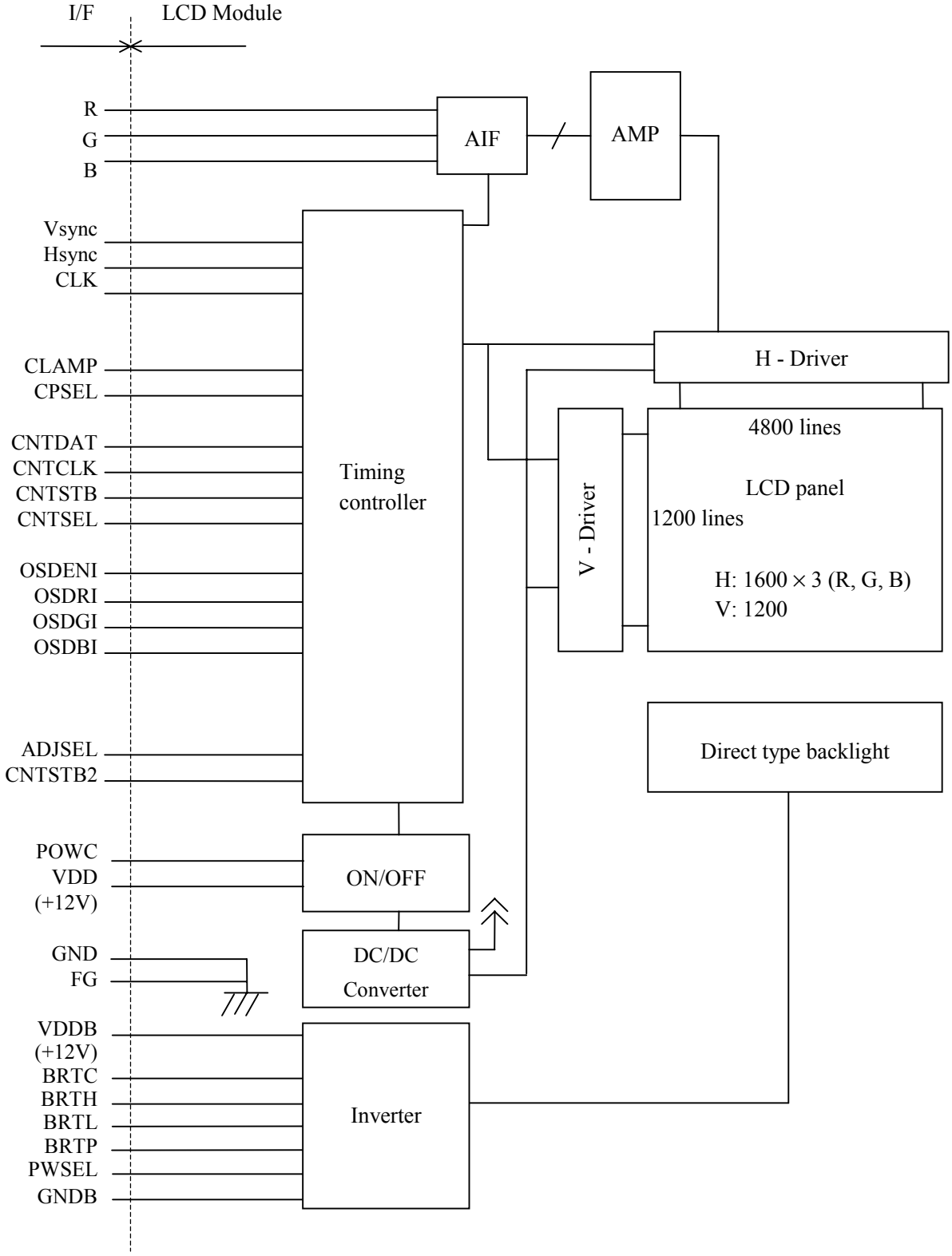
1.4 STRUCTURE AND FUNCTION

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.
RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.
Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

2. GENERAL SPECIFICATIONS

Display area	432.0 (W) × 324.0 (H) mm (typ.)
Diagonal size of display	54.0 cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display color	full-color
Pixel	1600 (H) × 1200 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.090 (W) × 0.270 (H) mm
Pixel pitch	0.270 (W) × 0.270 (H) mm
Module size	470.0 ± 1.0 (W) × 382.0 ± 1.0 (H) × 42.5 (D) mm (max.)
Weight	2,750 g (typ.)
Contrast ratio	300:1 (typ.)
Viewing angle	*At the contrast ratio 10:1* • Horizontal: Left side 85° (typ.), Right side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	• Optimum grayscale (γ=2.2): perpendicular
Polarizer pencil-hardness	3H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 60 % (typ.) [against NTSC color space]
Response time	31 ms (typ.), “black” to “white”
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK)
Power supply voltage	LCD panel signal processing board: 12V Backlight inverter: 12.0V
Backlight	Direct light type: 12 cold cathode fluorescent lamps with inverter Replaceable parts • Backlight unit: type No. 213LHS01 • Inverter: type No. 213PW011
Power consumption	*At maximum luminance and checkered flag pattern* 57 W (typ.)

3. BLOCK DIAGRAM



Note1: GND is connected to Frame (FG). Neither GND nor Frame (FG) is connected to GNDB and these grounds should be connected to system ground in customer equipment.

4. SPECIFICATIONS

4.1 GENERAL SPECIFICATIONS

Item	Content	Unit
Module size	470.0 ± 1.0 (H) × 382.0 ± 1.0 (V) × 42.5 Max. (D)	mm
Display area	432.0 (H) × 324.0 (V) [Diagonal display area: 54 cm (Type: 21.3)]	mm
Number of pixels	1600 (H) × 1200 (V)	pixel
Pixel pitch	0.270 (H) × 0.270 (V)	mm
Dot pitch	0.090 (H) × 0.270 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	-
Display colors	Full color	Color
Weight	2750 (Typ.), 2850 (Max.)	g

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta = 25°C
	VDDB	-0.3 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta = 25°C VDD = 12V
R,G, B input voltage	Vin2	-6.0 to +6.0	V	
CLK input voltage	Vin3	-7.0 to +7.0	V	
BRTL input voltage	Vin4	-0.3 to +1.5	V	
Storage temp.	Tst	-20 to +60	°C	-
Operating temp.	Top	0 to +55	°C	Note1
Relative humidity (RH) Note2	≤ 95		%	Ta ≤ 40 °C
	≤ 85		%	40 < Ta ≤ 50 °C
	≤ 70		%	50 < Ta ≤ 55 °C
Absolute humidity Note2	≤ 73 Note3		g/m^3	Ta > 55 °C

Note1: Measured at the module surface (including self-heat)

Note2: No condensation

Note3: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving, Backlight

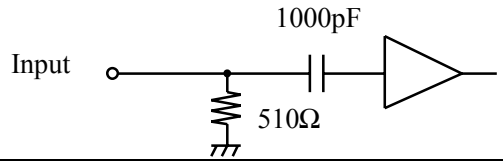
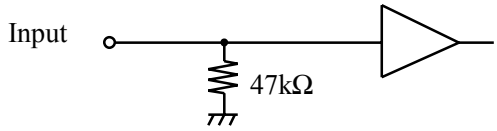
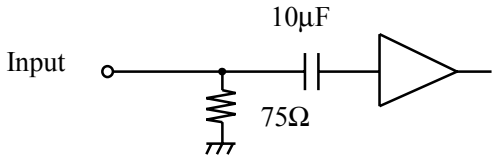
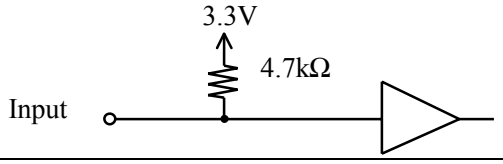
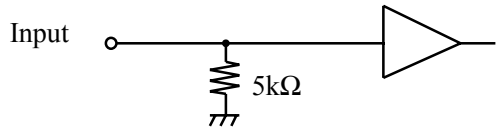
(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for LCD driving
	VDDB	10.8	12.0	13.2	V	for backlight
Logic input " L " voltage	ViL1	0	-	0.8	V	-
Logic input " H " voltage	ViH1	2.0	-	5.25	V	
CLK input voltage	ViCLK	0.6	-	1.0	Vp-p	for CLK
CLK DC input voltage	ViDCCLK	-4.5	-	+4.5	V	
Logic input " L " current 1	IiL1	-10	-	-	µA	for Hsync, Vsync
Logic input " H " current 1	IiH1	-	-	160	µA	
Logic input " L " current 2	IiL2	-900	-	-	µA	for POWC, CNTSEL, CPSEL, ADJSEL
Logic input " H " current 2	IiH2	-	-	10	µA	
Logic input " L " current 3	IiL3	-10	-	-	µA	for CNTDAT, CNTSTB, CNTCLK, CNTSTB2
Logic input " H " current 3	IiH3	-	-	150	µA	
Logic input " L " current 4	IiL4	-10	-	-	µA	for CLAMP, OSDENI, OSDRI, OSDGI, OSDBI
Logic input " H " current 4	IiH4	-	-	1440	µA	
Logic input " L " current 5	IiL5	-1.6	-	-	mA	for BRTP
Logic input " H " current 5	IiH5	-	-	3.5	mA	
Logic input " L " current 6	IiL6	-610	-	-	µA	for BRTC, PWSEL
Logic input " H " current 6	IiH6	-	-	440	µA	
Supply current	IDD	-	1200 Note1	1400 Note2	mA	for LCD driving VDD = 12.0V
	IDDB	-	3550 Note1	4000 Note2	mA	for backlight VDDB = 12.0V (Max. luminance)

Note1: Checker flag pattern

Note2: Theoretical maximum current pattern

(2) Input equivalent circuit

Signals	Equivalent circuit
CLK	
Hsync, Vsync, CNTDAT, CNTCLK, CNTSTB, CLAMP, CNTSTB2	
R, G, B	
POWC, CNTSEL, CPSEL, ADJSEL	
OSDRI, OSDGI, OSDBI, OSDENI	

(3) Video signal (R, G, B) input

(Ta = 25°C)

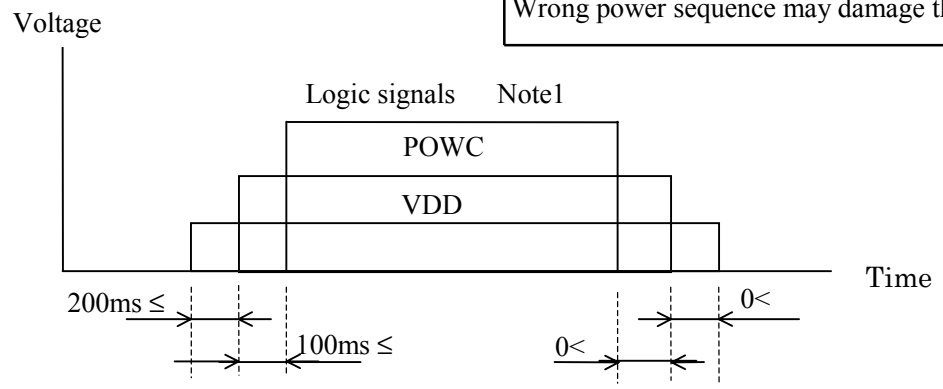
Item	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	0.7 (white)	Note1	Vp-p	Need to adjust contrast if input more 0.7Vp-p
DC input level (black)	-3.5	-	+3.5	V	-

Note1: Total value of video signal amplitude and sync amplitude are 1.4Vp-p max.

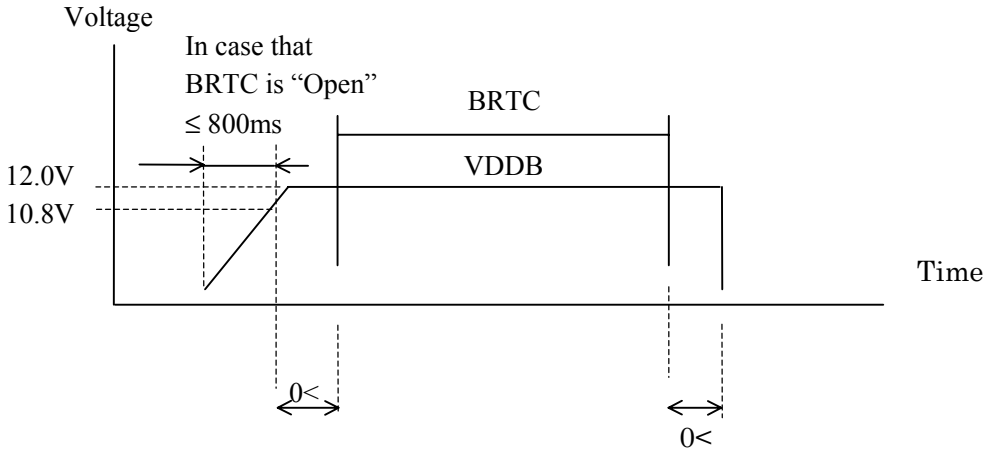
Remark: If input signals have noise, the display may include noise. And in case that frequency is bad characteristics, the display becomes blurry indication.

4.4 POWER SUPPLY SEQUENCE

CAUTION
Wrong power sequence may damage the module.



Note1: Synchronous signals, Control signals, CLK



(1) Logic signals (synchronous signals and control signals) must be "0" voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, and Vsync is not input more than 90 ms typically. As the display data are unstable in this period, the display maybe disordered. But the backlight works correctly even this period. So the backlight should be controlled by BRTC signal.

(3) The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.

(5) Analog RGB inputs are independent from this power supply sequence.

(6) The protection circuit makes the backlight turns off, when BRTP signal “L” input more than 50 ms.

(7) Do not input ACA signal ”H” and/or PWSEL signal ”H”, if VDD is 0V or BRTC signal is “L”.

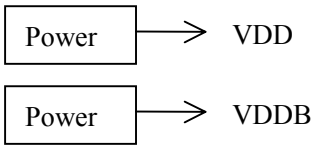
(8) Ripple of supply voltage

	VDD (for logic and LCD driver)	VDDB (for backligth)
Acceptable range	≤ 100 m Vp-p	≤ 200 m Vp-p

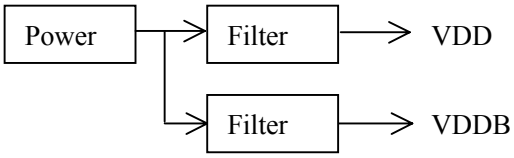
Note 1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

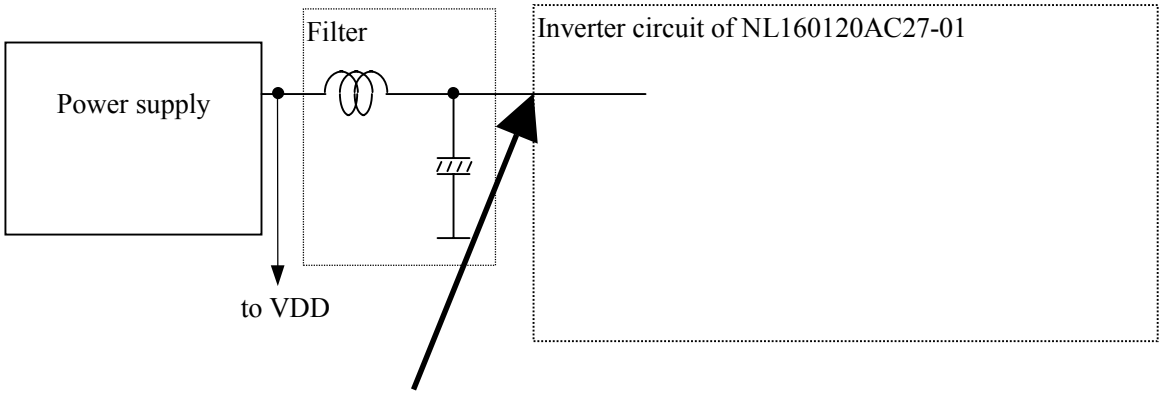
a) Separate the power supplies

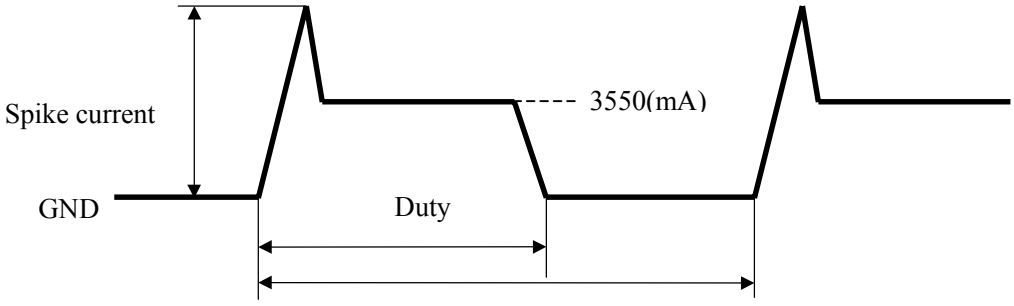


b) Put the filters



(9) Inverter current wave





262 to 290Hz, 276Hz (typ., frequency of luminance control)

Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 262-290Hz, 276Hz (Typ.)

Note1: The power supply lines (VDDB and GNDB) have large ripple voltage while dimming. There is the possibility that the ripple voltage produce an acoustic noise and signal wave noise in a system circuit (e.g. audio circuit).
If the noise occurred in a system circuit please assembles an aluminum electrolytic capacitor (5000 to 6000μF) between the power source lines (VDDB and GNDB), and the aluminum electrolytic capacitor will be able to reduce the noise.

Note2: Please refer to 4.6 PIN FUNCTIONS Note2 "luminance control by voltage and a variable resister."

(10) Fuse

Fusing line	Fuse		Rating	Fusing current Note1
	Type	Supplier		
VDD	CCF1NTE4	KOA Corporation	4.0 A 60 V	8.0 A
VDDB	R451007	Littel Fuse Inc.	7.0 A 125 V	14.0 A

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

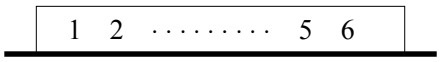
4.5 INTERFACE PIN CONNECTIONS

(1) CN1 socket

Part No.: MRF03-6R-SMT
Adaptable plug: MRF03-6PR-SMT (For board to board type)
MRF03-6P-1.27 (For cable type)
Supplier: HIROSE ELECTRIC Co., Ltd.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6	CLK

Figure from socket view

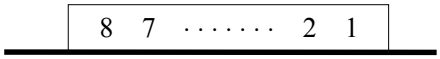


(2) CN2 socket

Part No.: IL-Z-8PL-SMTY
Adaptable plug: IL-Z-8S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	5	GND
2	VDD	6	GND
3	VDD	7	GND
4	VDD	8	GND

Figure from socket view

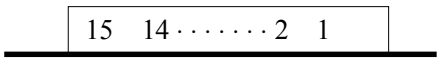


(3) CN3 socket

Part No.: IL-Z-15PL-SMTY
Adaptable plug: IL-Z-15S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	N.C.	9	GND
2	N.C.	10	CNTCLK
3	GND	11	CPSEL
4	GND	12	CLAMP
5	POWC	13	GND
6	CNTSEL	14	N.C.
7	CNTDAT	15	GND
8	CNTSTB		

Figure from socket view



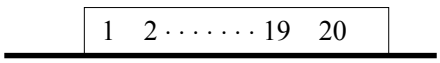
Note1: N.C. (No connection) must be open.

(4) CN4 socket

Part No.: DF14A-20P-1.25H
Adaptable plug: DF14-20S-1.25C
Supplier: HIROSE ELECTRIC Co., Ltd.

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	ADJSEL
2	OSDENI	12	N.C.
3	GND	13	CNTSTB2
4	OSDBI	14	GND
5	GND	15	N.C.
6	OSDGI	16	GND
7	GND	17	N.C.
8	OSDRI	18	N.C.
9	GND	19	N.C.
10	N.C.	20	N.C.

Figure from socket view



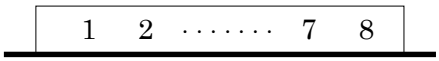
Note1: N.C. (No connection) must be open.

(5) CN201 socket

Part No.: DF3-8P-2H
Adaptable plug: DF3-8S-2C
Supplier: HIROSE ELECTRIC Co., Ltd.

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8	VDDB

Figure from socket view



(6) CN202 socket

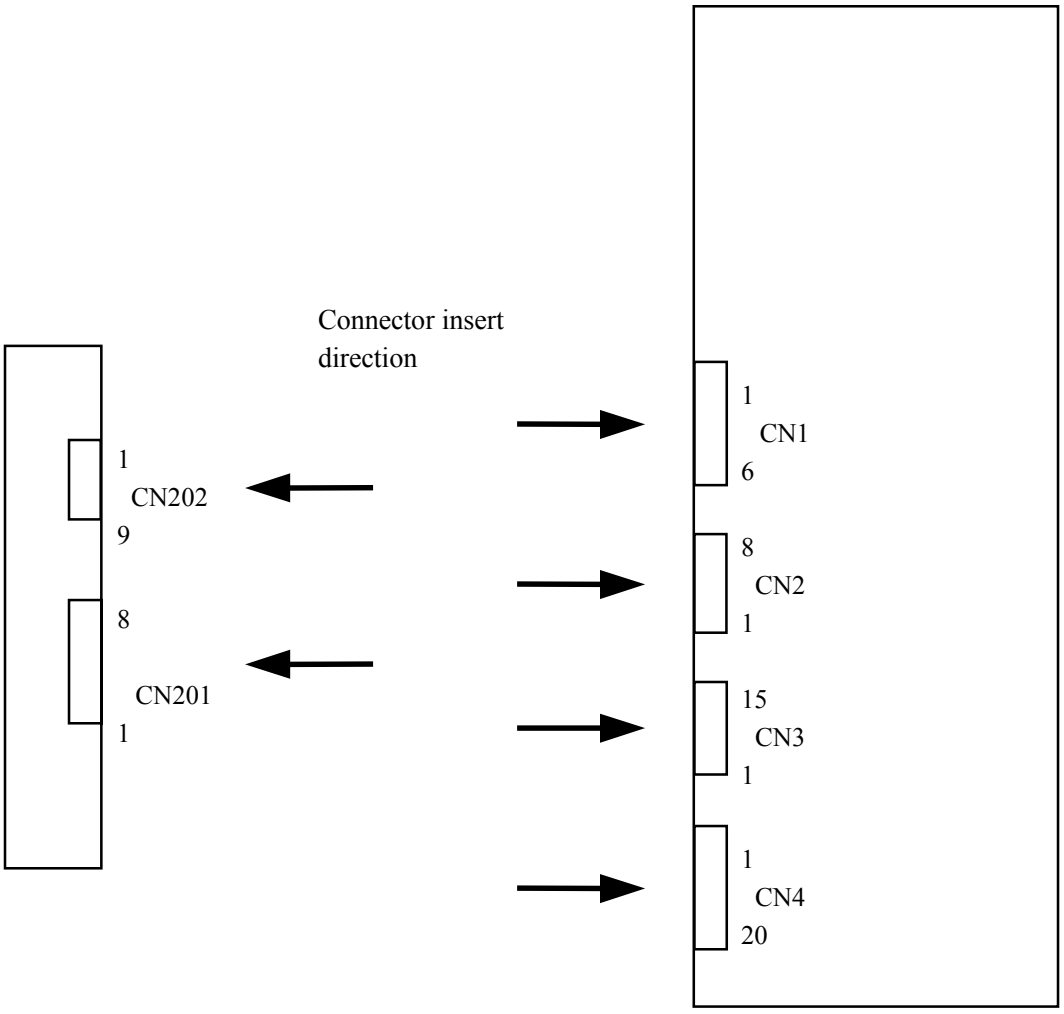
Part No.: IL-Z-9PL-SMTY
Adaptable socket: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GNDB	6	BRTL
2	GNDB	7	BRTP
3	N.C.	8	GNDB
4	BRTC	9	PWSEL
5	BRTH		

Note1: N.C. (No connection) must be open.

Figure from socket view

(7) Connector locations (Rear view)



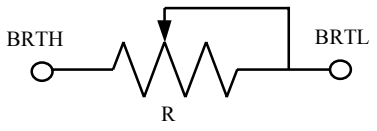
4.6 PIN FUNCTIONS

Symbol	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) Timing signal for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	-	Red video signal input (0.7Vp-p, input impedance 75Ω)
G	Input	-	Green video signal input (0.7Vp-p, input impedance 75Ω)
B	Input	-	Blue video signal input (0.7Vp-p, input impedance 75Ω)
POWC	Input	Positive	Power control signal (TTL level) “H” or “open”: Logic and LCD powers are on. “L” : Logic and LCD powers are off. (Note1)
CNTSEL	Input	-	Display control signal in case of serial communications.(TTL level) “H” or “Open”: Default “L” : External control Serial communications are set up by external control.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in 4.7. FUNCTIONS.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTCLK is mentioned in 4.7. FUNCTIONS.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTSTB is mentioned in 4.7. FUNCTIONS.
CPSEL	Input	-	Clamp function select signal (TTL level) “H” or “Open”: Default “L” : CLAMP signal is possible.(External control)
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
BRTC	Input	Positive	Backlight ON/OFF control signal(TTL level) “H” or “Open” : Backlight on “L” : Backlight off
BRTH	Input	-	Backlight luminance control-1(Note2) Variable resistor control or voltage control These controls work in BRTP = “Open”.
BRTL	Input	-	
BRTP	Input	-	Backlight luminance control-2 (TTL level) (Note2) BRTP signal control
PWSEL	Input	-	Luminance control select signal (TTL level) “H” or “Open”: Variable resistor control or voltage control “L” : BRTP signal control
ADJSEL	Input	Positive	Contrast, brightness select control signal (TTL level) “H” or “Open”: Default “L” : External control Serial communications are set up by external control.

Symbol	I/O	Logic	Description
CNTSTB2	Input	Positive	Latch pulse2 for display control data Detail of CNTSTB2 is mentioned in 4.9. OSD FUNCTIONS.
OSDRI	Input	-	OSD Red input (TTL level) Detail of OSDRI is mentioned in 4.9. OSD FUNCTIONS.
OSDGI	Input	-	OSD Green input (TTL level) Detail of OSDGI is mentioned in 4.9. OSD FUNCTIONS.
OSDBI	Input	-	OSD Blue input (TTL level) Detail of OSDBI is mentioned in 4.9. OSD FUNCTIONS.
OSDENI	Input	Positive	OSD enable signal (TTL level) Detail of OSDENI is mentioned in 4.9. OSD FUNCTIONS.
VDD	-	-	VDD (+12V ± 5%) power supply for logic and LCD driving.
VDDB	-	-	VDDB (+12V ± 10%) power supply for backlight. (Note1)
GND	-	-	Ground for logic and LCD driving (VDD) GND is connected to the FG.
GNDB	-	-	Ground for backlight power supply (VDDB) GNDB is not connected to GND.

Note1: When POWC is "L", serial communication data is clear, please set again. When POWC is “L”, logic input signal has to be all “0V”. If more than “0.3V” is inputted, the LCD module may be broken.

Note2: Luminance control

Form	PWM	Voltage	Variable resistor
How to adjust	PWSEL=“L”	PWSEL=“H” or “Open” and BRTP=”Open”	
	See 4.10. OUTSIDE CONTROL FOR LUMINANCE	BRTH should be fixed to 0V to control luminance by voltage. The range of input voltage between BRTL and GNDB is as follows. Maximum luminance (100%) : 1V Minimum luminance (30%) : 0V	The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Maximum luminance (100%): R=10kΩ Minimum luminance (30%) : R= 0Ω Mating variable resistor: 10kΩ ± 5%, B curve, 1/10W

4.7 FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Expansion mode: See table 2 and 4.8. EXPANSION FUNCTIONS
(2) Control Display position (VERTICAL): See table 3
(3) Control Display position (HORIZONTAL): See table 6
(4) Control CLK delay: See table 4
(5) Change CLK fall/rise synchronous: See table 5
(6) Sub-Contrast control:
(7) Sub-Brightness control: } See table 9, 10 and 4.8.4. COLOR CONTROL FUNCTION AND GRAPHIC IMAGE

Set up the following items to work the above functions

(A) CLK counts of horizontal period: See table 7
(B) CLK frequency range: See table 8

4.7.1 HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is "L", the above functions ((1)-(5)) are valid. (CNTSEL is "H" or "Open", default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions ((1)-(5)) are effective.

If ADJSEL is "L", the above functions ((6)-(7)) are valid. (ADJSEL is "H" or "Open", default values are valid.) After serial data are transferred, the data is latched by CNTSTB2. Once, the data is latched, the above functions ((6)-(7)) are effective.

Keep CNTSTB/2 to be "L" during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, NEC recommend that the backlight power is off using BRTC function.

Table 1. CNTDAT (Serial data) Composition

DATA	DATA name	Function	
D0	INT	Prohibit ”0”	
D1	VEX4	Expansion mode	See table 2
D2	VEX3	Expansion mode	
D3	VEX2	Expansion mode	
D4	VEX1	Expansion mode	
D5	VEX0	Expansion mode	
D6	VD7	Vertical display position (MSB)	See table 3
D7	VD6	Vertical display position	
D8	VD5	Vertical display position	
D9	VD4	Vertical display position	
D10	VD3	Vertical display position	
D11	VD2	Vertical display position	
D12	VD1	Vertical display position	
D13	VD0	Vertical display position (LSB)	
D14	DELAY6	CLK delay (MSB)	See table 4
D15	DELAY5	CLK delay	
D16	DELAY4	CLK delay	
D17	DELAY3	CLK delay	
D18	DELAY2	CLK delay	
D19	DELAY1	CLK delay	
D20	DELAY0	CLK delay (LSB)	
D21	CKS	CLK signal	See table 5
D22	HD9	Horizontal display position (MSB)	See table 6
D23	HD8	Horizontal display position	
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE11	CLK counts of horizontal period (MSB)	See table 7
D33	HSE10	CLK counts of horizontal period	
D34	HSE9	CLK counts of horizontal period	
D35	HSE8	CLK counts of horizontal period	
D36	HSE7	CLK counts of horizontal period	
D37	HSE6	CLK counts of horizontal period	
D38	HSE5	CLK counts of horizontal period	
D39	HSE4	CLK counts of horizontal period	
D40	HSE3	CLK counts of horizontal period	
D41	HSE2	CLK counts of horizontal period	
D42	HSE1	CLK counts of horizontal period	
D43	HSE0	CLK counts of horizontal period (LSB)	
D44	MOD2	CLK frequency select	See table 8
D45	MOD1	CLK frequency select	
D46	MOD0	CLK frequency select	

Table 1. CNTDAT Composition (continuation)

DATA	DATA name	Function	
AD0	DAD0	Color adjust data (LSB)	See table 9
AD1	DAD1	Color adjust data	
AD2	DAD2	Color adjust data	
AD3	DAD3	Color adjust data	
AD4	DAD4	Color adjust data	
AD5	DAD5	Color adjust data	
AD6	DAD6	Color adjust data	
AD7	DAD7	Color adjust data (MSB)	
AD8	DAA3	Color adjust select data (MSB)	See table 10
AD9	DAA2	Color adjust select data	
AD10	DAA1	Color adjust select data	
AD11	DAA0	Color adjust select data (LSB)	

Table 2. Expansion mode (VEX4 to VEX0: 5bit)

VEX4	VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	0	1	UXGA	Standard Note1
0	0	0	0	1	-	Prohibit	
0	0	0	1	0	-	Prohibit	
0	0	0	1	1	2.0	SVGA	
0	0	1	0	0	2.5	VGA	
0	0	1	0	1	-	Prohibit	
0	0	1	1	0	-	Prohibit	
0	0	1	1	1	-	Prohibit	
0	1	0	0	0	-	Prohibit	
0	1	0	0	1	-	Prohibit	
0	1	0	1	0	-	Prohibit	
0	1	0	1	1	-	Prohibit	
0	1	1	0	0	1.17	SXGA	
0	1	1	0	1	1.38	1152×864 (VESA)	See 4.8.3.
0	1	1	1	0	-	Prohibit	DISPLAY
0	1	1	1	1	1.56	XGA	IMAGES
1	0	0	0	0	3.0	VGA-TEXT	
1	0	0	0	1	-	Prohibit	
1	0	0	1	0	-	Prohibit	
1	0	0	1	1	1.33	1152×900 (SUN)	
1	0	1	0	0	-	Prohibit	
1	0	1	0	1	-	Prohibit	
1	0	1	1	0	1.92	832×624 (MAC)	
1	0	1	1	1	-	Prohibit	
1	1	0	0	0	-	Prohibit	
1	1	0	0	1	-	Prohibit	
1	1	0	1	0	-	Prohibit	
1	1	0	1	1	-	Prohibit	
1	1	1	0	0	-	Prohibit	
1	1	1	0	1	-	Prohibit	
1	1	1	1	0	-	Prohibit	
1	1	1	1	1	-	Prohibit	

Note1: Display mode is UXGA, when CNTSEL is "H" or "Open".

Table 3. Vertical display position (VD7 to VD0: 8bit)

VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] Note1
0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	1	0	0	4
0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	..	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255 Note2

Note1: The number of horizontal line between Vsync-fall and RGB data valid.

Note2: The maximum number is based on horizontal line count of the display mode.

Note3: Vertical position is fixed at 41H, when CNTCEL is "H" or "Open".

Table 4. CLK delay (DELAY6 to DELAY0: 7bit)

DELAY [6..0]	Delay [ns]	Relative value from "00H" [ns]	DELAY [6..0]	Delay [ns]	Relative value from "00H" [ns]	DELAY [6..0]	Delay [ns]	Relative value from "00H" [ns]
00H	4.22	0	30H	19.58	15.36	60H	35.00	30.78
01H	4.47	0.25	31H	19.88	15.66	61H	35.29	31.07
02H	4.85	0.63	32H	20.26	16.04	62H	35.67	31.45
03H	5.14	0.92	33H	20.55	16.33	63H	35.97	31.75
04H	5.43	1.21	34H	20.85	16.63	64H	36.26	32.04
05H	5.73	1.51	35H	21.14	16.92	65H	36.55	32.33
06H	6.13	1.91	36H	21.54	17.32	66H	36.95	32.73
07H	6.43	2.21	37H	21.85	17.63	67H	37.25	33.03
08H	6.69	2.47	38H	22.18	17.96	68H	37.54	33.32
09H	6.99	2.77	39H	22.49	18.27	69H	37.83	33.61
0AH	7.36	3.14	3AH	22.86	18.64	6AH	38.21	33.99
0BH	7.66	3.44	3BH	23.15	18.93	6BH	38.50	34.28
0CH	7.95	3.73	3CH	23.45	19.23	6CH	38.80	34.58
0DH	8.25	4.03	3DH	23.76	19.54	6DH	39.10	34.88
0EH	8.64	4.42	3EH	24.16	19.94	6EH	39.49	35.27
0FH	8.95	4.73	3FH	24.46	20.24	6FH	39.79	35.57
10H	9.29	5.07	40H	24.70	20.48	70H	40.17	35.95
11H	9.60	5.38	41H	25.00	20.78	71H	40.49	36.27
12H	9.98	5.76	42H	25.40	21.18	72H	40.87	36.65
13H	10.27	6.05	43H	25.70	21.48	73H	41.17	36.95
14H	10.57	6.35	44H	26.00	21.78	74H	41.47	37.25
15H	10.87	6.65	45H	26.29	22.07	75H	41.77	37.55
16H	11.26	7.04	46H	26.69	22.47	76H	42.17	37.95
17H	11.58	7.36	47H	26.98	22.76	77H	42.47	38.25
18H	11.87	7.65	48H	27.27	23.05	78H	42.74	38.52
19H	12.16	7.94	49H	27.56	23.34	79H	43.06	38.84
1AH	12.54	8.32	4AH	27.94	23.72	7AH	43.43	39.21
1BH	12.85	8.63	4BH	28.24	24.02	7BH	43.74	39.52
1CH	13.14	8.92	4CH	28.53	24.31	7CH	44.05	39.83
1DH	13.41	9.19	4DH	28.83	24.61	7DH	44.36	40.14
1EH	13.81	9.59	4EH	29.23	25.01	7EH	44.76	40.54
1FH	14.13	9.91	4FH	29.54	25.32	7FH	45.01	40.79
20H	14.41	10.19	50H	29.93	25.71			
21H	14.71	10.49	51H	30.23	26.01			
22H	15.08	10.86	52H	30.61	26.39			
23H	15.39	11.17	53H	30.91	26.69			
24H	15.68	11.46	54H	31.20	26.98			
25H	15.98	11.76	55H	31.50	27.28			
26H	16.37	12.15	56H	31.90	27.68			
27H	16.68	12.46	57H	32.20	27.98			
28H	16.97	12.75	58H	32.44	28.22			
29H	17.27	13.05	59H	32.75	28.53			
2AH	17.65	13.43	5AH	33.13	28.91			
2BH	17.95	13.73	5BH	33.42	29.20			
2CH	18.24	14.02	5CH	33.71	29.49			
2DH	18.53	14.31	5DH	34.01	29.79			
2EH	18.93	14.71	5EH	34.41	30.19			
2FH	19.23	15.01	5FH	34.73	30.51			

Note1: DELAY [6..0] is fixed at 00H, when CNTSEL is "H" or "Open".

Note2: This delay value is typical value at Ta=25°C. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/°C.

Calculated example:

In case that delay time is 20ns at Ta=25°C.

(a) In case of Ta rising to 50°C

Increase of delay time → (50°C - 25°C) × 0.002 × 20ns = +1ns

So, the total delay time is 21 ns at Ta=50°C.

(b) In case of Ta falling to 0°C

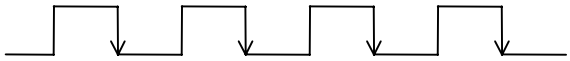
Decrease of delay time → (0°C - 25°C) × 0.002 × 20ns = -1ns

So, the total delay time is 19 ns at Ta=0°C.

② Variation of CLK delay time against each LCD module. (only reference)

-10.5% to +14.4%

Table 5. CLK reverse signal

CKS	Function
0	DATA is sampled on rising edge of CLK. 
1	DATA is sampled on falling edge of CLK. 

Note1: CKS is set "0", when CNTSEL is "H" or "open".

Table 6. Horizontal display position (HD9 to HD0: 10bit)

HD9	HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal positions [CLK] Note1
0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	1	Prohibit
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
0	0	0	0	1	1	1	1	1	1	Prohibit
0	0	0	1	0	0	0	0	0	0	64
0	0	0	1	0	0	0	0	0	1	65
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	0	1	1021
1	1	1	1	1	1	1	1	1	0	1022
1	1	1	1	1	1	1	1	1	1	1023

Note1: The number of CLK between Hsync-fall and RGB data valid.

Note2: Horizontal position is set at 496 CLK, when CNTSEL is "H" or "Open".

Table 7. CLK counts of horizontal period (HSE11 to HSE0: 12bit)

HSE 11	HSE 10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count Note1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

Note1: The number of CLK between Hsync signals.

Note2: CLK number is set 2160 CLK, when CNTSEL is "H" or "Open".

Note3: If setting value is different from actual input signal, it may cause to malfunction.

Table 8. CLK frequency select (MOD2 to MOD0: 3bit)

MOD2	MOD1	MOD0	CLK frequency [MHz]
0	0	0	Prohibit
0	0	1	Prohibit
0	1	0	140 ≤ CLK < 170
0	1	1	110 ≤ CLK < 140
1	0	0	80 ≤ CLK < 110
1	0	1	70 ≤ CLK < 80
1	1	0	60 ≤ CLK < 70
1	1	1	50 ≤ CLK < 60

Note1: Set complying with input CLK frequency.

Note2: CLK frequency is set 140 ≤ CLK < 170 MHz, when CNTSEL is "H" or "Open".

Table 9. Color control data (DAD7 to DAD0: 8bit)

DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0	Adjusting value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	..	.	.	.	.	.
0	1	1	1	1	1	1	1	127
1	0	0	0	0	0	0	0	128
1	0	0	0	0	0	0	1	129
.	.	.	.	.	.	.	.	.
.	.	.	..	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Note1: Adjust value for selecting function above table 10.

Note2: Different D/A-range depends on function selected.

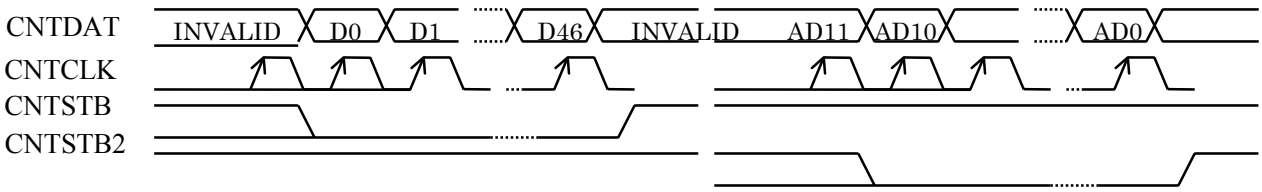
Note3: See more detail 4.8.4. COLOR CONTROL FUNCTIONS AND GRAPHIC IMAGE.

Table 10. Color adjust select data (DAA3 to DAA0: 4bit)

DAA3	DAA2	DAA1	DAA0	Functions
0	0	0	0	Prohibit
0	0	0	1	Prohibit
0	0	1	0	Prohibit
0	0	1	1	Prohibit
0	1	0	0	Sub-contrast R
0	1	0	1	Sub-contrast G
0	1	1	0	Sub-contrast B
0	1	1	1	Sub-brightness R
1	0	0	0	Sub-brightness G
1	0	0	1	Sub-brightness B
1	0	1	0	Prohibit
1	0	1	1	Prohibit
1	1	0	0	Prohibit
1	1	0	1	Prohibit
1	1	1	0	Prohibit
1	1	1	1	Prohibit

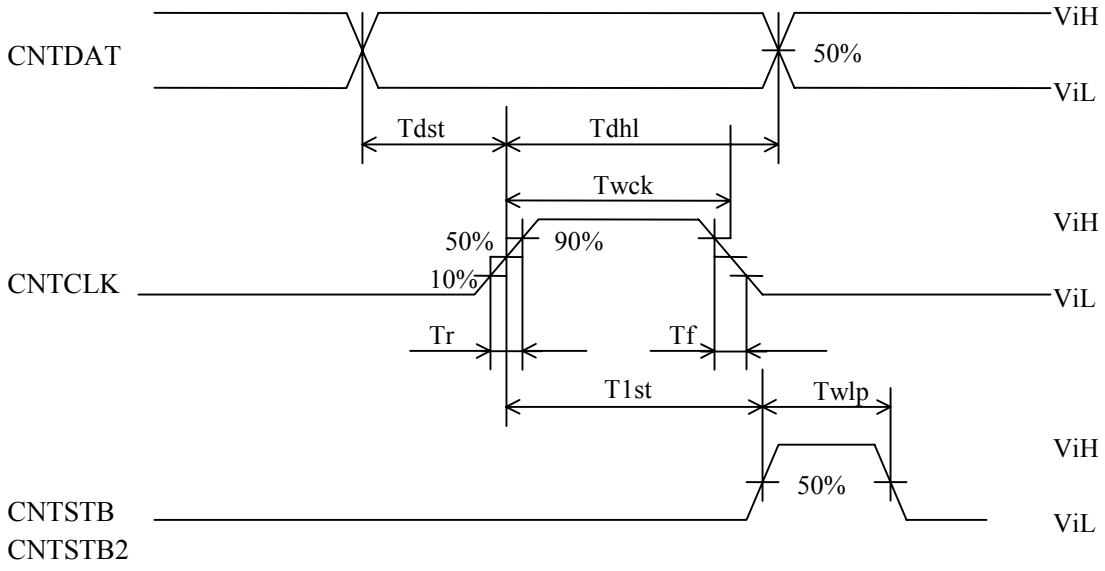
Note1: See more detail 4.8.4. COLOR CONTROL FUNCTIONS AND GRAPH IMAGE.

4.7.2 SERIAL COMMUNICATION TIMINGS



Parameter	Symbol	Min.	Max.	Unit	Remarks
CLK pulse-width	Twck	50	-	ns	CNTCLK
CLK frequency	Fclk	-	5	MHz	
DATA set-up-time	Tdst	50	-	ns	CNTDAT
DATA hold-time	Tdhl	50	-	ns	
Latch pulse-width	Twlp	50	-	ns	CNTSTB, CNTSTB2
Latch set-up-time	T1st	50	-	ns	
Rise / fall time	Tr, Tf	-	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM



4.8 EXPANSION FUNCTIONS

4.8.1 HOW TO USE EXPANSION MODES

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 2.5 times vertically and horizontally, VGA screen image can be displayed fully on the screen of UXGA resolution.

This LCD module has the function that expands vertical direction as shown in 4.7.1 Table 1. And expanding horizontal direction is possible by setting input CLK frequency equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

Please adopt this mode after evaluating display quality, because the appearance in expansion mode is happened to be relatively bad in some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal Note1
UXGA	1600 × 1200	1.0	1.0
SXGA	1280 × 1024	1.17	1.25
XGA	1152 × 864	1.38	1.38
	1024 × 768	1.56	1.56
SUN	1152 × 900	1.33	1.38
MAC	832 × 624	1.92	1.92
SVGA	800 × 600	2.0	2.0
VGA	640 × 480	2.5	2.5
VGA text	720 × 400	3.0	2.2

Note1: The horizontal magnification multiples the input clock (CLK).

Input CLK = system CLK × horizontal magnification

Example: In case of UXGA and VGA, CLK frequency can be decided as follows.

UXGA: System CLK (162.0MHz) × 1.0=162.0MHz

VGA: System CLK (25.175MHz) × 2.5= 62.94MHz

4.8.2 SETTING SERIAL DATA FOR EXPANSION

Input signal								Module serial-data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count Number [CLK]	DSP [CLK]	Count Number [H]	DSP [H]	Calculation formula		
				(A)	(B)	-	(C)	(A) × Ver. magni	(B) × Hor. magni	=(C)
UXGA (1600 × 1200)	162.0	75.000	60.000	2160	496	1250	49	(A) × 1	(B) × 1	
SXGA (1280 × 1024)	108.0*	63.981	60.02	1688	360	1066	41	(A) × 1.25	(B) × 1.25	
	117.0*	71.691	67.189	1632	336	1067	41			
	125.0*	75.120	71.204	1664	352	1055	28			
	130.076*	76.968	72.000	1690	378	1069	42			
	135.0*	78.125	72.005	1728	384	1085	58			
	135.0*	79.976	75.025	1688	392	1066	41			
SUN (1152 × 900)	94.500*	61.845	66.003	1528	336	937	35	(A) × 1.38	(B) × 1.38	
XGA (1024 × 768)	65*	48.363	60.004	1344	296	806	35	(A) × 1.56	(B) × 1.56	
	75*	56.476	70.069	1328	280	806	35			
	78.75*	60.023	75.029	1312	272	800	31			
XGA (1152 × 864)	94.5*	64.198	70.239	1472	288	914	49	(A) × 1.38	(B) × 1.38	
	108.0*	67.500	75.000	1600	384	900	35			
MAC (832 × 624)	57.283*	49.725	74.5	1152	288	667	42	(A) × 1.92	(B) × 1.92	
SVGA (800 × 600)	36*	35.156	56.25	1024	200	625	24	(A) × 2.0	(B) × 2.0	
	40*	37.879	60.317	1056	216	628	27			
	50*	48.077	72.188	1040	184	666	29			
	49.5*	46.875	75	1056	240	666	24			
VGA (640 × 480)	25.175*	31.469	59.94	800	144	525	35	(A) × 2.5	(B) × 2.5	
	31.5*	37.861	72.809	832	168	520	31			
	31.5*	37.5	75	840	184	500	19			
	30.24*	35.0	66.667	864	160	525	42			
VGA text (720 × 400)	28.322*	31.469	70.087	900	153	449	37	(A) × 2.22	(B) × 2.22	

*: Standard timings (Please set them up properly for correct expansion.)

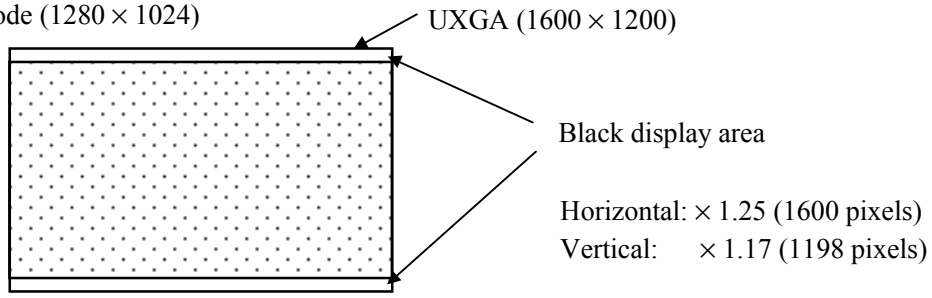
Note1: DSP = Display Start Period. DSP is total of "pulse-width" and "back-porch".

Note2: HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.

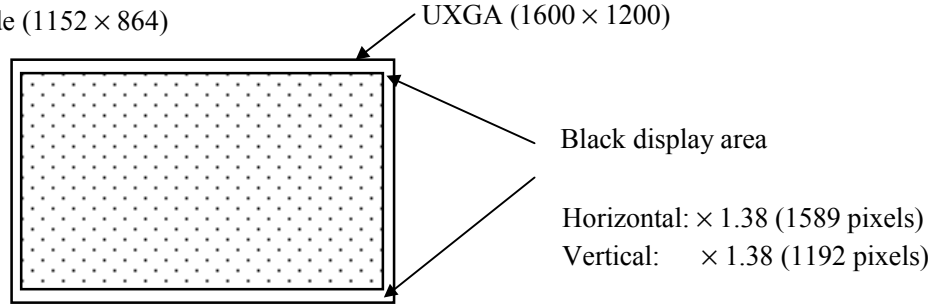
Note3: The pulse-width of Hsync, Vsync and Back-porch are the same as UXGA-mode (Standard-mode).

4.8.3 DISPLAY IMAGES

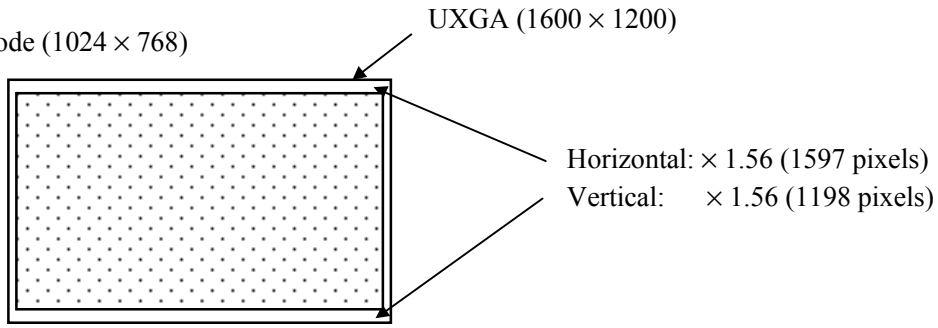
1) SXGA mode (1280 × 1024)



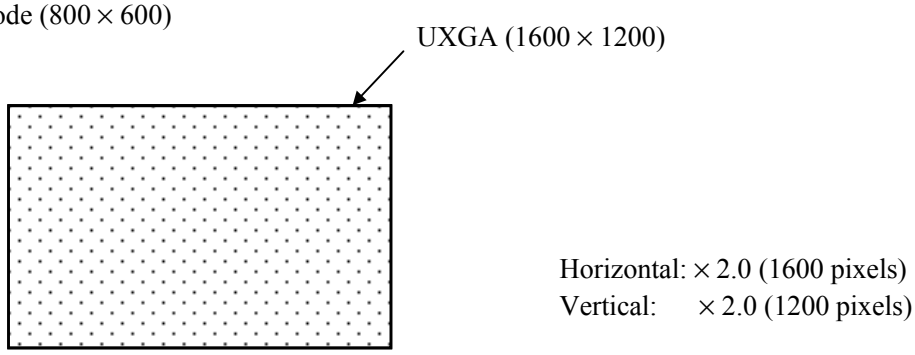
2) XGA mode (1152 × 864)



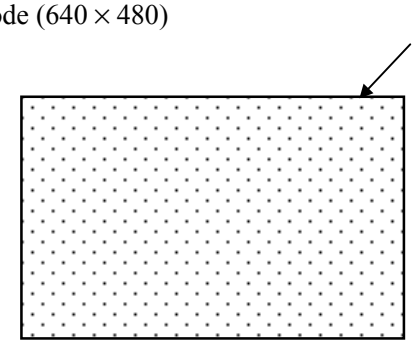
XGA mode (1024 × 768)



3) SVGA mode (800 × 600)

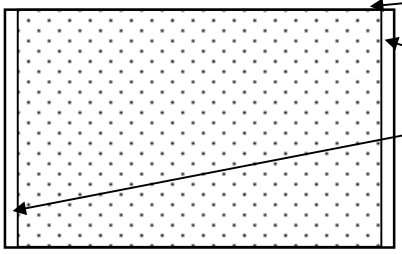


4) VGA mode (640 × 480)



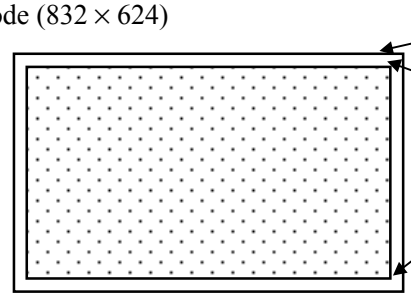
Horizontal: × 2.5 (1600 pixels)
Vertical: × 2.5 (1200 pixels)

5) VGA text mode (720 × 400)



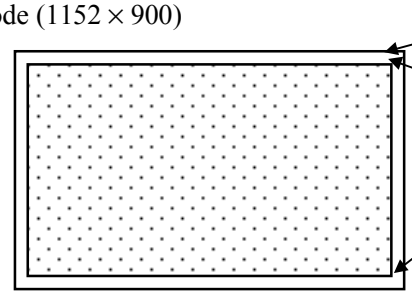
Horizontal: × 2.2 (1584 pixels)
Vertical: × 3.0 (1200 pixels)

6) MAC mode (832 × 624)



Horizontal: × 1.92 (1597 pixels)
Vertical: × 1.92 (1198 pixels)

7) SUN mode (1152 × 900)



Horizontal: × 1.38 (1589 pixels)
Vertical: × 1.33 (1197 pixels)

4.8.4 COLOR CONTROL FUNCTIONS AND GRAPHIC IMAGE

This LCD module can adjust the following functions by serial data input (Table 1)

(1) Sub-Contrast each R, G, B: } See 4.7.1 HOW TO USE THE ABOVE FUNCTIONS

(2) Sub-Brightness each R, G, B: } Table 9,10

(1) Sub-contrast R, G, B

Sub-contrast can adjust each R/G/B with controlling the amplitude of input video signal.

Default value: 128, Valid range: 78 to 198

Contrast minimum: 78

Contrast maximum: 198

ADJSEL="H" or "Open": Default value=128

(2) Sub-brightness R, G, B

Sub-brightness can adjust each R/G/B with adjusting the black level of input video signal.

Default value: 128, Valid range: 55 to 163

Brightness minimum: 163

Brightness maximum: 55

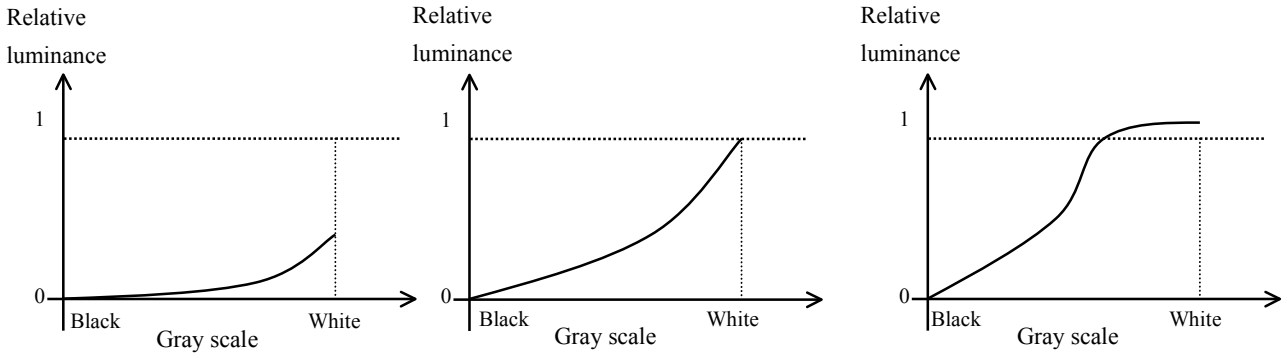
ADJSEL="H" or "Open": Default value=128

Note1: If use to go over above valid range, LCD module will be not destroy. However LCD will be inferiority. Please keep value of valid range.

Note2: Although set up the same value for each LCD, color will be caused the different. And also, will be afraid to deviate values from optical characteristics. Please adopt this functions evaluating display quality.

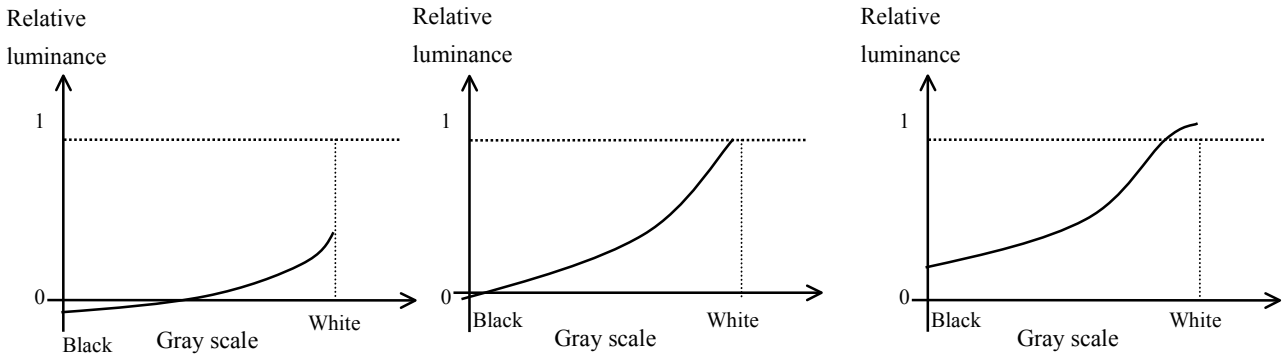
< GRAPHIC IMAGE >

· Sub contrast



Sub contrast
Min. value ⟵ DEFAULT ⟶ Max. value

· Sub brightness



Sub brightness
Min. value ⟵ DEFAULT ⟶ Max. value

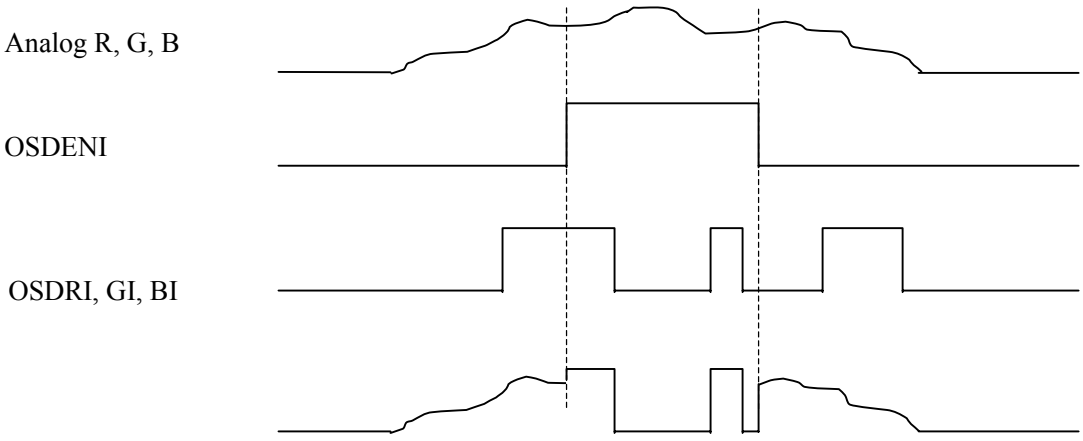
4.9 OSD FUNCTIONS

OSD (On Screen Display) is the function to display the other digital data on the input analog valid data. Possible to display 1 bit data for each R/G/B color (8 colors). OSD function is valid for the period of OSDENI.

OSDRI, OSDGI, OSDBI: digital data for OSD
OSDENI= "H": OSD signal is valid
OSDENI= "L": OSD signal is not valid

OSD is the sub-display for function-control and the display quality will not be guaranteed. Please adopt the OSD image evaluating display quality.

< OSD image >

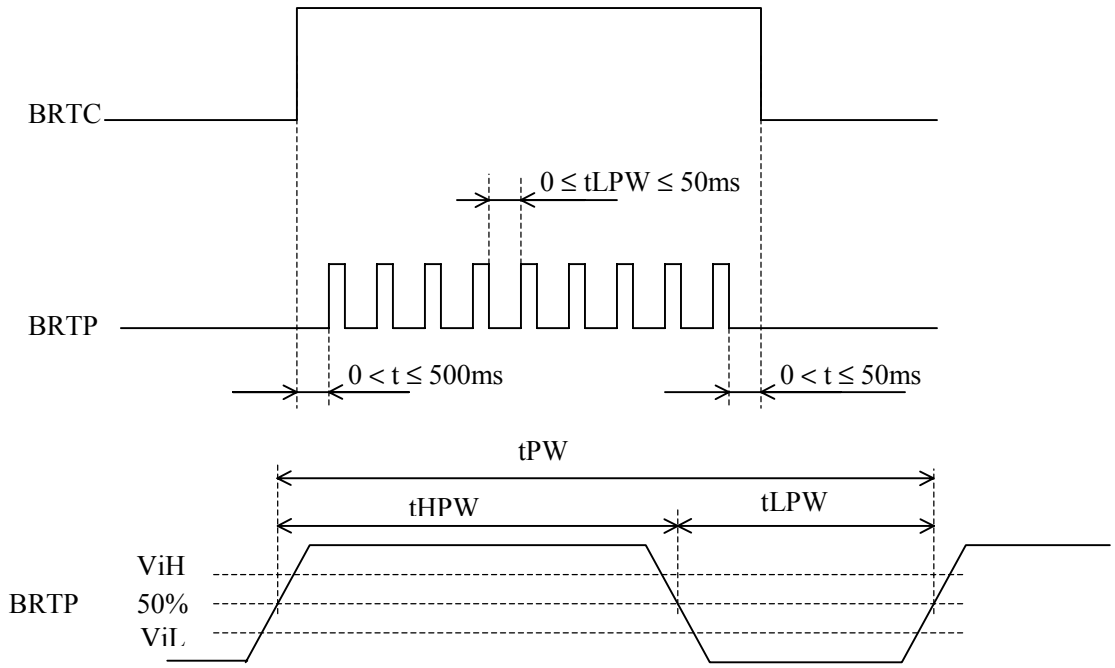


Real display image

4.10 OUTSIDE CONTROL FOR LUMINANCE

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.
Duty=100%: luminance is maximum.
Duty=40%: luminance is minimum.

Timing for BRTP



Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Frequency Note1	1/tPW	185	-	325	Hz	BRTP frequency
"L" period	tLPW	-	-	50	ms	Note2
Pulse-width	tHPW/tPW	40	-	100	%	at max. luminance (100%)
Input voltage	ViL	0	-	0.8	V	-
	ViH	2.0	-	5.0	V	-

Note1: Regarding set up for frequency, refer to the below method.
Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)
Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

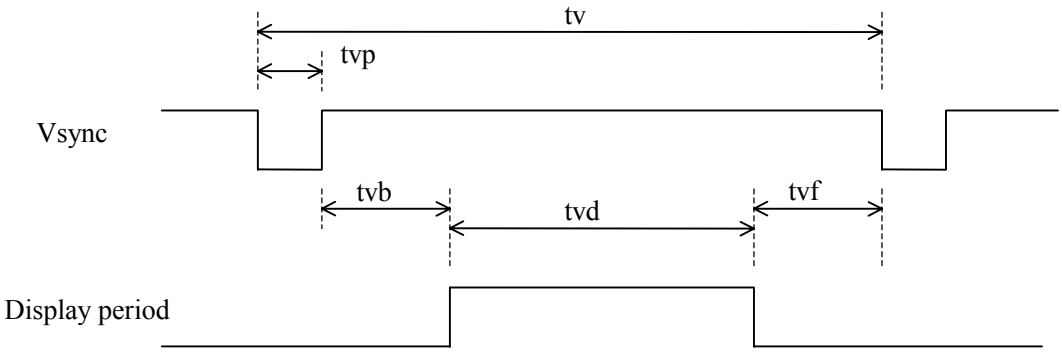
Note2: The protection circuit makes the backlight turn off, when tLPW is more than 50ms.

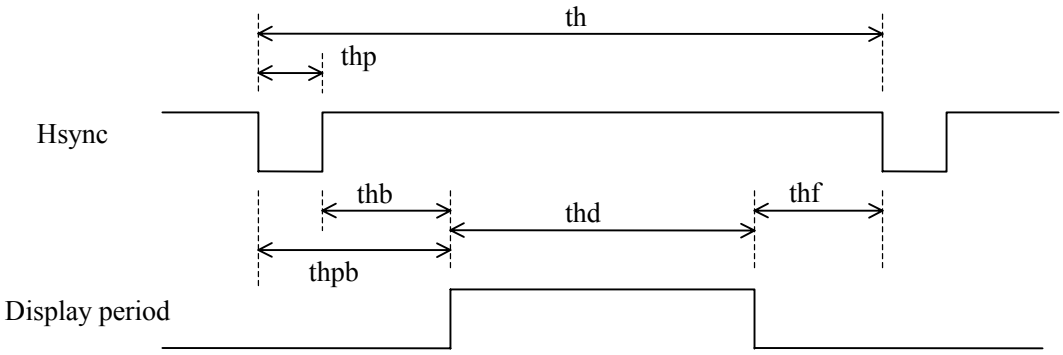
4.11 INPUT SIGNAL TIMINGS

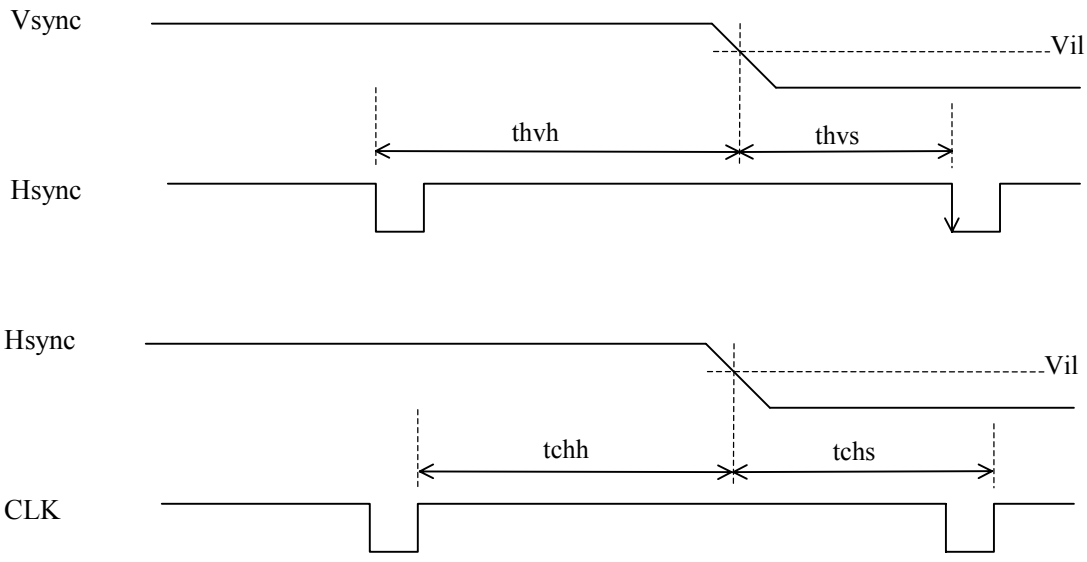
4.11.1 UXGA MODE (STANDARD)

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	- -	162.0 6.17	169.0 -	MHz ns	UXGA standard
	Rise / Fall	tcrf	-	-	0.5	ns	-
	Pulse-width	tc/tcl	0.4	0.5	0.6	-	-
	Hsync-clock timing	tchs	2.0	-	-	ns	-
		tchh	1.5	-	-	ns	-
Hsync	Period	th	12.3 -	13.333 2160	17.0 -	µs CLK	75.0kHz (Typ.)
	Display	thd	- -	9.877 1600	- -	µs CLK	-
	Front-porch	thf	- 10	0.395 64	- -	µs CLK	-
	Pulse-width	thp	- 16	1.185 192	- -	µs CLK	-
	Back-porch	thb	1.0 94	1.877 304	- -	µs CLK	Note1
	Pulse-width +Back-porch	thbp	1.8	-	-	µs	-
	Vsync-Hsync timing hold/setup time	thvh	3	-	-	CLK	-
		thvs	1	-	-	CLK	-
	Rise / Fall	thrf	-	-	10	ns	-
Vsync	Period	tv	13.3 -	16.667 1250	18.5 -	ms H	60.00Hz (Typ.)
	Display	tvd	- -	16.000 1200	- -	ms H	-
	Front-porch	tvf	- 1	0.013 1	- -	ms H	-
	Pulse-width	tvp	- 2	0.040 3	- -	ms H	-
	Back-porch	tvb	- 5	0.613 46	- -	ms H	-

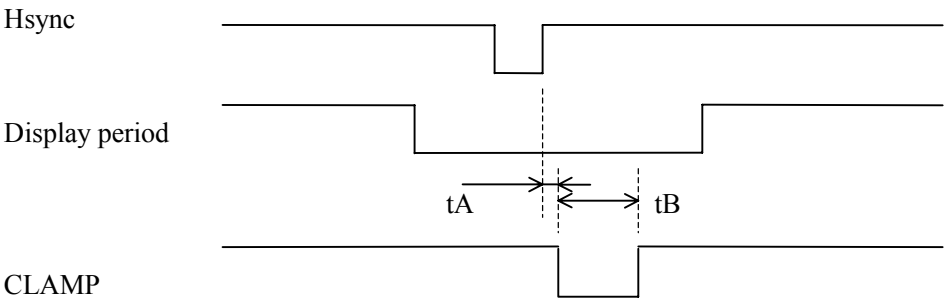
Note1: Minimum value of Back-porch (thb) must be satisfied with both 1.0µs and 94CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
Vil
thvh
thvs
Hsync
Hsync
Vil
tchh
tchs
CLK

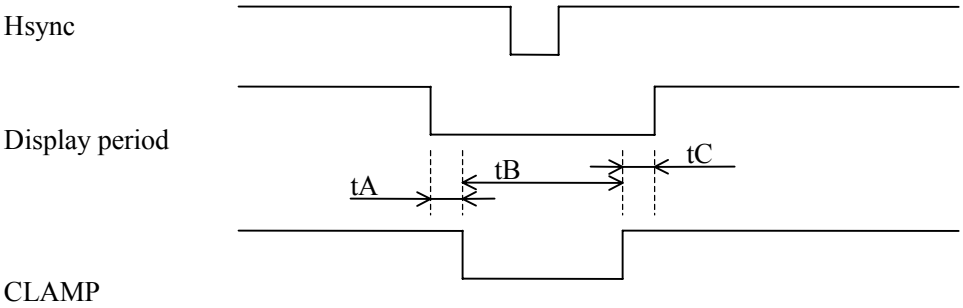
4.11.2 TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD2	MOD1	MOD2	tA [CLK]	tB [CLK]
0	0	0	2	69
0	0	1		60
0	1	0		51
0	1	1		42
1	0	0		33
1	0	1		24
1	1	0		21
1	1	1		18

Note1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

4.11.3 TIMING FOR INPUTTING CLAMP SIGNAL FROM OUTSIDE

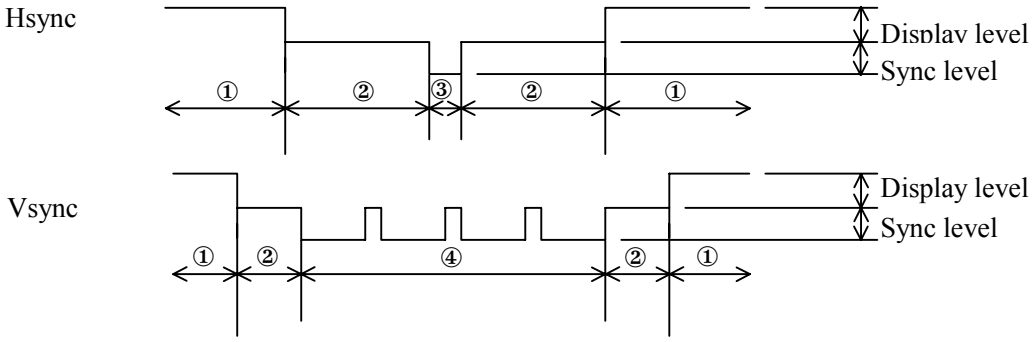


Item	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	-	-	µs	-
tB	0.3	-	-	µs	-
tC	0.2	-	-	µs	-

Note1: Exclude noises on analog R, G, B signals, because analog R, G, B signals are the black level reference during CLAMP="L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

Note2: Attention for using Sync On Green signal.
Clamp signals must be input during black level period as next page.
If Clamp signals are input during other period, the display becomes un-uniformity.

Sync on Green Input signal timings



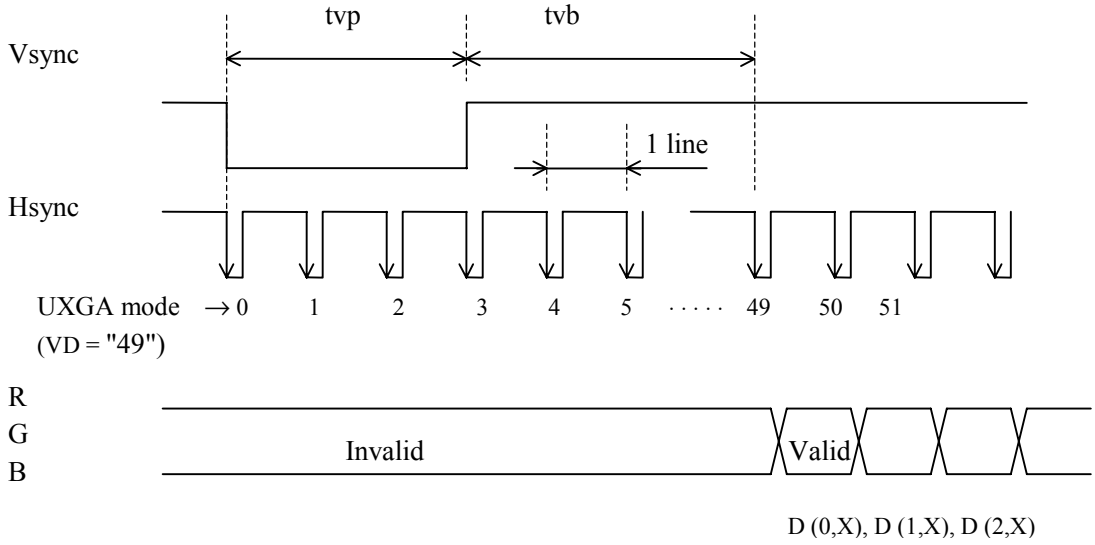
①Display period ②Black level period ③Hsync period ④Vsync period

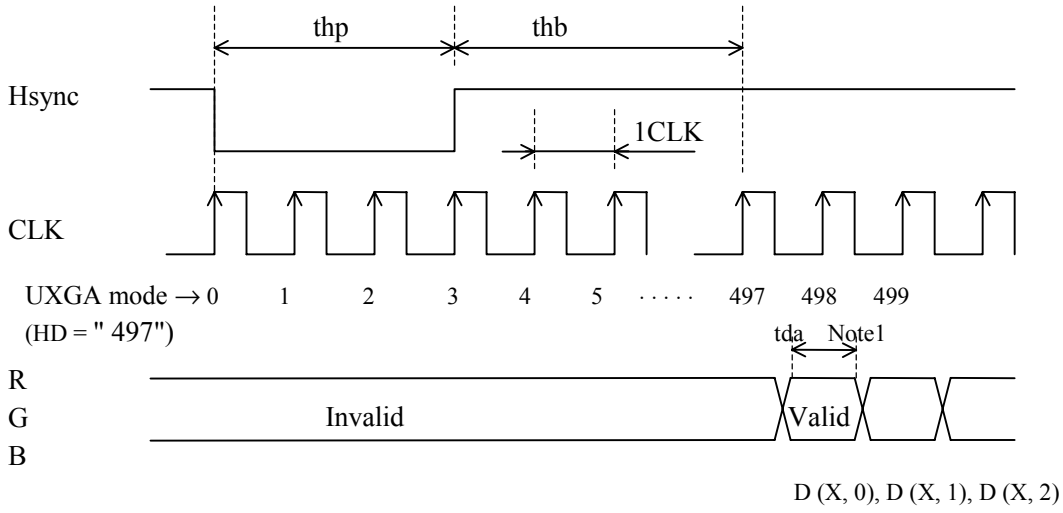
4.12 INPUT SIGNALS AND DISPLAY POSITIONS

4.12.1 UXGA STANDARD TIMINGS

Pixels

D(0,0)	D(1,0)	D(2,0)	· · · · · · · · · ·	D(1599,0)
D(0,1)	D(1,1)	D(2,1)	· · · · · · · · · ·	D(1599,1)
D(0,2)	D(1,2)	D(2,2)	· · · · · · · · · ·	D(1599,2)
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
D(0,1199)	D(1,1199)	D(2,1199)	· · · · · · · · · ·	D(1599,1199)





Note1: The “tda” should be more than 2ns

4.13 OPTICAL CHARACTERISTICS

(Ta = 25°C, VDD = 12V, VDDB = 12V, Note2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	γ=2.2 viewing angle θx ± =0°, θy ± =0°, White/Black, at center	200	300	-	-	Note1
Luminance	Lumax	White, at center	150	200	-	cd/m^2	-
Luminance uniformity	-	White	-	-	1.3	-	Note3

Reference data

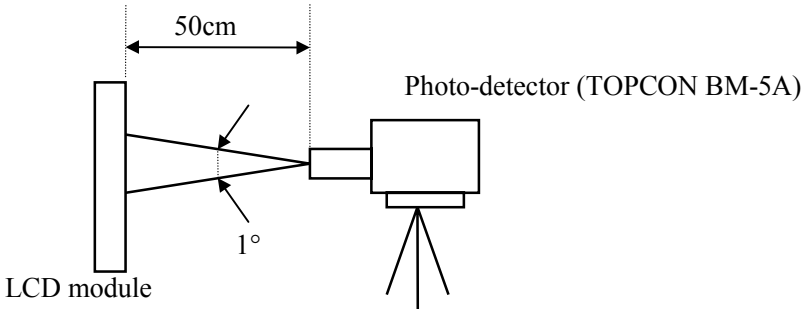
(Ta = 25°C, VDD = 12V, VDDB = 12V, Note2)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Remarks
Chromaticity Coordinates	C	θx ± =0°, θy ± =0°, at center, to NTSC		50	60	-	%	-
	W	White (x, y)		-	0.30,0.31	-	-	-
	R	Red (x, y)		-	0.61,0.34	-	-	-
	G	Green (x, y)		-	0.31,0.60	-	-	-
	B	Blue (x, y)		-	0.14,0.09	-	-	-
Viewing angle range (CR>10)	θx+	CR > 10, White/Black θy+=0°, θy-=0°		70	85	-	deg.	Note4
	θx-			70	85	-	deg.	
	θy+	CR > 10, White/Black θx+=0°, θx-=0°		70	85	-	deg.	
	θy-			70	85	-	deg.	
Viewing angle range (CR>5)	θx+	CR > 5, White/Black θy+=0°, θy-=0°		-	85	-	deg.	
	θx-			-	85	-	deg.	
	θy+	CR > 5, White/Black θx+=0°, θx-=0°		-	85	-	deg.	
	θy-			-	85	-	deg.	
Response time (Module surface temperature =32°C)	Ton	Black to White	0%→90%	-	36	50	ms	Note5
			10%→90%	-	31	45		
	Toff	White to Black	100%→10%	-	26	45		
			90%→10%	-	23	40		
Luminance control range	-	Maximum luminance (100%)		-	30 to 100	-	%	-

Note1: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

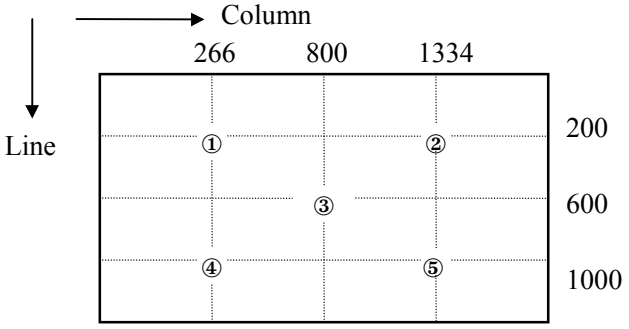
Note2: Optical characteristics are measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.
Display mode: VESA UXGA-60Hz
RGB input voltage: 0.7Vp-p
Contrast: Default



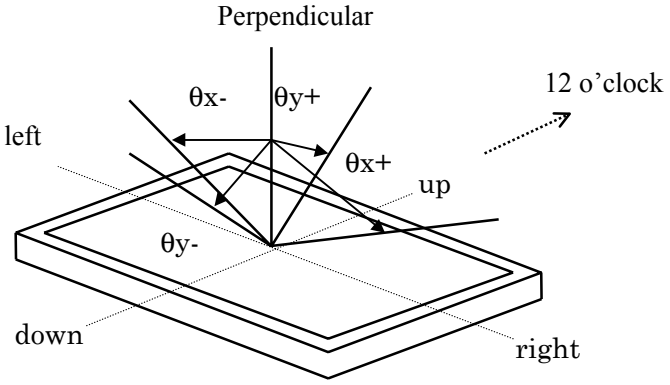
Note3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

The luminance is measured at near the five points shown below.

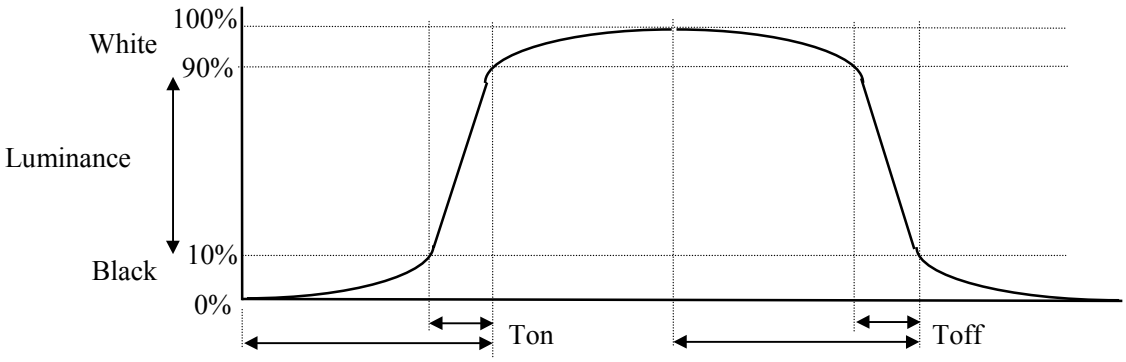


Note4: Definitions of viewing angle are as follows.



Note5: Definitions of response time is as follows.

Photo-detector out put signal is measured when the luminance changes "black" to "white".



5. RELIABILITY TEST

Test item	Test condition	Judgment
High temperature/humidity operation	60 ± 2ºC, RH= 60% 240 hours, Display data is black.	Note1
Heat cycle (operation)	① 0ºC ± 3ºC · · · 1 hour 55ºC ± 3ºC · · · 1 hour ② 50 cycles, 4 hours/cycle ③ Display data is black.	Note1
Thermal shock (non-operation)	① -20ºC ± 3ºC · · · 30 minutes 60ºC ± 3ºC · · · 30 minutes ② 100 cycles Temperature transition time is within 5 minutes.	Note1
Vibration (non-operation)	① 5-100Hz, 11.76m/s^2 1 minute/cycle, X, Y, Z direction ② 10 times each direction	Note1, 2
Mechanical shock (non-operation)	① 294m/s^2, 11ms X, Y, Z direction ② 3 times each direction	Note1, 2
ESD (operation)	150pF, 150Ω, ±10kV 9 places on a panel 10 times each place at one-second intervals	Note1,3
Dust (operation)	Sample dust: No. 15 (by JIS-Z8901) Hourly 15 seconds stir, 8 times repeat	Note1

Note1: Display function is checked by the same condition as LCD module out-going inspection.

Note2: Physical damage

Note3: Discharge points are shown in the figure.

6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS", after understanding this contents!**

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

∗ Do not touch the lamp cables while turn on. Customer will be in danger of an electric shock.

∗ Pay attention to burn injury for the working backlight and IC! It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight! Danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.39N·m. Higher torque values might result in distortion of the bezel.
⑥ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
⑦ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.
⑧ Do not give the stress too much on interface connectors. The module may become function deficiency by a contact defective and damages. Pay attention to handling at the time of matching connector connection and in the connection condition.

6.3.2 Environment

① Do not operate in dewdrop atmosphere and corrosive gases.
② Do not operate or store in high temperature or high humidity atmosphere. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

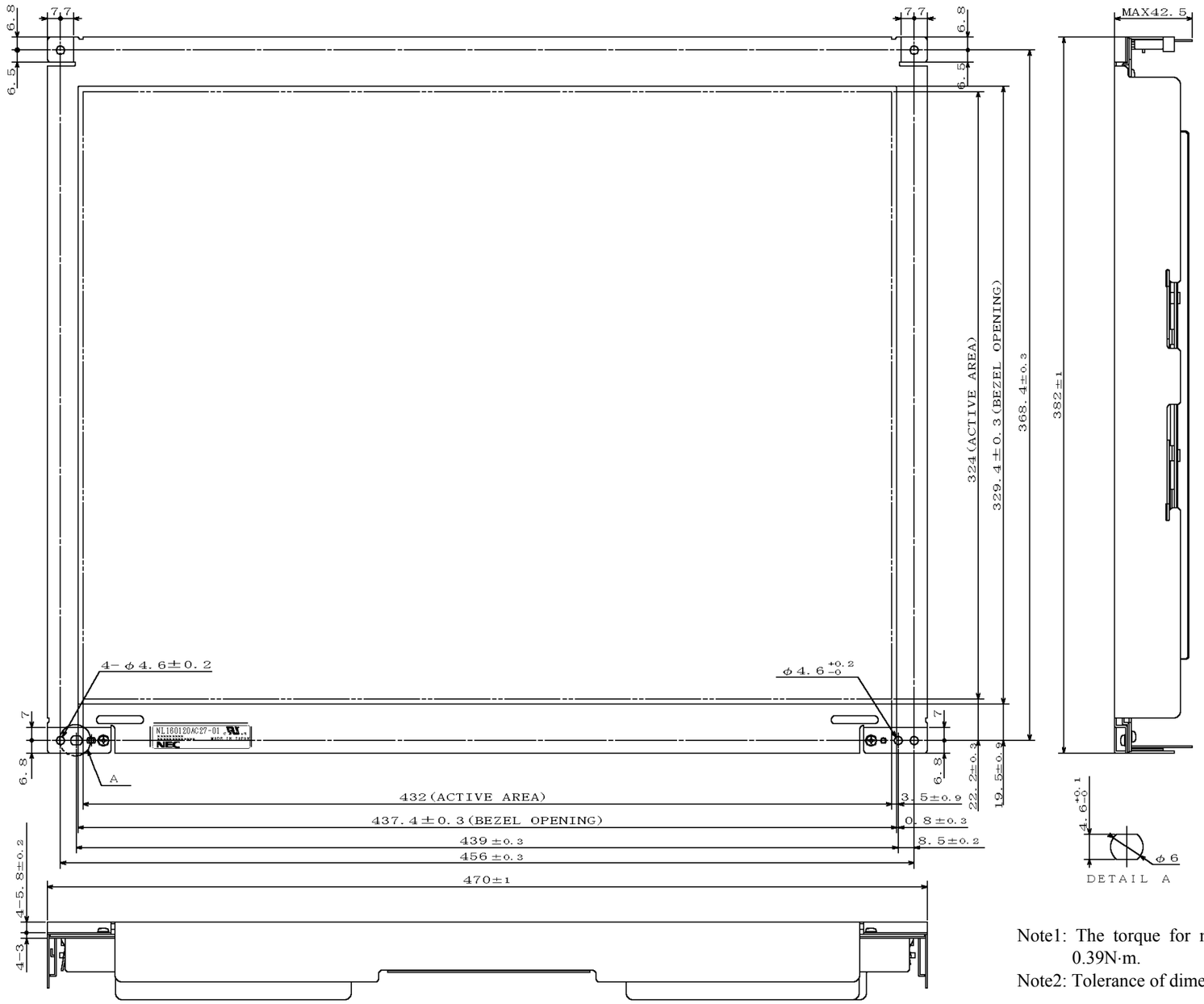
① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ Optical characteristics may be changed by input signal timings.
⑥ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without a non-connected line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
④ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC Corporation for repair and so on.
⑤ Not only the module but also the equipment that used the module should be packed and transported as the module becomes vertical. Otherwise, there is the fear that a display dignity decreases by an impact or vibrations.

7. OUTLINE DRAWINGS

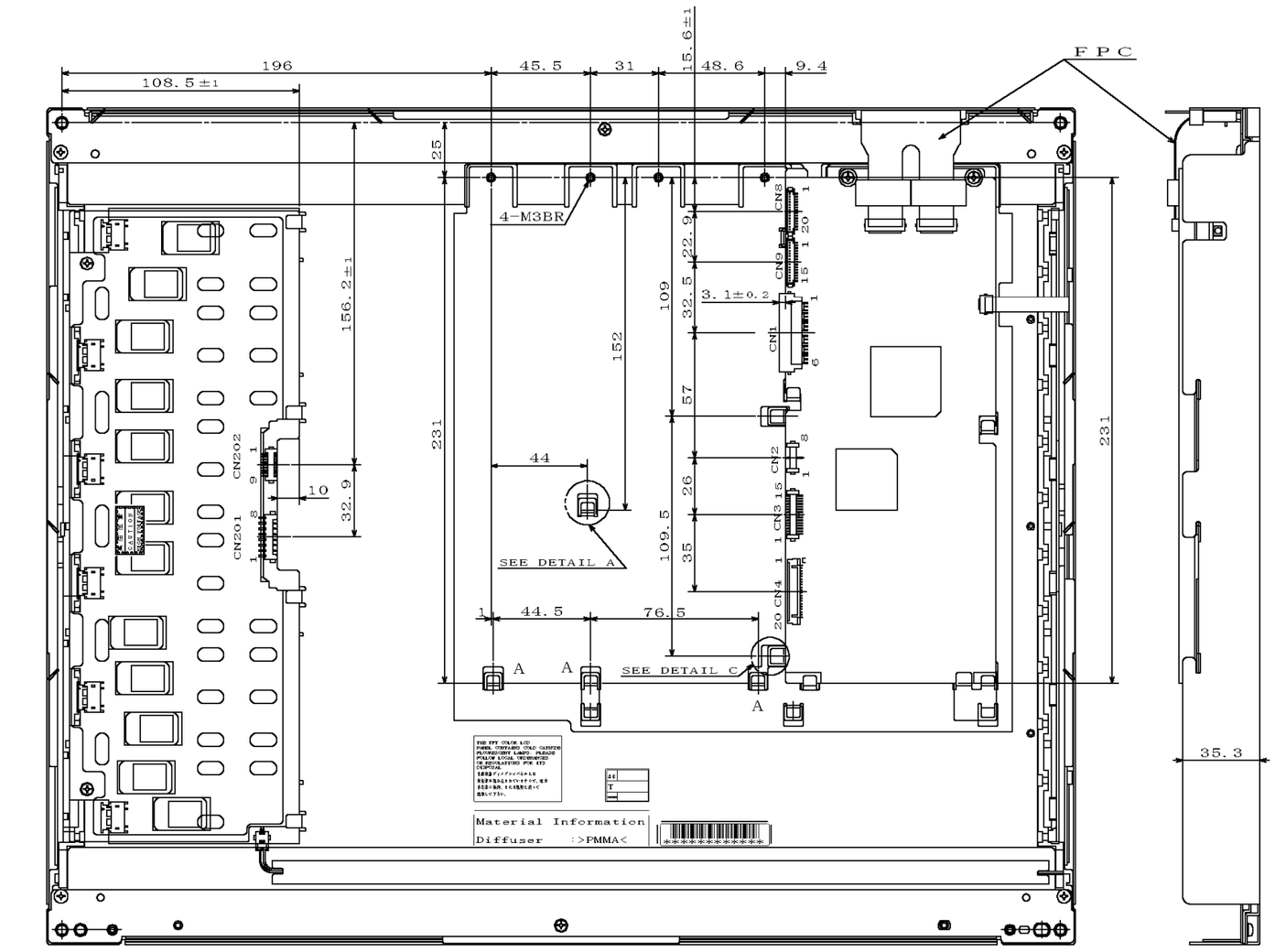
7.1 Front view

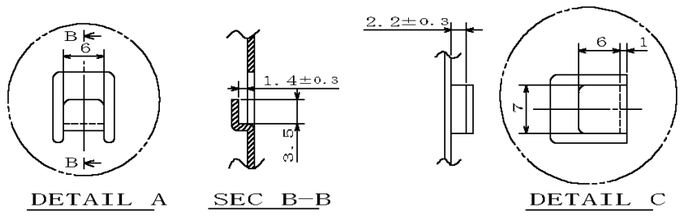


Note1: The torque for mounting screws should never exceed 0.39N·m.

Note2: Tolerance of dimensions not shown is ±0.5mm.

7.2 Rear view





Note1: The torque for mounting screws should never exceed 0.39N·m.
Note2: Tolerance of dimensions not shown is ±0.5mm.