

# TFT COLOR LCD MODULE

**NL160120AC27-05**

**54cm (21.3 Type)**

**UXGA**

**LVDS Interface (2 ports)**

**DATA SHEET** 

**DOD-PD-1233 (4th edition)**

**This DATA SHEET is updated document from  
DOD-PD-1103(3).**

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## INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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## 1. OUTLINE

### 1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL160120AC27-05 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

### 1.2 APPLICATION

- Monitor for PC

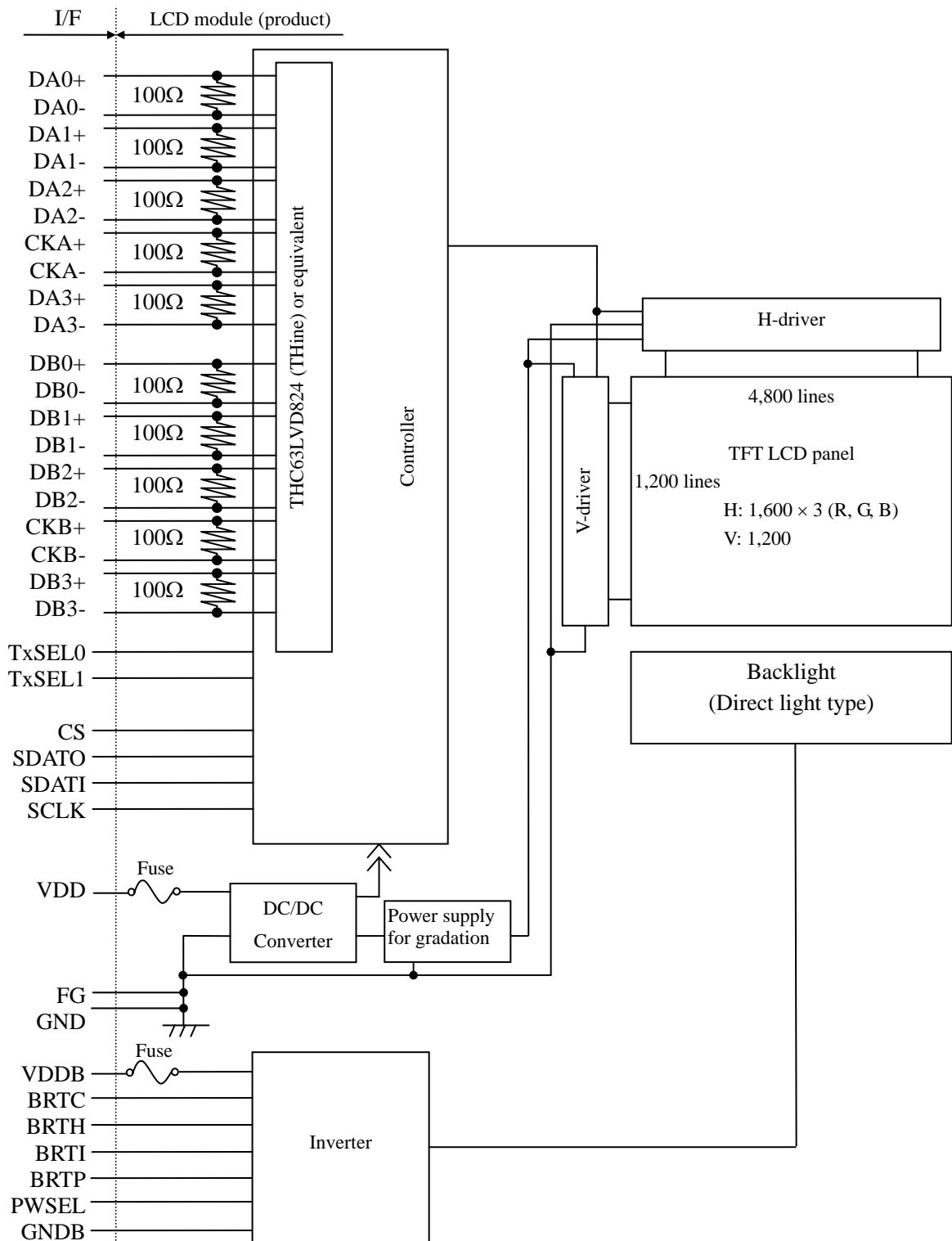
### 1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- Wide color gamut
- High resolution
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated direct light type backlight with inverter
- Replaceable inverter

**2. GENERAL SPECIFICATIONS**

<b>Display area</b>	432.0 (H) × 324.0 (V) mm
<b>Diagonal size of display</b>	54 cm (21.3 inches)
<b>Drive system</b>	a-Si TFT active matrix
<b>Display color</b>	16,777,216 colors
<b>Pixel</b>	1,600 (H) × 1,200 (V) pixels
<b>Pixel arrangement</b>	RGB (Red dot, Green dot, Blue dot) vertical stripe
<b>Dot pitch</b>	0.090 (H) × 0.270 (V) mm
<b>Pixel pitch</b>	0.270 (H) × 0.270 (V) mm
<b>Module size</b>	457.0 (W) × 350.0 (H) × 34.0 (D) mm (typ.)
<b>Weight</b>	2,610 g (typ.)
<b>Contrast ratio</b>	450:1 (typ.)
<b>Viewing angle</b>	At the contrast ratio ≥ 10:1 <ul style="list-style-type: none"> <li>• Horizontal: Right side 85° (typ.), Left side 85° (typ.)</li> <li>• Vertical: Up side 85° (typ.), Down side 85° (typ.)</li> </ul>
<b>Designed viewing direction</b>	Viewing angle with optimum grayscale ( $\gamma=2.2$ ): normal axis (perpendicular)
<b>Polarizer surface</b>	Antiglare
<b>Polarizer pencil-hardness</b>	2H (min.) [by JIS K5400]
<b>Color gamut</b>	At LCD panel center 72% (typ.) [against NTSC color space]
<b>Response time</b>	$T_{on} + T_{off}$ (10% ← → 90%) 16 ms (typ.)
<b>Luminance</b>	At the maximum luminance control 450 cd/m <sup>2</sup> (typ.)
<b>Signal system</b>	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc. or equivalent) [RGB 8-bit signals, Data enable signal (DE), Dot clock (CLK)]
<b>Power supply voltage</b>	LCD panel signal processing board: 12.0V Inverter: 12.0V
<b>Backlight</b>	Direct light type: 16 cold cathode fluorescent lamps with inverter <div style="border-left: 1px solid black; border-right: 1px solid black; border-bottom: 1px solid black; padding: 5px; margin-left: 20px;">                     Replaceable parts  <ul style="list-style-type: none"> <li>• Inverter: Type No. 213PW031</li> </ul> </div>
<b>Power consumption</b>	The maximum luminance control, Checkered flag pattern 63.7 W (typ.)

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and GNDB (Inverter ground) in the LCD module

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that GND, FG and GNDB are connected together in customer equipment.

**4. DETAILED SPECIFICATIONS**

**4.1 MECHANICAL SPECIFICATIONS**

Parameter	Specification	Unit
Module size	457.0 ±1.0 (W) × 350.0 ±1.0 (H) × 34.0 (typ., D) 36.5 (max., D) Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V) Note2	mm
Weight	2,610 (typ.), 2,800 (max.)	g

Note1: Excluding warpage of the signal processing board cover and the connection board cover

Note2: See "7. OUTLINE DRAWINGS".

**4.2 ABSOLUTE MAXIMUM RATINGS**

Parameter		Symbol	Rating	Unit	Remarks	
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C	
	Inverter	VDDB	-0.3 to +15.0	V		
Input voltage for signals	LCD panel signal processing board Note1	Vi	-0.3 to +2.8	V	Ta = 25°C VDD=12.0V	
	Inverter	BRTI signal	VBI	-0.3 to +1.5	V	Ta = 25°C VDDB = 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
PWSEL signal	VBS	-0.3 to +5.5	V			
Storage temperature		Tst	-20 to +60	°C	-	
Operating temperature	Front surface	TopF	0 to +55	°C	Note2	
	Rear surface	TopR	0 to + 60	°C	Note3	
Relative humidity Note4		RH	≤ 70	%	Ta ≤ 55°C	
Absolute humidity Note4		AH	≤ 73 Note5	g/m <sup>3</sup>	Ta > 55°C	
Operating altitude		-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C	
Storage altitude		-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C	

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-  
CS, SDATI, SCLK, TxSEL0, TxSEL1

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta=55°C and RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Supply voltage	VDD	10.8	12.0	13.2	V	-	
Supply current	IDD	-	310 Note1	700 Note2	mA	at VDD=12.0V	
Differential input Threshold voltage	High	VTH	-	-	+100	mV	at VCM=1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing	VI	0	-	2.4	V	Note4	
Terminating resistance	RT	-	100	-	Ω	-	
Control signal input threshold voltage	High	VIH	Keep this pin open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note6
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	
Output signal threshold voltage	High	VOH	1.9	-	-	V	Note7
	Low	VOL	-	-	0.4	V	
Output signal current	High	IOH	-4	-	-	mA	
	Low	IOL	-	-	4	mA	

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note5: TxSEL0, TxSEL1

Note6: CS, SDATI, SCLK

Note7: SDATO

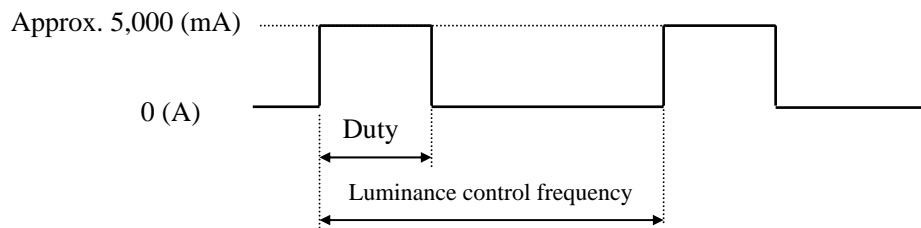


4.3.2 Inverter

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDB	11.4	12.0	12.6	V	-
Power supply current		IDDB	-	5,000	5,700	mA	VDDB = 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V
	BRTP signal	High	VBPH	2.0	-	5.25	V
		Low	VBPL	0	-	0.8	V
	BRTC signal	High	VBCH	2.0	-	5.25	V
		Low	VBCL	0	-	0.8	V
	PWSEL signal	High	VBSH	2.0	-	5.25	V
Low		VBSL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	1,000	μA
	BRTP signal	High	IBPH	-	-	1,000	μA
		Low	IBPL	-600	-	-	μA
	BRTC signal	High	IBCH	-	-	400	μA
		Low	IBCL	-600	-	-	μA
	PWSEL signal	High	IBSH	-	-	440	μA
Low		IBSL	-600	-	-	μA	

4.3.3 Inverter current wave



At the maximum luminance control: 100%  
 Minimum luminance control: 20%  
 Luminance control frequency: 255Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage (See "4.3.4 Power supply voltage ripple".) during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

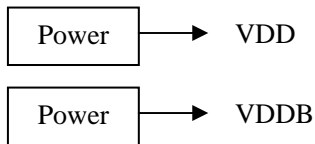
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	12.0 V	≤ 100		mVp-p
VDDb	12.0 V	≤ 200		mVp-p

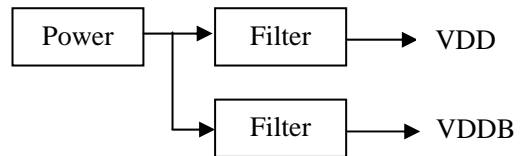
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.5 Fuse

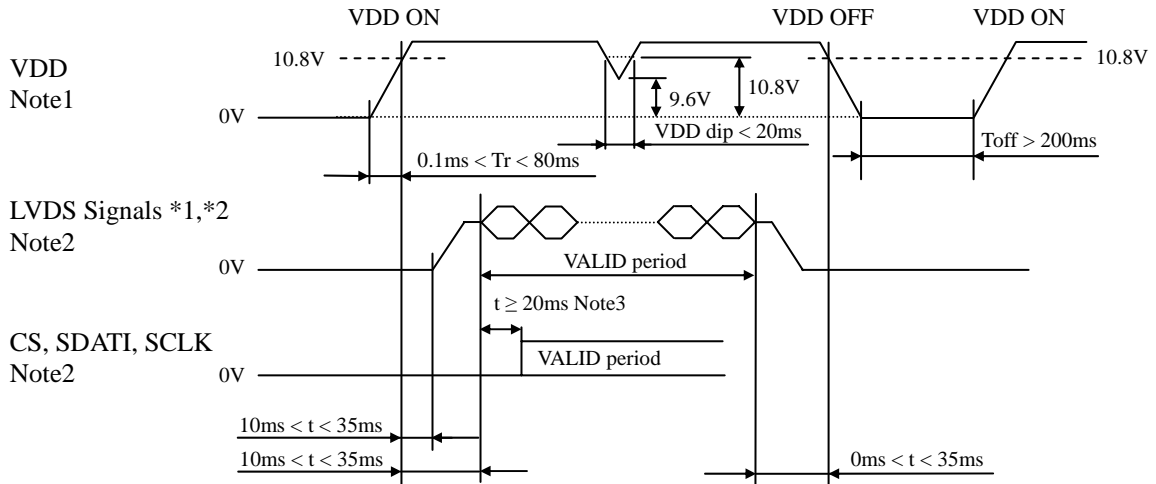
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25A	2.5A, 5s max.	Note1
			32V		
VDDb	0453010	Littelfuse Inc.	10A	20A, 5s max.	
			125V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

☆

4.4 POWER SUPPLY VOLTAGE SEQUENCE

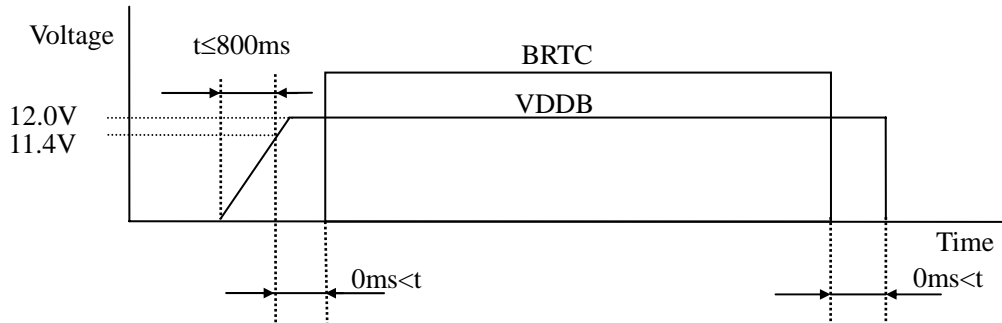
4.4.1 LCD panel signal processing board



- \*1: LVDS signals: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-
- \*2: LVDS signals should be measured at the terminal of 100Ω resistance.

- Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.
- Note2: LVDS signals and CS, SDATI, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.  
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.
- Note3: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing and reading the LUT data, see “4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT”.

4.4.2 Inverter



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display. ☆

Note2: If  $t_r$  is more than 800ms, the backlight will be turned off by a protection circuit for inverter.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

(1) CN1

Socket (LCD module side): DF19G-30P-1H (56) (Hirose Electric Co., Ltd. (HRS))

☆

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks																
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal) Note1																
2	DA0+																		
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal) Note1																
4	DA1+																		
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal) Note1																
6	DA2+																		
7	GND	Ground	Signal ground Note2																
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal) Note1																
9	CKA+																		
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal) Note1																
11	DA3+																		
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal) Note1																
13	DB0+																		
14	GND	Ground	Signal ground Note2																
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal) Note1																
16	DB1+																		
17	GND	Ground	Signal ground Note2																
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal) Note1																
19	DB2+																		
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal) Note1																
21	CKB+																		
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal) Note1																
23	DB3+																		
24	GND	Ground	Signal ground Note2																
25	TxSEL0	Selection of LVDS data input map	Note3, Note4	<table border="1"> <thead> <tr> <th>TxSEL1</th> <th>TxSEL0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>Open</td> <td>Open</td> <td>A</td> </tr> <tr> <td>Open</td> <td>Low</td> <td>B</td> </tr> <tr> <td>Low</td> <td>Open</td> <td>C</td> </tr> <tr> <td>Low</td> <td>Low</td> <td>A</td> </tr> </tbody> </table>	TxSEL1	TxSEL0	Mode	Open	Open	A	Open	Low	B	Low	Open	C	Low	Low	A
TxSEL1	TxSEL0			Mode															
Open	Open			A															
Open	Low			B															
Low	Open	C																	
Low	Low	A																	
26	TxSEL1																		
27	GND	Ground	Signal ground Note2																
28	VDD	Power supply	12V Note2																
29	VDD	Power supply	12V Note2																
30	VDD	Power supply	12V Note2																

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: These terminals are pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "4.7 DATA INPUT MAP".

(2) CN3

Socket (LCD module side): SM10B-SRSS-TB(LF)(SN) (J.S.T. Mfg Co., Ltd.)

☆

Adaptable plug: SHR-10V-S, SHR-10V-S-B or 10SR-3S (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	RSVD	Reserved	Keep this pin Open.
2	RSVD	Reserved	Keep this pin Open.
3	RSVD	Reserved	Keep this pin Open.
4	GND	Ground	Signal ground Note1
5	CS	Chip selection	For LUT communication control Note2
6	SDATO	Serial data output	For LUT output signal
7	SDATI	Serial data input	For LUT communication control Note3
8	SCLK	Serial clock	For LUT communication control Note3
9	GND	Ground	Signal ground Note1
10	RSVD	Reserved	Keep this pin Open.

Note1: All GND terminals should be used without any non-connected lines.

Note2: This terminal is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note3: These terminals are pulled-down in the product. (Pull-down resistance: 50kΩ)

4.5.2 Inverter

(1) CN201

Socket (LCD module side): DF3Z-10P-2H (2\*) (HIROSE ELECTRIC Co., Ltd. (HRS))

☆

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co., Ltd. (HRS))

Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All GNDB and VDDB terminals should be used without any non-connected lines.

(2) CN202

Socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

☆

Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

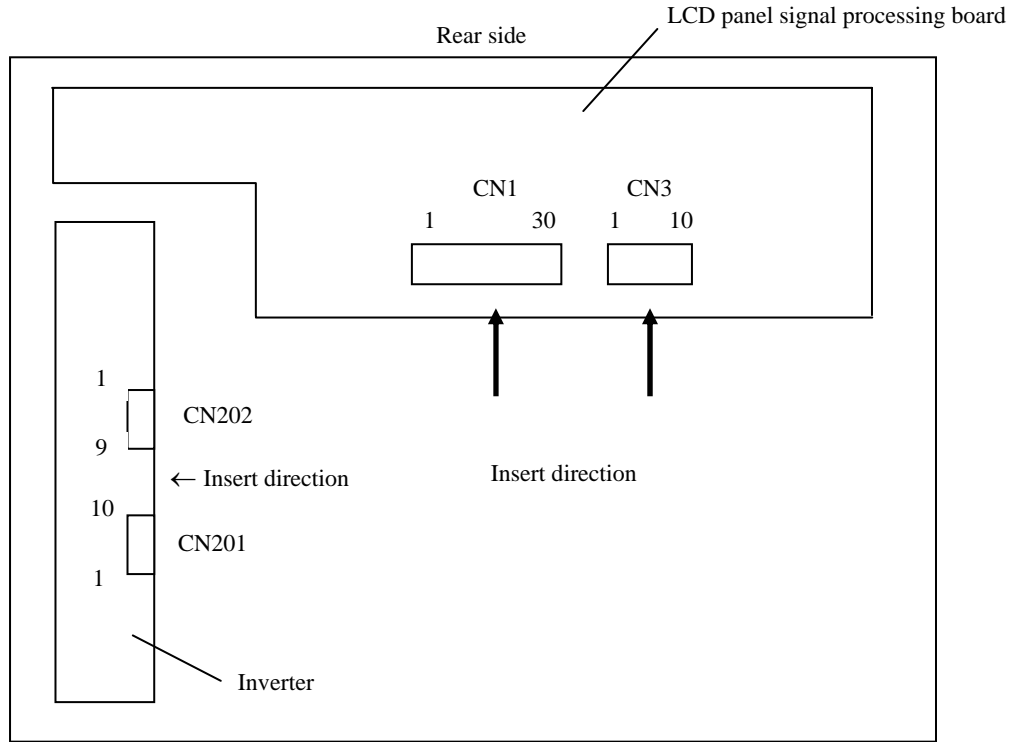
Pin No.	Symbol	Function	Description
1	GNDB	Inverter ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	B RTP	B RTP signal	
8	GNDB	Inverter ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.

Note2: See "4.6.1 Luminance control methods".

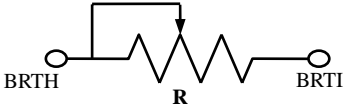
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket



4.6 LUMINANCE CONTROLS

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
Variable resistor control Note1	<ul style="list-style-type: none"> <li>Adjustment</li> </ul> <p>The variable resistor (<b>R</b>) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance, and maximum point of the resistance is the maximum luminance.                      The resistor (<b>R</b>) must be connected between BRTH-BRTI terminals.</p>  <ul style="list-style-type: none"> <li>Luminance ratio Note3</li> </ul> <table border="1" data-bbox="491 869 1002 987"> <thead> <tr> <th>Resistance</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0 Ω</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>10 kΩ</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Resistance	Luminance ratio	0 Ω	20% (Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
0 Ω	20% (Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
Voltage control Note1	<ul style="list-style-type: none"> <li>Adjustment</li> </ul> <p>Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI and BRTH terminals. This control method can carry out continuation adjustment of luminance.                      Luminance is the maximum when BRTI terminal is Open.</p> <ul style="list-style-type: none"> <li>Luminance ratio Note3</li> </ul> <table border="1" data-bbox="491 1279 1002 1397"> <thead> <tr> <th>BRTI signal (VBI)</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0V</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>1.0V</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	BRTI signal (VBI)	Luminance ratio	0V	20% (Min. Luminance)	1.0V	100% (Max. Luminance)		
BRTI signal (VBI)	Luminance ratio								
0V	20% (Min. Luminance)								
1.0V	100% (Max. Luminance)								
Pulse width modulation Note1 Note2 Note4	<ul style="list-style-type: none"> <li>Adjustment</li> </ul> <p>Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.</p> <ul style="list-style-type: none"> <li>Luminance ratio Note3</li> </ul> <table border="1" data-bbox="491 1637 1002 1756"> <thead> <tr> <th>Duty ratio Note4</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0.2</td> <td>20% (Min. Luminance)</td> </tr> <tr> <td>1.0</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Duty ratio Note4	Luminance ratio	0.2	20% (Min. Luminance)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio Note4	Luminance ratio								
0.2	20% (Min. Luminance)								
1.0	100% (Max. Luminance)								

Note1: In case of the resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

**Use PWM method, if interference noises appear on the display image!**

Note2: The inverter will stop working, if the Low period of BRTP signal is more than 50ms while BRTP signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The inverter will start to work when power is supplied again.

Note3: These data are the target values.

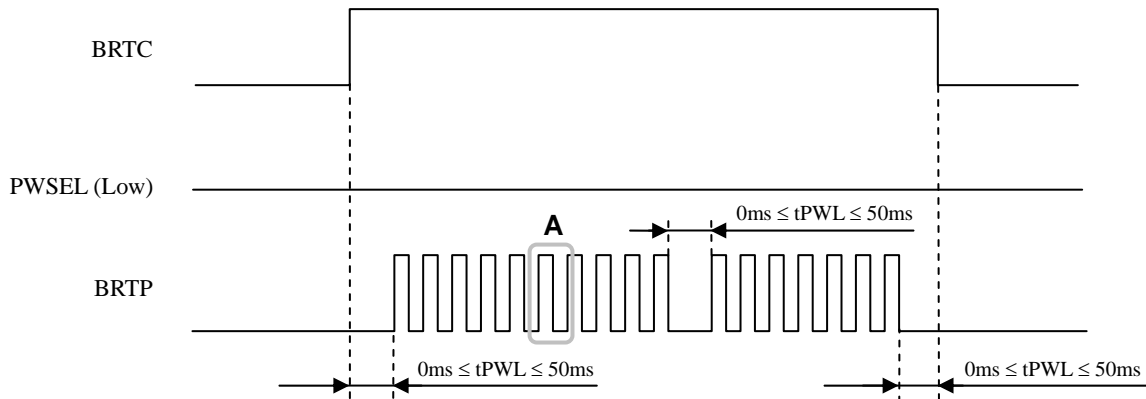
Note4: See "4.6.2 Detail of BRTP timing".



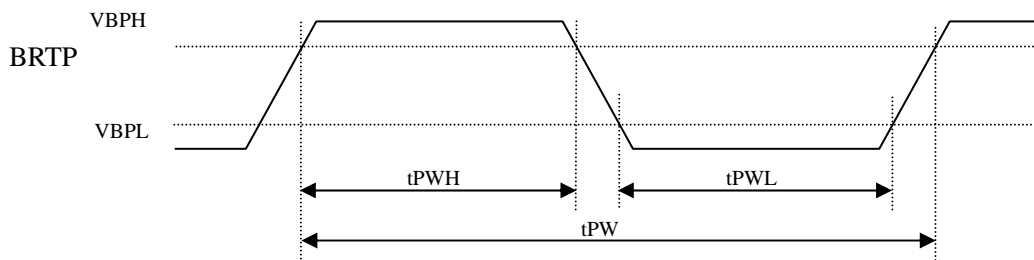
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Detail of A part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Low period	tPWL	0	-	50	ms	Note4

Note1: Definition of parameters is as follows.

$$FL = \frac{1}{t\text{PW}} \quad DL = \frac{t\text{PWH}}{t\text{PW}}$$

Note2: See the following formula for luminance control frequency.

$$\text{Luminance control frequency} = 1/tv \times (n+0.25) \text{ [or } (n + 0.75)]$$

$$n = 1, 2, 3 \dots \dots$$

tv: Vertical Cycle period (See "4.9.1 Timing characteristics".)

**The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!**

Note3: See "4.6.1 Luminance control methods".

Note4: If tPWL is more than 50ms, the backlight will be turned off by a protection circuit for inverter. The inverter will start to work when power is supplied again.

4.7 DATA INPUT MAP  
4.7.1 Mode A

Input data		Note1	Transmitter				CN1		
			Pin	THC63LVDF83A	Pin	THC63LVD823	Pin	Symbol	
Odd pixel data and control signal	RA2	→	51	TA0	53	R12			
	RA3	→	52	TA1	54	R13	TA1-	1 DA0-	
	RA4	→	54	TA2	57	R14	TA1+	2 DA0+	
	RA5	→	55	TA3	58	R15			
	RA6	→	56	TA4	59	R16	TB1-	3 DA1-	
	RA7	→	3	TA5	60	R17	TB1+	4 DA1+	
	GA2	→	4	TA6	63	G12			
	GA3	→	6	TB0	64	G13	TC1-	5 DA2-	
	GA4	→	7	TB1	65	G14	TC1+	6 DA2+	
	GA5	→	11	TB2	66	G15		7 GND	
	GA6	→	12	TB3	67	G16	TCLK1-	8 CKA-	
	GA7	→	14	TB4	68	G17	TCLK1+	9 CKA+	
	BA2	→	15	TB5	73	B12			
	BA3	→	19	TB6	74	B13	TD1-	10 DA3-	
	BA4	→	20	TC0	75	B14	TD1+	11 DA3+	
	BA5	→	22	TC1	76	B15			
	BA6	→	23	TC2	77	B16			
	BA7	→	24	TC3	78	B17			
	Note3	RSVD	→	27	TC4	7	RSVD		
	Note3	RSVD	→	28	TC5	8	RSVD		
		DE	→	30	TC6	9	DE		
		RA0	→	50	TD0	51	R10		
		RA1	→	2	TD1	52	R11		
		GA0	→	8	TD2	61	G10		
		GA1	→	10	TD3	62	G11		
		BA0	→	16	TD4	69	B10		
		BA1	→	18	TD5	70	B11		
	Note3	RSVD	→	25	TD6	-			
		CLK	→	31	CLKIN	10	CLK		
	Even pixel data	RB2	→	51	TA0	81	R22		
		RB3	→	52	TA1	82	R23	TA2-	12 DB0-
RB4		→	54	TA2	83	R24	TA2+	13 DB0+	
RB5		→	55	TA3	84	R25		14 GND	
RB6		→	56	TA4	85	R26	TB2-	15 DB1-	
RB7		→	3	TA5	86	R27	TB2+	16 DB1+	
GB2		→	4	TA6	91	G22		17 GND	
GB3		→	6	TB0	92	G23	TC2-	18 DB2-	
GB4		→	7	TB1	93	G24	TC2+	19 DB2+	
GB5		→	11	TB2	94	G25			
GB6		→	12	TB3	95	G26	TCLK2-	20 CKB-	
GB7		→	14	TB4	96	G27	TCLK2+	21 CKB+	
BB2		→	15	TB5	99	B22			
BB3		→	19	TB6	100	B23	TD2-	22 DB3-	
BB4		→	20	TC0	1	B24	TD2+	23 DB3+	
BB5		→	22	TC1	2	B25		24 GND	
BB6		→	23	TC2	5	B26		25 TxSEL0	
BB7		→	24	TC3	6	B27		26 TxSEL1	
Note3		RSVD	→	27	TC4	-		27 GND	
Note3		RSVD	→	28	TC5	-		28 VDD	
Note3		RSVD	→	30	TC6	-		29 VDD	
		RB0	→	50	TD0	79	R20	30 VDD	
		RB1	→	2	TD1	80	R21		
		GB0	→	8	TD2	89	G20		
		GB1	→	10	TD3	90	G21		
		BB0	→	16	TD4	97	B20		
		BB1	→	18	TD5	98	B21		
Note3		RSVD	→	25	TD6	-			
		CLK	→	31	CLKIN	-			

4.7.2 Mode B

Input data		Note1	Transmitter		CN1		
			Pin	DS90CF383, C385		Pin Symbol	
Odd pixel data and control signal	RA7	→	51	TXIN0			
	RA6	→	52	TXIN1	Note2	1 DA0-	
	RA5	→	54	TXIN2		2 DA0+	
	RA4	→	55	TXIN3			
	RA3	→	56	TXIN4		3 DA1-	
	RA2	→	3	TXIN6		4 DA1+	
	GA7	→	4	TXIN7			
	GA6	→	6	TXIN8		5 DA2-	
	GA5	→	7	TXIN9		6 DA2+	
	GA4	→	11	TXIN12		7 GND	
	GA3	→	12	TXIN13		8 CKA-	
	GA2	→	14	TXIN14		9 CKA+	
	BA7	→	15	TXIN15			
	BA6	→	19	TXIN18		10 DA3-	
	BA5	→	20	TXIN19	1st	11 DA3+	
	BA4	→	22	TXIN20			
	BA3	→	23	TXIN21			
	BA2	→	24	TXIN22			
	Note3	RSVD	→	27	TXIN24		
	Note3	RSVD	→	28	TXIN25		
		DE	→	30	TXIN26		
		RA1	→	50	TXIN27		
		RA0	→	2	TXIN5		
		GA1	→	8	TXIN10		
		GA0	→	10	TXIN11		
		BA1	→	16	TXIN16		
	BA0	→	18	TXIN17			
Note3	RSVD	→	25	TXIN23			
	CLK	→	31	CLKIN			
Even pixel data	RB7	→	51	TXIN0			
	RB6	→	52	TXIN1		12 DB0-	
	RB5	→	54	TXIN2		13 DB0+	
	RB4	→	55	TXIN3		14 GND	
	RB3	→	56	TXIN4		15 DB1-	
	RB2	→	3	TXIN6		16 DB1+	
	GB7	→	4	TXIN7		17 GND	
	GB6	→	6	TXIN8		18 DB2-	
	GB5	→	7	TXIN9		19 DB2+	
	GB4	→	11	TXIN12			
	GB3	→	12	TXIN13		20 CKB-	
	GB2	→	14	TXIN14		21 CKB+	
	BB7	→	15	TXIN15			
	BB6	→	19	TXIN18		22 DB3-	
	BB5	→	20	TXIN19	2nd	23 DB3+	
	BB4	→	22	TXIN20		24 GND	
	BB3	→	23	TXIN21		25 TxSELO	
	BB2	→	24	TXIN22		26 TxSELI	
	Note3	RSVD	→	27	TXIN24		27 GND
	Note3	RSVD	→	28	TXIN25		28 VDD
	Note3	RSVD	→	30	TXIN26		29 VDD
		RB1	→	50	TXIN27		30 VDD
		RB0	→	2	TXIN5		
		GB1	→	8	TXIN10		
		GB0	→	10	TXIN11		
		BB1	→	16	TXIN16		
	BB0	→	18	TXIN17			
Note3	RSVD	→	25	TXIN23			
	CLK	→	31	CLKIN			

4.7.3 Mode C

Input data		Note1	Transmitter		CN1		
			Pin	DS90CF383, C385		Pin Symbol	
Odd pixel data and control signal	RA0	→	51	TXIN0			
	RA1	→	52	TXIN1	TA1-	1 DA0-	
	RA2	→	54	TXIN2	TA1+	2 DA0+	
	RA3	→	55	TXIN3			
	RA4	→	56	TXIN4	TB1-	3 DA1-	
	RA5	→	3	TXIN6	TB1+	4 DA1+	
	GA0	→	4	TXIN7			
	GA1	→	6	TXIN8	TC1-	5 DA2-	
	GA2	→	7	TXIN9	TC1+	6 DA2+	
	GA3	→	11	TXIN12		7 GND	
	GA4	→	12	TXIN13	TCLK1-	8 CKA-	
	GA5	→	14	TXIN14	TCLK1+	9 CKA+	
	BA0	→	15	TXIN15			
	BA1	→	19	TXIN18	TD1-	10 DA3-	
	BA2	→	20	TXIN19	TD1+	11 DA3+	
	BA3	→	22	TXIN20			
	BA4	→	23	TXIN21			
	BA5	→	24	TXIN22			
	Note3	RSVD	→	27	TXIN24		
	Note3	RSVD	→	28	TXIN25		
		DE	→	30	TXIN26		
		RA6	→	50	TXIN27		
		RA7	→	2	TXIN5		
		GA6	→	8	TXIN10		
		GA7	→	10	TXIN11		
		BA6	→	16	TXIN16		
		BA7	→	18	TXIN17		
	Note3	RSVD	→	25	TXIN23		
		CLK	→	31	CLKIN		
	Even pixel data	RB0	→	51	TXIN0		
		RB1	→	52	TXIN1	TA2-	12 DB0-
RB2		→	54	TXIN2	TA2+	13 DB0+	
RB3		→	55	TXIN3		14 GND	
RB4		→	56	TXIN4	TB2-	15 DB1-	
RB5		→	3	TXIN6	TB2+	16 DB1+	
GB0		→	4	TXIN7		17 GND	
GB1		→	6	TXIN8	TC2-	18 DB2-	
GB2		→	7	TXIN9	TC2+	19 DB2+	
GB3		→	11	TXIN12			
GB4		→	12	TXIN13	TCLK2-	20 CKB-	
GB5		→	14	TXIN14	TCLK2+	21 CKB+	
BB0		→	15	TXIN15			
BB1		→	19	TXIN18	TD2-	22 DB3-	
BB2		→	20	TXIN19	TD2+	23 DB3+	
BB3		→	22	TXIN20		24 GND	
BB4		→	23	TXIN21		25 TxSEL0	
BB5		→	24	TXIN22		26 TxSEL1	
Note3		RSVD	→	27	TXIN24		27 GND
Note3		RSVD	→	28	TXIN25		28 VDD
Note3		RSVD	→	30	TXIN26		29 VDD
		RB6	→	50	TXIN27		30 VDD
		RB7	→	2	TXIN5		
		GB6	→	8	TXIN10		
		GB7	→	10	TXIN11		
		BB6	→	16	TXIN16		
		BB7	→	18	TXIN17		
Note3		RSVD	→	25	TXIN23		
		CLK	→	31	CLKIN		

Note1: LSB (Least Significant Bit) – RA0, GA0, BA0, RB0, GB0, BB0  
 MSB (Most Significant Bit) – RA7, GA7, BA7, RB7, GB7, BB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0								GA7 GA6 GA5 GA4 GA3 GA2 GA1 GA0								BA7 BA6 BA5 BA4 BA3 BA2 BA1 BA0							
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:																			
	↓					:																			
bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:																			
	↓					:																			
bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:																			
	↓					:																			
bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

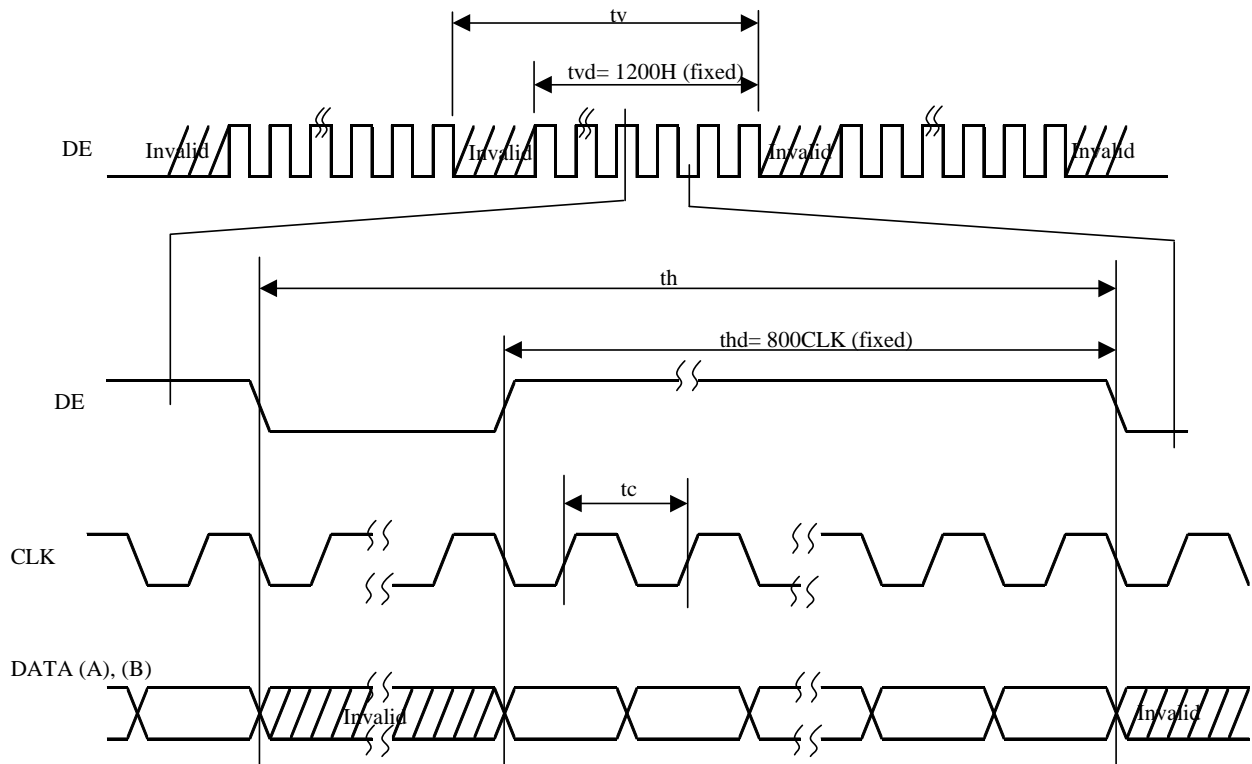
4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

Parameter	Symbol	min.	typ.	max.	Unit	Remarks		
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input	
	Pulse width	tc	15.38	15.5	-	ns		
	Duty	-	See the data sheet of LVDS transmitter.			-		-
	Rise, fall	-				ns		
Horizontal	Cycle period	th	13.1	13.3	19.2	$\mu$ s	-	
			848	860	1,156	CLK		
	Display period	thd	800			CLK	-	
Vertical	Cycle period	1/tv	59	60	61	Hz	-	
		tv	1,206	1,250	-	H		
	Display period	tvd	1,200			H	-	
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-	
	Hold time	-				ns		
	Rise, fall	-				ns		

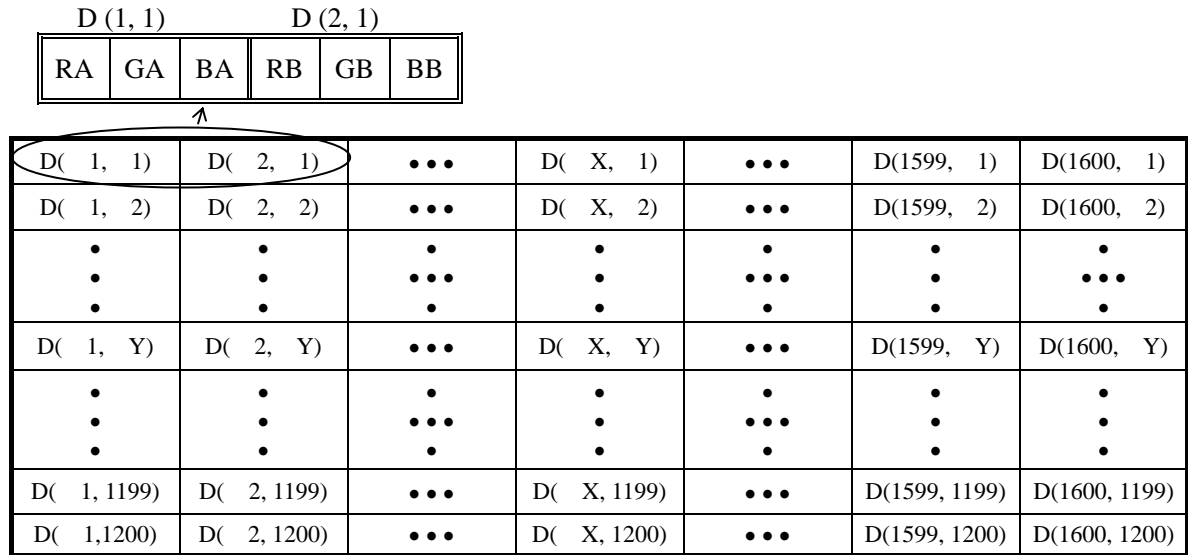
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4.9.2 Input signal timing chart



4.10 DISPLAY POSITIONS

Odd pixel: RA= Red data      Even pixel: RB= Red data  
 GA= Green data            GB= Green data  
 BA= Blue data              BB= Blue data



4.11 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit RGB color data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines the R/W actions: READ, Random/Sequential Address WRITE and Individual/Simultaneous RGB setting.

The serial data is composed as Table 1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	
D15	Dummy	Dummy Data "0"	See Table5.
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	



Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Selection of WRITE/READ mode "1": WRITE mode "0": READ mode	When CMD5 is "0", CMD4-CMD0 must be set as follows. CMD4: "1", CMD3: "0", CMD2: "1" CMD1: "0", CMD0: "0"
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous RGB setting "1": Individual RGB setting "0": Simultaneous RGB setting	"1": Select the color by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command Combination table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Mode
1	1	1	1	1	0	Random Address WRITE, Individual RGB setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous RGB setting
1	1	0	1	1	0	Sequential Address WRITE, Individual RGB setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous RGB setting
0	1	0	1	0	0	READ mode

\*Other combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9	Color Selection ADD[9:8]= 0:0 Red 0:1 Green 1:0 Blue 1:1 ON/OFF selection of Gamma Correction	When "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD8		
ADD7		
ADD6		
ADD5	LUT Address 256 address = 00h - FFh	When ADD[9:8] = 1:1, ADD[7:0] must be set to 00h.
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table5: Data table (DATA15 to DATA0: 16-bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB]	-
DATA8	DATA8	10-bit LUT Data 000h - 3FFh	
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5		
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0	[LSB]	

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GMA2	[MSB]	See Table7.
DATA1	GMA1	GMA Data	
DATA0	GMA0	[LSB]	

Table7: Control code GMA[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data. Note1

\*Other combinations are prohibited, and may cause function error.

Note1: Initial setting of the LUT is undefined data. The LUT should be enabled by setting of the GMA after writing the LUT data in all the 256 addresses, in order to avoid undefined data display.

Note2: Transfer the data every power-on, because the LUT data isn't stored in the LCD module.

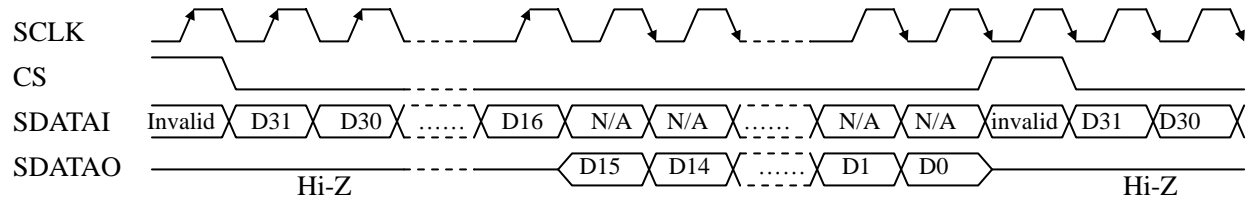
Note3: As writing and reading the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.

- (1) The LUT data should be rewritten during invalid period of pixel data (See "4.9 INPUT SIGNAL TIMINGS").
- (2) The LUT data should be rewritten when the Gamma Correction is OFF (GMA[2:0] = 000).

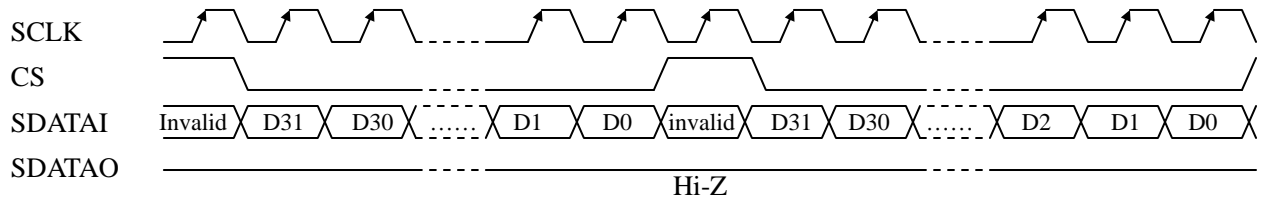
4.12 LUT SERIAL COMMUNICATION TIMINGS

4.12.1 Timing Chart

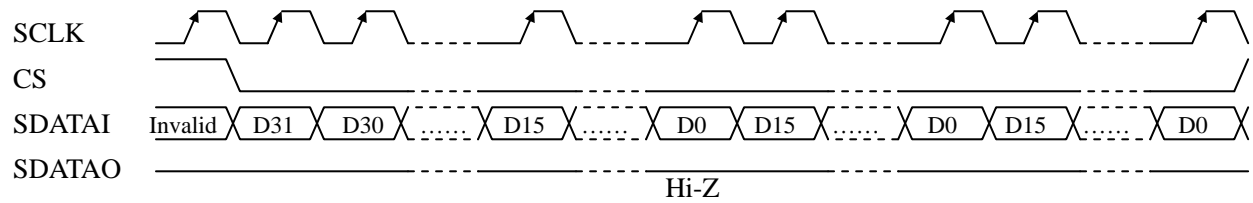
(1) READ Timing Chart



(2) Random Address WRITE Timing Chart



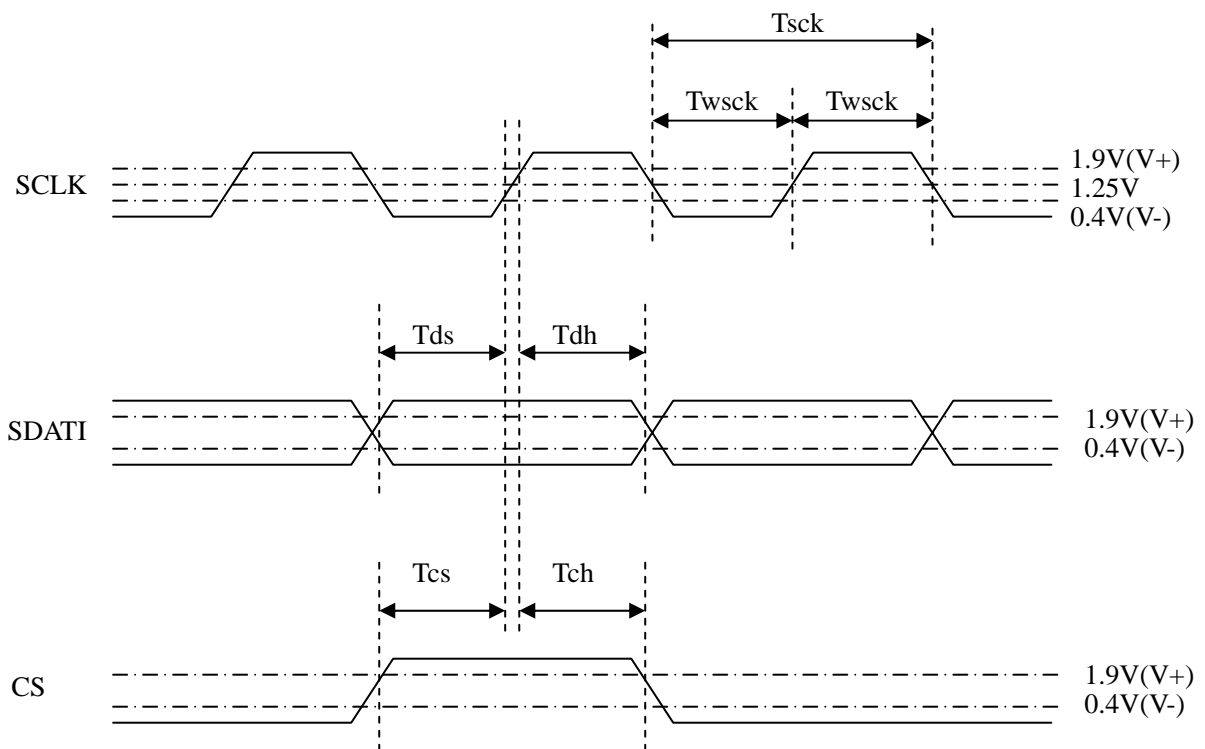
(3) Sequential Address WRITE Timing Chart



4.12.2 Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse Width (WRITE)	Twscck	50	-	-	ns	-
SCLK Pulse Width (READ)	Twscck	5	-	-	tc	Note1
SDATI-SCLK Setup Time	Tds	50	-	-	ns	-
SDATI-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-

Note1: At the READ of the serial communication mode, the SCLK Pulse Width (Twscck) must be greater than 5CLK (5 tc's). (See "4.9.1 Timing characteristics".)



Note2: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the LUT data when the pixel data is invalid or the Gamma Correction is OFF (GMA[2:0] = 000). The external noise may cause the data change, refresh the data regularly according to need.

4.13 OPTICS

4.13.1 Optical characteristics

(Note1, Note2)

Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	350	450	-	cd/m <sup>2</sup>	BM-5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	300	450	-	-	BM-5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.2	1.3	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	-	0.313	-	-	SR-3	Note5
		y coordinate	Wy	-	0.329	-	-		
	Red	x coordinate	Rx	-	0.65	-	-		
		y coordinate	Ry	-	0.33	-	-		
	Green	x coordinate	Gx	-	0.29	-	-		
		y coordinate	Gy	-	0.61	-	-		
Blue	x coordinate	Bx	-	0.14	-	-			
	y coordinate	By	-	0.079	-	-			
Color gamut	$\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$ at center, against NTSC color space	C	65	72	-	%			
Response time	Black to White	Ton	-	8	20	ms	BM-5A	Note6	
	White to Black	Toff	-	8	20	ms		Note7	
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta R$	70	85	-	BM-5A	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta L$	70	85	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta U$	70	85	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta D$	70	85	-			

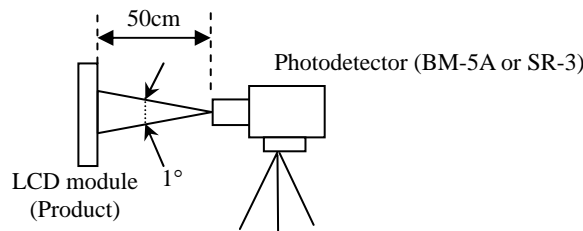
Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12.0V, VDDB = 12.0V, Luminance control = maximum,

Display mode: UXGA, Horizontal cycle = 1/75.19kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "4.13.2 Definition of contrast ratio".

Note4: See "4.13.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 37 °C

Note7: See "4.13.4 Definition of response times".

Note8: See "4.13.5 Definition of viewing angles".

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

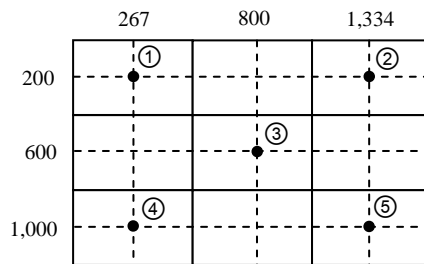
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

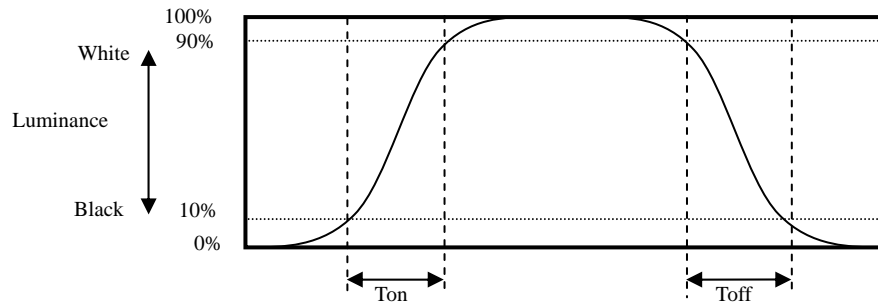
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

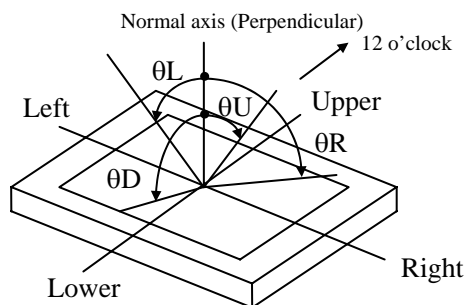


4.13.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.13.5 Definition of viewing angles

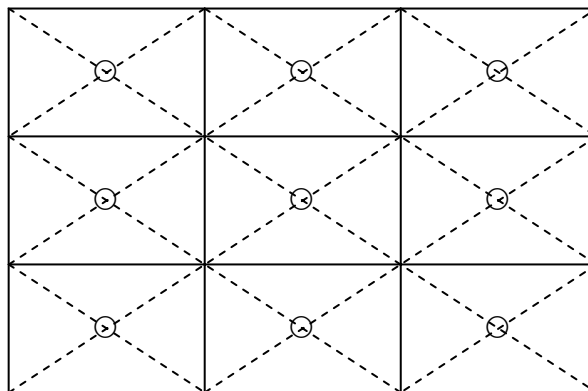


**5. RELIABILITY TESTS**

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)	① 0 ± 3°C...1hour 55 ± 3°C...1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① -20 ± 3°C...30minutes 60 ± 3°C...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)	① 5 to 100Hz, 11.76m/s <sup>2</sup> ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① 294m/s <sup>2</sup> , 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)	① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Non-operation	No display malfunctions
	Operation	
	① 15 kPa (Equivalent to altitude 13,600m) ② -20°C±3°C...24 hours ③ +60°C±3°C...24 hours	
	① 53.3 kPa (Equivalent to altitude 4,850m) ② 0°C±3°C...24 hours ③ +55°C±3°C...24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.




Note2: See the following figure for discharge points




6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS


The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



**\* Do not touch the working backlight. There is a danger of an electric shock.**



**\* Do not touch the working backlight. There is a danger of burn injury.**  
**\* Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s<sup>2</sup> and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

6.3 ATTENTIONS 

6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735 N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 5.3mm.
- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.



- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

### 6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

### 6.3.3 Characteristics

**The following items are neither defects nor failures.**

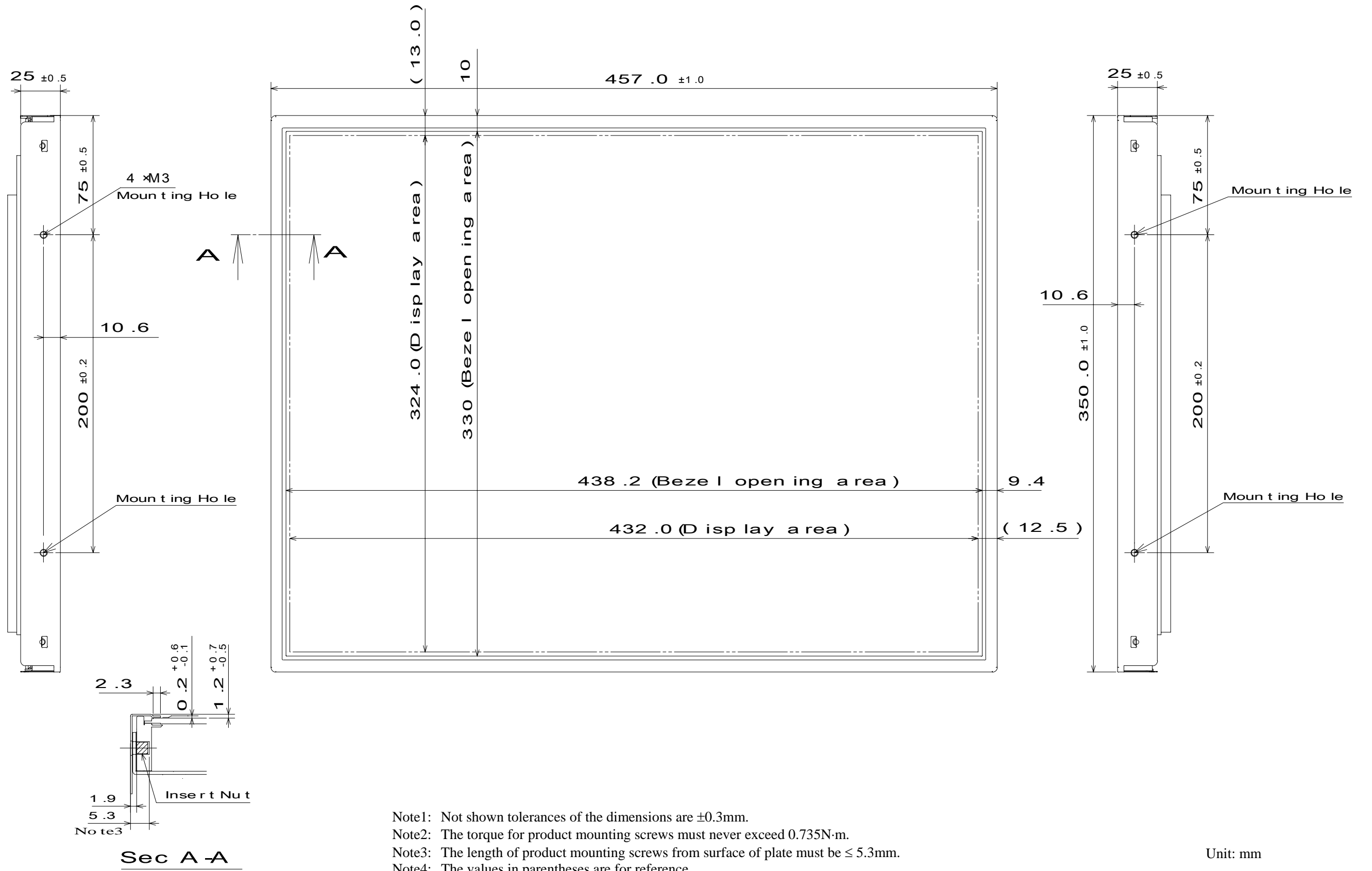
- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

### 6.3.4 Other

- ① All GND, GNDB VDD and VDDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ See “REPLACEMENT MANUAL FOR INVERTER”, when replacing the inverter.
- ④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS

7.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are ±0.3mm.
- Note2: The torque for product mounting screws must never exceed 0.735N·m.
- Note3: The length of product mounting screws from surface of plate must be ≤ 5.3mm.
- Note4: The values in parentheses are for reference.

Unit: mm

