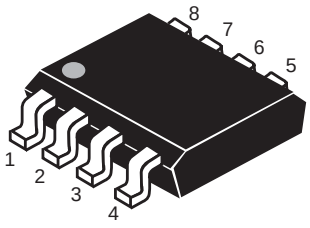
South Sea Semiconductor

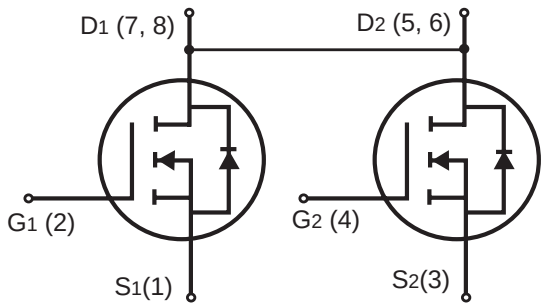
SSM9926A

Comman Drain Dual N-Channel Enhancement Mode MOSFET

Product Summary		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
20V	6A	30 @V_{GS} = 4.0V
		40 @V_{GS} = 2.5V

SOP-8





FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- SOP-8 package.
- Pb Free.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current-Continuous @ T_C = 25°C	I_D	6	A
-Pulsed [b]	I_{DM}	35	A
Drain-Source Diode Forward Current [a]	I_S	1.7	A
Maximum Power Dissipation [a]	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.5	0.8	1.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.0V, I_D=6A		25	30	mΩ
		V_{GS}=2.5V, I_D=3A		35	40	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=5V, V_{GS}=4V	30			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=4A		12		S
Input Capacitance	C_{ISS}	V_{DS}=8V		810		pF
Output Capacitance	C_{OSS}	V_{GS}=0V		155		
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz		125		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=10V,		18		ns
Rise Time	t_r	I_D=1A,		5		
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GEN}=4.5V,		44		
Fall Time	t_f	R_{GEN}=10Ω, R_L=10Ω		20		
Total Gate Charge	Q_g	V_{DS}=10V,		11		nC
Gate-Source Charge	Q_{gs}	I_D=4A,		3		
Gate-Drain Charge	Q_{gd}	V_{GS}=4.5V		2.5		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=1A		0.8	1.2	V

Notes：

a. Surface Mounted on FR4 Board, t ≤10 sec.

b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

c. Guaranteed by design, not subject to production testing.

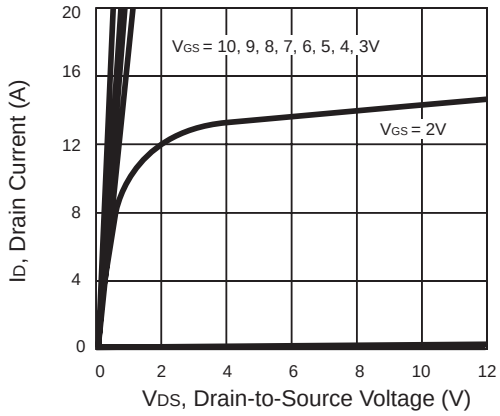


Figure 1. Output Characteristics

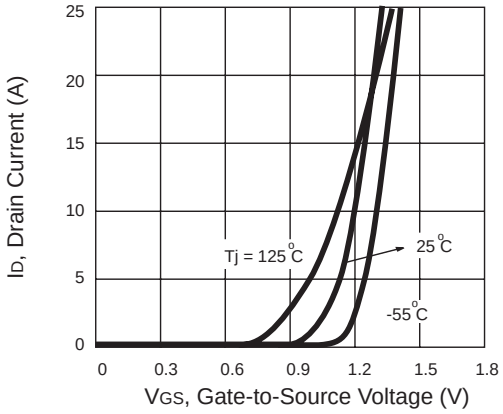


Figure 2. Thansfer Characteristics

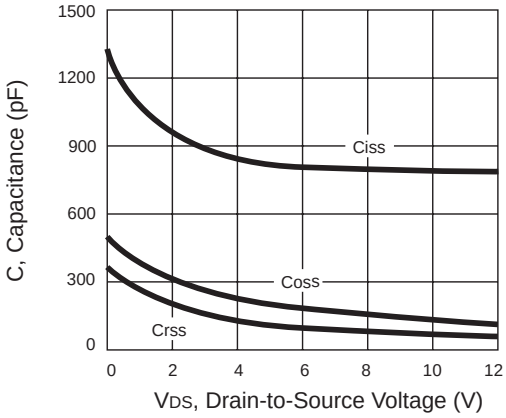


Figure 3. Capacitance

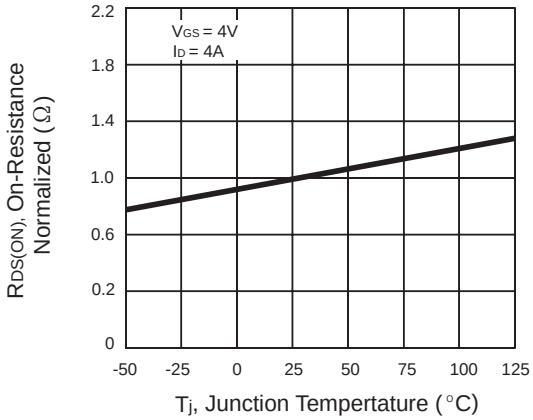


Figure 4. On-Resistance Variation with Temperature

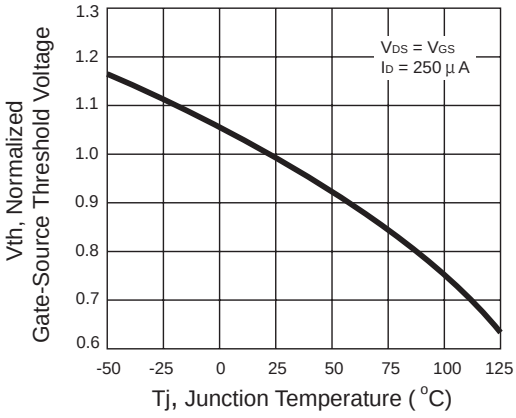


Figure 5. Gate Threshold Variation with Temperature

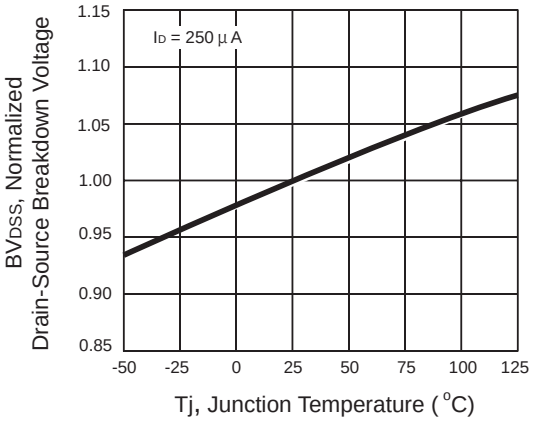


Figure 6. Breakdown Voltage Variation with Temperature

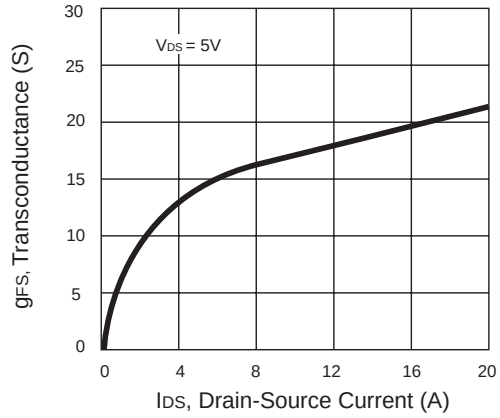


Figure 7. Transconductance Variation with Drain Current

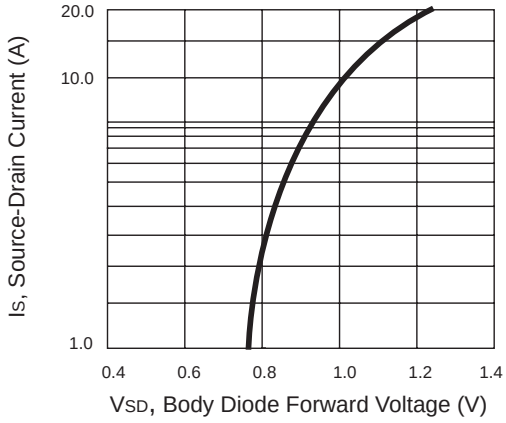


Figure 8. Body Diode Forward Voltage Variation with Source Current

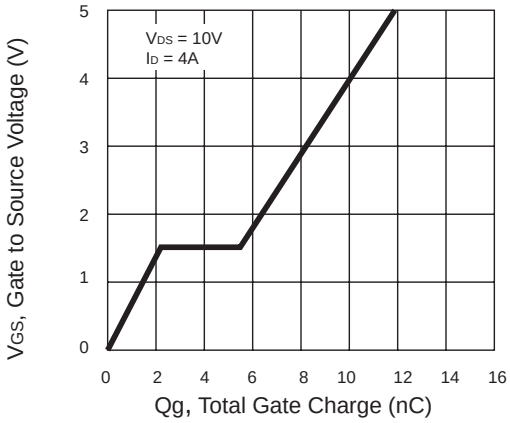


Figure 9. Gate Charge

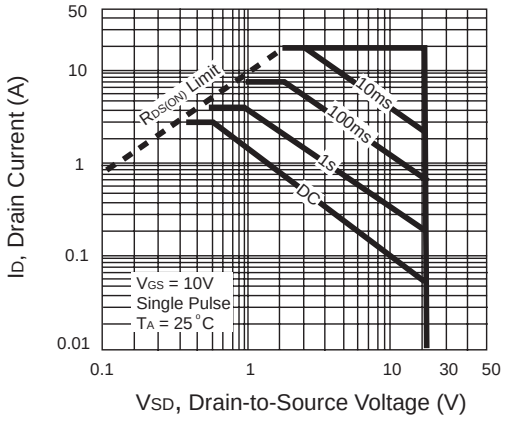


Figure 10. Maximum Safe Operating Area

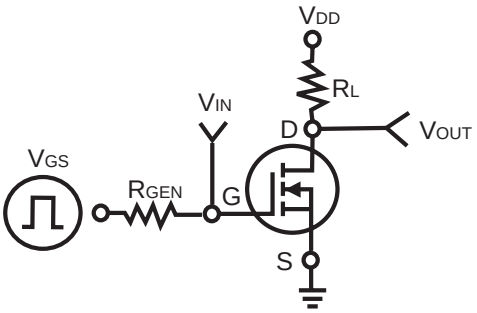


Figure 11. Switching Test Circuit

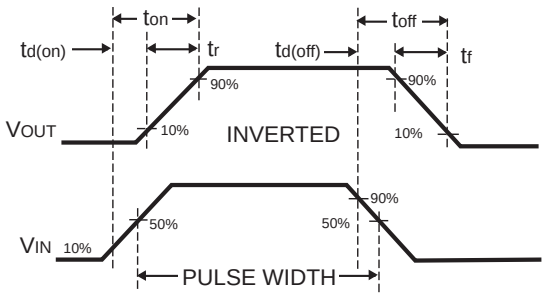


Figure 12. Switching Waveforms

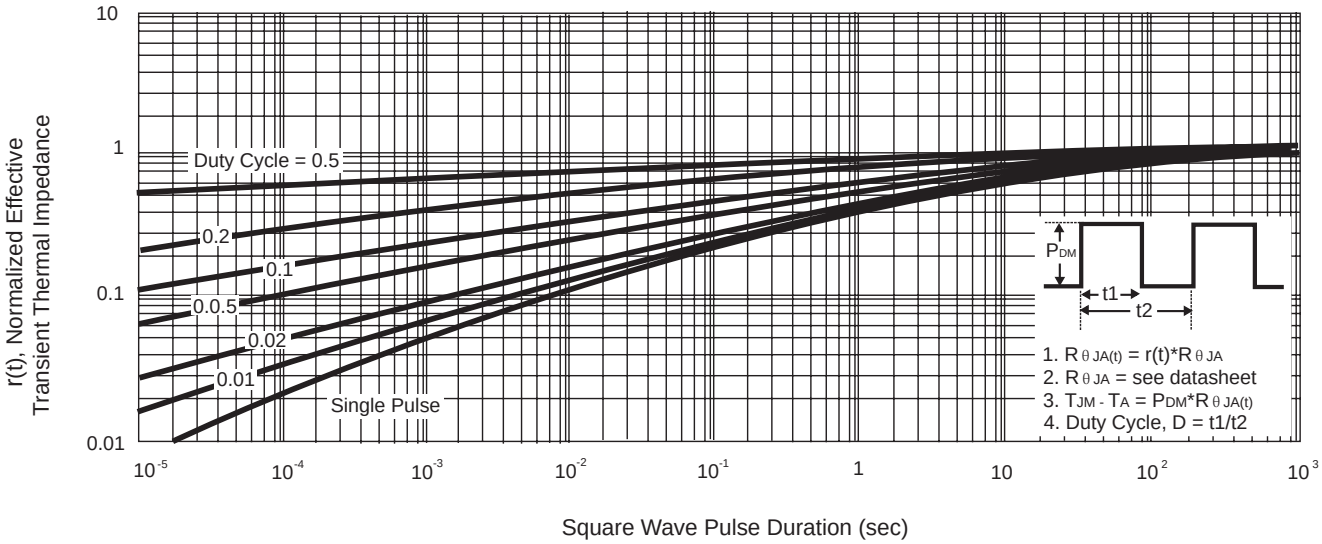


Figure 13. Normalized Thermal Transient Impedance Curve