



SamHop Microelectronics Corp.

**STU/D441S**

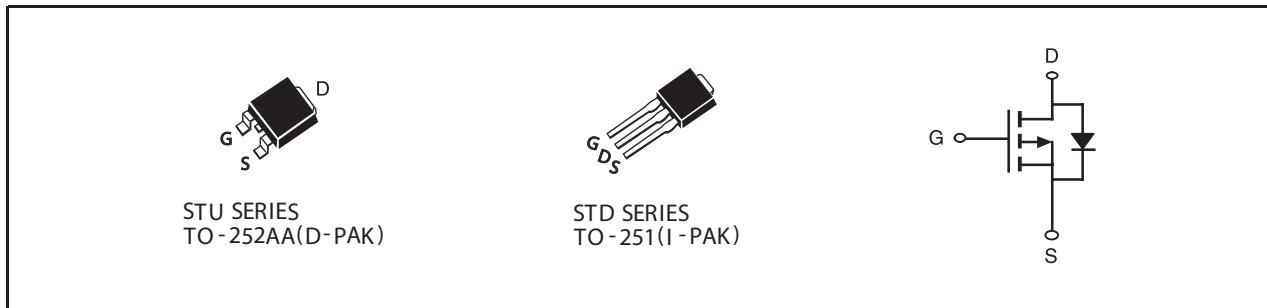
Ver 1.0

## P-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
VDSS	ID	RDS(ON) (mΩ) Max
-40V	-27A	35 @ VGS=10V
		61 @ VGS=4.5V

### FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous <sup>a</sup>	$-27$	A
		$-21.6$	A
$I_{DM}$	-Pulsed <sup>b</sup>	-82	A
$E_{AS}$	Single Pulse Avalanche Energy <sup>d</sup>	49	mJ
$P_D$	Maximum Power Dissipation <sup>a</sup>	42	W
		27	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>a</sup>	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	$^\circ\text{C/W}$

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.9	-3	V
R <sub>D(S(ON))</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-13.5A		28	35	m ohm
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A		45	61	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-13.5A		23		S
<b>DYNAMIC CHARACTERISTICS</b> <sup>c</sup>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V f=1.0MHz		1025		pF
C <sub>OSS</sub>	Output Capacitance			127		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			110		pF
<b>SWITCHING CHARACTERISTICS</b> <sup>c</sup>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-20V I <sub>D</sub> =-1.0A V <sub>GS</sub> =-10V R <sub>GEN</sub> = 6 ohm		18		ns
t <sub>r</sub>	Rise Time			19		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			68		ns
t <sub>f</sub>	Fall Time			25		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-20V, I <sub>D</sub> =-13.5A, V <sub>GS</sub> =-10V		22.5		nC
		V <sub>DS</sub> =-20V, I <sub>D</sub> =-13.5A, V <sub>GS</sub> =-4.5V		10.5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-20V, I <sub>D</sub> =-13.5A, V <sub>GS</sub> =-10V		2.1		nC
Q <sub>gd</sub>	Gate-Drain Charge			6.5		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Forward Current			-2		A
V <sub>SD</sub>	Diode Forward Voltage <sup>b</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> = -2A		-0.8	-1.3	V
<b>Notes</b>						
a. Surface Mounted on FR4 Board, t ≤ 10sec.						
b. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.						
c. Guaranteed by design, not subject to production testing.						
d. Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 20V .(See Figure13)						

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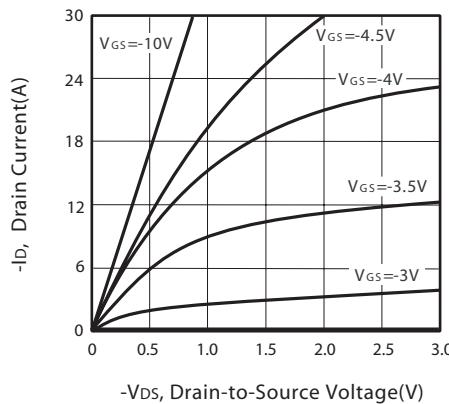


Figure 1. Output Characteristics

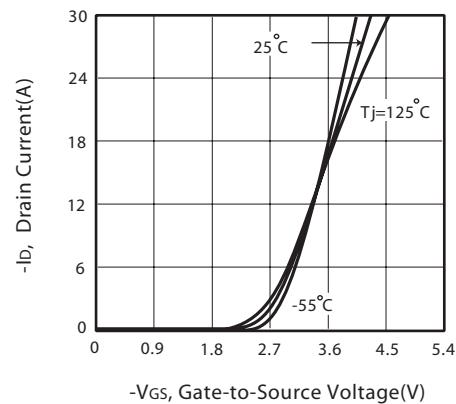


Figure 2. Transfer Characteristics

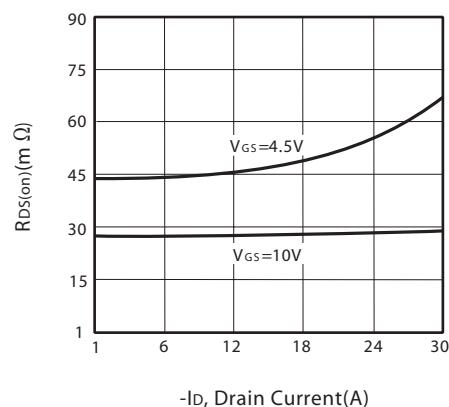


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

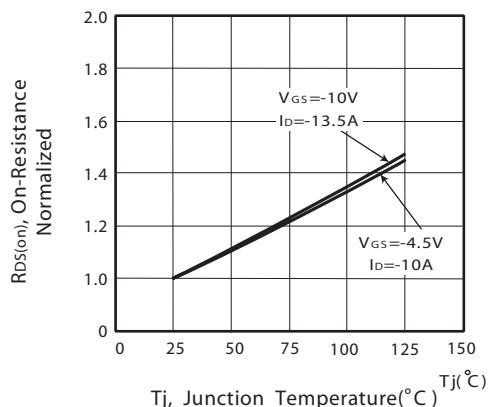


Figure 4. On-Resistance Variation with Drain Current and Temperature

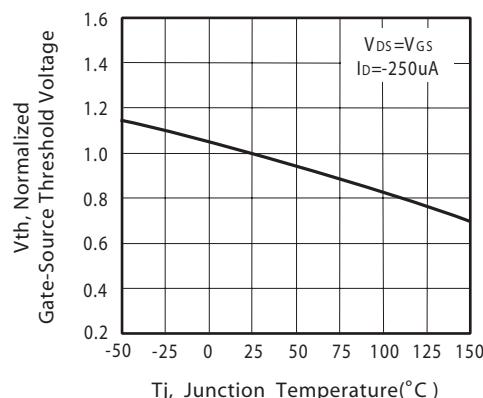


Figure 5. Gate Threshold Variation with Temperature

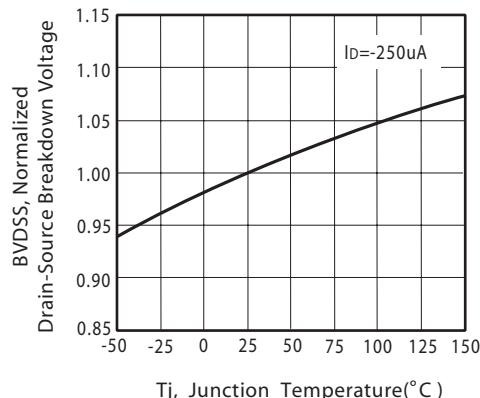


Figure 6. Breakdown Voltage Variation with Temperature

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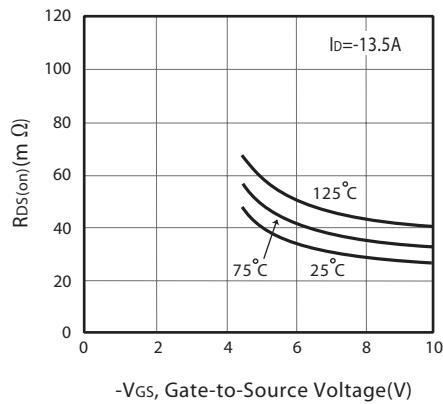


Figure 7. On-Resistance vs.  
Gate-Source Voltage

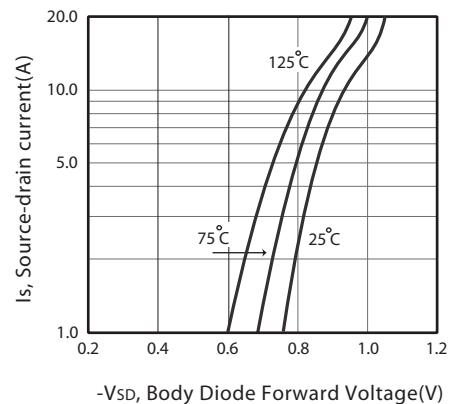


Figure 8. Body Diode Forward Voltage  
Variation with Source Current

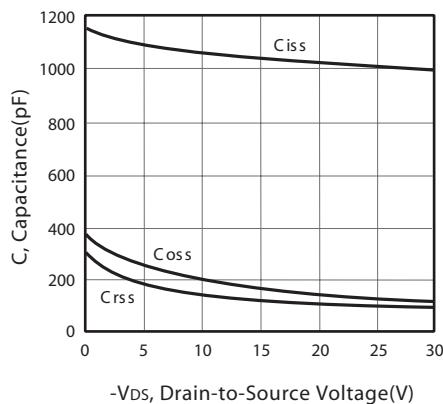


Figure 9. Capacitance

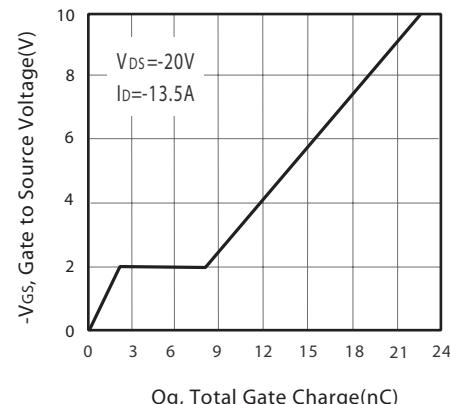


Figure 10. Gate Charge

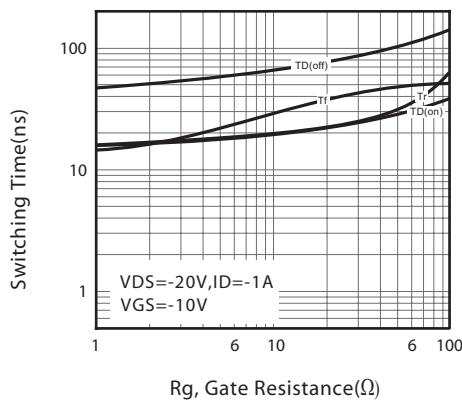


Figure 11. switching characteristics

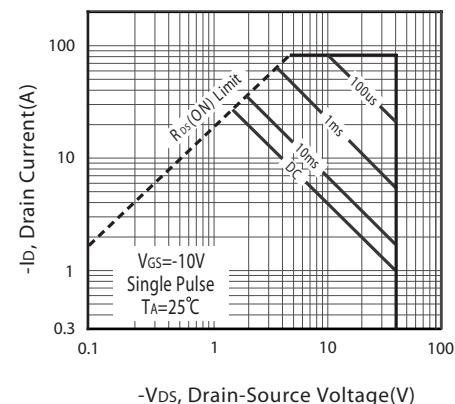
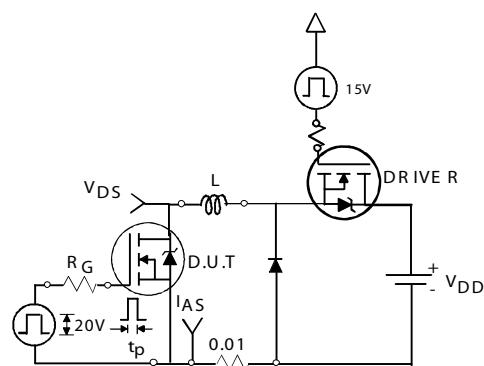


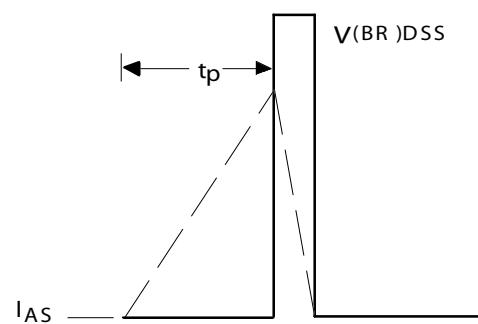
Figure 12. Maximum Safe Operating Area

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Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

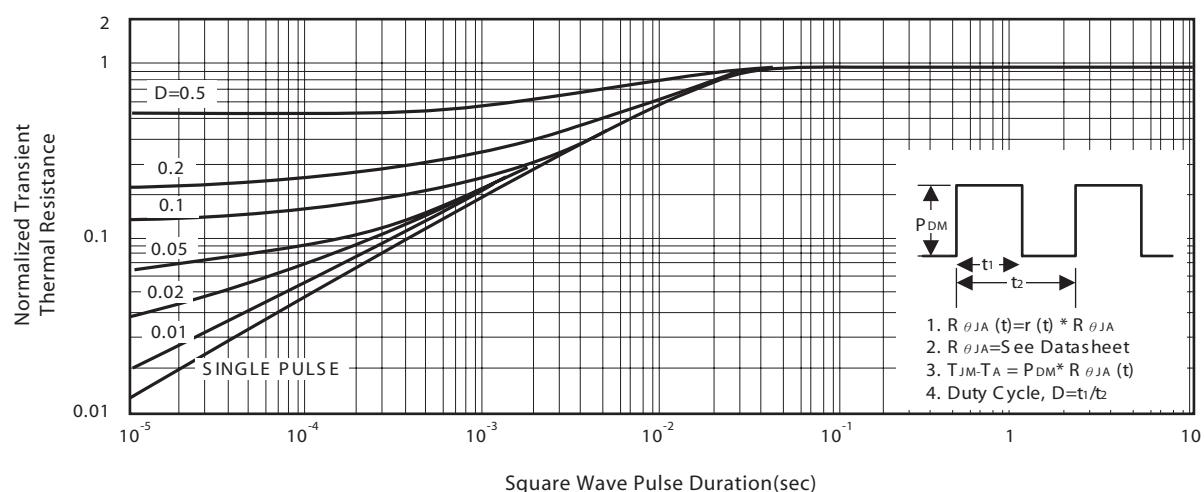
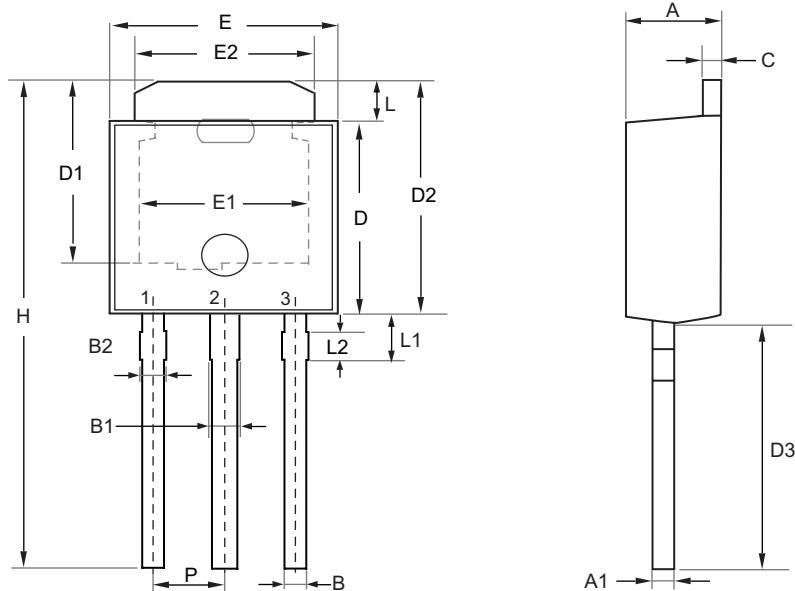


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

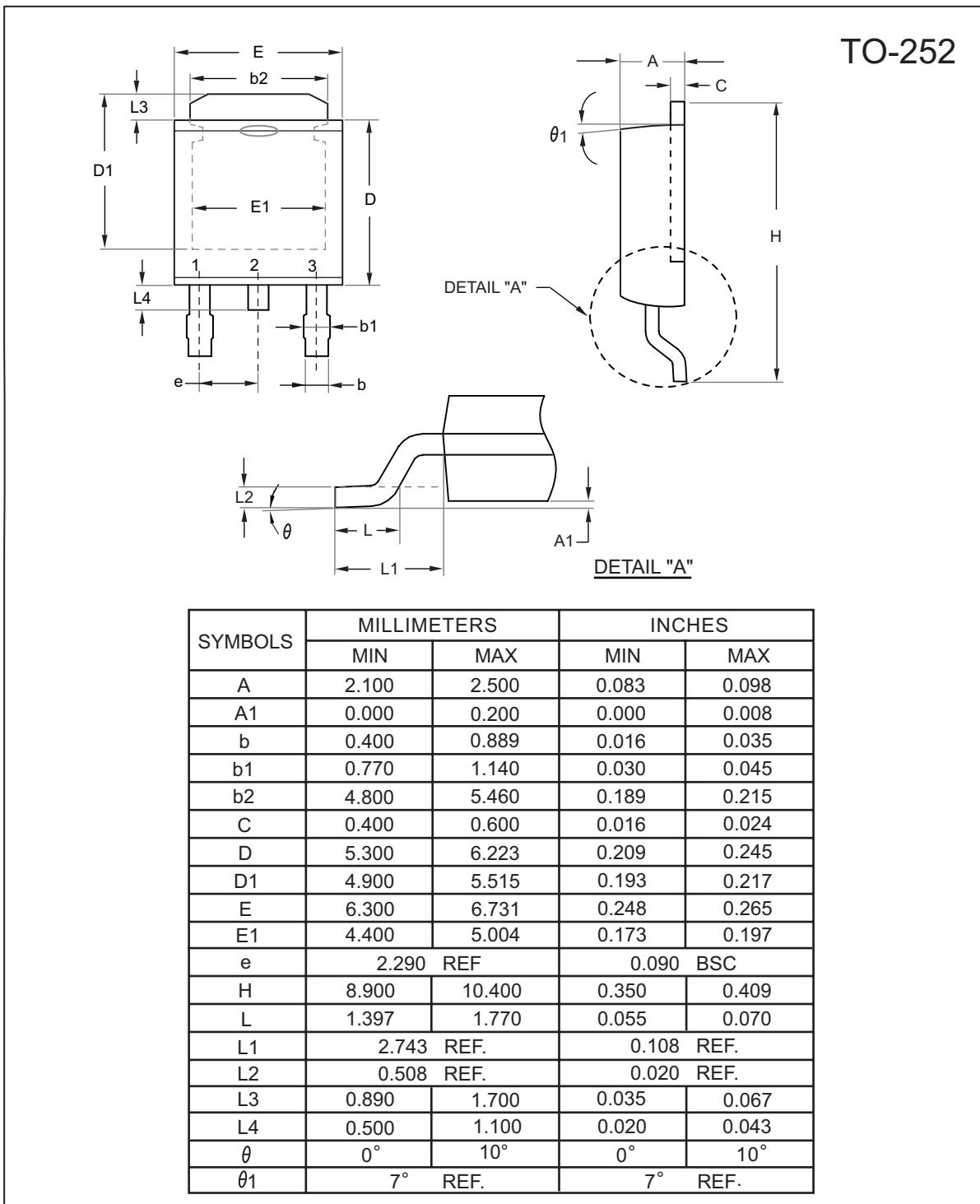
**TO-251**



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.100	2.500	0.083	0.098
A1	0.350	0.650	0.014	0.026
B	0.400	0.800	0.016	0.031
B1	0.650	1.050	0.026	0.041
B2	0.500	0.900	0.020	0.035
C	0.400	0.600	0.016	0.024
D	5.300	5.700	0.209	0.224
D1	4.900	5.300	0.193	0.209
D2	6.700	7.300	0.264	0.287
D3	7.000	8.000	0.276	0.315
H	13.700	15.300	0.539	0.602
E	6.300	6.700	0.248	0.264
E1	4.600	4.900	0.181	0.193
E2	4.800	5.200	0.189	0.205
L	1.300	1.700	0.051	0.067
L1	1.400	1.800	0.055	0.071
L2	0.500	0.900	0.020	0.035
P	2.300 BSC		0.091 BSC	

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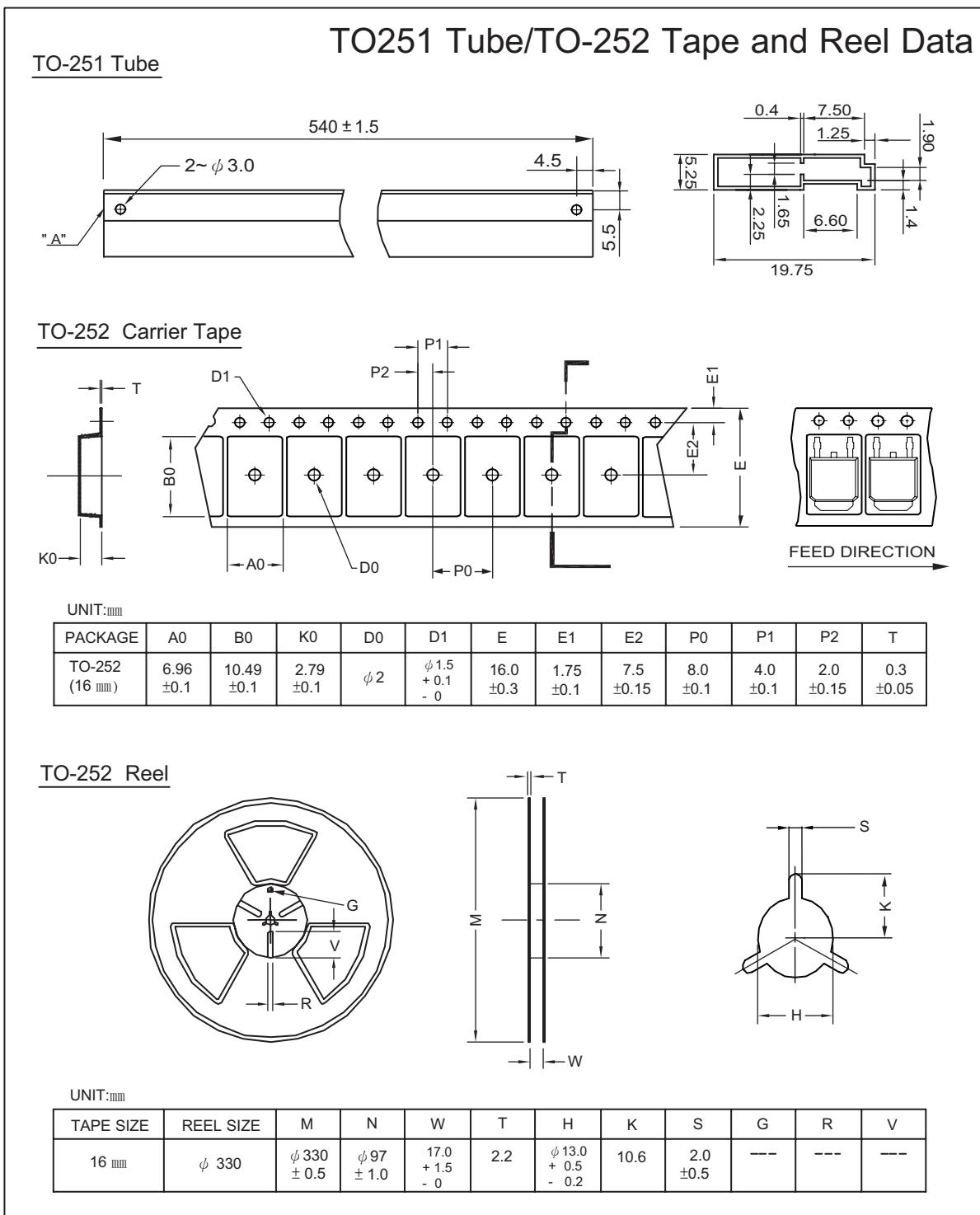
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