

# 74LVC1G74-Q100

Single D-type flip-flop with set and reset; positive edge trigger

Rev. 2 — 14 May 2013

Product data sheet

## 1. General description

The 74LVC1G74-Q100 is a single positive edge triggered D-type flip-flop. It has individual data (D) inputs, clock (CP) inputs, set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) inputs, and complementary Q and  $\overline{Q}$  outputs.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- $\pm 24\text{ mA}$  output drive ( $V_{CC} = 3.0\text{ V}$ )
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G74DP-Q100	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G74DC-Q100	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC1G74GD-Q100	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2

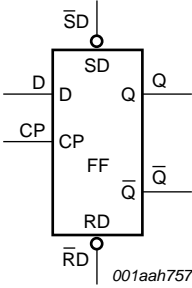
4. Marking

Table 2. Marking codes

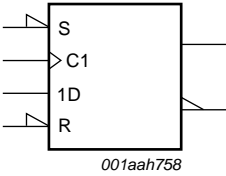
Type number	Marking code <sup>[1]</sup>
74LVC1G74DP-Q100	V74
74LVC1G74DC-Q100	V74
74LVC1G74GD-Q100	V74

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



The logic symbol for the 74LVC1G74-Q100 is a rectangular block. It has two inputs on the left: 'D' and 'CP'. The 'D' input has a bubble, indicating it is active-low. The 'CP' input has a triangle, indicating it is a clock input. On the right, there are two outputs: 'Q' and 'Q-bar'. The 'Q' output has a bubble, indicating it is active-low. At the top, there is an input labeled 'SD' with a bubble, and at the bottom, there is an input labeled 'RD' with a bubble. The text '001aah757' is located below the symbol.



The IEC logic symbol for the 74LVC1G74-Q100 is a rectangular block. It has three inputs on the left: 'S', 'C1', and 'R'. The 'S' and 'R' inputs have bubbles, indicating they are active-low. The 'C1' input has a triangle, indicating it is a clock input. On the right, there are two outputs: 'Q' and 'Q-bar'. The text '001aah758' is located below the symbol.

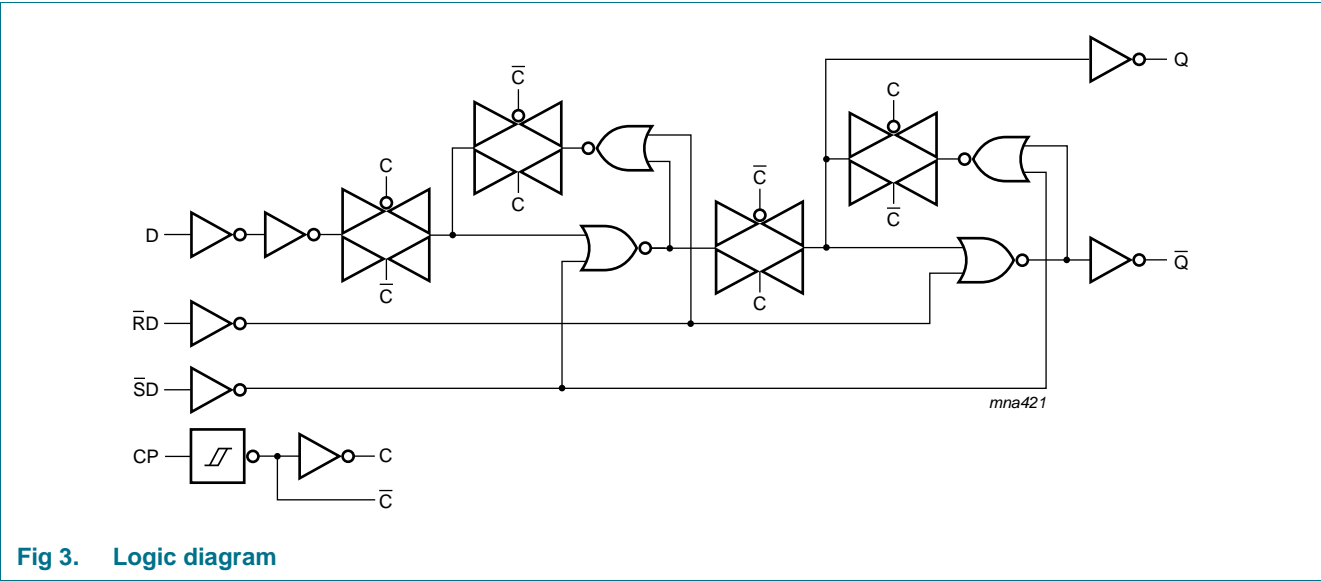


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

74LVC1G74-Q100

CP 1, D 2, Q̄ 3, GND 4, V<sub>CC</sub> 8, SD̄ 7, RD̄ 6, Q 5

aaa-003916

74LVC1G74-Q100

CP 1, D 2, Q̄ 3, GND 4, V<sub>CC</sub> 8, SD̄ 7, RD̄ 6, Q 5

aaa-006258

Transparent top view

Fig 4. Pin configuration SOT505-2 and SOT765-1

Fig 5. Pin configuration SOT996-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
$\overline{Q}$	3	complement output
GND	4	ground (0 V)
Q	5	true output
$\overline{RD}$	6	asynchronous reset-direct input (active LOW)
$\overline{SD}$	7	asynchronous set-direct input (active LOW)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4.** Function table for asynchronous operation<sup>[1]</sup>

Input				Output	
$\overline{\text{SD}}$	$\overline{\text{RD}}$	CP	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

**Table 5.** Function table for synchronous operation<sup>[1]</sup>

Input				Output	
$\overline{\text{SD}}$	$\overline{\text{RD}}$	CP	D	$\text{Q}_{n+1}$	$\overline{\text{Q}}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
 $\text{Q}_{n+1}$  = state after the next LOW-to-HIGH CP transition.

## 8. Limiting values

**Table 6.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{CC}}$	supply voltage		-0.5	+6.5	V
$I_{\text{IK}}$	input clamping current	$V_{\text{I}} < 0 \text{ V}$	-50	-	mA
$V_{\text{I}}$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$I_{\text{OK}}$	output clamping current	$V_{\text{O}} > V_{\text{CC}}$ or $V_{\text{O}} < 0 \text{ V}$	-	±50	mA
$V_{\text{O}}$	output voltage	Active mode	<sup>[1]</sup> -0.5	$V_{\text{CC}} + 0.5$	V
		Power-down mode	<sup>[1][2]</sup> -0.5	+6.5	V
$I_{\text{O}}$	output current	$V_{\text{O}} = 0 \text{ V}$ to $V_{\text{CC}}$	-	±50	mA
$I_{\text{CC}}$	supply current		-	100	mA
$I_{\text{GND}}$	ground current		-100	-	mA
$P_{\text{tot}}$	total power dissipation	$T_{\text{amb}} = -40 \text{ °C}$ to $+125 \text{ °C}$	<sup>[3]</sup> -	300	mW
$T_{\text{stg}}$	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] When  $V_{\text{CC}} = 0 \text{ V}$  (Power-down mode), the output voltage can be 5.5 V in normal operation.  
 [3] For TSSOP8 packages: above 55 °C the value of  $P_{\text{tot}}$  derates linearly with 2.5 mW/K.  
 For VSSOP8 packages: above 110 °C the value of  $P_{\text{tot}}$  derates linearly with 8.0 mW/K.  
 For XSON8 packages: above 118 °C the value of  $P_{\text{tot}}$  derates linearly with 7.8 mW/K.

## 9. Recommended operating conditions

**Table 7. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10. Static characteristics

**Table 8. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	1.54	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	2.15	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.50	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	2.62	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	4.11	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	0.07	0.45	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	0.12	0.30	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.17	0.40	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.33	0.55	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	0.39	0.55	V
$I_I$	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	$\pm 0.1$	$\pm 5$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	$\pm 0.1$	$\pm 10$	$\mu$ A

**Table 8. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$I_{CC}$	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to $5.5\text{ V}$ ; $I_O = 0\text{ A}$	-	0.1	10	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	-	5	500	$\mu\text{A}$
$C_I$	input capacitance		-	4.0	-	pF
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C}</math> to <math>+125\text{ }^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}$ ; $V_{CC} = 1.65\text{ V}$ to $5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}$ ; $V_{CC} = 1.65\text{ V}$	0.95	-	-	V
		$I_O = -8\text{ mA}$ ; $V_{CC} = 2.3\text{ V}$	1.7	-	-	V
		$I_O = -12\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	1.9	-	-	V
		$I_O = -24\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}$ ; $V_{CC} = 1.65\text{ V}$ to $5.5\text{ V}$	-	-	0.10	V
		$I_O = 4\text{ mA}$ ; $V_{CC} = 1.65\text{ V}$	-	-	0.70	V
		$I_O = 8\text{ mA}$ ; $V_{CC} = 2.3\text{ V}$	-	-	0.45	V
		$I_O = 12\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	-	-	0.60	V
		$I_O = 24\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	-	-	0.80	V
$I_I$	input leakage current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 0\text{ V}$ to $5.5\text{ V}$	-	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5\text{ V}$ ; $V_{CC} = 0\text{ V}$	-	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to $5.5\text{ V}$ ; $I_O = 0\text{ A}$	-	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	-	-	5000	$\mu\text{A}$

[1] All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{pd}$	propagation delay	CP to Q, $\bar{Q}$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.0	13.4	1.5	13.4	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.5	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		$\bar{SD}$ to Q, $\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		$\bar{RD}$ to Q, $\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	5.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
$t_w$	pulse width	CP HIGH or LOW; see <a href="#">Figure 6</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.7	1.3	-	2.7	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	ns
		$\bar{SD}$ and $\bar{RD}$ LOW; see <a href="#">Figure 7</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.7	1.6	-	2.7	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	ns

**Table 9. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>rec</sub>	recovery time	$\overline{SD}$ or $\overline{RD}$ ; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns
		V <sub>CC</sub> = 2.7 V	1.3	-	-	1.3	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	+1.2	–3.0	-	+1.2	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
t <sub>su</sub>	set-up time	D to CP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V <sub>CC</sub> = 2.7 V	1.7	-	-	1.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns
t <sub>h</sub>	hold time	D to CP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	-	-	1.0	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	-	-	1.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0.6	-	1.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
f <sub>max</sub>	maximum frequency	CP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	80	-	-	80	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	175	280	-	175	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V	<sup>[3]</sup>	-	15	-	-	pF

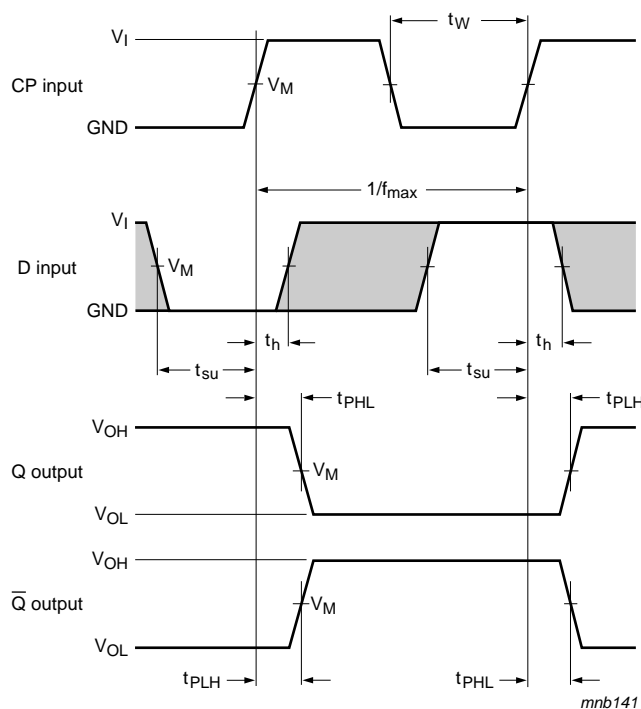
[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:f<sub>i</sub> = input frequency in MHz;f<sub>o</sub> = output frequency in MHz;C<sub>L</sub> = output load capacitance in pF;V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.



## 12. Waveforms



Measurement points are given in [Table 10](#).

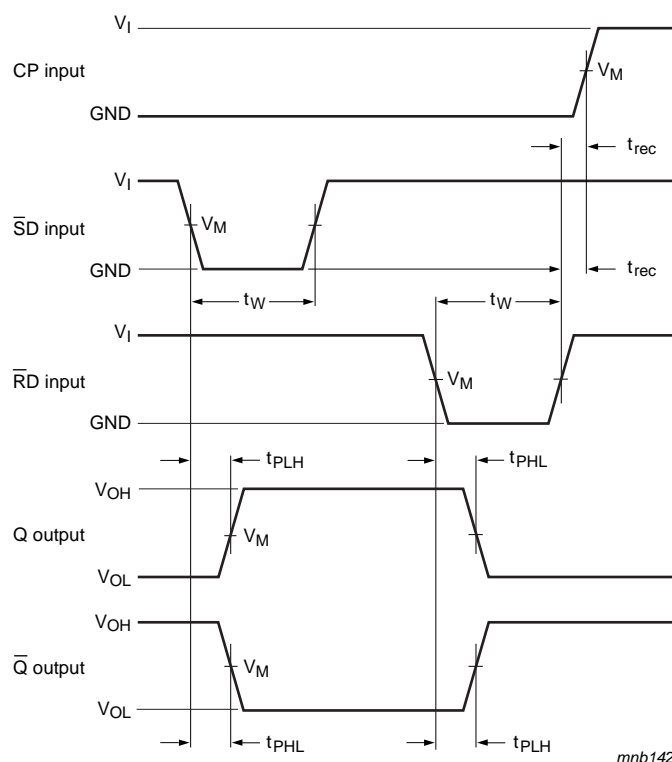
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6.** The clock input (CP) to output (Q,  $\bar{Q}$ ) propagation delays and pulse width, D to CP set-up, CP to D hold times and the maximum frequency

**Table 10.** Measurement points

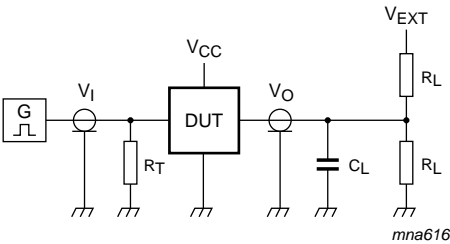
Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in [Table 10](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7.** The set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) input to output (Q,  $\overline{Q}$ ) propagation delays, pulse widths and the  $\overline{RD}$  to CP recovery time



Test data is given in [Table 11](#).  
Definitions for test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V <sub>CC</sub>	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm    SOT505-2

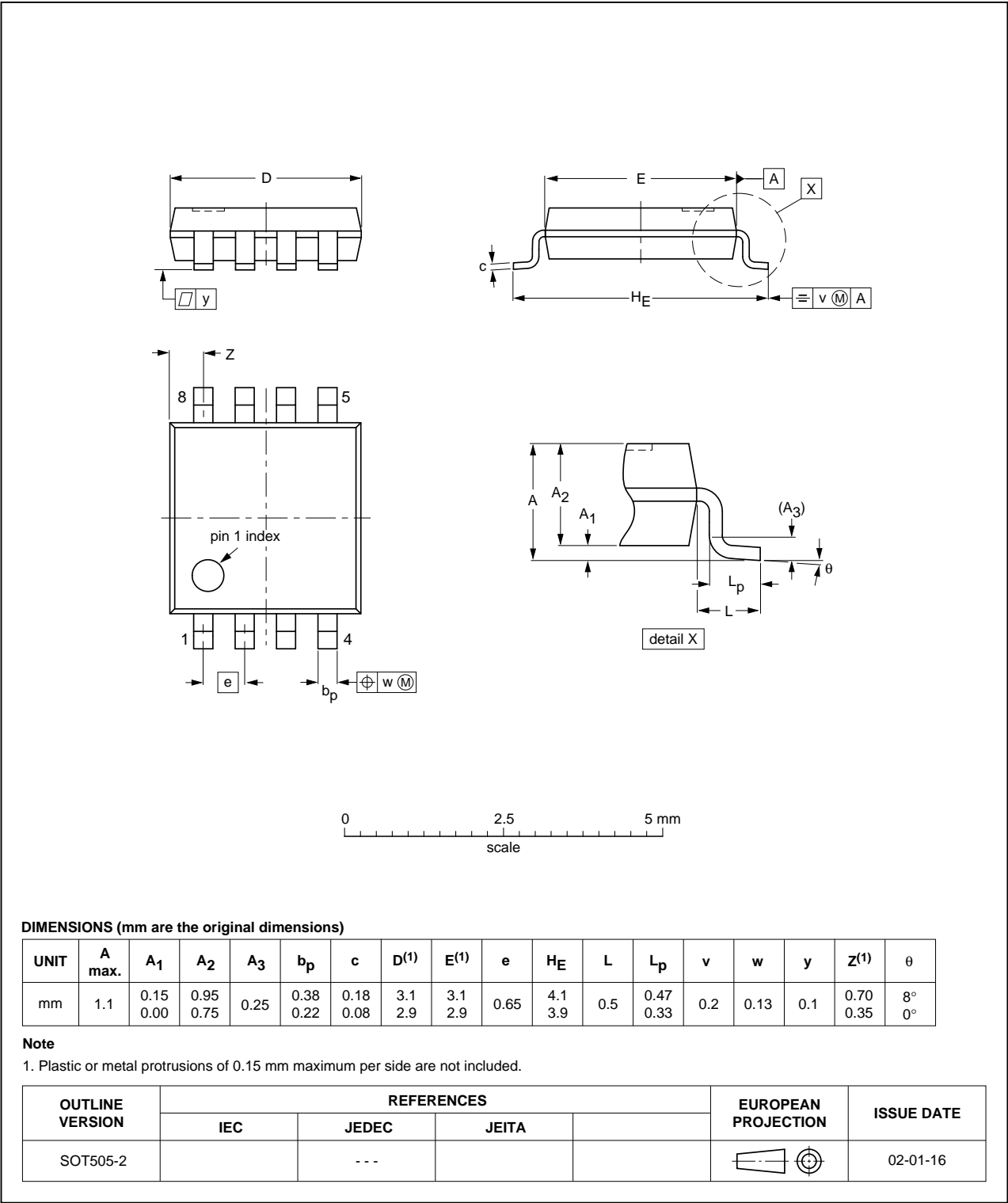


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

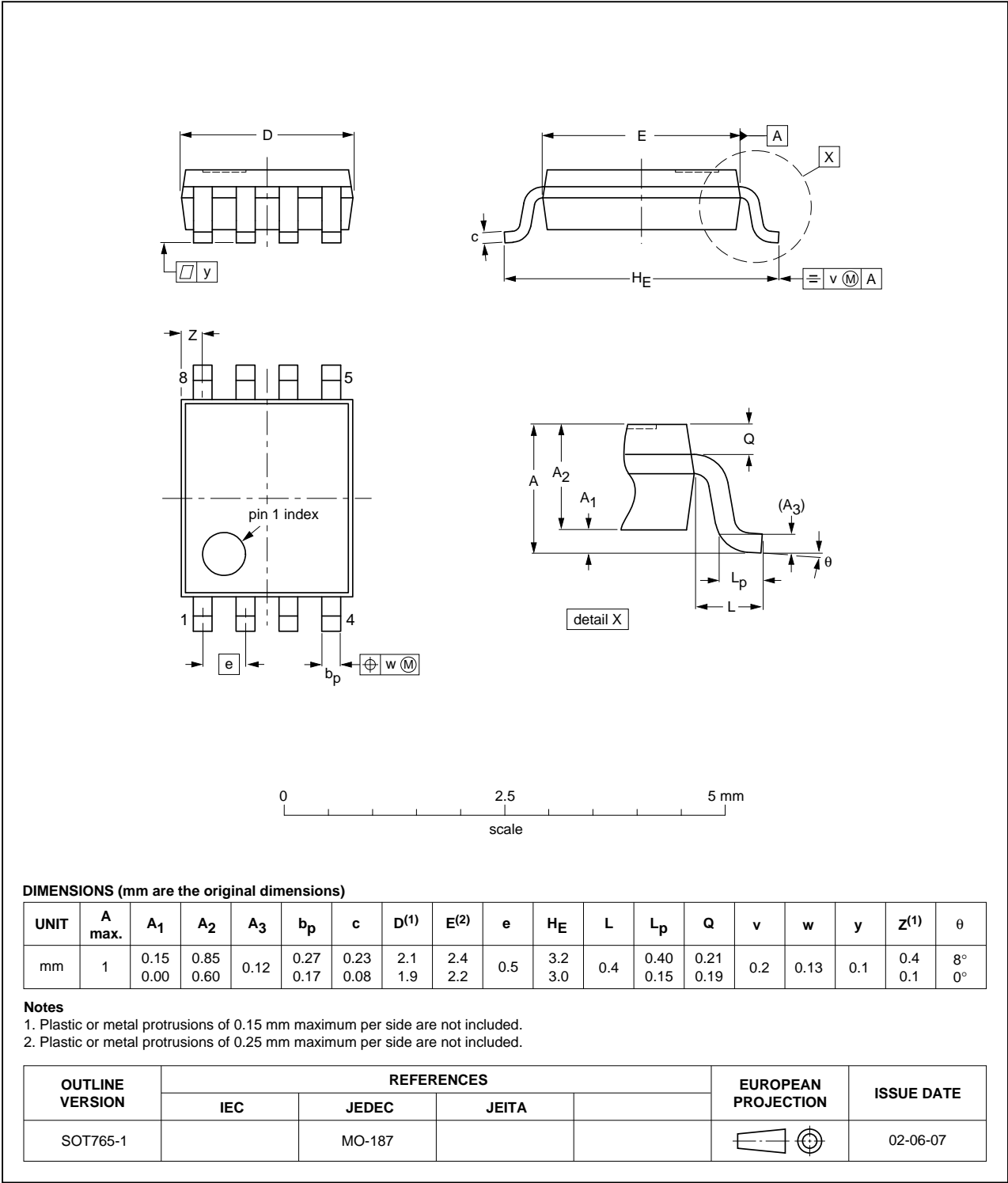


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;  
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

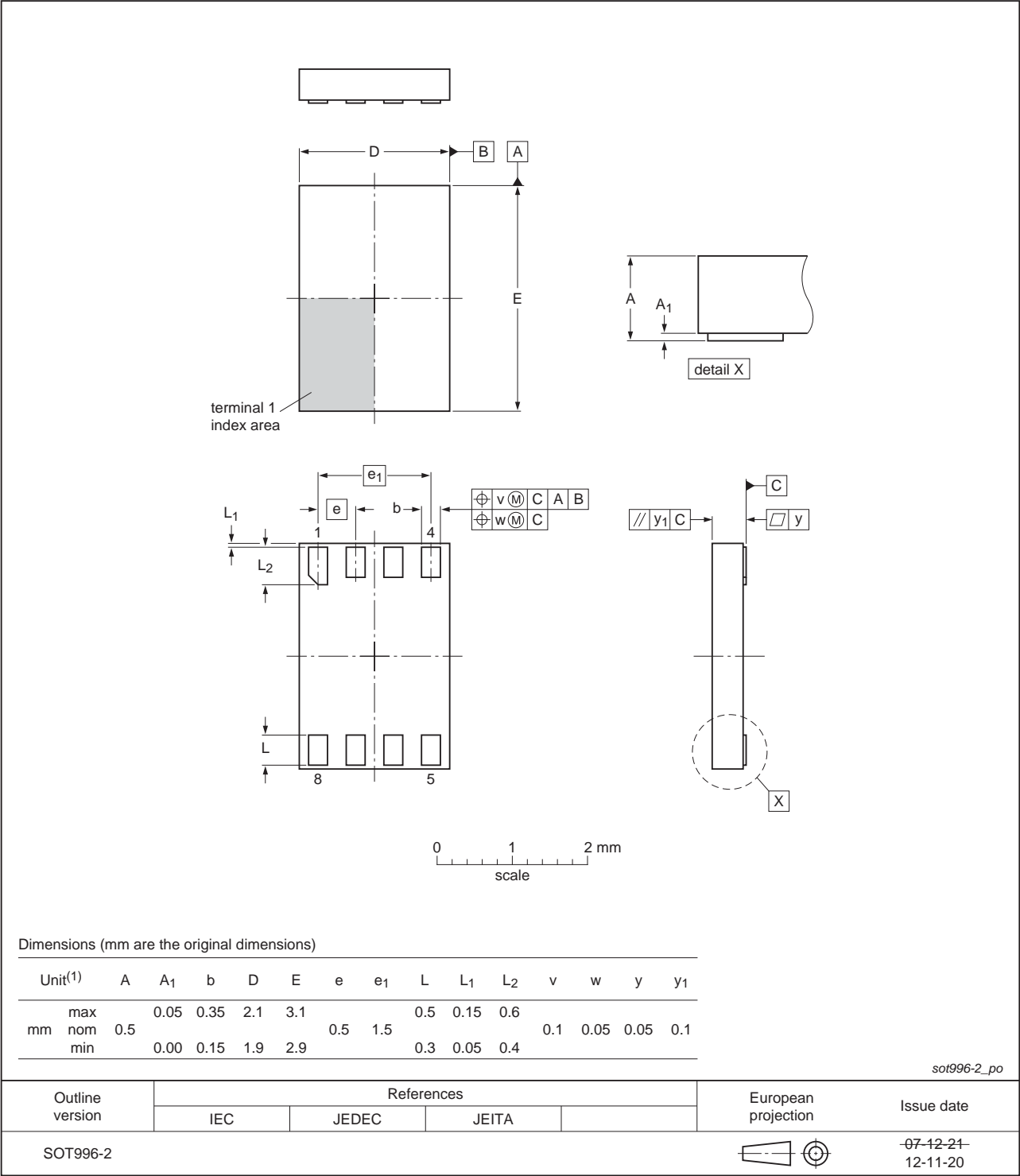


Fig 11. Package outline SOT996-2 (XSON8)

## 14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test
TTL	Transistor-Transistor Logic
MIL	Military

## 15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G74_Q100 v.2	20130514	Product data sheet	-	74LVC1G74_Q100 v.1
Modifications:	• 74LVC1G74GD-Q100 (XSON8) added.			
74LVC1G74_Q100 v.1	20120807	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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