AN7292NSC, AN7292NFBP

FM-IF, Detector, Noise Canceler, MPX Demodulator IC

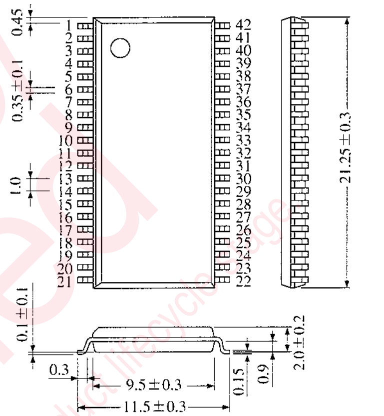
■ Overview

The AN7292NSC and AN7292NFBP are ICs, incorporating FM-IF/Det. for car radio, PNL, MPX section into a single chip. The SD and frequency band mute function are added to their basic-construction same as of the AN7291SC/FBP and they have also some improved temperature characteristics.

■ Features

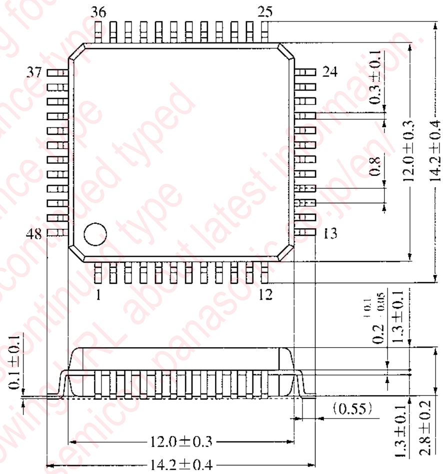
- Functions conventionally separated in two chips (IF/Det., PNL/MPX) incorporated into a single chip
- High IF sensitivity
- With IF counter output, SD output, SEEK sensitivity adjuster
- Adjustment-free VCO (Ceramic lock 912kHz)
- Fewer external components required (fewer capacitors with large capacitance)
- Good linearity of control voltage and wide adjustable range
- Amp. for multipath detection built-in
- Frequency band mute function

AN7292NSC Unit : mm



42-Lead SOP Package (SSOP042-P-0450A)

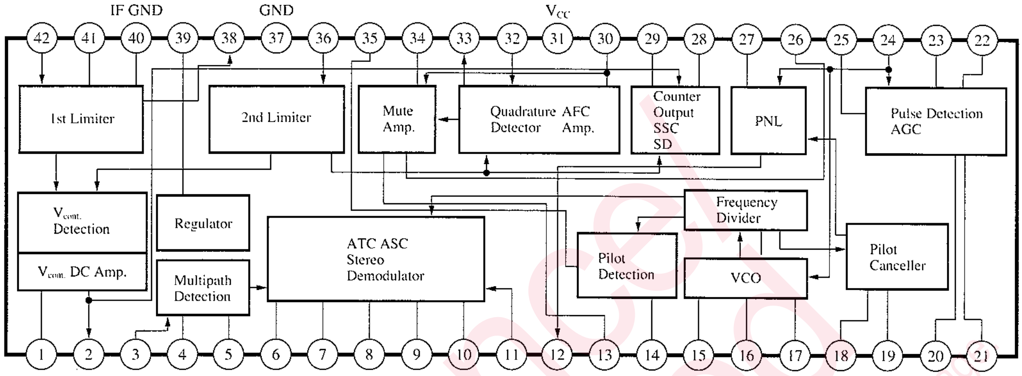
AN7292NFBP Unit : mm



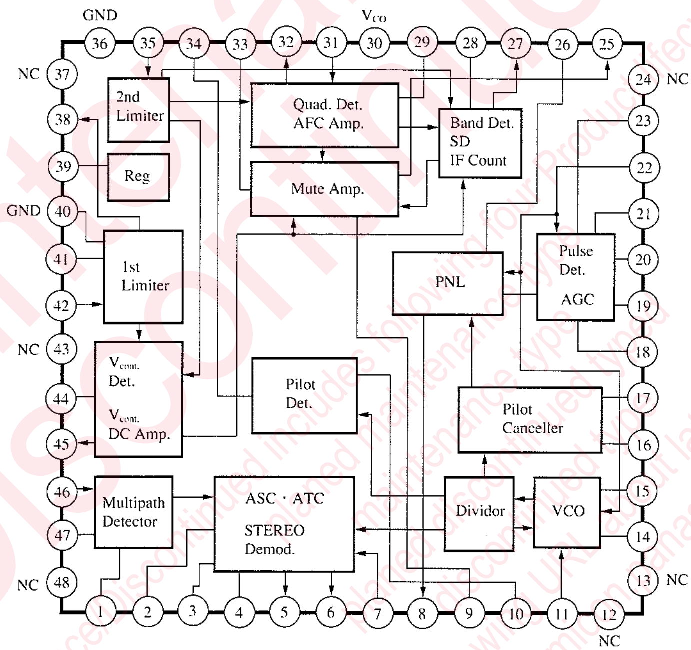
48-Lead QFH Package (QFH048-P-1212)

■Block Diagram

AN7292NSC



AN7292NFBP



■ Pin No. Correspondence Table

AN7292NSC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AN7292NFBP	44	45	46	47	1	2	3	4	5	6	7	8	9	10	11	14	15	16	17	18	19
AN7292NSC	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
AN7292NFBP	20	21	22	23	25	26	27	28	29	30	31	32	33	34	35	36	38	39	40	41	42

*Pin 12,13,24,37,43 and 48 of the AN7292NFBP are NC.

■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	9.6	V
Supply Current	I_{CC}	43	mA
Power Dissipation (Ta=75℃)	P_D	787 Note1)/670 Note2)	mW
Operating Ambient Temperature	T_{opr}	−30～+80	℃
Storage Temperature	T_{stg}	−55～+125	℃

Note1) AN7292NSC Note2) AN7292NFBP

ICs for Tuner

■ Recommended Operating Range (Ta = 25℃)

Parameter	Symbol	Range
Operating Supply Voltage Range	V_{CC}	7.2V ~ 9.6V

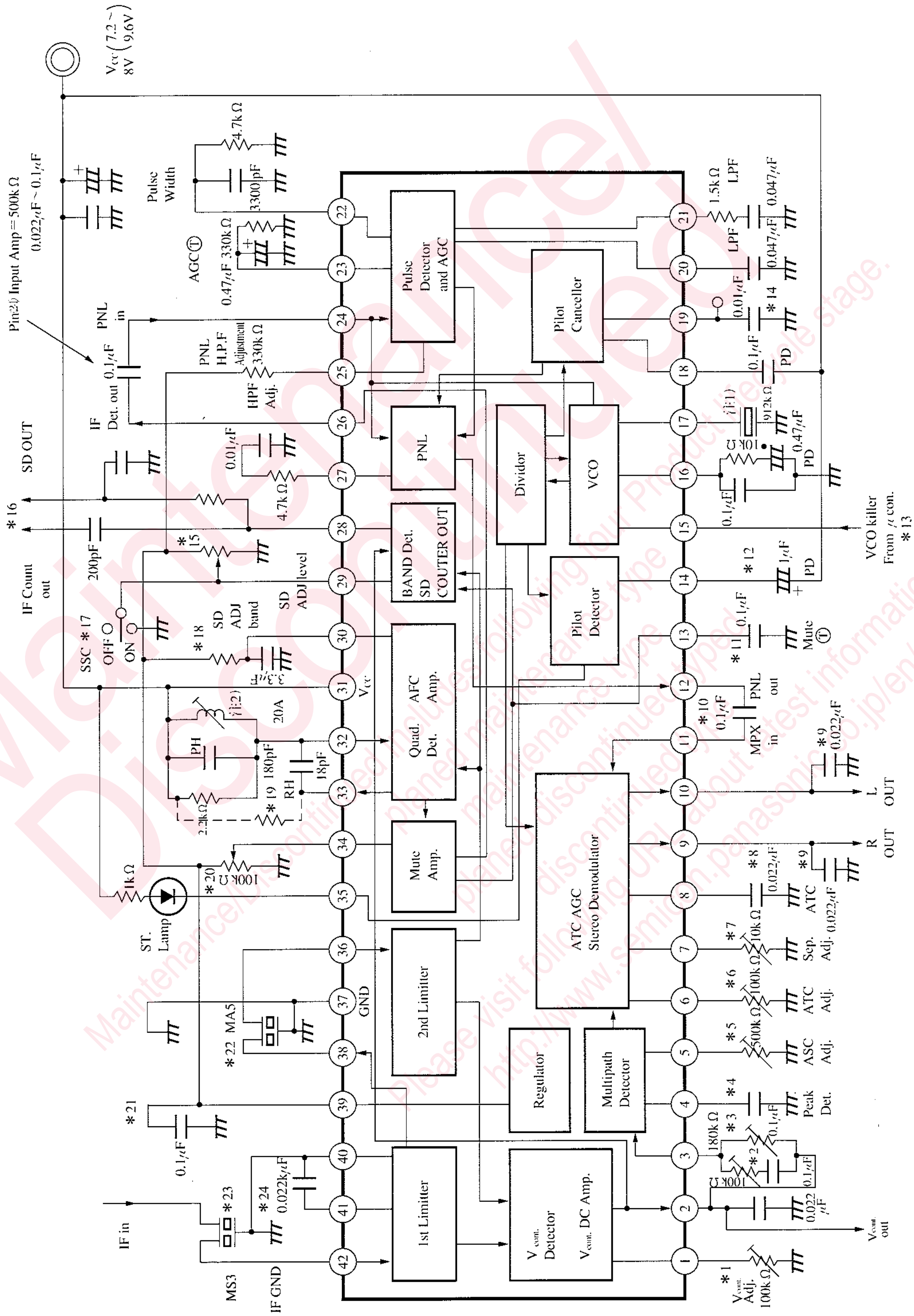
* Pin numbers used below are for the AN7292NSC. For the AN7292NFBP, refer to Pin No. Correspondence Table.

■ Electrical Characteristics (V_{CC} = 8V, f_{in} = 10.7MHz, $f_{Mod.}$ = 1kHz 30%FM, Ta = 25℃)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Control Voltage (1)	V_{C1}	No input, Pin② DC voltage	0.1	0.5	0.9	V
Control Voltage (2)	V_{C2}	V_{in} = 40dBμ, Pin② DC voltage	1.05	1.50	1.95	V
Control Voltage (3)	V_{C3}	V_{in} = 70dBμ, Pin② DC voltage	2.55	3.25	3.95	V
Control Voltage (4)	V_{C4}	V_{in} = 100dBμ, Pin② DC voltage	4.15	5.10	5.95	V
Control Voltage (5)	V_{C5}	$V_{C5} = V_{C3} - V_{C2}$	1.55	1.75	1.95	V
Control Voltage (6)	V_{C6}	$V_{C6} = V_{C4} - V_{C3}$	1.65	1.85	2.05	V
AFC Offset Voltage	V_{AFC}	No signal input, DC voltage between Pin㉚ and ㊴	−0.065	0	0.065	V
Output Level L	V_{OL}	V_{in} = 70dBμ, Pin⑩ AC voltage	105	125	145	mVrms
Output Level R	V_{OR}	V_{in} = 70dBμ, Pin⑨ AC voltage	105	125	145	mVrms
Channel Balance	CB	CB = 20log (V_{OL}/V_{OR})	−1	0	1	dB
Limiting Sensitivity	V_{lim}	V_{OL} = 0dB, Input level at which input Pin⑩ AC voltage decreases by 3dB	18	24	28	dBμV
Residual Pilot Voltage	V_{PC}	V_{in} = 70dBμ, Pilot signal 10% modulation, Pin⑫ AC voltage	—	7	14	mVrms
Stereo Lamp ON Level	Lamp (ON)	Modulation only by pilot signal. Pin㉟ DC voltage < 2V	2.0	4.7	6.3	%
Stereo Lamp OFF Level	Lamp (OFF)	Modulation only by pilot signal. Stereo lamp ON/OFF level ratio	2	4.5	7	dB
Separation Lch	Sep. L	V_{in} = 70dBμ, L+R = 90% Pilot 10%	22	35	—	dB
Separation Rch	Sep. R	V_{in} = 70dBμ, L+R = 90% Pilot 10%	22	35	—	dB
Capture range	CR	V_{in} = 70dBμ, Pilot signal 8% modulation	±0.45	±1	—	%
Counter Output Level (1)	V_{IF1}	V_{in} = 70dBμ, Pin㉙ = 0V, Pin㉘ 10.7MHz output voltage	0	1	5	mVrms
Counter Output Level (2)	V_{IF2}	V_{in} = 70dBμ, Pin㉙ = V_{CC}, Pin㉘ AC output voltage	50	65	80	mVrms
Supply Current	I_{tot}	No input, Pin⑮ = 0V	29.5	36.5	43.5	mA
Monaural THD (Lch)	THDL	Monaural input 400mV, 1kHz, Lch distortion	—	0.15	0.3	%
Monaural THD (Rch)	THDR	Monaural input 400mV, 1kHz, Rch distortion	—	0.15	0.3	%
Stereo THD (Lch)	THD SL	Stereo, L+R = 360mV, V_P = 40mV, Lch distortion	—	0.15	0.3	%
Stereo THD (Rch)	THD SR	Stereo, L+R = 360mV, V_P = 40mV, Rch distortion	—	0.15	0.3	%
AGC Voltage (1)	V_{AGC1}	Input = 0mVrms, R_S = 600Ω, Pin㉓ DC voltage	—	0	0.4	V
AGC Voltage (2)	V_{AGC2}	Input V_{in2} = 2mVrms, 150kHz, Pin㉓ DC voltage	1.3	1.48	1.65	V
Noise Detection Voltage	V_{DET}	V_{in2} = 100mVrms, 150kHz, Pin㉒ DC voltage	—	0	0.3	V
Gate Pulse Width	PW	V_{in2} = 0.3V_{P-P}, tw = 1μs f = 1kHz, Pin⑫ output	23	28	33	μs
Residual Noise Voltage	V_{NR}	V_{in2} = 1V_{P-P}, tw = 10μs, f = 1kHz, Input through LPF, Lch output	—	0	0.7	mVrms
SD Frequency Band Width	SDW	Frequency band width when SD output is 4.5V or more (V29 = 2V)	60	100	140	kHz
SD Sensitivity	SDS	Input when SD output is 4.5V or more (V29 = 2V)	38	44	56	dBμ

■ Application Circuit

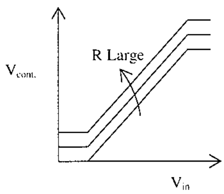
AN7292NSC



Note 1) Ceramic CSB912JF101 (Murata Seisakusyo)
Note 2) IFT ZIF−5EB020A (Matsushita)

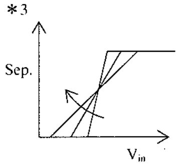
■ Description on Pins Show in the Diagram of the Application Circuit

*1



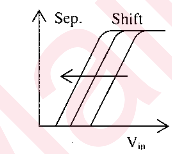
*2 HPF for multipath detection
Too low fc decreases Sep.
at high modulation

*3

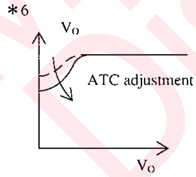


*4 Capacitor for S-meter detection 0.1 to 1μF
at multipath detection

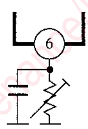
*5



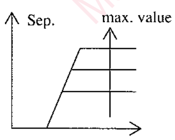
*6



Insert C if noise is
conspicuous.



*7

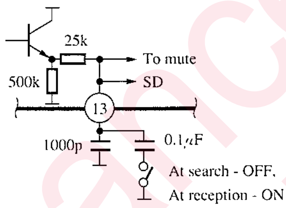


*8 f (time) setting at ATC ON

*9 75μs for de-emphasis

*10 Pin ⑪ input Amp. =400k Ω
0.1μ is min.
The larger the better

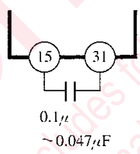
*11 ① Soft mute time constant setting
② SD rise time constant



*12 For pilot detection
If small, lamp on,
malfunction

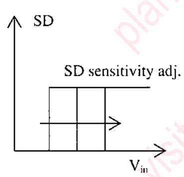
*13 $3.9V < V_{15} < V_{CC}$ ··· V_{CO} stop
$1.7V < V_{15} < 3.2V$ ··· Forced monaural
$0V < V_{15} < 1.0V$ ··· Stereo mode

· When Pin ⑮ is not used, preferably
insert C between V_{CC}.



*14 For pilot canceler
Pseudo sine wave output : c=6800pF to 0.015μF

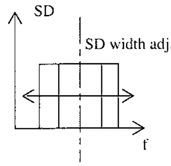
*15



*16 IF counter output (Keep it away from input)

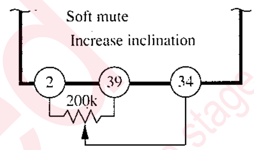
*17 $V_{29} < 0.2V$ ··· IF counter OFF
$V_{29} > 1V$ ··· IF counter ON

*18

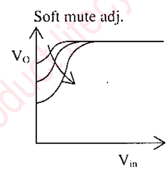


*19 Several k Ω THD improved

*20



*21

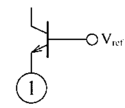
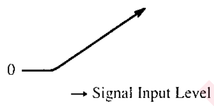
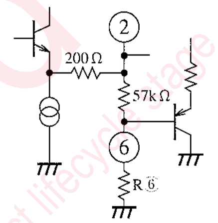
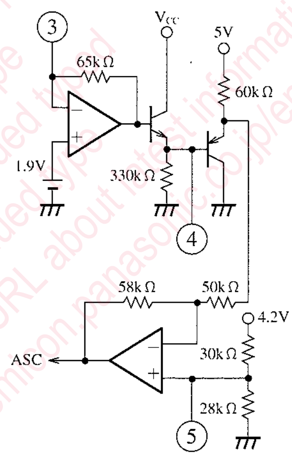
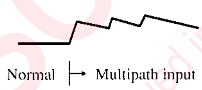
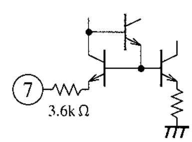


*22 Regulator by-pass
(Pay attention to GND location)

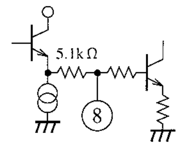
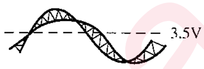
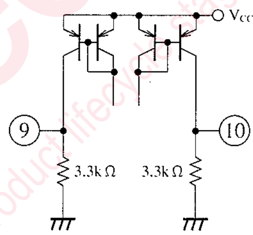
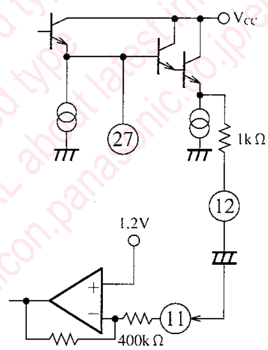
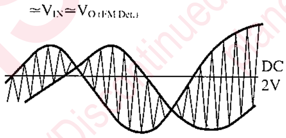
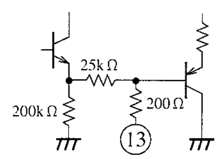
*23 Change to applications.

*24 1st limiter bypass
(Pay attention to GND location)

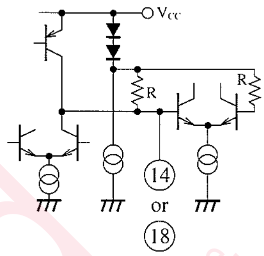
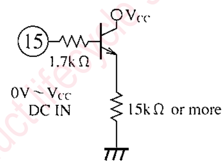
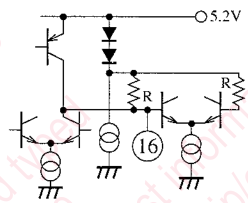
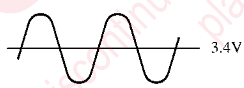
■ Pin Description (AN7292NSC)

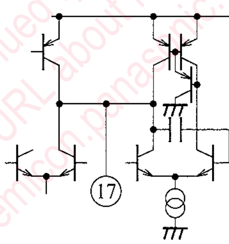
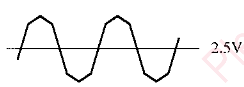
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
1	$V_{CONT.}$ Adj.	DC≃3.5V	Low	
2	$V_{CONT.}$ OUT (Level Meter)		200 Ω	
6	ATC Adj.	$V_6 = \frac{R_6}{57k\Omega + R_6} V_2$	57k Ω	
3	AMDC IN	DC about 1.9V	Low	
4	AMDC Peak Det.		Rise Low Fall 330k Ω	
5	AMDC Adj.	DC about 2.3V or less	14.5k Ω	
	NOTE) AMDC: Automatic Multi Path Distortion Canceller			
7	Separation Adj.	DC (max.)≃1.2V AC=0∼V_{11}	2k Ω	

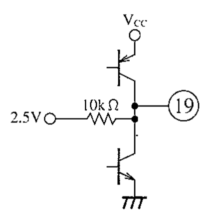
■ Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
8	ATC L. P. F	Same as V_{11}, however level of high frequency band down by external capacitor $V_{(DC)} \simeq 2V$	5.1kΩ	
9	L-ch. OUT	AC varies with input condition. 	3.3kΩ	
10	R-ch. OUT	AC varies with input condition. 	3.3kΩ	
11	MPX. IN	AC : Same as for Pin⑫ DC = 1.3V	400kΩ	
12	NC. OUT		1kΩ	
27	NC. Hold	$V_{(AC)} \simeq V_{12}$ $V_{(DC)} \simeq 3.3V$	Low	
13	Soft Mute Time Const.	DC≃0V ~ 4.1V	25kΩ	

■ Pin Description (Cont.) (AN7292NSC)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Pin Waveform, Voltage</th><th>I/O Impedance</th><th>Equivalent Circuit</th></tr>
<tr><td>14</td><td>Pilot Det.
L. P. F</td><td>DC≃V_{CC} − 1.4V</td><td>R = 36kΩ</td><td rowspan="2">
</td></tr>
<tr><td>18</td><td>Pi. Can.
Control
L. P. F</td><td>DC≃V_{CC} − 1.4V</td><td>R = 68kΩ</td></tr>
<tr><td>15</td><td>ST/Mono.
Control</td><td><table><tr><th>Pin Voltage</th><th>Demo-dulation</th><th>LED</th><th>Pilot Can.</th><th>VCO</th></tr><tr><td>0V ~ 1V</td><td>○</td><td>○</td><td>○</td><td>○</td></tr><tr><td>1.7V ~ 3.2V</td><td>×</td><td>×</td><td>○</td><td>○</td></tr><tr><td>3.9V ~ V_{CC}</td><td>×</td><td>×</td><td>×</td><td>×</td></tr></table></td><td>High</td><td>
</td></tr>
<tr><td>16</td><td>PLL
L. P. F</td><td>DC≃4.3V</td><td>R = 66kΩ</td><td>
</td></tr>
<tr><td>17</td><td>VCO
(Ceramic
resonator Pin)</td><td>

f = 912kHz
AC≃3V_{P-P}</td><td>High</td><td>
</td></tr>
<tr><td>19</td><td>Pi. Can.
Quasi − sin</td><td>

f = 19kHz
AC≃100mV_{P-P}</td><td>—</td><td>
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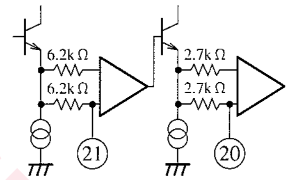
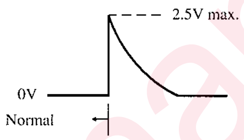
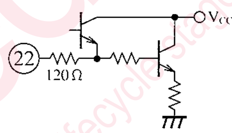
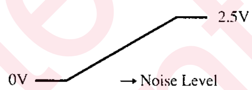
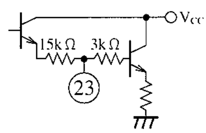
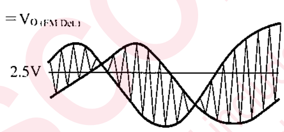
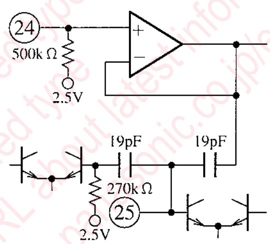
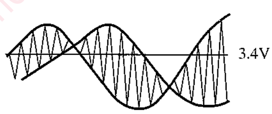
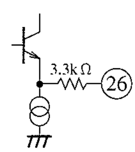
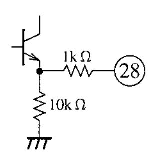
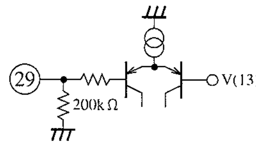
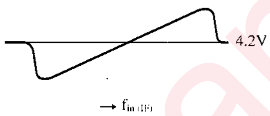
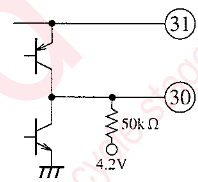
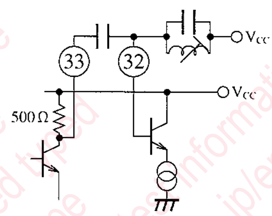
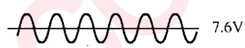
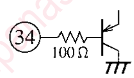
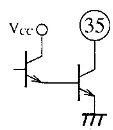
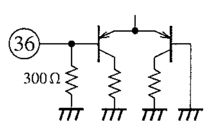
■ Pin Description (Cont.) (AN7292NSC)

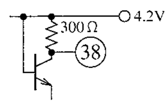
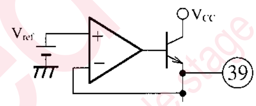
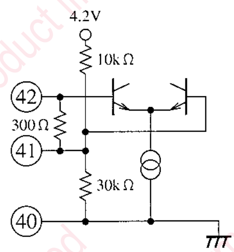
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
20	AGC Amp. L. P. F	DC≃3.5V AC is noise.	6.2kΩ	
21	Pulse Amp. L. P. F	DC≃4.2V AC is noise.	2.7kΩ	
22	Gate Time Adj.		Usually High Low at Operation	
23	Noise Amp. AGC		10 Rise 15kΩ Fall High	
24	NC IN		500kΩ	
25	NC H. P. F	Level of low frequency band down from Pin㉔ waveform. DC is determined by external voltage (4.2V).	High	
26	IF Det. OUT	 (Varies with input conditions)	3.3kΩ	
28	IF Count Out SD Out	DC≒5V (at tuning) ≒0V (at detuning) 10.7MHz when DC≒5V	1kΩ	

■ Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
29	SCC (Seek Sence. Adj.)	Apply bias voltage from outside. IF counter stops when V29< 0.3V, SD=L fixed	200k Ω	
30	AFC OUT		50k Ω	
31	V_{CC}	8V	Low	————
32	Quad. IN	DC=8V (Determined by external voltage) <90 phase shift	High	
33	Limitter OUT		500 Ω	
34	Soft Mute Adj.	Voltage input from outside 0V ~ V_{ref} (4.2V)	High	
35	LED Driver	At stereo DC=0V ~ 0.5V At monaural Determined by external voltage	Low High	
36	2nd IF IN	≃0V	300 Ω	

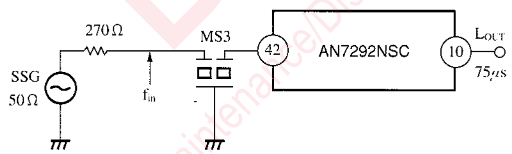
ICs for Tuner

■ Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
37	System GND	0V	Low	———
38	IF1 Limitter OUT	4V, f=10.7MHz	300Ω	
39	V_{ref}	4.2V constant voltage	Low	
40	IF GND	———	Low	
41	IF Amp. Bypass	DC=3.1V	7.5kΩ	
42	IF IN	DC=3.1V AC=$V_{in(IF)}$	300Ω	

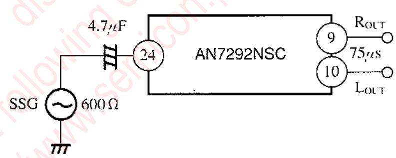
■ Characteristic Curve

①Measuring Condition at IF Input



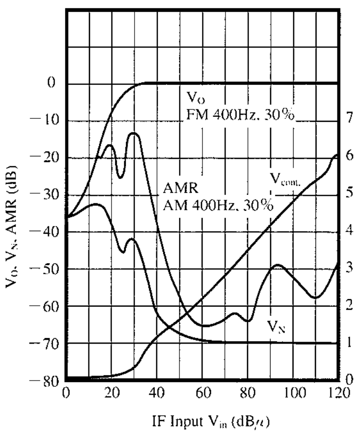
Unless otherwise specified,
V_{CC}=8V, f_{in}=10.7MHz
FM Modulation 30%, 400Hz, V_{in}=70dBμ

②Measuring Condition at NC Input

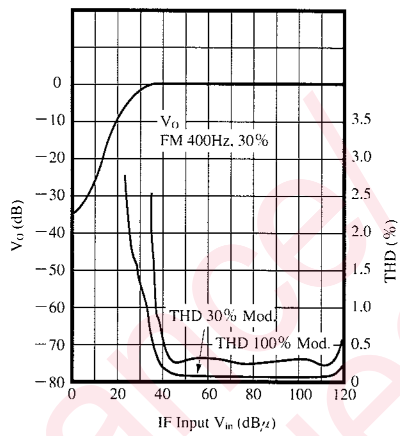


Unless otherwise specified, V_{CC}=8V, f_{in}=1kHz,
V_{in}=400mV (Monaural)
L+R=360mV (Stereo)
V_P=40mV (Stereo)

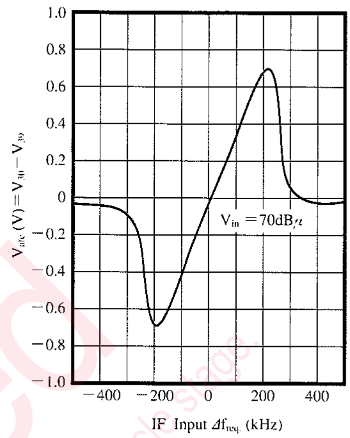
V_O, V_N, AMR, $V_{cont.}$—V_{in}



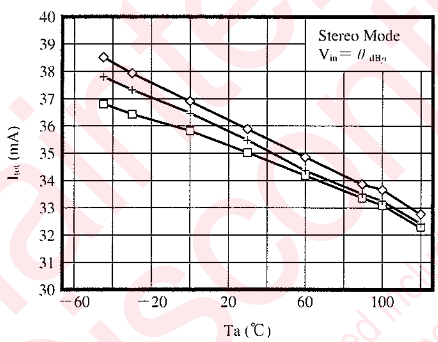
V_O, THD—V_{in}



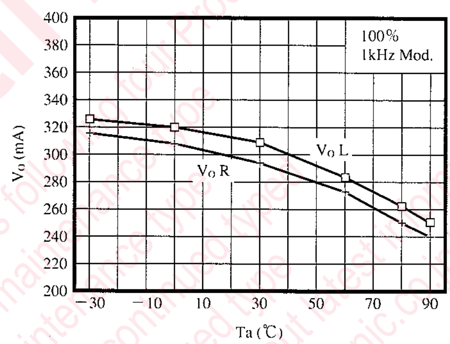
V_{afc}—$\Delta f_{req.}$



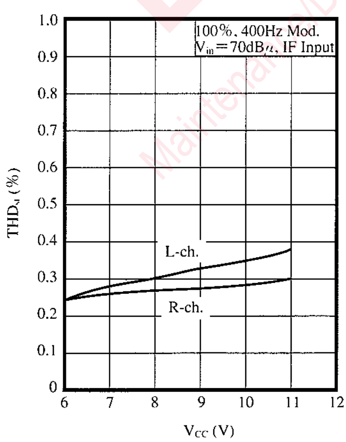
I_{tot}—Ta



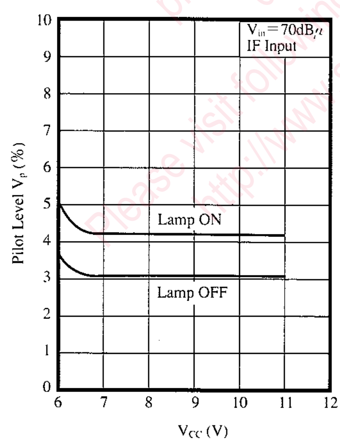
V_O—Ta



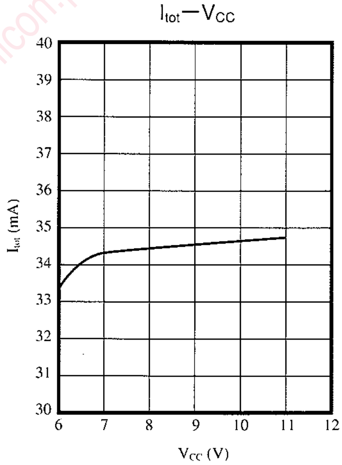
THD_{st}—V_{CC}



Pilot ON/OFF—V_{CC}

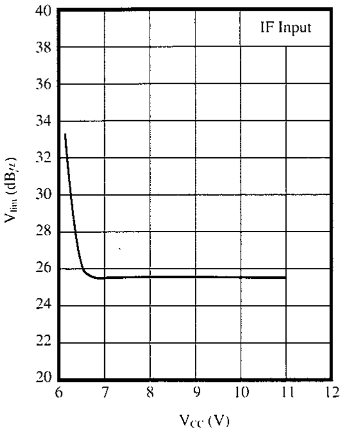


I_{tot}—V_{CC}

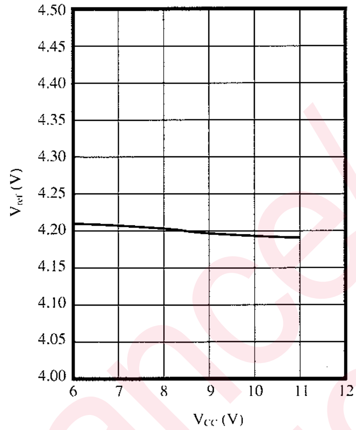


ICs for Tuner

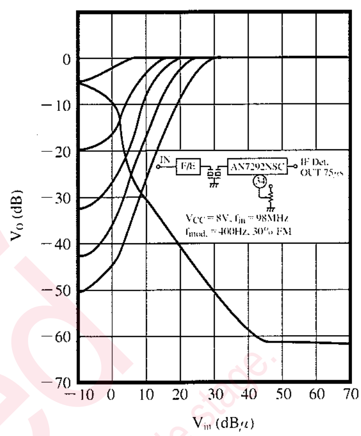
V_{lim} — V_{CC}



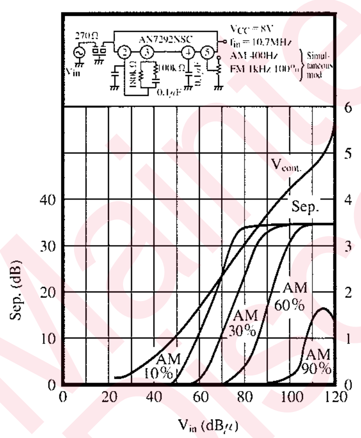
V_{ref} — V_{CC}



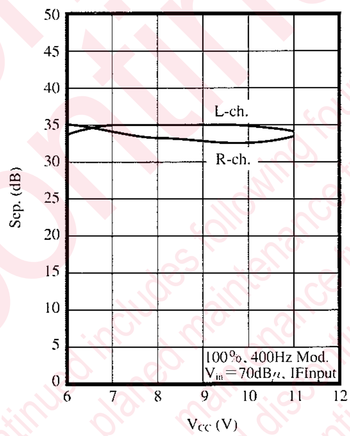
Soft Mute Example V_O — V_{in}



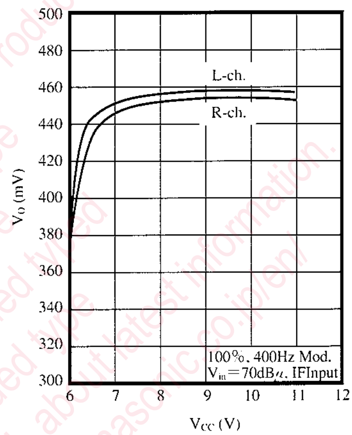
Sep. $V_{cont.}$ — V_{in}



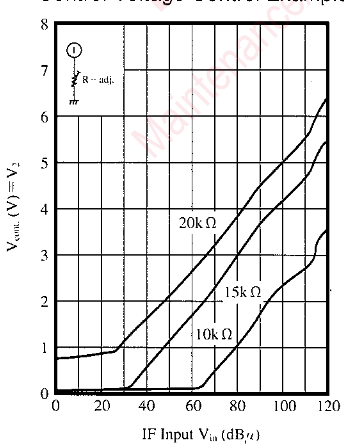
Sep. — V_{CC}



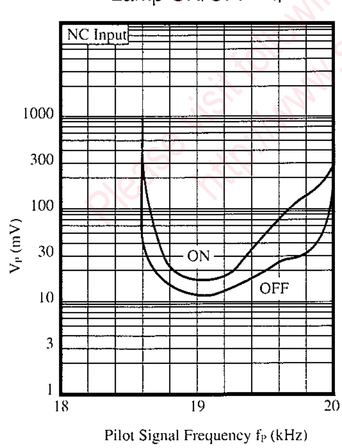
V_O — V_{CC}



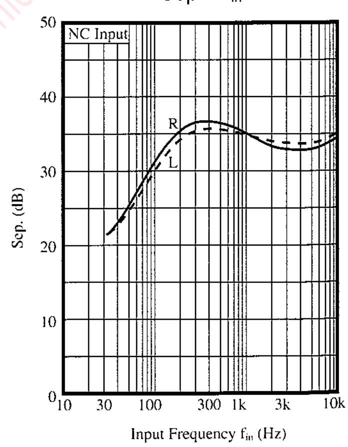
Control Voltage Control Example



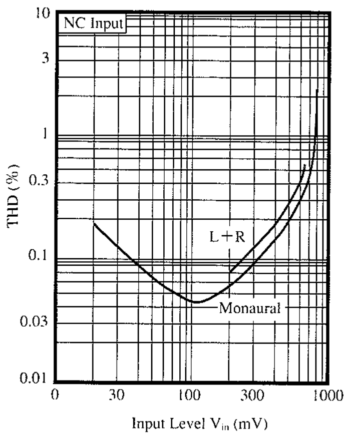
Lamp ON/OFF — f_P



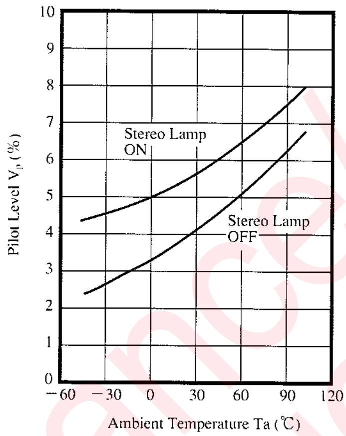
Sep. — f_{in}



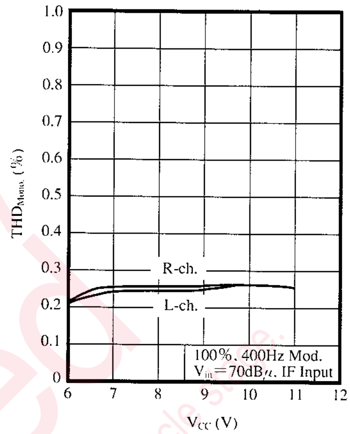
THD — V_{in}



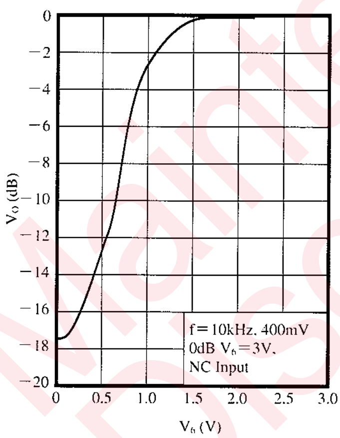
Stereo Lamp ON/OFF — Ta



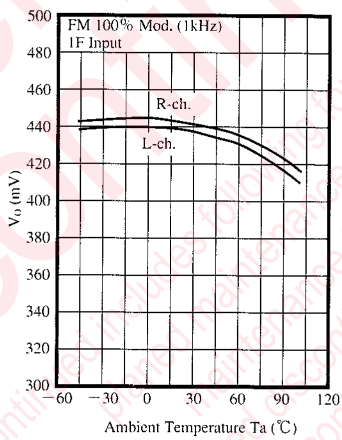
$THD_{Mono.}$ — V_{CC}



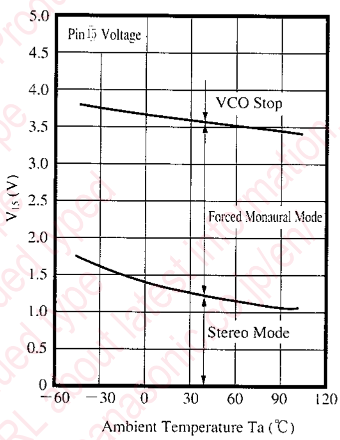
ATC Characteristics



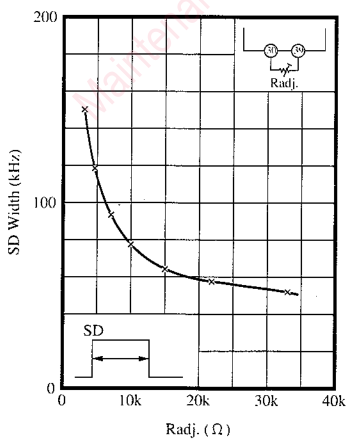
V_O — Ta



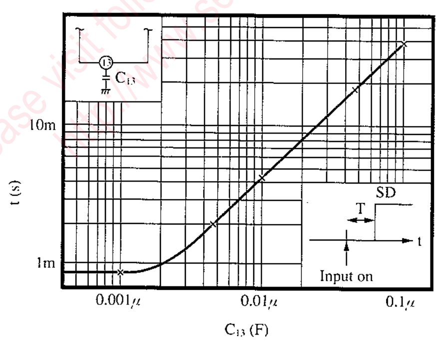
Forced Monaural Operation Voltage — Ta



SD Width versus Radj.



C_{13} versus SD Rise Delay



■ Supplementary Explanation

[1] On Multipath Distortion Preventive Circuit (AN7292NSC pin numbers are used below)

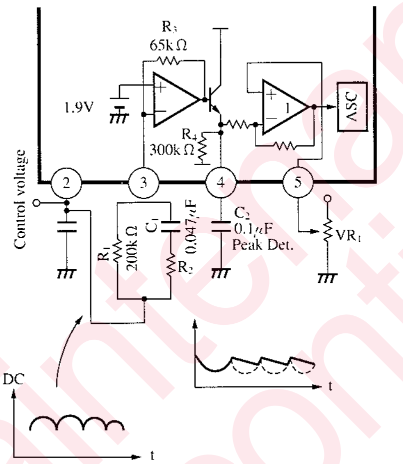
1. Principle

Multipath distortion is apt to increase especially in the stereo receiving mode. In consideration of this phenomenon, the AN7292NSC has been designed so as to suppress the feeling of physical disorder incidental to multipath noise bydegrading the separation against multipath distortion.

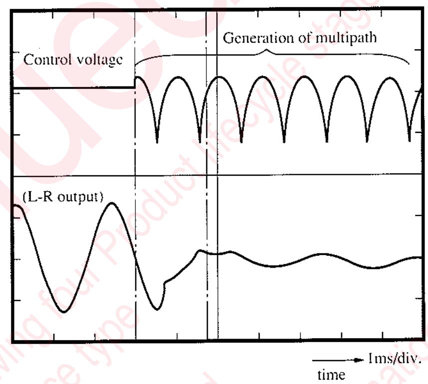
Detection method : Detection of AM components included in control voltage (level meter) output

Separation method : Operation of conventional ASC circuit by conversion of detected AM components into DC voltage

2. Circuit and Operation

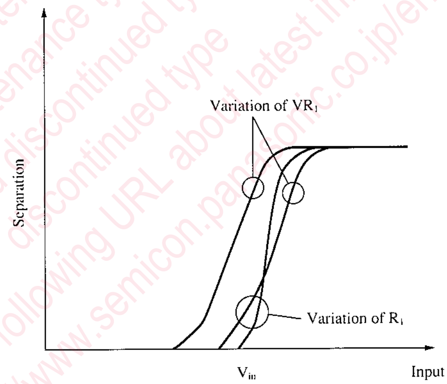


3. Actual Operation Example



(1) Operation in a state free from multipath
(Operation as ASC)

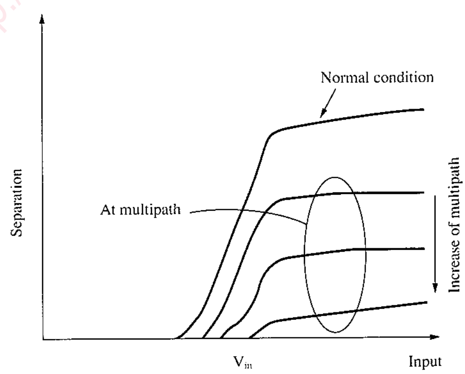
The control voltage of ② is sent to the ASC through the two operational amplifiers. The gradient of the characteristics curve can be set by R_3/R_1, and the start point can be set by VR_1.



(2) Operation in a state exposed to multipath

The variation to appear in the control voltage on account of multipath distortion is put to AM detection, and the DC voltage to the ASC is suitably lowered to degrade the separation.

The frequency characteristics of the AM components are adjusted through C_1 shown in the sketch, and the AM components are put to peak value detection by R_4, C_2.



[2] SD/Frequency Band Mute

1. Operation

The figure shown below is a block diagram of SD/Frequency Band Mute of the AN7292NSC.

The frequency band signal obtained from the AFC voltage of Pin㉚ is applied to Pin⑬. If V13<V29, comparing the voltage between Pin⑬ and Pin㉙, (sensitivity adjustment) SD=H and the band signal is outputted to Pin㉘.

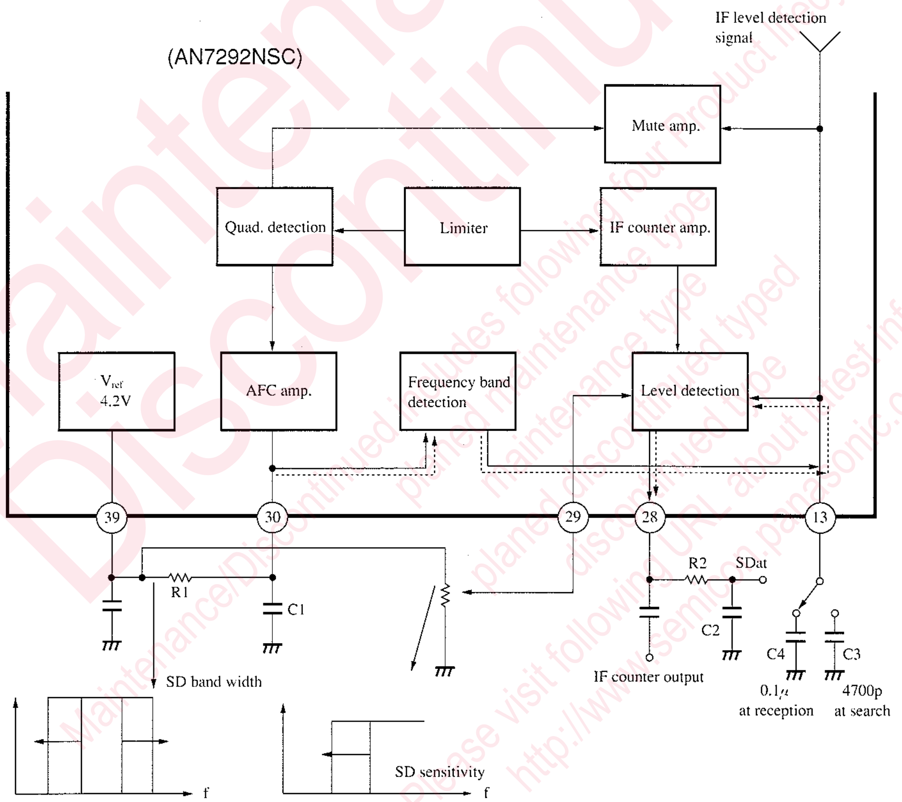
The band mute width and SD band width become equal, because the band mute is applied by using the voltage of Pin⑬.

The AC components are superimposed to SD voltage (DC) of Pin㉘ and IF counter output is outputted.

2. How to use

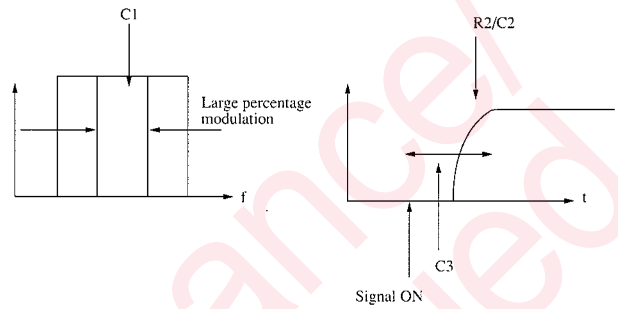
(1) The SD band is adjusted by R1 between Pin㉚ and Pin㊴. Also, the SD sensitivity is adjusted by the voltage of Pin㉙. These can be independently set.

(2) To determine the SD rise speed and percentage modulation characteristics, C1 of Pin㉚, C3 of Pin⑬ and R2 of C2 of Pin㉘ work.



· IF counter stops and SD=L when $0<V_{29}<0.3V$
· IF counter ON when SD=H.

- C1 of Pin㉚ relates to SD at large percentage modulation.(0.33μ ~0.47μF)
  ※It must be increased when THD in the low frequency band is deteriorated. (up to 3.3μF)
- C3 of Pin⑬ determines the time to SD rise after signal input.
  The rise time is about 1ms at 1000pF and about 2ms at 4700pF.
- R2/C2 of Pin㉘ is a filter decreasing the IF counter components and relates to the speed of rise components.

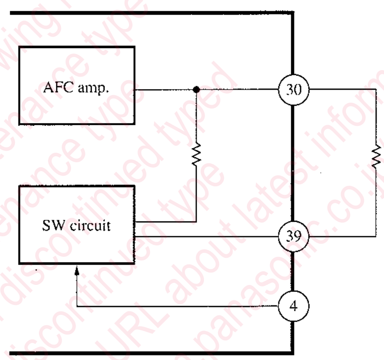


For these topics, refer to the data.

3. Miscellaneous

The SD of AN7292NSC has the function to narrow the band width when the voltage of Pin④ increases to 1.9V or more.

It works so as to increase the inclination of S-curve to operate the SD band mute more positively when signals are disrupted.



SD band variable

[3] Selection Standard of Noise Canceler Resistance Value

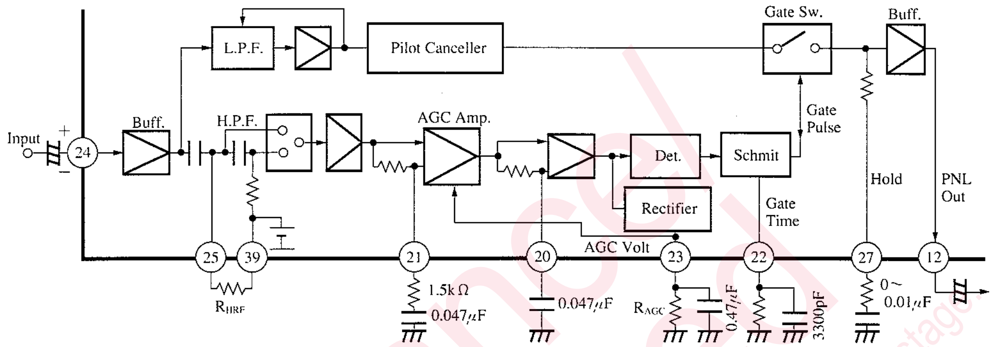


Fig.1 Pulse Noise Limiter (PNL) Block Diagram

(1) Relation to field strength

1. In weak electric field

In a weak electric field where noise is apt to increase, the AGC effectively controls the PNL operation.

a) In case operation error is frequently caused by white noise

Suitably increase the value of Pin㉓ R_{AGC} (220kΩ to 1MΩ).

b) In case operation error is frequently caused by overmodulation.

Suitably increase the value of R_{HPF} between Pin㉕ and ㊴ R_{HPF} (47kΩ to 470kΩ).

2. In medium to strong electric field

In a medium to strong electric field relatively free from noise generation, the AGC becomes less effective and noise is detected almost at the maximum sensitivity.

a) In case the detection sensitivity is too high

Suitably decrease the value of Suitably decrease the value of R_{HPF} between Pin㉕ and ㊴ (10kΩ to 47kΩ).

3. In every electric filed

a) In case the detection sensitivity is excellent but the PNL effect deteriorated due to holding level fluctuation by noise, suitably increase the resistance value of the resistor connected in series with the Pin㉗ holding capacitor (1kΩ to 4.7kΩ).

b) In case noise of the gate pulse itself is conspicuous, suitably narrow the gate pulse width by decreasing the resistance value of the Pin㉒ resistor (3kΩ to 6.8kΩ).

ICs for Tuner

(2) Selection of AGC Resistor R_{AGC} Pin㉓

Pin㉓ is the AGC LPF, and enables AGC effective level adjustment. The equivalent circuit in the vicinity of this pin has been so constituted as shown in Fig. 2, and the output impedance at the charging time is 15kΩ while the input impedance at the discharging time is about 1MΩ.

The standard value of R_{AGC} is 330kΩ, but in case operation error is frequently caused in a weak electric field by white noise, selectively increase the value of R_{AGC} to a suitable level between 200kΩ and 1MΩ. So long as the value of R_{AGC} was properly increased, the AGC voltage proportionally becomes higher to prolong the dischargingtimeconstant, and the rate of operation error sharply drops with decrease of the gain of the AGC Amp. (Though Pin㉓, the noise components are put to peak (envelope) detection. Even if the value of R_{AGC} was increased, the charging time and voltage remain almost unchanged because $Z_O = 15k\Omega$.)

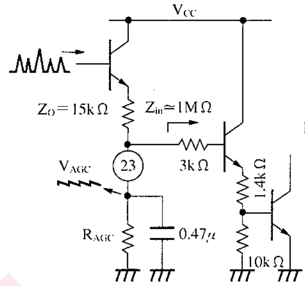
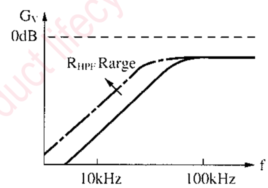


Fig. 2

(3) Selection of HPF Resistor R_{HPF} Pin㉕

When the resistance value R_{HPF} of the resistor between Pin㉕ and ㉚ was increased, the cut-off frequency of the HPF proportionally becomes lower.

The standard value of R_{HPF} is 330kΩ, but in case operation error is frequently caused in a weak electricfield by white noise at the modulation time or non-modulation time, selectively increase this R_{HPF} to a suitable value not exceeding 470kΩ.



[4] Precautions on PNL Use

Care should be taken to use the PNL, because under the following conditions, in the PNL circuit of this IC, the output wave form may be distorted due to oscillation.

1. Oscillation conditions

When the PNL is used under the conditions described in the following items (1) to (3) and the PNL－AGC voltage (Pin㉓ voltage) becomes 2.3V or more, oscillation may occur.

(1) The PNL input frequency is 15kHz or more and 500mVrms is exceeded.

(2) The voltage of AGC pin (Pin㉓) is forced to exceed the above voltage.

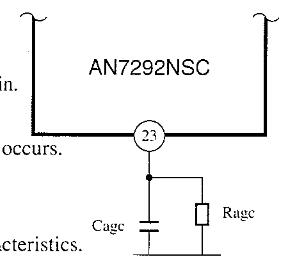
(3) The voltage AC or DC of ＋/－several ten mV or more is directly applied to the PNL filter pins (Pin⑳ and Pin㉑). The oscillation occurrence depends on V_{CC}.

The oscillation can not be stopped unless V_{CC} is much increased, if it occurs.The above three conditions are not given under the normal operation, and therefore oscillation problems are not suffered in practical use.

However, in the review stage, keep in mind that oscillation may occur when the above conditions are given.

2. Effect by external components

The PNL circuit oscillation depends on an external resistor and capacitor of AGC pin.



(1) Cagc is currently set to 0.47μF. The larger it is, the less frequently oscillation occurs.

(2) Ragc is 330kΩ. The smaller it is, the less frequently oscillation occurs.

When the above values are changed, take sufficient consideration for setting characteristics.
Also, when the use under the special conditions is expected, review the countermeasures against oscillation.

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