1.5MHz 3A, Synchronous Step-Down Regulator

General Description

EML3170 is a high efficiency current mode synchronous buck PWM DC-DC regulator. The internal generated 0.8V precision feedback reference voltage is designed for low output voltage. Low $R_{DS\ (ON)}$ synchronous switch dramatically reduces conduction loss. To extend battery life for portable application, 100% duty cycle is supported for low-dropout operation. Shutdown mode also helps saving the current consumption.

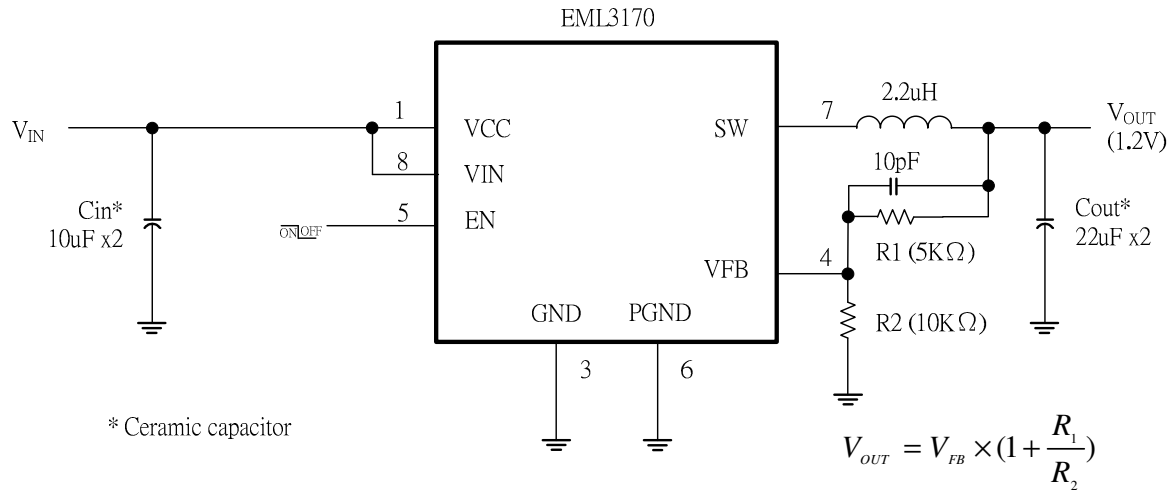
Features

- Input Voltage Range: 2.5 to 5.5V
- Adjustable Output Voltage From 0.8V to V_{IN}
- Precision Feedback Reference Voltage: 0.8V (±2%)
- Output Current: 3A (Max.)
- Duty Cycle: 0~100%
- Internal Fixed PWM Frequency: 1.5MHz
- Low Quiescent Current: 100μA
- No Schottky Diode Required
- Built-in Soft Start
- Current Mode Operation
- Over Temperature Protection

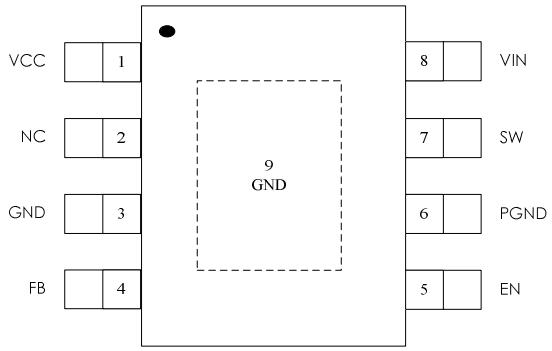
Applications

- Cellular Telephone
- Wireless and DSL Modems
- Digital Still Cameras
- Portable Products
- MP3 Players

Typical Application



Package Configuration

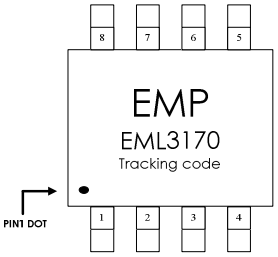


E-SOP-8L

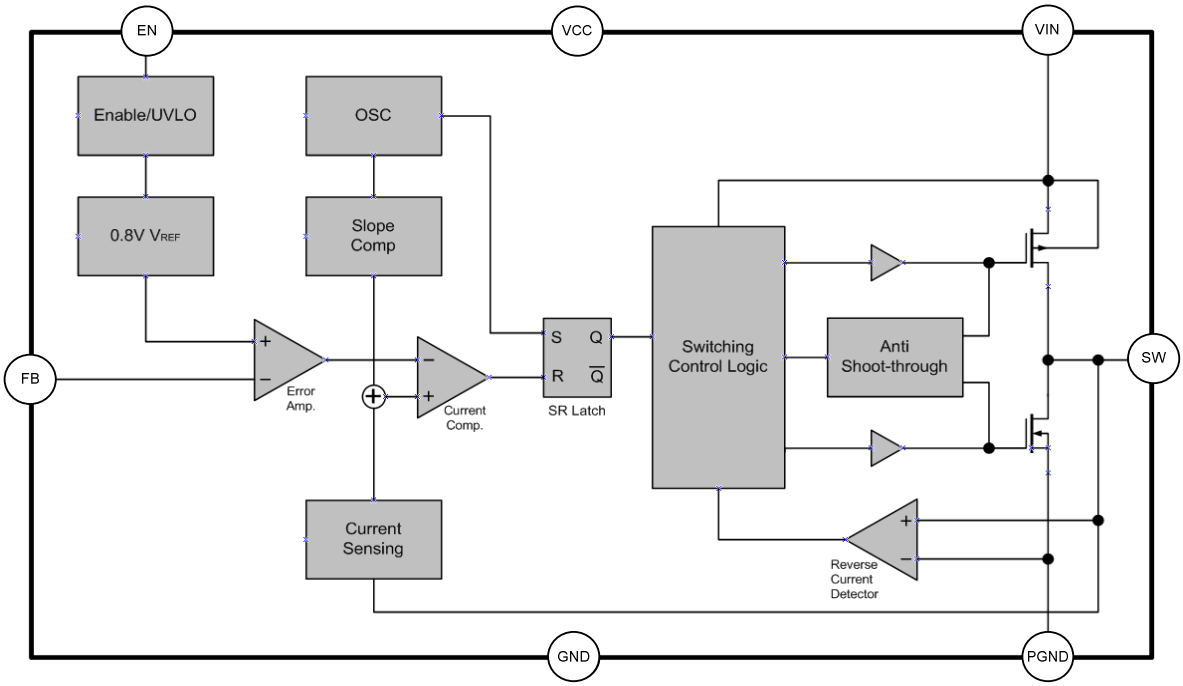
EML3170-00SE08NRR

00	Adjustable
SE08	E-SOP-8L Package
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	adjustable	EML3170-00SE08NRR		Tape & Reel 3K units

Functional Block Diagram



Pin Functions

Pin Name	E-SOP-8L	Function
VCC	1	**Power Input Pin.** Must be closely decoupled to GND pin with a 10μF or greater ceramic capacitor.
NC	2	**NC.**
GND	3	**Ground Pin.**
FB	4	**Feedback Pin.** Receives the feedback voltage from an external resistive divider across the output.
EN	5	**Enable Pin.** Minimum 1.5V to enable the device. Maximum 0.3V to shut down the device.
PGND	6	**Power Switch Ground Pin.**
SW	7	**Switch Pin.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN	8	**Input Supply Pin.** Must be closely decoupled to GND pin with a 10μF or greater ceramic capacitor.
Exposed pad	9	**Thermal pad.** Connect to GND.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (VIN, VCC) ---------- – 0.3V to 6V
EN, FB Voltages ---------- – 0.3V to V_{IN}
SW Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
SW Pin Switch Current (DC) ---------- 3.9A
SW Pin Switch Current (AC) ---------- 6A
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Note 1) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
MM ---------- 200V

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 2)	Junction-ambient	50°C/W
	θ_{JC} (Note 3)	Junction-case	10°C/W

Electrical Characteristics

V_{IN}=V_{VCC}=V_{EN}=3.6V, V_{OUT}=1.2V, V_{FB}=0.8V, L=2.2uH, C_{IN}=10uF, C_{OUT}=22uF, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IN}	Input Voltage Range			2.5		5.5	V
V_{FB}	Regulated Feedback Voltage			0.784	0.800	0.816	V
V_{OUT}%	Output voltage accuracy	I_{OUT}=10mA to 3.0A		-3		+3	%
I_{LSW}	SW Leakage	V_{EN}=0V, V_{IN}=5V			±0.01	±1	μA
IQ	Quiescent Current	Shutdown , V_{EN} = 0V			0.1	1	μA
		Active, V_{FB}=0.7V, V_{EN}=V_{IN}			100		μA
		PFM, V_{FB}=0.9V, V_{EN}=V_{IN}			80		μA
I_{OCP}	Over Current Limit	V_{FB}=0.7V		3.75	5	6	A
f_{OSC}	Oscillator Frequency	VFB=0.8V, -40℃~+85℃		1.2	1.5	1.8	MHz
$R_{ON(P)}$	$R_{DS(ON)}$ of PMOS	I_{OUT}=100mA			60	90	mΩ
$R_{ON(N)}$	$R_{DS(ON)}$ of NMOS	I_{OUT}=100mA			60	90	mΩ
V_{EN}	Enable Threshold	-40℃~+85℃		0.3	1	1.5	V
I_{EN}	EN Leakage Current	-40℃~+85℃			±0.01	±1	μA
ΔV_{FB}	Line Regulation with V_{REF}	V_{IN}=2.5V to 5.5V			0.04	0.4	% / V
ΔV_{OUT}	Output Voltage LineRegulation	V_{IN}=2.5V to 5.5V			0.04	0.4	% / V

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D (T_J = T_A + (P_D) * θ_{JA})).

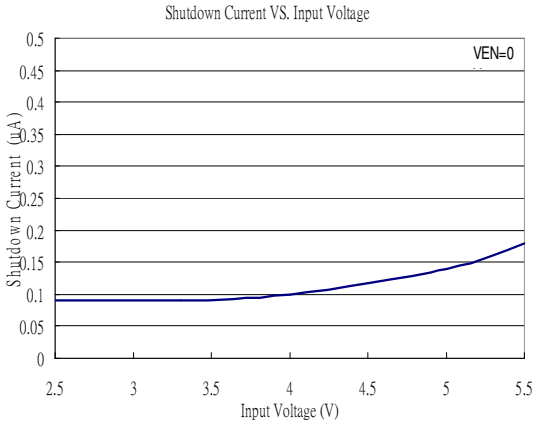
Note 2: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 3: θ_{JC} represents the heat resistance between the chip and the package top case.

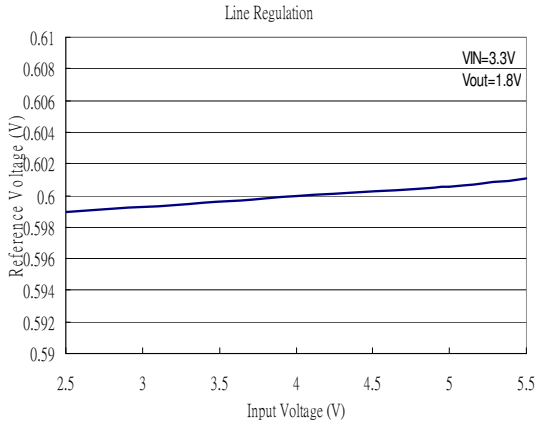
Typical Performance Characteristics

V_{IN}=3.3V, T_A=25℃, unless otherwise specified

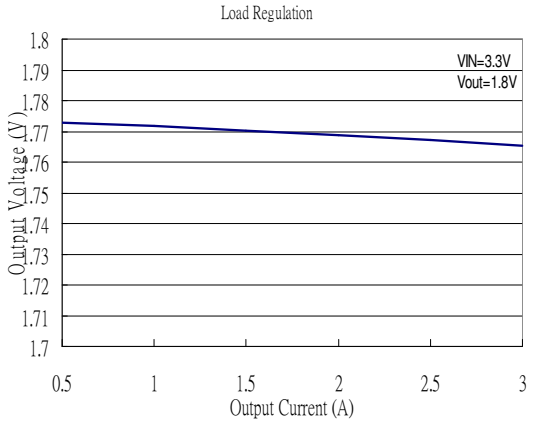
Shutdown Current vs. Input Voltage



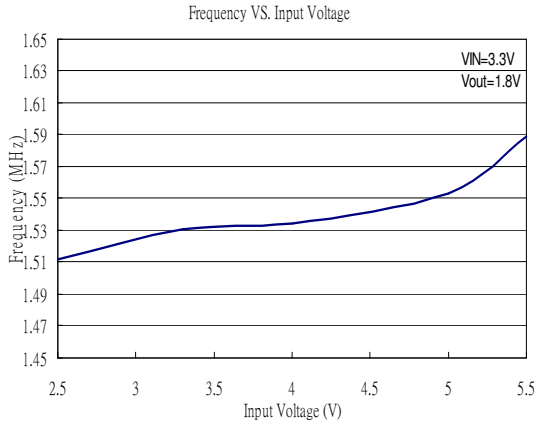
Line regulation



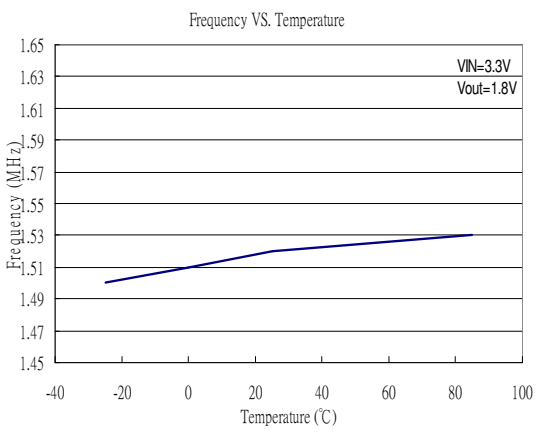
Load Regulation



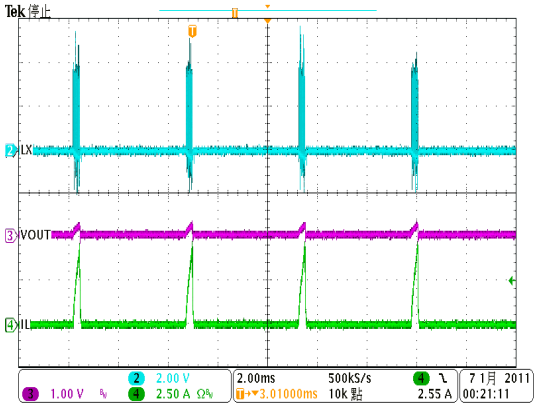
Frequency vs. Input Voltage



Frequency vs. Temperature



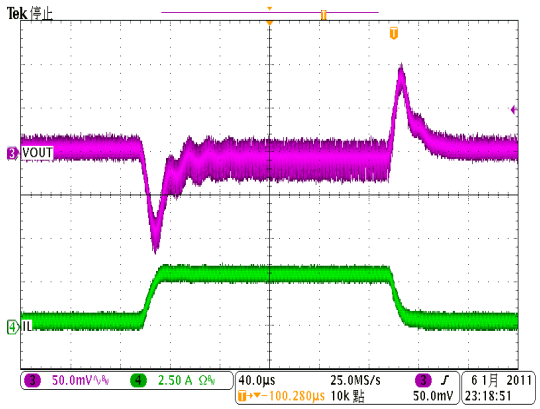
Short Circuit



Typical Performance Characteristics

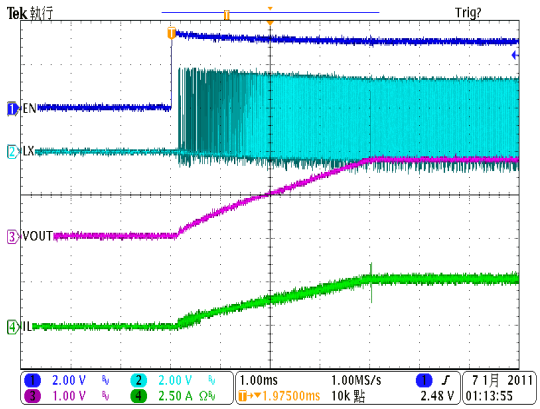
V_{IN}=3.3V, T_A=25℃, unless otherwise specified

Load Transient Response



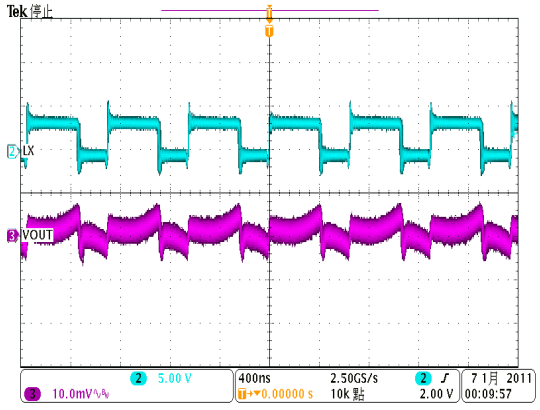
I_{LOAD}: 300mA~3A

Enable ON



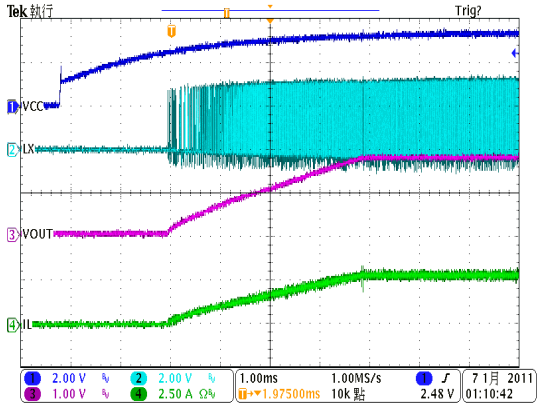
I_{LOAD}: 3A

Output Ripple Voltage



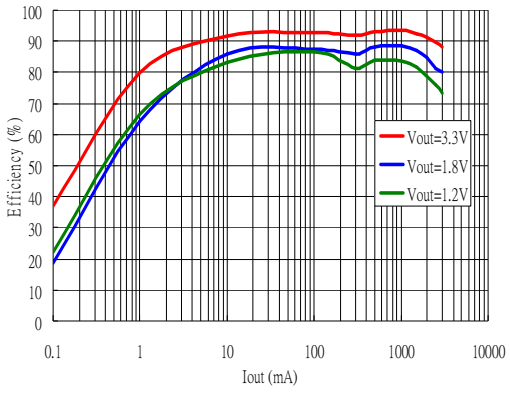
I_{LOAD}: 3A

Power ON

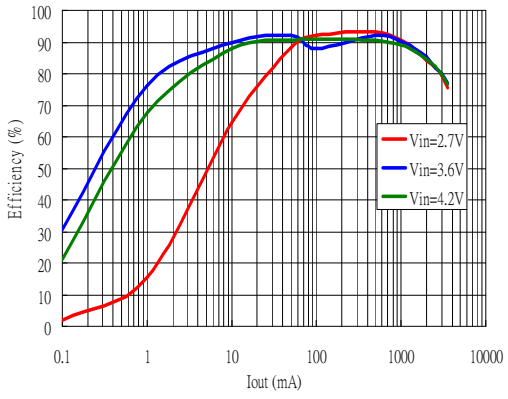


I_{LOAD}: 3A

Efficiency (Vin=5V)



Efficiency (Vout=1.8V)



Function Description

Control Loop

The EML3170 is a high efficiency current mode synchronous buck regulator. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are built internally. With current mode operation, the PWM duty is controlled both by the error amplifier output and the peak inductor current. At the beginning of each cycle, the oscillator turn on the P-MOSFET switch to source current from V_{IN} to SW output. Then, the chip starts to compare the inductor current with the error amplifier output. Once the inductor current is larger than the error amplifier output, the P-MOSFET switch is turned off. When the load current increases, the feedback voltage FB will drop slightly. This causes the error amplifier to output a higher current level until the prior mentioned peak inductor current reach the same level. The output voltage then can be sustained at the same.

When the top P-MOSFET switch is off, the bottom synchronous N-MOSFET switch is turned on. Once the inductor current reverses, both top and bottom MOSFET will be turn off to leave the SW pin into high impedance state.

The EML3170's current mode control loop also includes slope compensation to suppress sub-harmonic oscillations at high duty cycles. This slope compensation is achieved by adding a compensation ramp to the inductor current signal.

LDO Mode

The EML3170's maximum duty cycle can reach 100%. That means the driver's main switch is turn on through out whole clock cycle. Once the duty reaches 100%, the feedback path no longer controls the output voltage. The output voltage will be the input voltage minus the main switch voltage drop.

Over Current Protection

EML3170 limits the peak main switch current cycle by cycle. When over current occurs, chip will turn off the main switch and turn the synchronous switch on until next cycle.

Short Circuit Protection

When the FB pin is drop below 300mV, the chip will tri-state the output pin SW automatically. After 300us rest to avoid over heating, chip will re-initiate PWM operation with soft start.

Thermal Protection

EML3170 will shutdown automatically when the internal junction temperature reaches 150℃ to protect both the part and the system.

Application Information

Input capacitor Selection

The input capacitor must be connected to the VIN pin and GND pin of EML3170 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

In switch mode, the input current is discontinuous in a buck converter. The source current waveform of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{O\_MAX}\sqrt{\frac{V_O}{V_{IN}}\left(1-\frac{V_O}{V_{IN}}\right)}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $I_{O\_MAX}/2$.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. In experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN}-V_O)}{f\times\Delta I_L}\frac{V_O}{V_{IN}} = \frac{(V_{IN}-V_O)}{f\times[2\times(10\%\sim 20\%)I_O]}\frac{V_O}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_O}{f\times L}\times\left[1-\frac{V_O}{V_{IN}}\right]$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L\_PEAK} = I_O + \frac{\Delta I_L}{2}$$

The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Inductor Value (μH)	Dimensions (mm)	Component Supplier	Model
1.0	8.3×8.3×4.5	FENG-JUI	TPRH8D43-2R2M
1.0	10.3×10.3×4.0	FENG-JUI	TPRH10D40-2R2M
2.2	8.3×8.3×4.5	FENG-JUI	TPRH8D43-3R3M
2.2	10.3×10.3×4.0	FENG-JUI	TPRH10D40-3R3M

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_O = \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

Where f = operating frequency, COUT= output capacitance and ΔIL = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increases with input voltage.

Capacitor Value	Case Size	Component Supplier	Model
10μF	0805	Taiyo Yuden	JMK212BJ106MG
10μF	0805	TDK	C12012X5ROJ106K
22μF	0805 1206	TDK	C2012JB0J226M

Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush current through the long wires can potentially cause a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R specification. Their dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

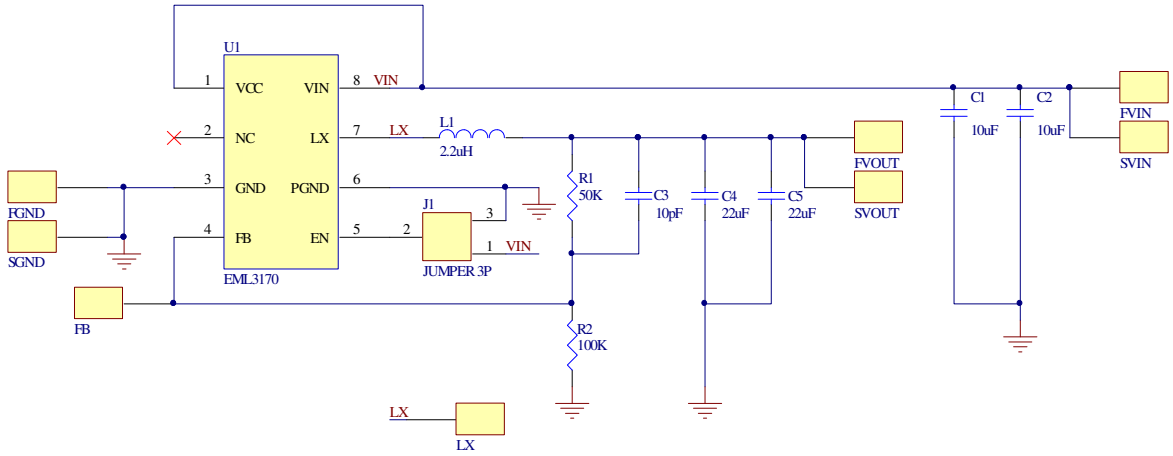
Output Voltage Programming

In the adjustable version, the output voltage is set using a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_O = 0.8V\left(1 + \frac{R_1}{R_2}\right)$$

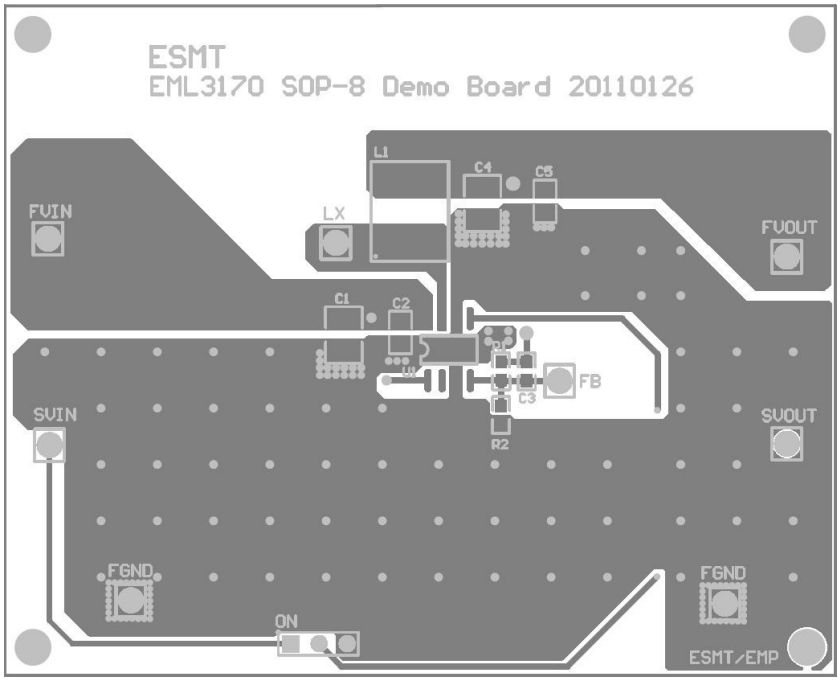
Applications

PCB Layout Considerations

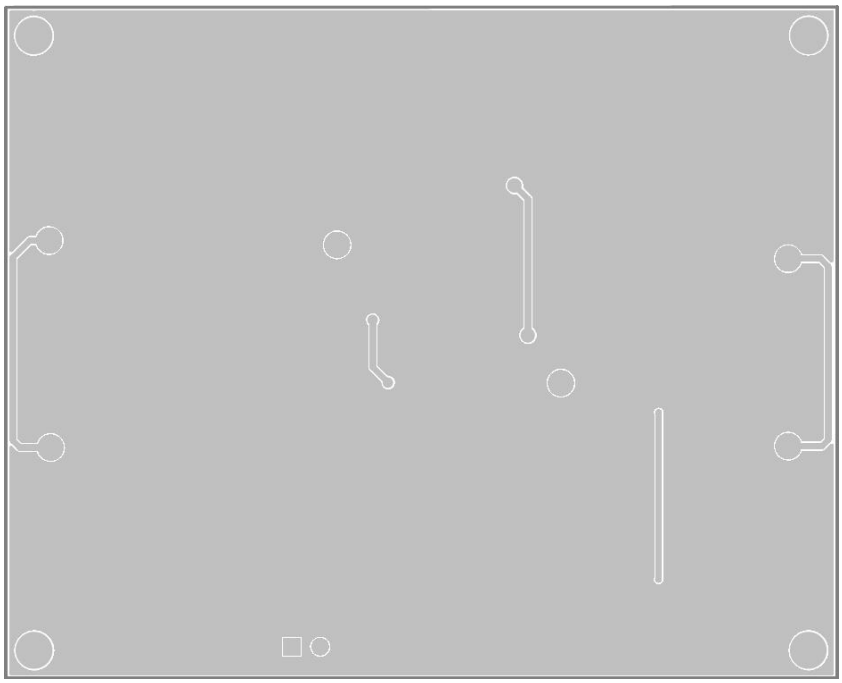


1. The power traces, consisting of the GND, SW and V_{IN} trace should be kept short, direct and wide.
2. Place C_{IN} near V_{IN} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
3. The resistive divider R_1 and R_2 must be connected to FB pin directly and as closely as possible.
4. FB is a sensitive node. Please keep it away from switching node, SW. A good approach is to route the feedback trace on another PCB layer and have a ground plane between the top and feedback trace routing layer. This reduces EMI radiation on to the DC-DC converter its own voltage feedback trace.
5. Keep the GND plates of C_{IN} and C_{OUT} as close as possible. Then connect this to the ground plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at EML3170 by giving it a low impedance ground connection.

Typical Schematic for PCB layout (cont.)



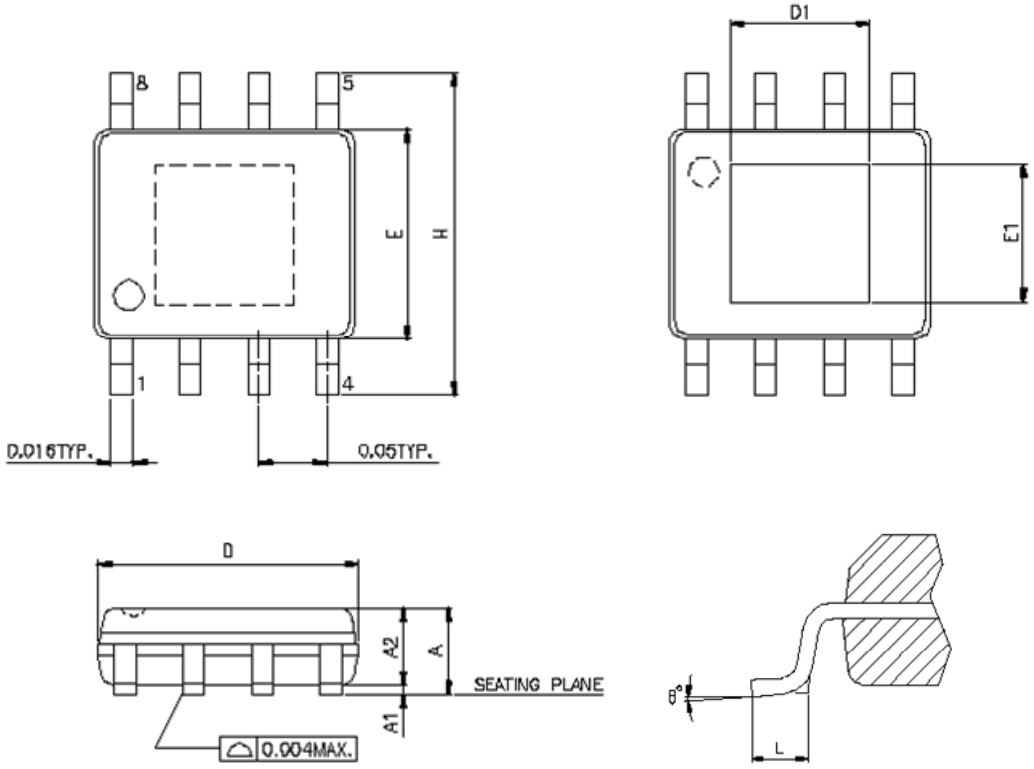
Top Layer



Bottom Layer

Package Information

E-SOP-8L



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	-	1.75	0.053	-	0.069
A1	0.05		0.15	0.002	-	0.006
A2	-	-	1.50	-	-	0.059
b	0.4 BSC			0.016 BSC		
D	4.8	-	5.0	0.189	-	0.196
D1	2.0 REF			0.081 REF		
E	3.8	-	4.0	0.150	-	0.157
E1	2.0 REF			0.081 REF		
e	1.27 BSC			0.05 BSC		
H	5.8	-	6.2	0.228	-	0.244
L	0.4	-	1.27	0.016	-	0.050
θ	0	-	8	0	-	8

Revision History

Revision	Date	Description
0.1	2012.02.07	Original.

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