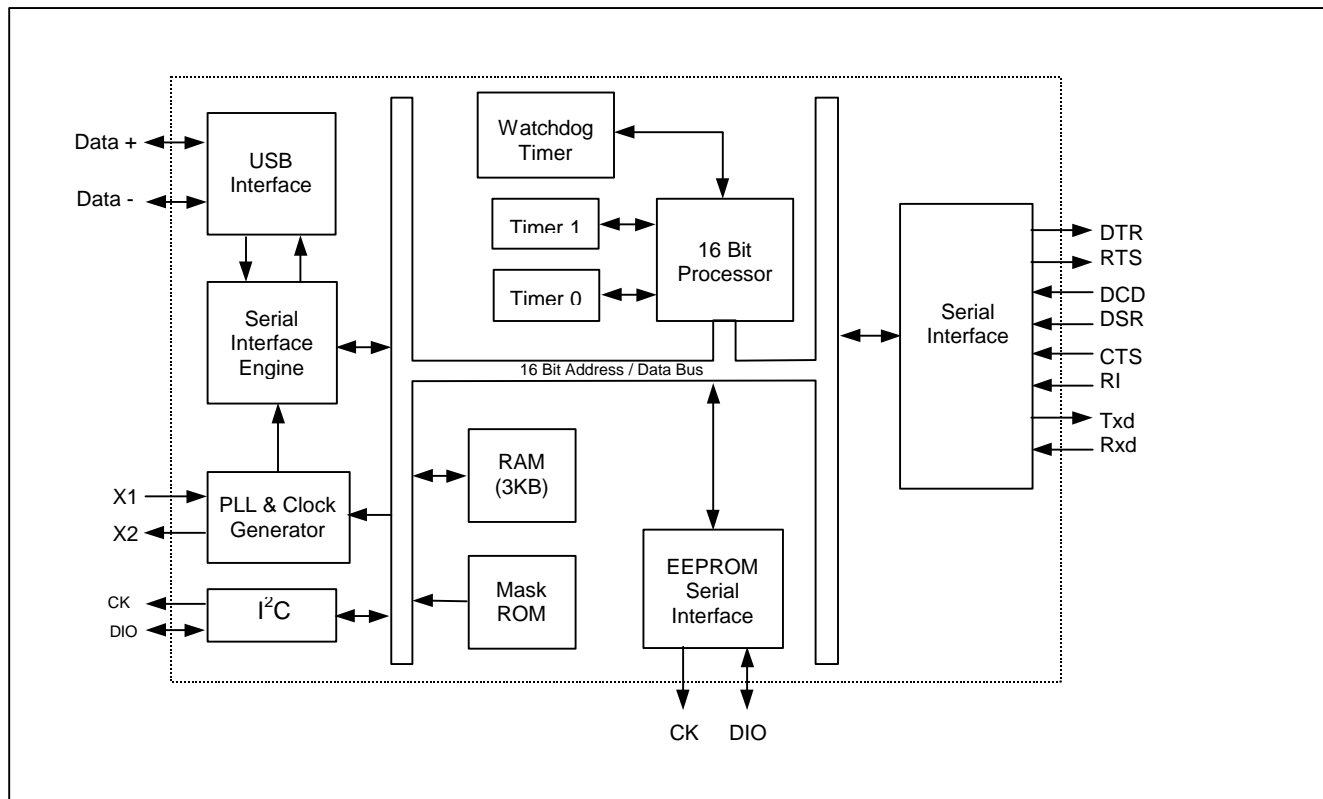K KAWASAKI
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USB to Serial

Description

The Kawasaki USB to Serial enables your system to have the capability to communicate between the USB (Universal Serial Bus) port and up to four serial port peripherals. This device meets the USB 1.0/1.1 and standard serial port specifications.   All the advantages of USB are available to peripherals with serial port interface such as plug and play capabilities. With the USB Standard of high-speed data transfers, this device is ideal for connections. Kawasaki's device and software enable the USB interface to be transparent to the peripheral and requires no firmware changes. This makes it possible for peripherals with serial interfaces to easily interface with USB with minimum modifications. This feature is ideal for Legacy applications.
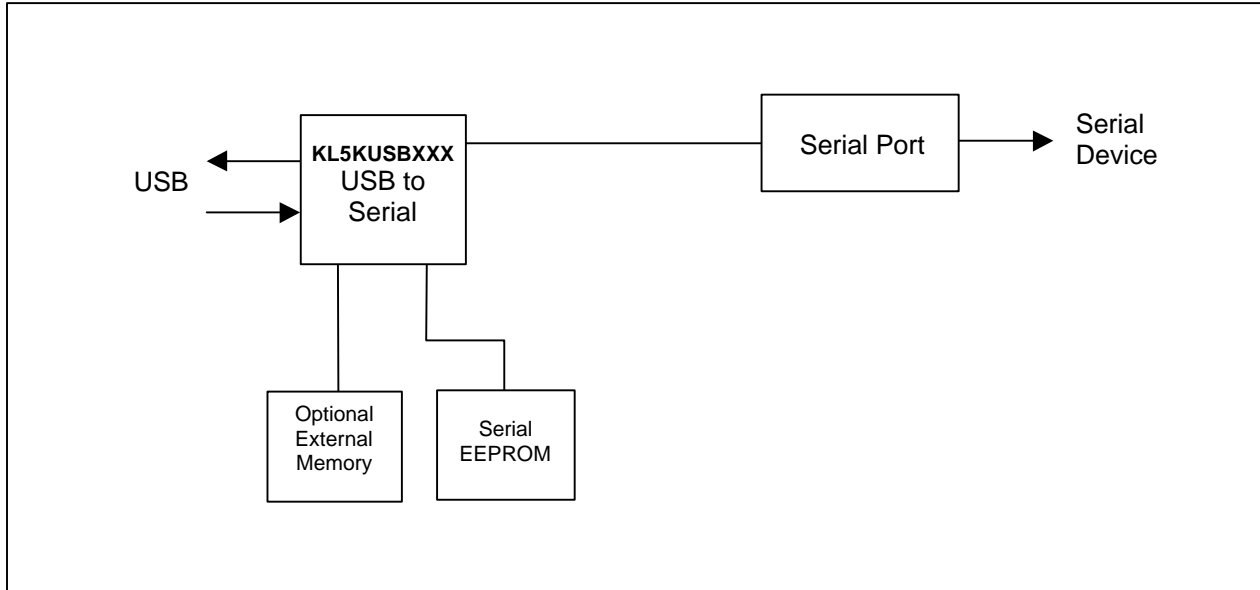
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- Compliant with the USB 1.0/1.1 (Universal Serial Bus)
- 1 Serial Port
- 115kbps Rate
- Plug and Play compatible

- I^2C interface
- Utilizes low cost external crystal circuitry
- 1.5K x 16 internal RAM buffer for fast communications
- USB host device drivers available
- Single-chip solution in a 100 pin QFP

Block Diagram

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USB to Serial

KL5KUSB XXXX Application Block Diagram

Pin Diagram 100QFP

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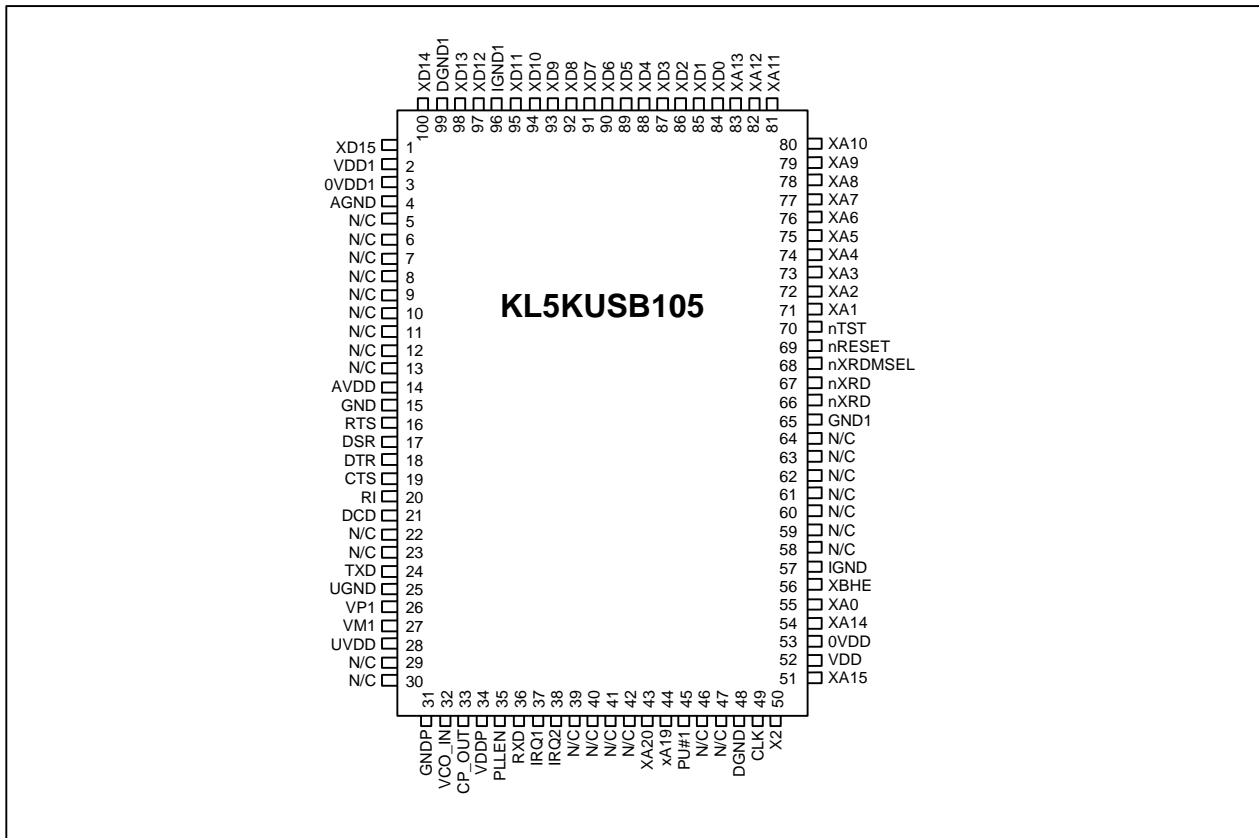
Pin Description

Pin # QFP	I/O	Pin Name	Description
1	IN/OUT	XD15	External Data Pins
2		VDD1	VDD
3		0VDD1	VDD
4		AGND	GND
5	N/C	N/C	N/C
6	N/C	N/C	N/C
7	N/C	N/C	N/C
8	N/C	N/C	N/C
9	N/C	N/C	N/C
10	N/C	N/C	N/C
11	N/C	N/C	N/C
12	N/C	N/C	N/C
13	N/C	N/C	N/C
14		AVDD	VDD
15		GND	GND
16	OUT	RTS	Request To Send
17	IN	DSR	Data Set Ready
18	OUT	DTR	Data Transmit Ready
19	IN	CTS	Clear To Send
20	IN	RI	Ring Indicate
21	IN	DCD	Data Carrier Detect
22	N/C	N/C	N/C
23	N/C	N/C	N/C
24	OUT	TXD	Transmit Data
25		UGND	USB GND
26	IN/OUT	VP1	USB +Pin
27	IN/OUT	VM1	USB -Pin
28		UVDD	USB VDD
29	N/C	N/C	N/C
30	N/C	N/C	N/C
31		GNDP	GND
32	IN	VCO_IN	PLL VCO In
33	OUT	CP_OUT	PLL VCO Out
34		VDDP	VDD
35	IN	PLLEN	PLL Enable
36	IN	RXD	Receive Data
37	IN	IRQ1	N/C
38	IN	IRQ2	N/C
39		N/C	N/C
40		N/C	N/C
41		N/C	N/C
42		N/C	N/C
43	OUT	XA_20	External Address Pins

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USB to Serial

Pin # QFP	I/O	Pin Name	Description
44	OUT	XA_19	External Address Pins
45		PU#1	Connected to Pullup Resistor
46		N/C	N/C
47		N/C	N/C
48		DGND	GND
49	IN	CLK	12MHz Clock/Crystal Input
50	OUT	X2	12MHz Crystal Output
51	OUT	XA15	External Address Pins
52		VDD	VDD
53		0VDD	VDD
54	OUT	XA14	External Address Pins
55	OUT	XA0	External Address Pins
56	OUT	nXBHE	N/C - External byte High Enable (Active low)
57		IGND	GND
58		N/C	N/C
59		N/C	N/C
60		N/C	N/C
61		N/C	N/C
62		N/C	N/C
63		N/C	N/C
64		N/C	N/C
65		GND1	GND
66	OUT	nXRD	External Memory Read (active LO)
67	OUT	nXWR	External Memory Write (active LO)
68	OUT	nXROMSEL	External ROM CS (active LO)
69	OUT	nRESET	Reset Pin
70	OUT	nTST	Test Pin, Disconnect for Normal Operation
71	OUT	XA1	External Address Pins
72	OUT	XA2	External Address Pins
73	OUT	XA3	External Address Pins
74	OUT	XA4	External Address Pins
75	OUT	XA5	External Address Pins
76	OUT	XA6	External Address Pins
77	OUT	XA7	External Address Pins
78	OUT	XA8	External Address Pins
79	OUT	XA9	External Address Pins
80	OUT	XA10	External Address Pins
81	OUT	XA11	External Address Pins
82	OUT	XA12	External Address Pins
83	OUT	XA13	External Address Pins
84	IN/OUT	XD0	External Data Pins
85	IN/OUT	XD1	External Data Pins
86	IN/OUT	XD2	External Data Pins
87	IN/OUT	XD3	External Data Pins
88	IN/OUT	XD4	External Data Pins
89	IN/OUT	XD5	External Data Pins
90	IN/OUT	XD6	External Data Pins
91	IN/OUT	XD7	External Data Pins
92	IN/OUT	XD8	External Data Pins

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Pin # QFP	I/O	Pin Name	Description
93	IN/OUT	XD9	External Data Pins
94	IN/OUT	XD10	External Data Pins
95	IN/OUT	XD11	External Data Pins
96		IGND1	GND
97	IN/OUT	XD12	External Data Pins
98	IN/OUT	XD13	External Data Pins
99		DGND1	GND
100	IN/OUT	XD14	External Data Pins

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM in the this device or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers

The processor supports prioritized vectored hardware interrupts and has as many as 240 software interrupt vectors.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

RAM Buffer

The USB controller contains internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block

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sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock requirements. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to the USB3 pins X1 and X2. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit and connected directly to the X1 input pin.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0 and 1.1. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

UART Serial Interface

The UART can be configured for a wide selection of baud rates, 300 to 230.4 K baud, and support a set of control signals. Each UART provides a means for external serial devices to access the USB.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of serial EEPROM formats.

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Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD5}	-0.6 to 6.0	V
	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_{IN} (Normal)	-0.6 to V_{DD5}+0.6	V
		-0.3 to V_{DD}+0.3	V
	V_{IN} (5V Tolerant)	-0.3 to 7.3	V
DC Output Current	I_{OUT}	±30	mA
Storage Temperature	TSTG	-55 to 125 **	°C

**Plastic Package

DC Characteristics and conditions (V_{DD5} @ 3V±.3V)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
V_{DD5}	Supply Voltage	-	3.0	3.3	3.6	V
V_{IH}	Input high voltage	CMOS	2.15	-	-	V
V_{IL}	Input low voltage	CMOS	-	-	0.95	V
V+	Input high voltage	TTL Schmitt		1.32	1.75	V
		CMOS Schmitt		2.17	2.65	V
V-	Input low voltage	TTL Schmitt	0.45	0.86	-	V
		CMOS Schmitt	0.50	1.03	-	V
V_H	Hysteresis voltage	TTL Schmitt	0.25	-	-	V
		CMOS Schmitt	0.56	-	-	V
I_{IH}	Input high current	$V_{IN} = V_{DD5}$	-10	-	10	μA
I_{IL}	Input low current	$V_{IN} = V_{ss}$	-10	-	10	μA
V_{OH}	Output high voltage	I_{OH} = -4mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 4mA	-	-	0.4	V
I_{OZ}	3-state leakage current	$V_{OL}=V_{DD5}$	-10	-	10	μA
		$V_{IN}=V_{SS}$	-12	-34	-100	μA

*IDDS is design dependent

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