MACRONIX
INTERNATIONAL CO., LTD.

MX29GA129/257E C/F
DATASHEET

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MX29GA129E C/F
MX29GA257E C/F

SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Word mode switchable
  - 16,777,216 x 16
  - 8,388,608 x 16
- 64KW uniform sector architecture
  - MX29GA257E C/F: 256 equal sectors
  - MX29GA129E C/F: 128 equal sectors
- 8-word page read buffer
- 32-word write buffer
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- Deep power down mode

PERFORMANCE
- High Performance
  - MX29GA257E C/F: 90ns (Vcc=3.0~3.6V), 100ns (Vcc=2.7~3.6V)
  - MX29GA129E C/F: 90ns (Vcc=2.7~3.6V)
  - Page access time: 25ns
  - Fast program time: 11us/word
  - Fast erase time: 0.6s/sector
- Low Power Consumption
  - Low active read current: 30mA (typical) at 5MHz
  - Low standby current: 30uA (typical)
- Typical 100,000 erase/program cycle
- 20 years data retention

SOFTWARE FEATURES
- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability

SECURITY
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Advanced write protection function (Solid and Password Protect)
  - Provides sector protect/unprotect function to disable or enable program or erase operation in the sector
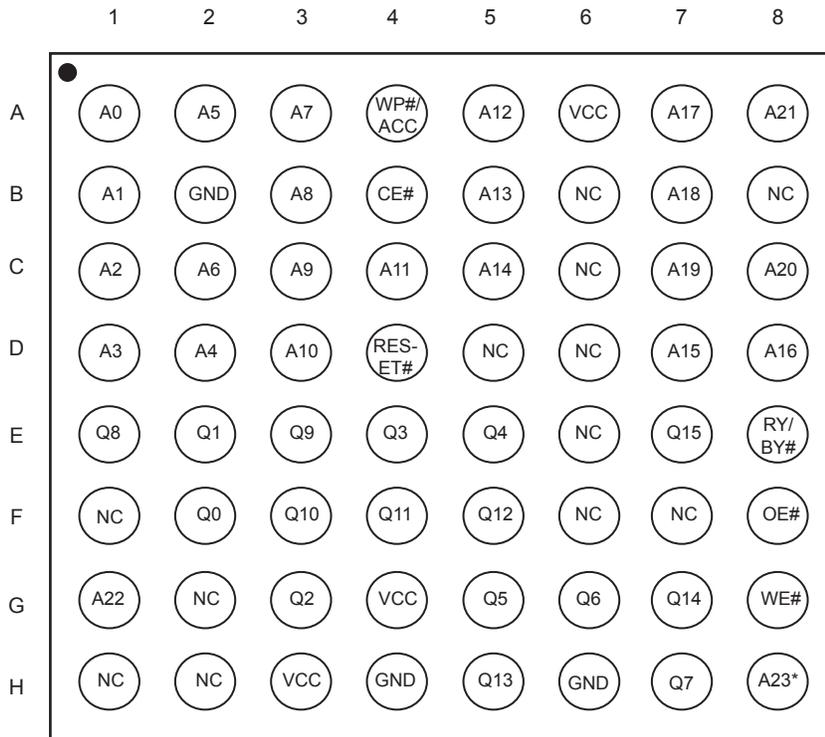
• Advanced read protection function (Password protection & Crypto engine)
  - Provides read lock feature to protect sectors against the unauthorized reading of memory
Please contact Macronix sales for specific information regarding this advanced sector write and read protection feature.

PACKAGE
• 64-Ball FBGA (10mm x 13mm)
• **All Pb-free devices are RoHS Compliant**

PIN CONFIGURATION

64 FBGA

|	1	2	3	4	5	6	7	8
A	A0	A5	A7	WP#/ACC	A12	VCC	A17	A21
B	A1	GND	A8	CE#	A13	NC	A18	NC
C	A2	A6	A9	A11	A14	NC	A19	A20
D	A3	A4	A10	RESET#	NC	NC	A15	A16
E	Q8	Q1	Q9	Q3	Q4	NC	Q15	RY/BY#
F	NC	Q0	Q10	Q11	Q12	NC	NC	OE#
G	A22	NC	Q2	VCC	Q5	Q6	Q14	WE#
H	NC	NC	VCC	GND	Q13	GND	Q7	A23*

Notes:
1. A23 is NC for MX29GA129E

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A23	Address Input/LSB addr
Q0~Q15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC	Hardware Write Protect/Programming Acceleration input
RY/BY#	Read/Busy Output
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL

BLOCK DIAGRAM

AM: MSB address
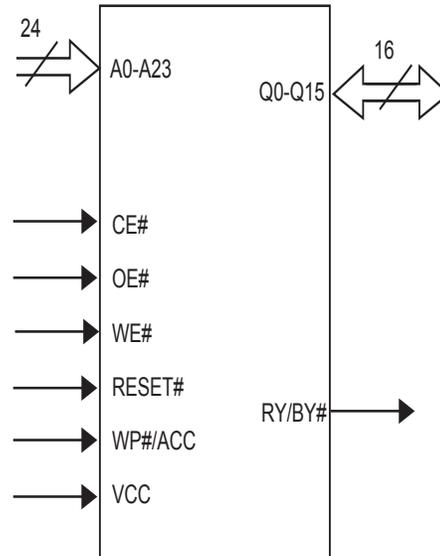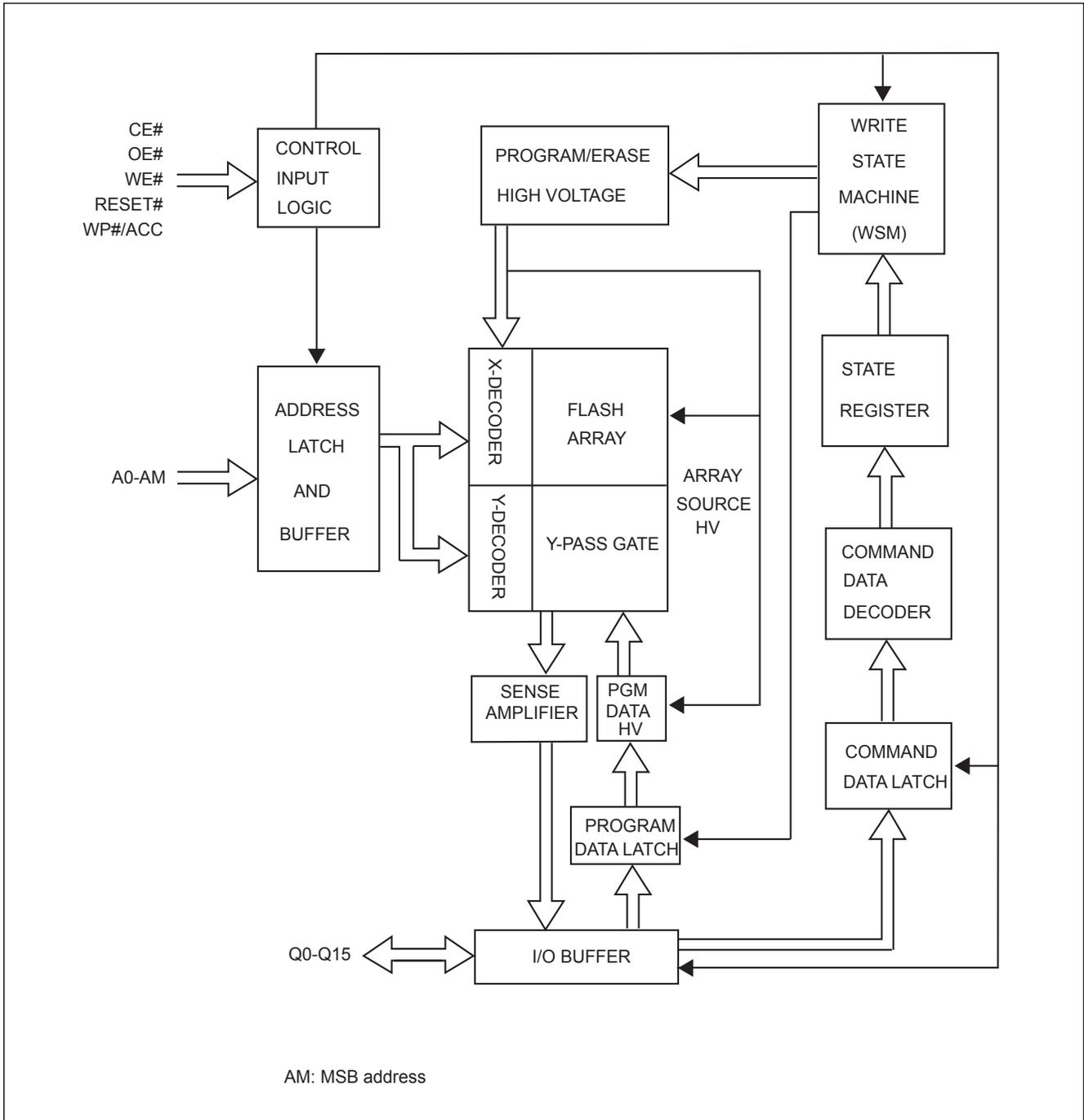
BLOCK DIAGRAM DESCRIPTION

The block diagram on Page 5 illustrates a simplified architecture of MX29GA256E C/F. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A23). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. SENSE AMPLIFIERS are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15 pads. During read operation, the I/O BUFFER receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the I/O BUFFER transmits the data on Q0-Q15 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-A15 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

ARRAY ARCHITECTURE

The main flash memory array can be organized as Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

BLOCK STRUCTURE

Table 1-1: MX29GA129E C/F SECTOR ARCHITECTURE

Sector Size Kwords	Sector	Sector Address A22-A16	(x16) Address Range
64	SA0	0000000	000000h-00FFFFh
64	SA1	0000001	010000h-01FFFFh
64	SA2	0000010	020000h-02FFFFh
64	SA3	0000011	030000h-03FFFFh
64	SA4	0000100	040000h-04FFFFh
64	SA5	0000101	050000h-05FFFFh
64	SA6	0000110	060000h-06FFFFh
64	SA7	0000111	070000h-07FFFFh
64	SA8	0001000	080000h-08FFFFh
64	SA9	0001001	090000h-09FFFFh
64	SA10	0001010	0A0000h-0AFFFFh
64	SA11	0001011	0B0000h-0BFFFFh
64	SA12	0001100	0C0000h-0CFFFFh
64	SA13	0001101	0D0000h-0DFFFFh
64	SA14	0001110	0E0000h-0EFFFFh
64	SA15	0001111	0F0000h-0FFFFFh
64	SA16	0010000	100000h-10FFFFh
64	SA17	0010001	110000h-11FFFFh
64	SA18	0010010	120000h-12FFFFh
64	SA19	0010011	130000h-13FFFFh
64	SA20	0010100	140000h-14FFFFh
64	SA21	0010101	150000h-15FFFFh
64	SA22	0010110	160000h-16FFFFh
64	SA23	0010111	170000h-17FFFFh
64	SA24	0011000	180000h-18FFFFh
64	SA25	0011001	190000h-19FFFFh
64	SA26	0011010	1A0000h-1AFFFFh
64	SA27	0011011	1B0000h-1BFFFFh
64	SA28	0011100	1C0000h-1CFFFFh
64	SA29	0011101	1D0000h-1DFFFFh
64	SA30	0011110	1E0000h-1EFFFFh
64	SA31	0011111	1F0000h-1FFFFFh
64	SA32	0100000	200000h-20FFFFh
64	SA33	0100001	210000h-21FFFFh
64	SA34	0100010	220000h-22FFFFh
64	SA35	0100011	230000h-23FFFFh
64	SA36	0100100	240000h-24FFFFh
64	SA37	0100101	250000h-25FFFFh
64	SA38	0100110	260000h-26FFFFh
64	SA39	0100111	270000h-27FFFFh
64	SA40	0101000	280000h-28FFFFh
64	SA41	0101001	290000h-29FFFFh

Sector Size Kwords	Sector	Sector Address A22-A16	(x16) Address Range
64	SA42	0101010	2A0000h-2AFFFFh
64	SA43	0101011	2B0000h-2BFFFFh
64	SA44	0101100	2C0000h-2CFFFFh
64	SA45	0101101	2D0000h-2DFFFFh
64	SA46	0101110	2E0000h-2EFFFFh
64	SA47	0101111	2F0000h-2FFFFFh
64	SA48	0110000	300000h-30FFFFh
64	SA49	0110001	310000h-31FFFFh
64	SA50	0110010	320000h-32FFFFh
64	SA51	0110011	330000h-33FFFFh
64	SA52	0110100	340000h-34FFFFh
64	SA53	0110101	350000h-35FFFFh
64	SA54	0110110	360000h-36FFFFh
64	SA55	0110111	370000h-37FFFFh
64	SA56	0111000	380000h-38FFFFh
64	SA57	0111001	390000h-39FFFFh
64	SA58	0111010	3A0000h-3AFFFFh
64	SA59	0111011	3B0000h-3BFFFFh
64	SA60	0111100	3C0000h-3CFFFFh
64	SA61	0111101	3D0000h-3DFFFFh
64	SA62	0111110	3E0000h-3EFFFFh
64	SA63	0111111	3F0000h-3FFFFFh
64	SA64	1000000	400000h-40FFFFh
64	SA65	1000001	410000h-41FFFFh
64	SA66	1000010	420000h-42FFFFh
64	SA67	1000011	430000h-43FFFFh
64	SA68	1000100	440000h-44FFFFh
64	SA69	1000101	450000h-45FFFFh
64	SA70	1000110	460000h-46FFFFh
64	SA71	1000111	470000h-47FFFFh
64	SA72	1001000	480000h-48FFFFh
64	SA73	1001001	490000h-49FFFFh
64	SA74	1001010	4A0000h-4AFFFFh
64	SA75	1001011	4B0000h-4BFFFFh
64	SA76	1001100	4C0000h-4CFFFFh
64	SA77	1001101	4D0000h-4DFFFFh
64	SA78	1001110	4E0000h-4EFFFFh
64	SA79	1001111	4F0000h-4FFFFFh
64	SA80	1010000	500000h-50FFFFh
64	SA81	1010001	510000h-51FFFFh
64	SA82	1010010	520000h-52FFFFh
64	SA83	1010011	530000h-53FFFFh
64	SA84	1010100	540000h-54FFFFh

Sector Size Kwords	Sector	Sector Address A22-A16	(x16) Address Range
64	SA85	1010101	550000h-55FFFFh
64	SA86	1010110	560000h-56FFFFh
64	SA87	1010111	570000h-57FFFFh
64	SA88	1011000	580000h-58FFFFh
64	SA89	1011001	590000h-59FFFFh
64	SA90	1011010	5A0000h-5AFFFFh
64	SA91	1011011	5B0000h-5BFFFFh
64	SA92	1011100	5C0000h-5CFFFFh
64	SA93	1011101	5D0000h-5DFFFFh
64	SA94	1011110	5E0000h-5EFFFFh
64	SA95	1011111	5F0000h-5FFFFFh
64	SA96	1100000	600000h-60FFFFh
64	SA97	1100001	610000h-61FFFFh
64	SA98	1100010	620000h-62FFFFh
64	SA99	1100011	630000h-63FFFFh
64	SA100	1100100	640000h-64FFFFh
64	SA101	1100101	650000h-65FFFFh
64	SA102	1100110	660000h-66FFFFh
64	SA103	1100111	670000h-67FFFFh
64	SA104	1101000	680000h-68FFFFh
64	SA105	1101001	690000h-69FFFFh
64	SA106	1101010	6A0000h-6AFFFFh
64	SA107	1101011	6B0000h-6BFFFFh
64	SA108	1101100	6C0000h-6CFFFFh
64	SA109	1101101	6D0000h-6DFFFFh
64	SA110	1101110	6E0000h-6EFFFFh
64	SA111	1101111	6F0000h-6FFFFFh
64	SA112	1110000	700000h-70FFFFh
64	SA113	1110001	710000h-71FFFFh
64	SA114	1110010	720000h-72FFFFh
64	SA115	1110011	730000h-73FFFFh
64	SA116	1110100	740000h-74FFFFh
64	SA117	1110101	750000h-75FFFFh
64	SA118	1110110	760000h-76FFFFh
64	SA119	1110111	770000h-77FFFFh
64	SA120	1111000	780000h-78FFFFh
64	SA121	1111001	790000h-79FFFFh
64	SA122	1111010	7A0000h-7AFFFFh
64	SA123	1111011	7B0000h-7BFFFFh
64	SA124	1111100	7C0000h-7CFFFFh
64	SA125	1111101	7D0000h-7DFFFFh
64	SA126	1111110	7E0000h-7EFFFFh
64	SA127	1111111	7F0000h-7FFFFFh

Table 1-2: MX29GA257E C/F SECTOR ARCHITECTURE

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA0	00000000	000000h-00FFFFh
64	SA1	00000001	010000h-01FFFFh
64	SA2	00000010	020000h-02FFFFh
64	SA3	00000011	030000h-03FFFFh
64	SA4	00000100	040000h-04FFFFh
64	SA5	00000101	050000h-05FFFFh
64	SA6	00000110	060000h-06FFFFh
64	SA7	00000111	070000h-07FFFFh
64	SA8	00001000	080000h-08FFFFh
64	SA9	00001001	090000h-09FFFFh
64	SA10	00001010	0A0000h-0AFFFFh
64	SA11	00001011	0B0000h-0BFFFFh
64	SA12	00001100	0C0000h-0CFFFFh
64	SA13	00001101	0D0000h-0DFFFFh
64	SA14	00001110	0E0000h-0EFFFFh
64	SA15	00001111	0F0000h-0FFFFFh
64	SA16	00010000	100000h-10FFFFh
64	SA17	00010001	110000h-11FFFFh
64	SA18	00010010	120000h-12FFFFh
64	SA19	00010011	130000h-13FFFFh
64	SA20	00010100	140000h-14FFFFh
64	SA21	00010101	150000h-15FFFFh
64	SA22	00010110	160000h-16FFFFh
64	SA23	00010111	170000h-17FFFFh
64	SA24	00011000	180000h-18FFFFh
64	SA25	00011001	190000h-19FFFFh
64	SA26	00011010	1A0000h-1AFFFFh
64	SA27	00011011	1B0000h-1BFFFFh
64	SA28	00011100	1C0000h-1CFFFFh
64	SA29	00011101	1D0000h-1DFFFFh
64	SA30	00011110	1E0000h-1EFFFFh
64	SA31	00011111	1F0000h-1FFFFFh
64	SA32	00100000	200000h-20FFFFh
64	SA33	00100001	210000h-21FFFFh
64	SA34	00100010	220000h-22FFFFh
64	SA35	00100011	230000h-23FFFFh
64	SA36	00100100	240000h-24FFFFh
64	SA37	00100101	250000h-25FFFFh
64	SA38	00100110	260000h-26FFFFh
64	SA39	00100111	270000h-27FFFFh

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA40	00101000	280000h-28FFFFh
64	SA41	00101001	290000h-29FFFFh
64	SA42	00101010	2A0000h-2AFFFFh
64	SA43	00101011	2B0000h-2BFFFFh
64	SA44	00101100	2C0000h-2CFFFFh
64	SA45	00101101	2D0000h-2DFFFFh
64	SA46	00101110	2E0000h-2EFFFFh
64	SA47	00101111	2F0000h-2FFFFFh
64	SA48	00110000	300000h-30FFFFh
64	SA49	00110001	310000h-31FFFFh
64	SA50	00110010	320000h-32FFFFh
64	SA51	00110011	330000h-33FFFFh
64	SA52	00110100	340000h-34FFFFh
64	SA53	00110101	350000h-35FFFFh
64	SA54	00110110	360000h-36FFFFh
64	SA55	00110111	370000h-37FFFFh
64	SA56	00111000	380000h-38FFFFh
64	SA57	00111001	390000h-39FFFFh
64	SA58	00111010	3A0000h-3AFFFFh
64	SA59	00111011	3B0000h-3BFFFFh
64	SA60	00111100	3C0000h-3CFFFFh
64	SA61	00111101	3D0000h-3DFFFFh
64	SA62	00111110	3E0000h-3EFFFFh
64	SA63	00111111	3F0000h-3FFFFFh
64	SA64	01000000	400000h-40FFFFh
64	SA65	01000001	410000h-41FFFFh
64	SA66	01000010	420000h-42FFFFh
64	SA67	01000011	430000h-43FFFFh
64	SA68	01000100	440000h-44FFFFh
64	SA69	01000101	450000h-45FFFFh
64	SA70	01000110	460000h-46FFFFh
64	SA71	01000111	470000h-47FFFFh
64	SA72	01001000	480000h-48FFFFh
64	SA73	01001001	490000h-49FFFFh
64	SA74	01001010	4A0000h-4AFFFFh
64	SA75	01001011	4B0000h-4BFFFFh
64	SA76	01001100	4C0000h-4CFFFFh
64	SA77	01001101	4D0000h-4DFFFFh
64	SA78	01001110	4E0000h-4EFFFFh
64	SA79	01001111	4F0000h-4FFFFFh
64	SA80	01010000	500000h-50FFFFh
64	SA81	01010001	510000h-51FFFFh
64	SA82	01010010	520000h-52FFFFh

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA83	01010011	530000h-53FFFFh
64	SA84	01010100	540000h-54FFFFh
64	SA85	01010101	550000h-55FFFFh
64	SA86	01010110	560000h-56FFFFh
64	SA87	01010111	570000h-57FFFFh
64	SA88	01011000	580000h-58FFFFh
64	SA89	01011001	590000h-59FFFFh
64	SA90	01011010	5A0000h-5AFFFFh
64	SA91	01011011	5B0000h-5BFFFFh
64	SA92	01011100	5C0000h-5CFFFFh
64	SA93	01011101	5D0000h-5DFFFFh
64	SA94	01011110	5E0000h-5EFFFFh
64	SA95	01011111	5F0000h-5FFFFFh
64	SA96	01100000	600000h-60FFFFh
64	SA97	01100001	610000h-61FFFFh
64	SA98	01100010	620000h-62FFFFh
64	SA99	01100011	630000h-63FFFFh
64	SA100	01100100	640000h-64FFFFh
64	SA101	01100101	650000h-65FFFFh
64	SA102	01100110	660000h-66FFFFh
64	SA103	01100111	670000h-67FFFFh
64	SA104	01101000	680000h-68FFFFh
64	SA105	01101001	690000h-69FFFFh
64	SA106	01101010	6A0000h-6AFFFFh
64	SA107	01101011	6B0000h-6BFFFFh
64	SA108	01101100	6C0000h-6CFFFFh
64	SA109	01101101	6D0000h-6DFFFFh
64	SA110	01101110	6E0000h-6EFFFFh
64	SA111	01101111	6F0000h-6FFFFFh
64	SA112	01110000	700000h-70FFFFh
64	SA113	01110001	710000h-71FFFFh
64	SA114	01110010	720000h-72FFFFh
64	SA115	01110011	730000h-73FFFFh
64	SA116	01110100	740000h-74FFFFh
64	SA117	01110101	750000h-75FFFFh
64	SA118	01110110	760000h-76FFFFh
64	SA119	01110111	770000h-77FFFFh
64	SA120	01111000	780000h-78FFFFh
64	SA121	01111001	790000h-79FFFFh
64	SA122	01111010	7A0000h-7AFFFFh
64	SA123	01111011	7B0000h-7BFFFFh
64	SA124	01111100	7C0000h-7CFFFFh
64	SA125	01111101	7D0000h-7DFFFFh

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA126	01111110	7E0000h-7EFFFFh
64	SA127	01111111	7F0000h-7FFFFFh
64	SA128	10000000	800000h-80FFFFh
64	SA129	10000001	810000h-81FFFFh
64	SA130	10000010	820000h-82FFFFh
64	SA131	10000011	830000h-83FFFFh
64	SA132	10000100	840000h-84FFFFh
64	SA133	10000101	850000h-85FFFFh
64	SA134	10000110	860000h-86FFFFh
64	SA135	10000111	870000h-87FFFFh
64	SA136	10001000	880000h-88FFFFh
64	SA137	10001001	890000h-89FFFFh
64	SA138	10001010	8A0000h-8AFFFFh
64	SA139	10001011	8B0000h-8BFFFFh
64	SA140	10001100	8C0000h-8CFFFFh
64	SA141	10001101	8D0000h-8DFFFFh
64	SA142	10001110	8E0000h-8EFFFFh
64	SA143	10001111	8F0000h-8FFFFFh
64	SA144	10010000	900000h-90FFFFh
64	SA145	10010001	910000h-91FFFFh
64	SA146	10010010	920000h-92FFFFh
64	SA147	10010011	930000h-93FFFFh
64	SA148	10010100	940000h-94FFFFh
64	SA149	10010101	950000h-95FFFFh
64	SA150	10010110	960000h-96FFFFh
64	SA151	10010111	970000h-97FFFFh
64	SA152	10011000	980000h-98FFFFh
64	SA153	10011001	990000h-99FFFFh
64	SA154	10011010	9A0000h-9AFFFFh
64	SA155	10011011	9B0000h-9BFFFFh
64	SA156	10011100	9C0000h-9CFFFFh
64	SA157	10011101	9D0000h-9DFFFFh
64	SA158	10011110	9E0000h-9EFFFFh
64	SA159	10011111	9F0000h-9FFFFFh
64	SA160	10100000	A00000h-A0FFFFh
64	SA161	10100001	A10000h-A1FFFFh
64	SA162	10100010	A20000h-A2FFFFh
64	SA163	10100011	A30000h-A3FFFFh
64	SA164	10100100	A40000h-A4FFFFh
64	SA165	10100101	A50000h-A5FFFFh
64	SA166	10100110	A60000h-A6FFFFh
64	SA167	10100111	A70000h-A7FFFFh
64	SA168	10101000	A80000h-A8FFFFh

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA169	10101001	A90000h-A9FFFFh
64	SA170	10101010	AA0000h-AAFFFFh
64	SA171	10101011	AB0000h-ABFFFFh
64	SA172	10101100	AC0000h-ACFFFFh
64	SA173	10101101	AD0000h-ADFFFFh
64	SA174	10101110	AE0000h-AEFFFFh
64	SA175	10101111	AF0000h-AFFFFFh
64	SA176	10110000	B00000h-B0FFFFh
64	SA177	10110001	B10000h-B1FFFFh
64	SA178	10110010	B20000h-B2FFFFh
64	SA179	10110011	B30000h-B3FFFFh
64	SA180	10110100	B40000h-B4FFFFh
64	SA181	10110101	B50000h-B5FFFFh
64	SA182	10110110	B60000h-B6FFFFh
64	SA183	10110111	B70000h-B7FFFFh
64	SA184	10111000	B80000h-B8FFFFh
64	SA185	10111001	B90000h-B9FFFFh
64	SA186	10111010	BA0000h-BAFFFFh
64	SA187	10111011	BB0000h-BBFFFFh
64	SA188	10111100	BC0000h-BCFFFFh
64	SA189	10111101	BD0000h-BDFFFFh
64	SA190	10111110	BE0000h-BEFFFFh
64	SA191	10111111	BF0000h-BFFFFFh
64	SA192	11000000	C00000h-C0FFFFh
64	SA193	11000001	C10000h-C1FFFFh
64	SA194	11000010	C20000h-C2FFFFh
64	SA195	11000011	C30000h-C3FFFFh
64	SA196	11000100	C40000h-C4FFFFh
64	SA197	11000101	C50000h-C5FFFFh
64	SA198	11000110	C60000h-C6FFFFh
64	SA199	11000111	C70000h-C7FFFFh
64	SA200	11001000	C80000h-C8FFFFh
64	SA201	11001001	C90000h-C9FFFFh
64	SA202	11001010	CA0000h-CAFFFFh
64	SA203	11001011	CB0000h-CBFFFFh
64	SA204	11001100	CC0000h-CCFFFFh
64	SA205	11001101	CD0000h-CDFFFFh
64	SA206	11001110	CE0000h-CEFFFFh
64	SA207	11001111	CF0000h-CFFFFFh
64	SA208	11010000	D00000h-D0FFFFh
64	SA209	11010001	D10000h-D1FFFFh
64	SA210	11010010	D20000h-D2FFFFh
64	SA211	11010011	D30000h-D3FFFFh

Sector Size Kwords	Sector	Sector Address A23-A16	(x16) Address Range
64	SA212	11010100	D40000h-D4FFFFh
64	SA213	11010101	D50000h-D5FFFFh
64	SA214	11010110	D60000h-D6FFFFh
64	SA215	11010111	D70000h-D7FFFFh
64	SA216	11011000	D80000h-D8FFFFh
64	SA217	11011001	D90000h-D9FFFFh
64	SA218	11011010	DA0000h-DAFFFFh
64	SA219	11011011	DB0000h-DBFFFFh
64	SA220	11011100	DC0000h-DCFFFFh
64	SA221	11011101	DD0000h-DDFFFFh
64	SA222	11011110	DE0000h-DEFFFFh
64	SA223	11011111	DF0000h-DFFFFFh
64	SA224	11100000	E00000h-E0FFFFh
64	SA225	11100001	E10000h-E1FFFFh
64	SA226	11100010	E20000h-E2FFFFh
64	SA227	11100011	E30000h-E3FFFFh
64	SA228	11100100	E40000h-E4FFFFh
64	SA229	11100101	E50000h-E5FFFFh
64	SA230	11100110	E60000h-E6FFFFh
64	SA231	11100111	E70000h-E7FFFFh
64	SA232	11101000	E80000h-E8FFFFh
64	SA233	11101001	E90000h-E9FFFFh
64	SA234	11101010	EA0000h-EAFFFFh
64	SA235	11101011	EB0000h-EBFFFFh
64	SA236	11101100	EC0000h-ECFFFFh
64	SA237	11101101	ED0000h-EDFFFFh
64	SA238	11101110	EE0000h-EEFFFFh
64	SA239	11101111	EF0000h-EFFFFFh
64	SA240	11110000	F00000h-F0FFFFh
64	SA241	11110001	F10000h-F1FFFFh
64	SA242	11110010	F20000h-F2FFFFh
64	SA243	11110011	F30000h-F3FFFFh
64	SA244	11110100	F40000h-F4FFFFh
64	SA245	11110101	F50000h-F5FFFFh
64	SA246	11110110	F60000h-F6FFFFh
64	SA247	11110111	F70000h-F7FFFFh
64	SA248	11111000	F80000h-F8FFFFh
64	SA249	11111001	F90000h-F9FFFFh
64	SA250	11111010	FA0000h-FAFFFFh
64	SA251	11111011	FB0000h-FBFFFFh
64	SA252	11111100	FC0000h-FCFFFFh
64	SA253	11111101	FD0000h-FDFFFFh
64	SA254	11111110	FE0000h-FEFFFFh
64	SA255	11111111	FF0000h-FFFFFFh

BUS OPERATION

Table 2-1. BUS OPERATION

Mode Select	RESET#	CE#	WE#	OE#	Address (Note4)	Data I/O Q0~Q15	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc± 0.3V	X	X	X	HighZ	H
Output Disable	H	L	H	H	X	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	L/H
Write	H	L	L	H	AIN	DIN	Note1,2
Accelerate Program	H	L	L	H	AIN	DIN	Vhv

Notes:
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advaned protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode, the addresses are AM to A0, AM: MSB of address.

Table 2-2. BUS OPERATION

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q0 ~ Q7	Q8 ~ Q15
	CE#	WE#	OE#											
Sector Lock Status Verification	L	H	L	SA	X	V_{hv}	X	L	X	L	H	L	01h or 00h (Note 1)	X
Read Silicon ID Manufacturer Code	L	H	L	X	X	V_{hv}	X	L	X	L	L	L	C2H	X
Read Silicon ID -- MX29GA129E C/F														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	37H	22H
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H	22H
Read Silicon ID -- MX29GA257E C/F														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	38H	22H
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H	22H

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 99h.
                            WP# protects low address sector: 89h
   Factory unlocked code: WP# protects high address sector: 19h.
                            WP# protects low address sector: 09h
3. AM: MSB of address.

FUNCTIONAL OPERATION DESCRIPTION

READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

PAGE READ

This device is able to conduct MXIC MaskROM compatible high performance page read. Page size is 8 words. The higher address Amax ~ A3 select the certain page, A2~A0 select the particular word in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in Figure 1 on Page 53. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device.   Writing an invalid command may put the device in an undefined state.

DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Word Data (I/O) pins will drive data.

HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.

WRITE BUFFER PROGRAMMING OPERATION

Programs 32words in a programming operation. To trigger the Write Buffer Programming, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined programming Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax-A5.

"Write-Buffer-Page" address has to be the same for all address/ data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it'll return to normal READ mode.

ABORT will be executed for the Write Buffer Programming Sequence if following condition occurs:
*   The value loaded is bigger than the page buffer size during "Number of Locations to Program"
*   Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
*   Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during
    the "write buffer data loading" operation.
*   Writing not "Confirm Command" after the assigned number of "data load" cycles.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

WRITE BUFFER PROGRAMMING OPERATION (cont'd)

The abort is triggered by Q1=1, Q7=DATA# (last address written), Q6=toggle, Q5=0. A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

SECTOR PROTECT OPERATION

The device provides user programmable protection against program/erase operations for selected sectors. Please refer to Table 1 which show all Sector assignments.

During the protection operation, the sector address of any sector within a Sector may be used to specify the Sector being protected.

AUTOMATIC SELECT BUS OPERATIONS

The following five bus operations require A9 to be raised to Vhv. Please see AUTOMATIC SELECT COMMAND SEQUENCE in the COMMAND OPERATIONS section for details of equivalent command operations that do not require the use of Vhv.

SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to address pins A22 to A12, address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

READ SILICON ID MANUFACTURER CODE

To determine the Silicon ID Manufacturer Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be present on data bits Q0 to Q7.

READ INDICATOR BIT (Q7) FOR SECURITY SECTOR

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. If the Security Sector has been locked at the factory, the code 99h(H)/89h(L) will be present on data bits Q0 to Q7. Otherwise, the factory unlocked code of 19h(H)/09h(L) will be present.

FUNCTIONAL OPERATION DESCRIPTION (cont'd)

INHERENT DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

COMMAND OPERATIONS

READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding 20us) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector(s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Word mode. As long as the users enters the correct cycle defined in the Table 3 (including 2 unlock cycles and the A0H program command), any word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

COMMAND OPERATIONS (cont'd)

AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY (cont'd)

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hard ware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

Status	Q7[*1]	Q6[*1]	Q5	Q1	RY/BY# (Note)
In progress	Q7#	Toggling	0	0	0
Exceed time limit	Q7#	Toggling	1	N/A	0

Note: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in section 5.

SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

COMMAND OPERATIONS (cont'd)

SECTOR ERASE (cont'd)

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3[*1]	Q2	RY/BY#[*2]
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

Note:
1. The Q3 status bit is the 50us time-out indicator. When Q3=0, the 50us time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the 50us time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.
2. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector(s), the erase operation will abort thus preventing any data changes in the protected sector(s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#[*1]
In progress	0	Toggling	0	Toggling	0
Exceed time limit	0	Toggling	1	Toggling	0

*1: RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.

COMMAND OPERATIONS (cont'd)

ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until 20us time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector(s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 400us interval between Ease Resume and the next Erase Suspend command.

COMMAND OPERATIONS (cont'd)

PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend is the only valid command that may be issued. The system can determine if the device has entered the Program-Suspended Read mode through Q6, and RY/BY#.

After the device has entered Program-Suspended mode, the system can read any sector(s) except those being programd by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Program suspend read in program suspended sector	Invalid						1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security silicon.

PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a 5us interval between Program Resume and the next Program Suspend command.

BUFFER WRITE ABORT

Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register shown as following table:

Status	Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Buffer Write Busy	Q7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	Q7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	Q7#	Toggle	1	N/A	N/A	0	0

COMMAND OPERATIONS (cont'd)

AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Program Suspend Read mode, Erase-Suspended Read mode, or CFI mode, the user can issue the Automatic Select command shown in Table 3 (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active or Program Suspend Read mode if Program Suspend was active).

Another way to enter Automatic Select mode is to use one of the bus operations shown in Table 2. BUS OPERATION_2. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

		Address	Data (Hex)	Representation
Manufacturer ID		X00	C2	
Device ID	MX29GA129E	X01/0E/0F	227E/2237/2201	
	MX29GA257E	X01/0E/0F	227E/2238/2201	
Secured Silicon		X03	99/19 (H)	Factory locked/unlocked
			89/09 (L)	
Sector Protect Verify		(Sector address) X 02	00/01	Unprotected/protected

After entering automatic select mode, no other commands are allowed except the reset command.

COMMAND OPERATIONS (cont'd)

READ MANUFACTURER ID OR DEVICE ID

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JE-DEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins.

RESET

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Auto-Select mode
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in Auto-Select mode or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 128 words in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 8-word ESN in the security region. The ESN occupies addresses 00000h to 00007h.

Secured Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked	Customer Lockable
000000h-000007h	ESN	ESN or Determined by Customer	Determined by Customer
000008h-00007Fh	Unavailable	Determined by Customer	

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

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TABLE 3. COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select				Security Sector Region	Exit Security Sector	Program
				Silicon ID	Device ID	Factory Protect Verify	Sector Protect Verify			
1st Bus Cycle	Addr	Addr	XXX	555	555	555	555	555	555	555
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	2AA	2AA	2AA	2AA	2AA	2AA
	Data			55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	555	555	555	555	555	555
	Data			90	90	90	90	88	90	A0
4th Bus Cycle	Addr			X00	X01	X03	(Sector) X02		XXX	Addr
	Data			C2h	ID1	99/19(H) 89/09(L)	00/01		00	Data
5th Bus Cycle	Addr				X0E					
	Data				ID2					
6th Bus Cycle	Addr				X0F					
	Data				ID3					

Command		Write to Buffer Program	Write to Buffer Program Abort Reset	Write to Buffer Program confirm	Chip Erase	Sector Erase	CFI Read	Program/ Erase Suspend	Program/ Erase Resume	Deep Power Down	
										Enter	Exit
1st Bus Cycle	Addr	555	555	SA	555	555	55	XXX	XXX	555	XXX
	Data	AA	AA	29	AA	AA	98	B0	30	AA	AB
2nd Bus Cycle	Addr	2AA	2AA		2AA	2AA				2AA	
	Data	55	55		55	55				55	
3rd Bus Cycle	Addr	SA	555		555	555				XXX	
	Data	25	F0		80	80				B9	
4th Bus Cycle	Addr	SA			555	555					
	Data	N-1			AA	AA					
5th Bus Cycle	Addr	WA			2AA	2AA					
	Data	WD			55	55					
6th Bus Cycle	Addr	WBL			555	Sector					
	Data	WD			10	30					

WA= Write Address
WD= Write Data
SA= Sector Address
N= Word Count
WBL= Write Buffer Location
ID1/ID2/ID3: Refer to Table 2-2 for detail ID of each device.

Notes:
* It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.

COMMON FLASH MEMORY INTERFACE (CFI) MODE

QUERY COMMAND AND COMMAND FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on word mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can issuereset command to exit CFI mode and return to read array mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code	17	0000
	18	0000
Address for alternate algorithm extended query table	19	0000
	1A	0000

Table 4-2. CFI mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word write, 2^n us	1F	0003
Typical timeout for maximum-size buffer write, 2^n us (00h, not support)	20	0006
Typical timeout per individual block erase, 2^n ms	21	0009
Typical timeout for full chip erase, 2^n ms (00h, not support)	22	0013
Maximum timeout for word write, 2^n times typical	23	0003
Maximum timeout for buffer write, 2^n times typical	24	0005
Maximum timeout per individual block erase, 2^n times typical	25	0003
Maximum timeout for chip erase, 2^n times typical (00h, not support)	26	0002

Table 4-3. CFI mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Data (h)
Device size = 2^n in number of bytes (19=256Mb, 18=128Mb)	27	0019/ 0018
Flash device interface description (refer to CFI publication 100)	28	0002
	29	0000
Maximum number of bytes in buffer write = 2^n (00h, not support)	2A	0006
	2B	0000
Number of erase regions within device (01h:uniform, 02h:boot)	2C	0001
Index for Erase Bank Area 1: [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 64KW 256Mb=00FF, 0000, 0000, 0002 128Mb=007F, 0000, 0000, 0002	2D	00xx
	2E	0000
	2F	0000
	30	0002
Index for Erase Bank Area 2	31	0000
	32	0000
	33	0000
	34	0000
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0033
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0014
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0001
Temporary sector unprotect (1=supported)	48	0000
Sector protect/Chip unprotect scheme	49	0008
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4C	0002
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	0095
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	00A5
WP# Protection 04=Uniform sectors bottom WP# protect 05=Uniform sectors top WP# protect	4F	0004/ 0005
Program Suspend (0=not support, 1=support)	50	0001

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS

|		
Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0 V
	A9, WP#/ACC	-0.5V to +10.5 V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade	Surrounding Temperature (T$_A$)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T$_A$)	-40°C to +85°C
VCC Supply Voltages	VCC range	+2.7 V to 3.6 V

DC CHARACTERISTICS

Symbol	Description	Min.	Typ.	Max.	Remark
Iilk	Input Leak			±2.0uA	
Iilk9	A9 Leak			35uA	A9=10.5V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current		6mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=1MHz
			30mA	50mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=5MHz
			60mA	100mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
Icr2	VCC Page Read Current		2mA	10mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=10MHz
			5mA	20mA	CE#=Vil, OE#=Vih, Vcc=Vccmax; f=33MHz
Iio	V_{IO} non-active current		0.2mA	10mA	
Icw	Write Current		26mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		30uA	100uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		30uA	100uA	Vcc=Vccmax, RESET# enable, other pin disable
Isbs	Sleep Mode Current		30uA	100uA	
Idpd	Vcc deep power down current		10uA		
Icp1	Accelerated Pgm Current, WP#/Acc pin		5mA	10mA	CE#=Vil, OE#=Vih
Icp2	Accelerated Pgm Current, Vcc pin		20mA	30mA	CE#=Vil, OE#=Vih
Vil	Input Low Voltage	-0.1V		0.3xVCC	
Vih	Input High Voltage	0.7xVCC		VCC+0.3V	
Vhv	Very High Voltage for hardware Auto Select/Accelerated Program	9.5V		10.5V	
Vol	Output Low Voltage			0.45V	Iol=100uA
Voh1	Ouput High Voltage	0.85xVCC			Ioh1=-100uA
Voh2	Ouput High Voltage	VCC-0.4V			Ioh2=-100uA
Vlko	Low Vcc Lock-out voltage	2.3V		2.5V	

SWITCHING TEST CIRCUITS
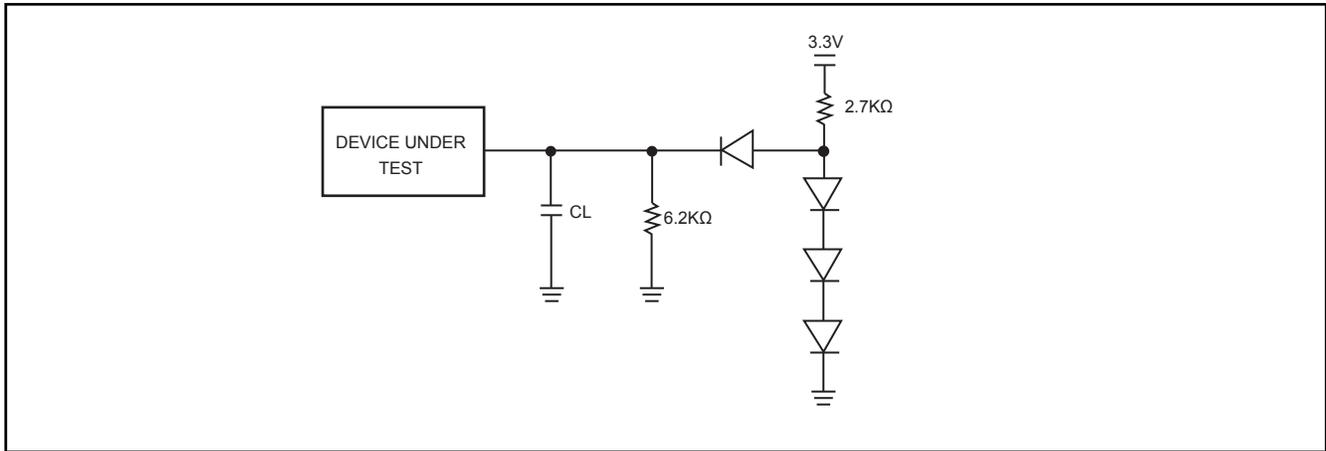
Test Condition
Output Load Capacitance, CL : 1TTL gate, 30pF(90ns)
Rise/Fall Times : 5ns
Input pulse levels : 0.0 ~ VCC
In/Out reference levels : VCC / 2

## SWITCHING TEST WAVEFORMS
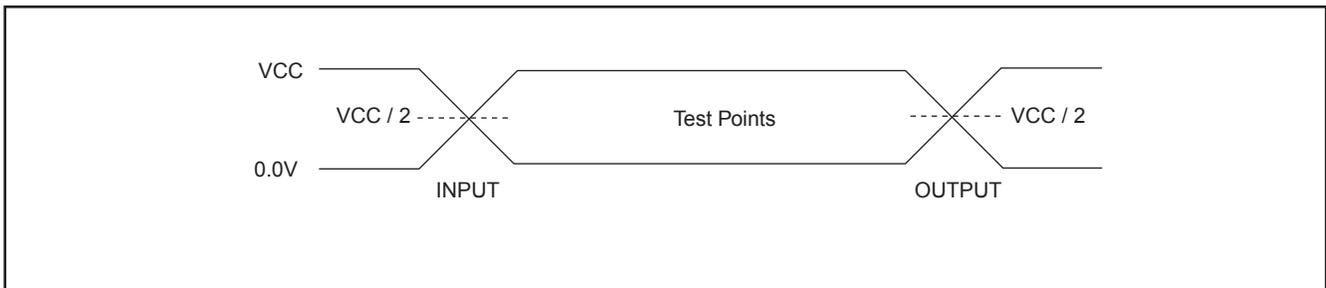
AC CHARACTERISTICS-(1)

Symbol	Description		29GL129E (VCC=2.7V~3.6V)			Unit
			Min.	Typ.	Max.	
Taa	Valid data output after address				90	ns
Tpa	Page access time				25	ns
Tce	Valid data output after CE# low				90	ns
Toe	Valid data output after OE# low				25	ns
Tdf	Data output floating after OE# high				20	ns
Tsrw	Latency between read and write operation		35			ns
Toh	Output hold time from the earliest rising edge of address,CE#, OE#		0			ns
Trc	Read period time		90			ns
Twc	Write period time		90			ns
Tcwc	Command write period time		90			ns
Tas	Address setup time		0			ns
Taso	Address setup time to OE# low during toggle bit polling		15			ns
Tah	Address hold time		45			ns
Taht	Address hold time from CE# or OE# high during toggle bit polling		0			ns
Tds	Data setup time		30			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		500			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcepw	CE# pulse width		35			ns
Tcepwh	CE# pulse width high		30			ns
Twp	WE# pulse width		35			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation			11		us
Twhwh1	Acc program operation			11		us
Twhwh2	Sector erase operation			0.6	5	sec
Tbal	Sector add hold time				50	us
Trdp	Release from deep power down mode				200	us

AC CHARACTERISTICS-(2)

| Symbol	Description		29GL257E (VCC=2.7V~3.6V)			29GL257E (VCC=3.0V~3.6V)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Taa	Valid data output after address				100			90	ns
Tpa	Page access time				25			25	ns
Tce	Valid data output after CE# low				100			90	ns
Toe	Valid data output after OE# low				25			25	ns
Tdf	Data output floating after OE# high				20			20	ns
Tsrw	Latency between read and write operation		35			35			ns
Toh	Output hold time from the earliest rising edge of address,CE#, OE#		0			0			ns
Trc	Read period time		100			90			ns
Twc	Write period time		100			90			ns
Tcwc	Command write period time		100			90			ns
Tas	Address setup time		0			0			ns
Taso	Address setup time to OE# low during toggle bit polling		15			15			ns
Tah	Address hold time		45			45			ns
Taht	Address hold time from CE# or OE# high during toggle bit polling		0			0			ns
Tds	Data setup time		30			30			ns
Tdh	Data hold time		0			0			ns
Tvcs	Vcc setup time		500			500			us
Tcs	Chip enable Setup time		0			0			ns
Tch	Chip enable hold time		0			0			ns
Toes	Output enable setup time		0			0			ns
Toeh	Output enable hold time	Read	0			0			ns
		Toggle & Data# Polling	10			10			ns
Tws	WE# setup time		0			0			ns
Twh	WE# hold time		0			0			ns
Tcepw	CE# pulse width		35			35			ns
Tcepwh	CE# pulse width high		30			30			ns
Twp	WE# pulse width		35			35			ns
Twph	WE# pulse width high		30			30			ns
Tbusy	Program/Erase active time by RY/BY#				100			90	ns
Tghwl	Read recover time before write		0			0			ns
Tghel	Read recover time before write		0			0			ns
Twhwh1	Program operation			11			11		us
Twhwh1	Acc program operation			11			11		us
Twhwh2	Sector erase operation			0.6	5		0.6	5	sec
Tbal	Sector add hold time				50			50	us
Trdp	Release from deep power down mode				200			200	us

Note : Not 100% tested.

Figure 1. COMMAND WRITE OPERATION

VA: Valid Address
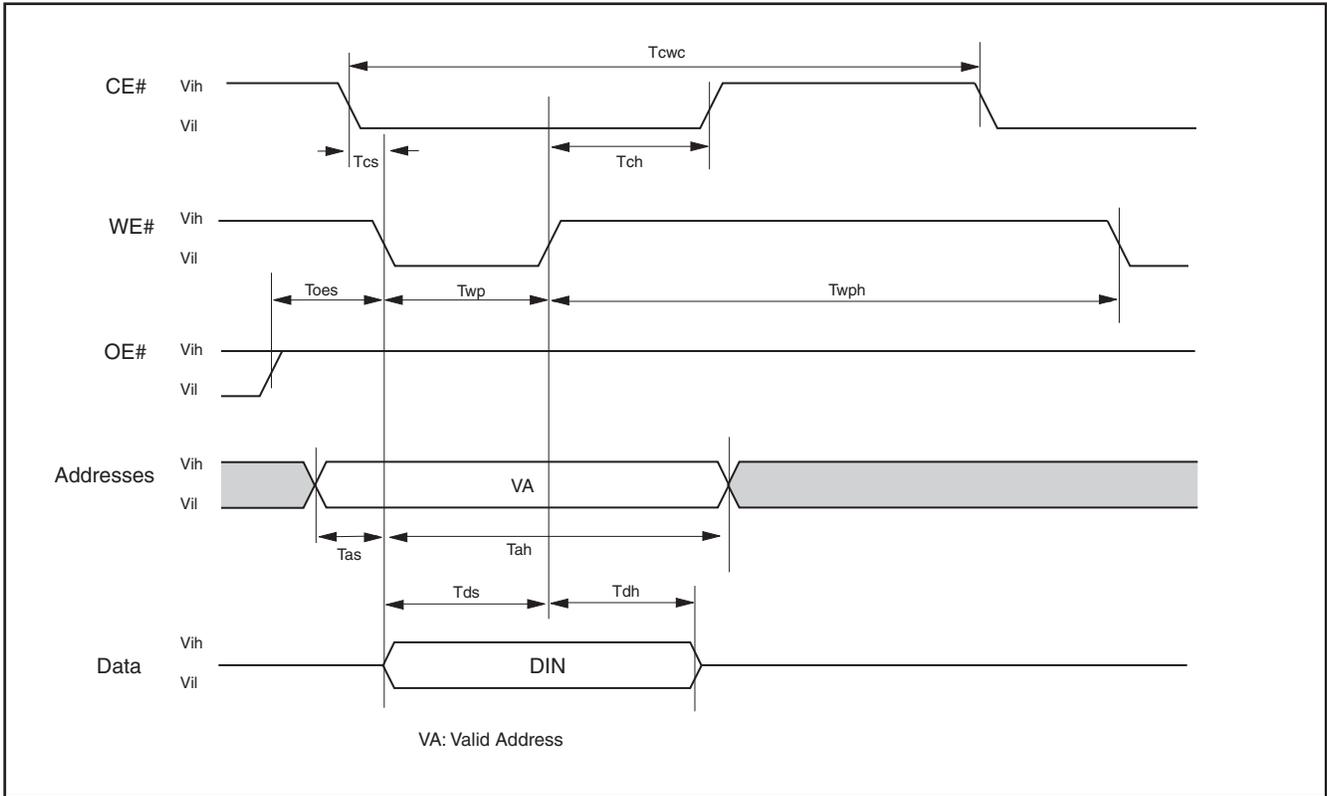
READ/RESET OPERATION

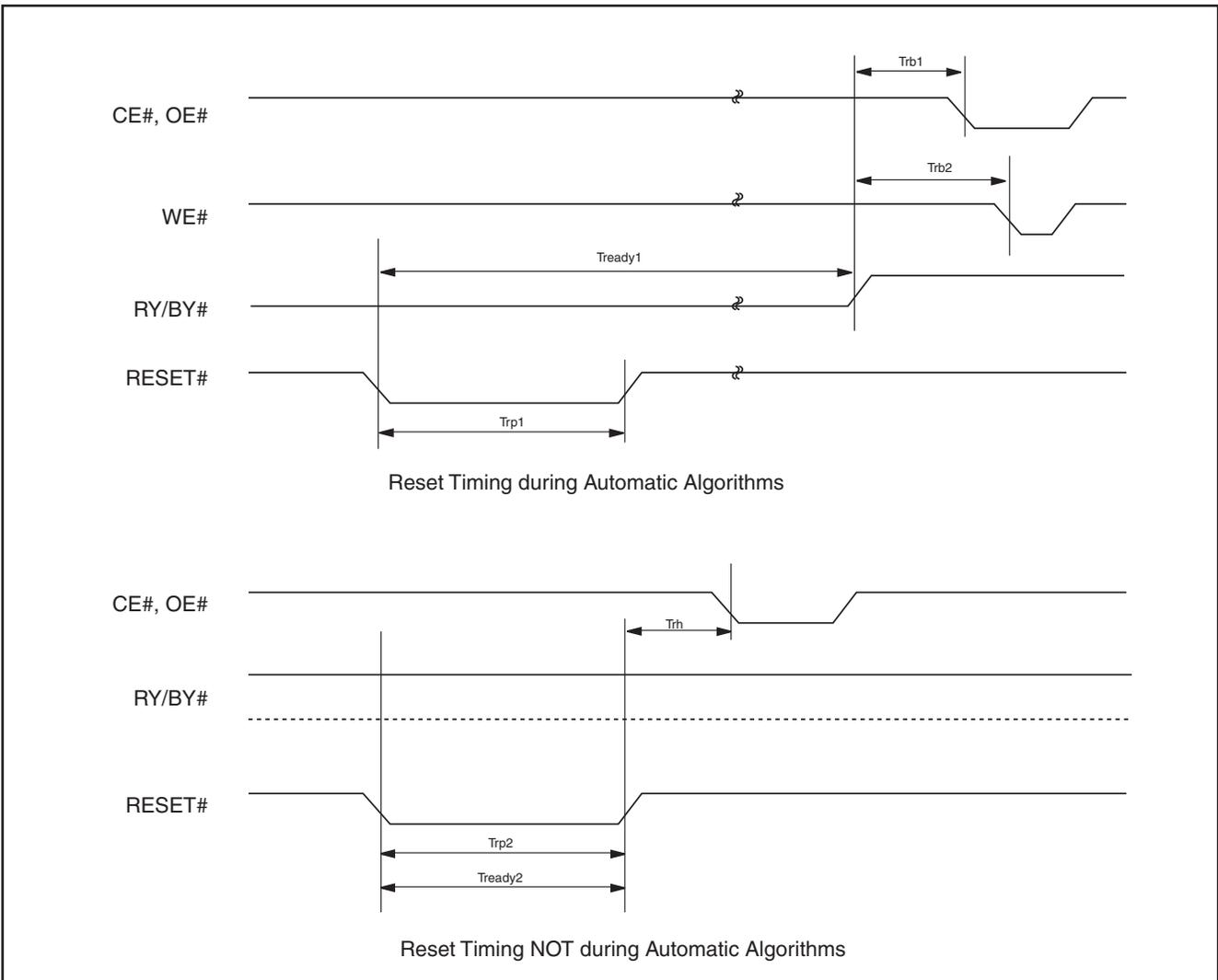**Figure 2. READ TIMING WAVEFORMS**
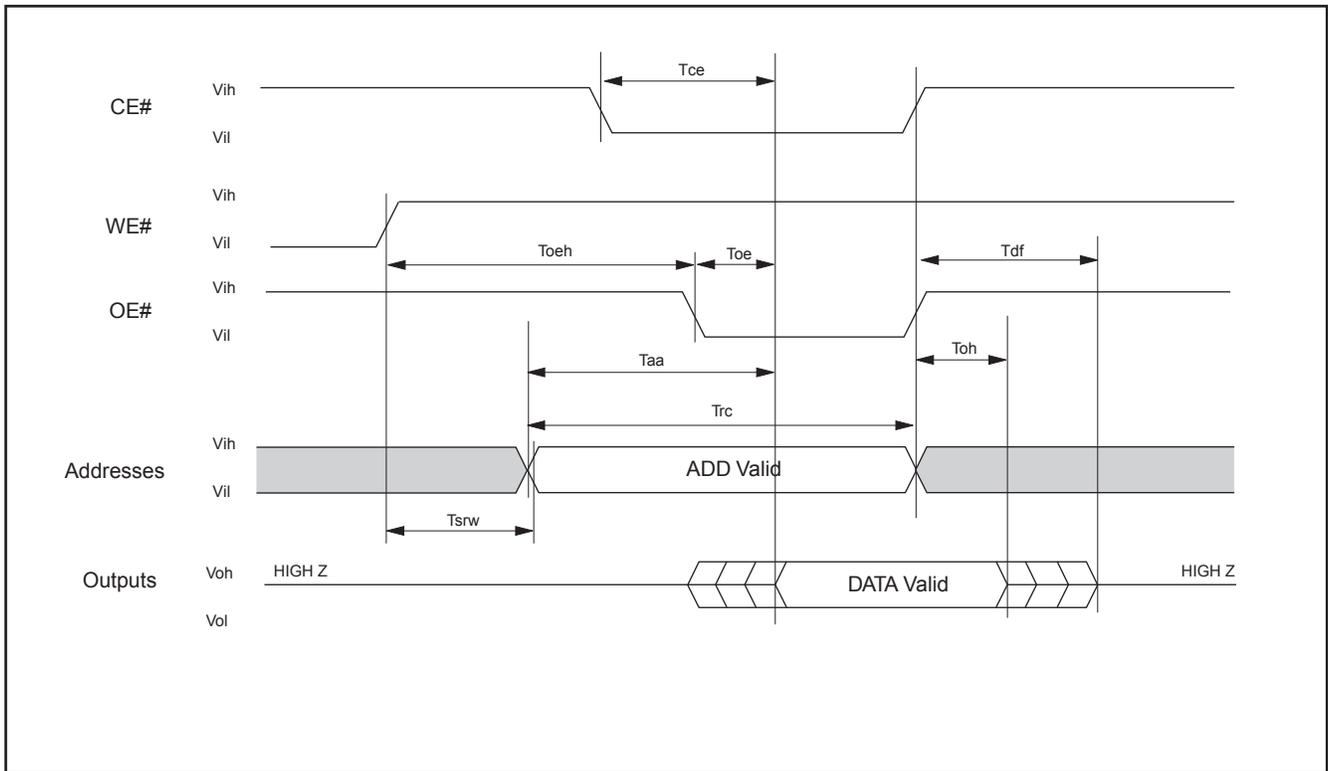
AC CHARACTERISTICS

Item	Description	MIN/MAX	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	200	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM

Reset Timing during Automatic Algorithms

Reset Timing NOT during Automatic Algorithms

ERASE/PROGRAM OPERATION

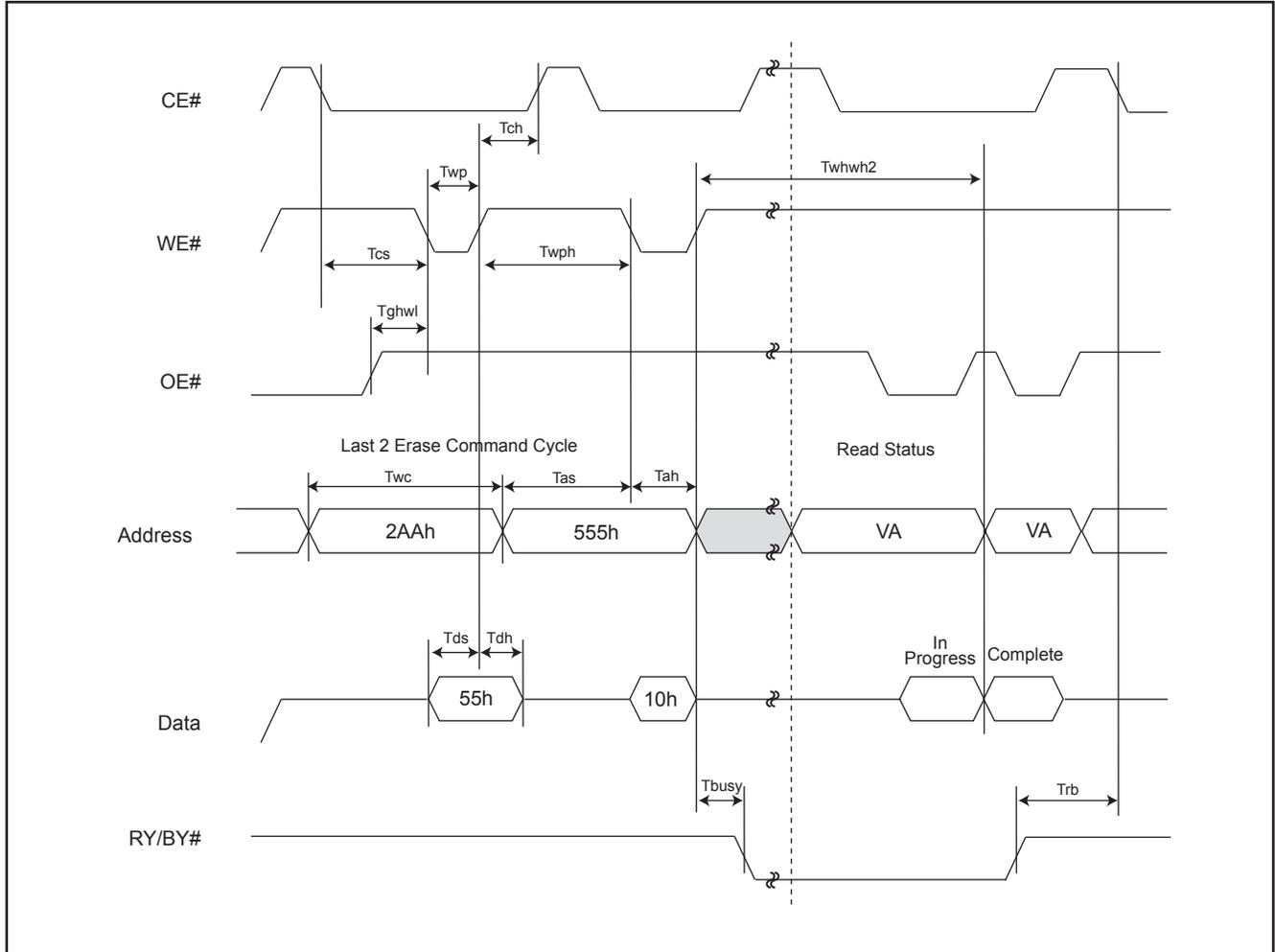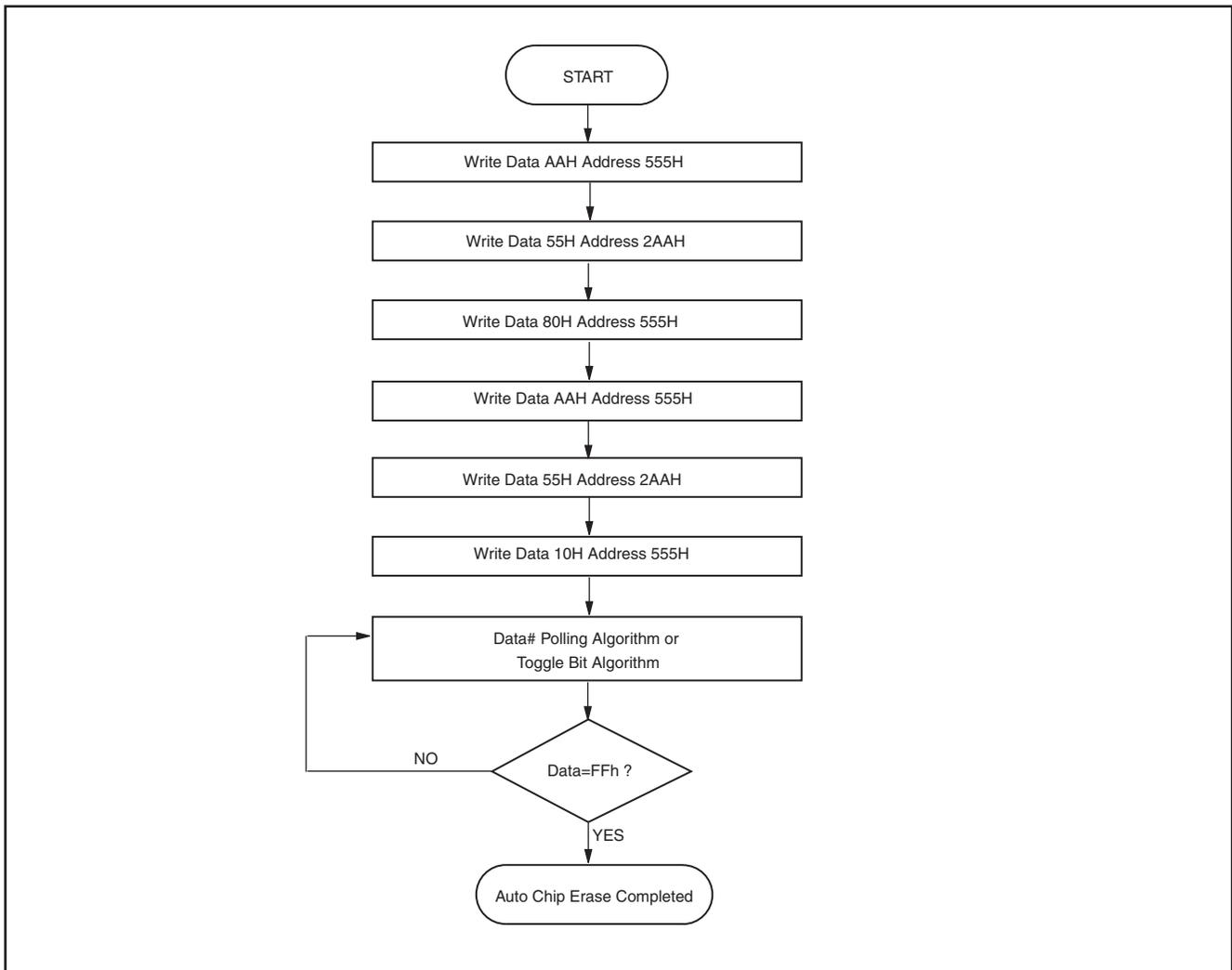### Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART
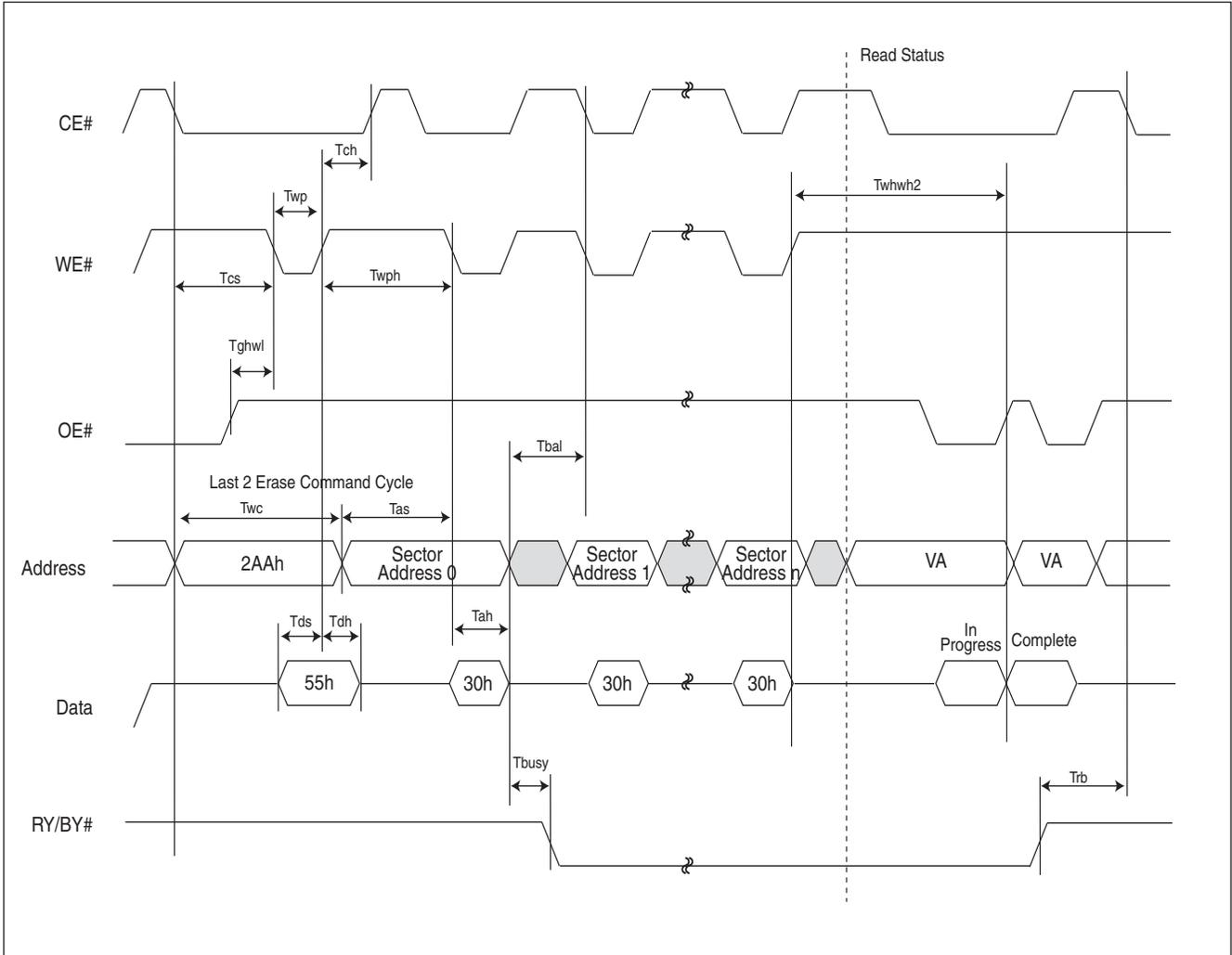
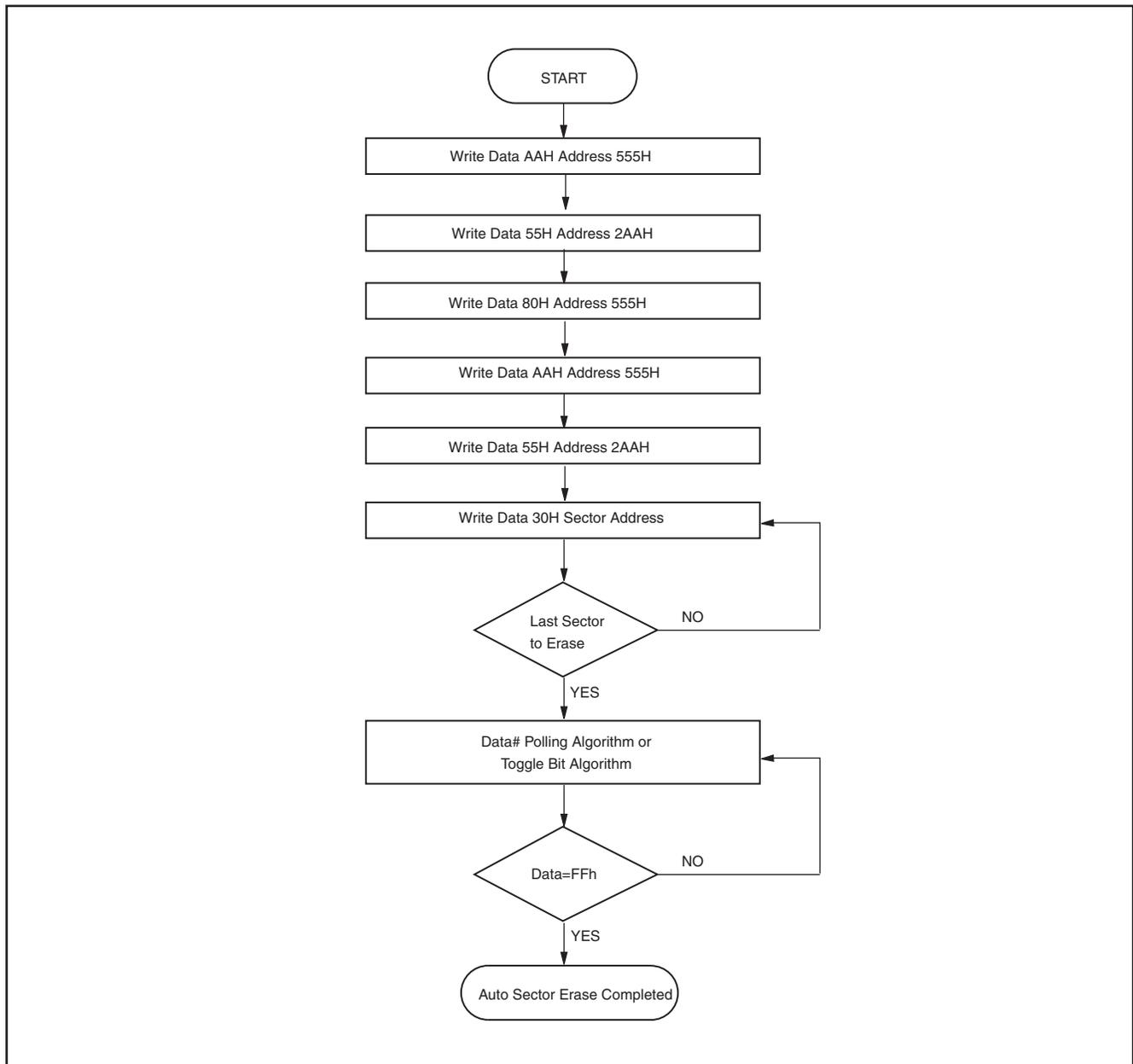**Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM**

Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

```
                          ┌─────────┐
                          │  START  │
                          └────┬────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data AAH Address 555H     │
              └────────────────┬────────────────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data 55H Address 2AAH     │
              └────────────────┬────────────────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data 80H Address 555H     │
              └────────────────┬────────────────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data AAH Address 555H     │
              └────────────────┬────────────────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data 55H Address 2AAH     │
              └────────────────┬────────────────┘
                               │
              ┌────────────────▼────────────────┐
              │  Write Data 30H Sector Address   │◄──────┐
              └────────────────┬────────────────┘       │
                               │                         │
                          ╱────▼────╲            NO       │
                         ╱ Last Sector ╲─────────────────┘
                         ╲  to Erase   ╱
                          ╲────┬────╱
                               │ YES
              ┌────────────────▼────────────────┐
              │  Data# Polling Algorithm or      │◄──────┐
              │  Toggle Bit Algorithm            │       │
              └────────────────┬────────────────┘       │
                               │                         │
                          ╱────▼────╲            NO       │
                         ╱ Data=FFh   ╲──────────────────┘
                          ╲────┬────╱
                               │ YES
                    ┌──────────▼──────────────┐
                    │ Auto Sector Erase Completed │
                    └─────────────────────────┘
```
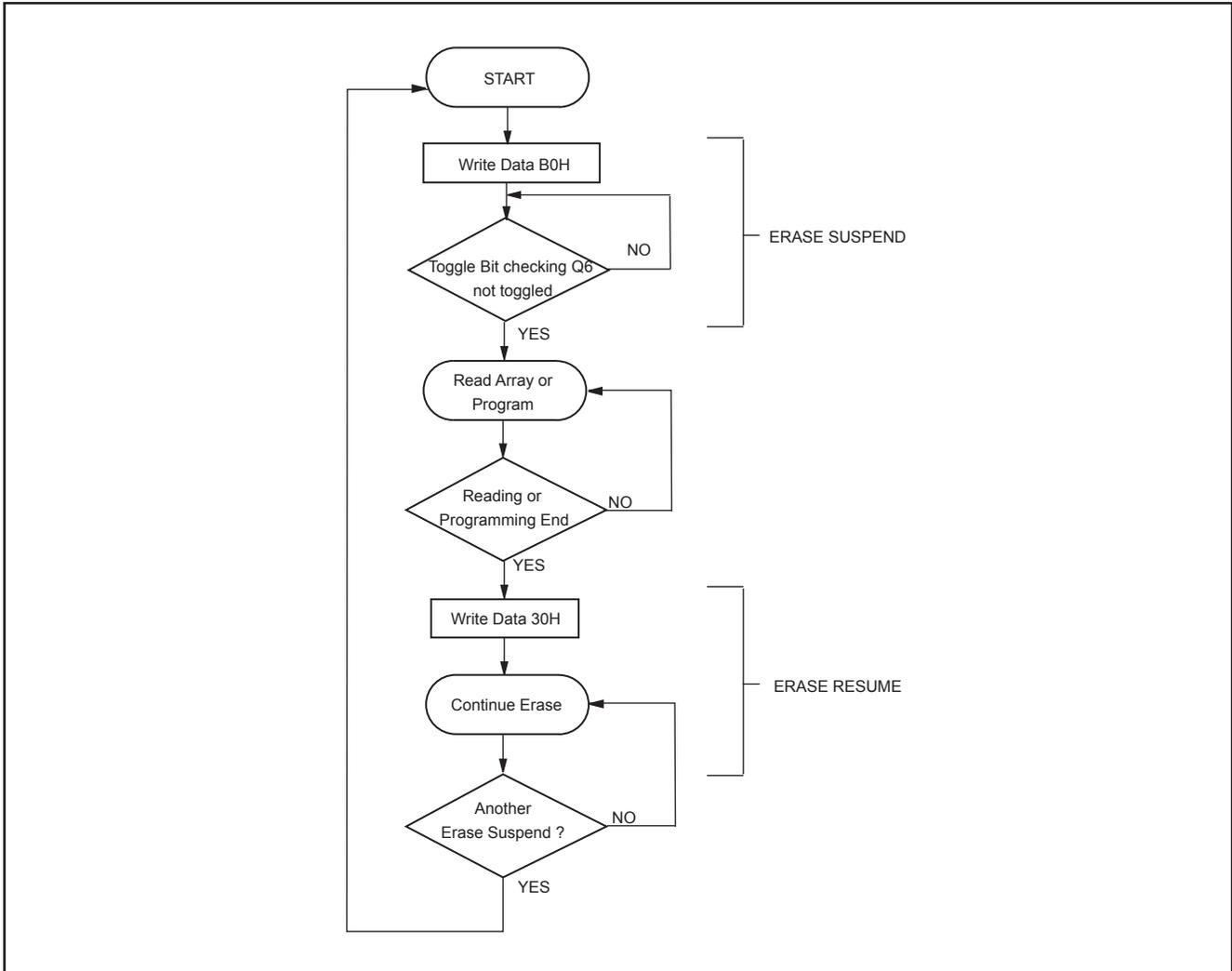
Figure 8. ERASE SUSPEND/RESUME FLOWCHART

Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS
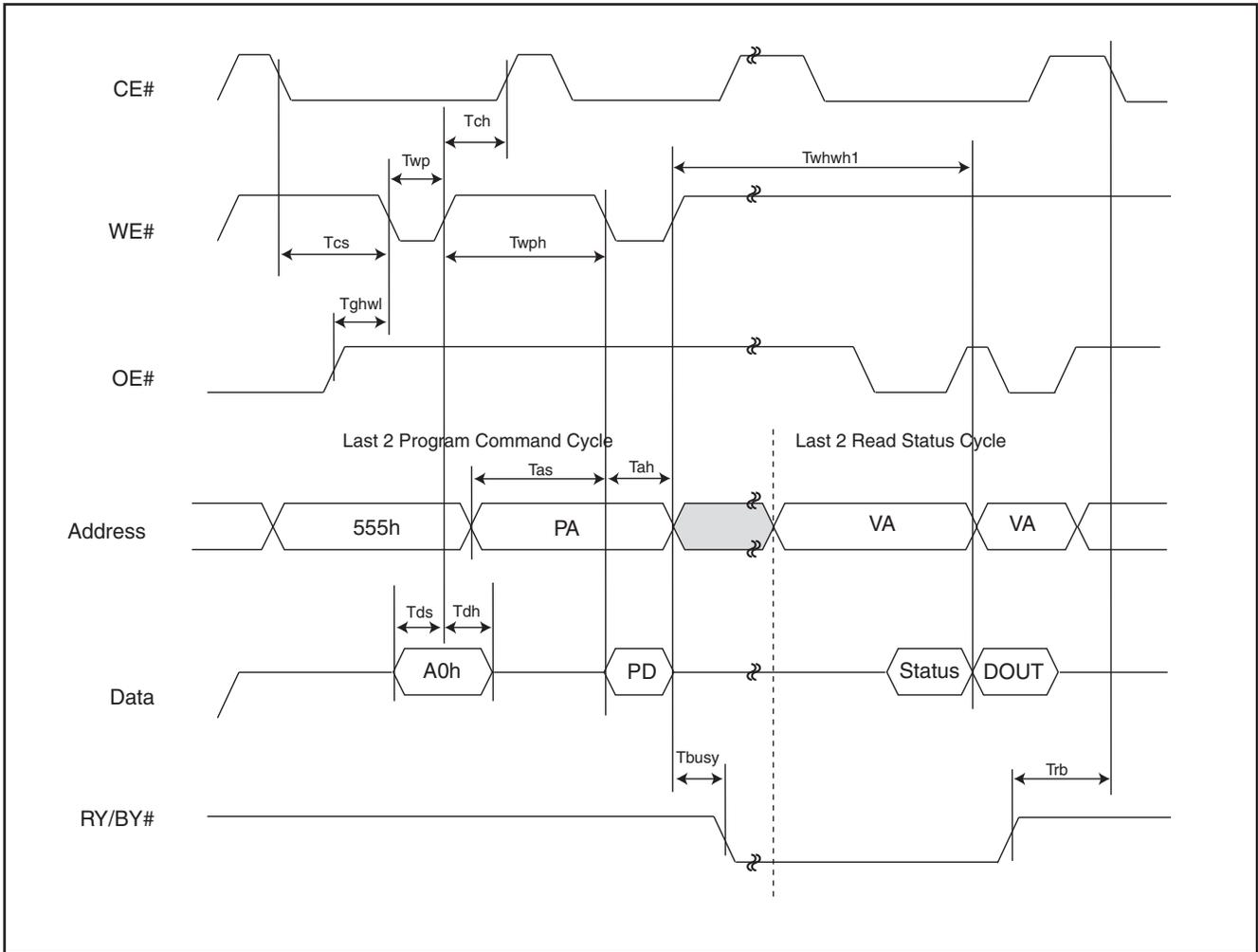
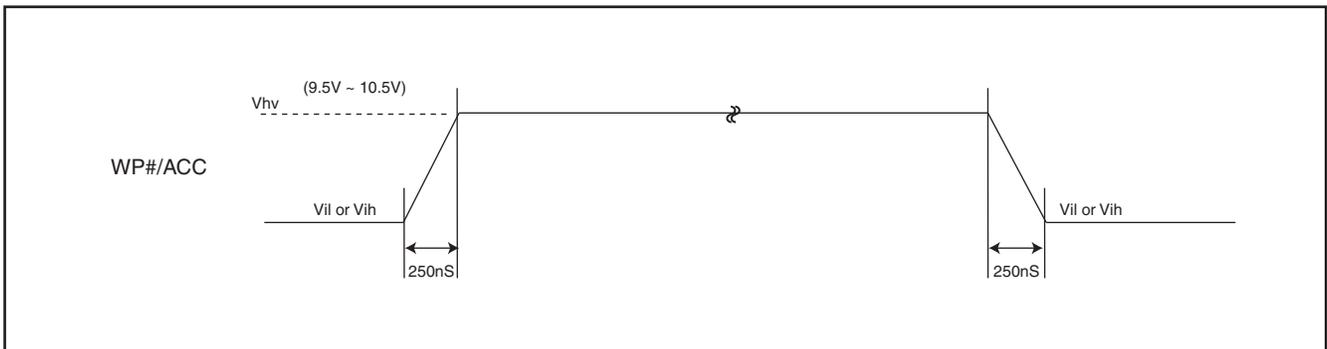**Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM**

Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART
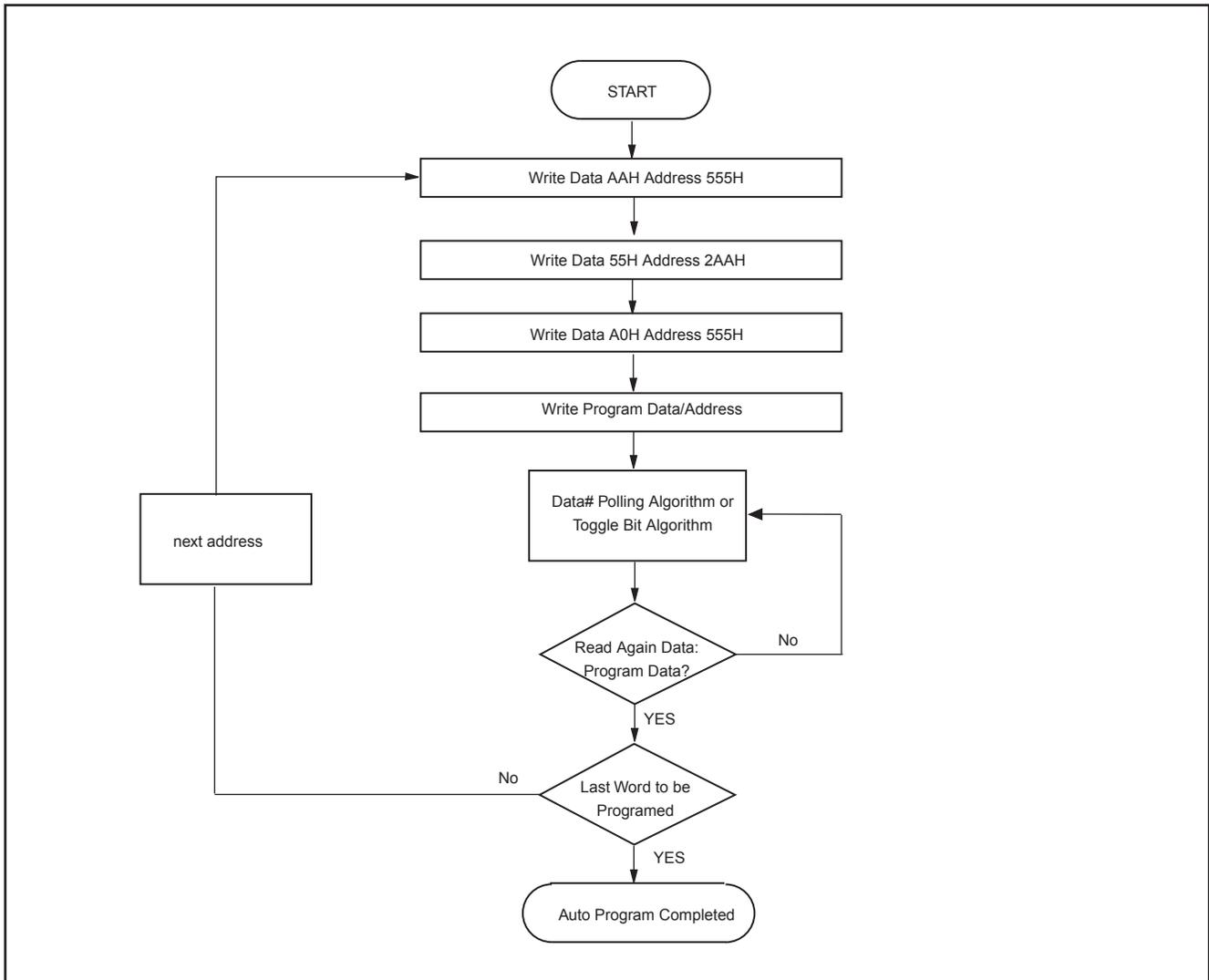
Figure 13. SILICON ID READ TIMING WAVEFORM

Manufacturer ID

Device ID Cycle 1

Device ID Cycle 2

Device ID Cycle 3
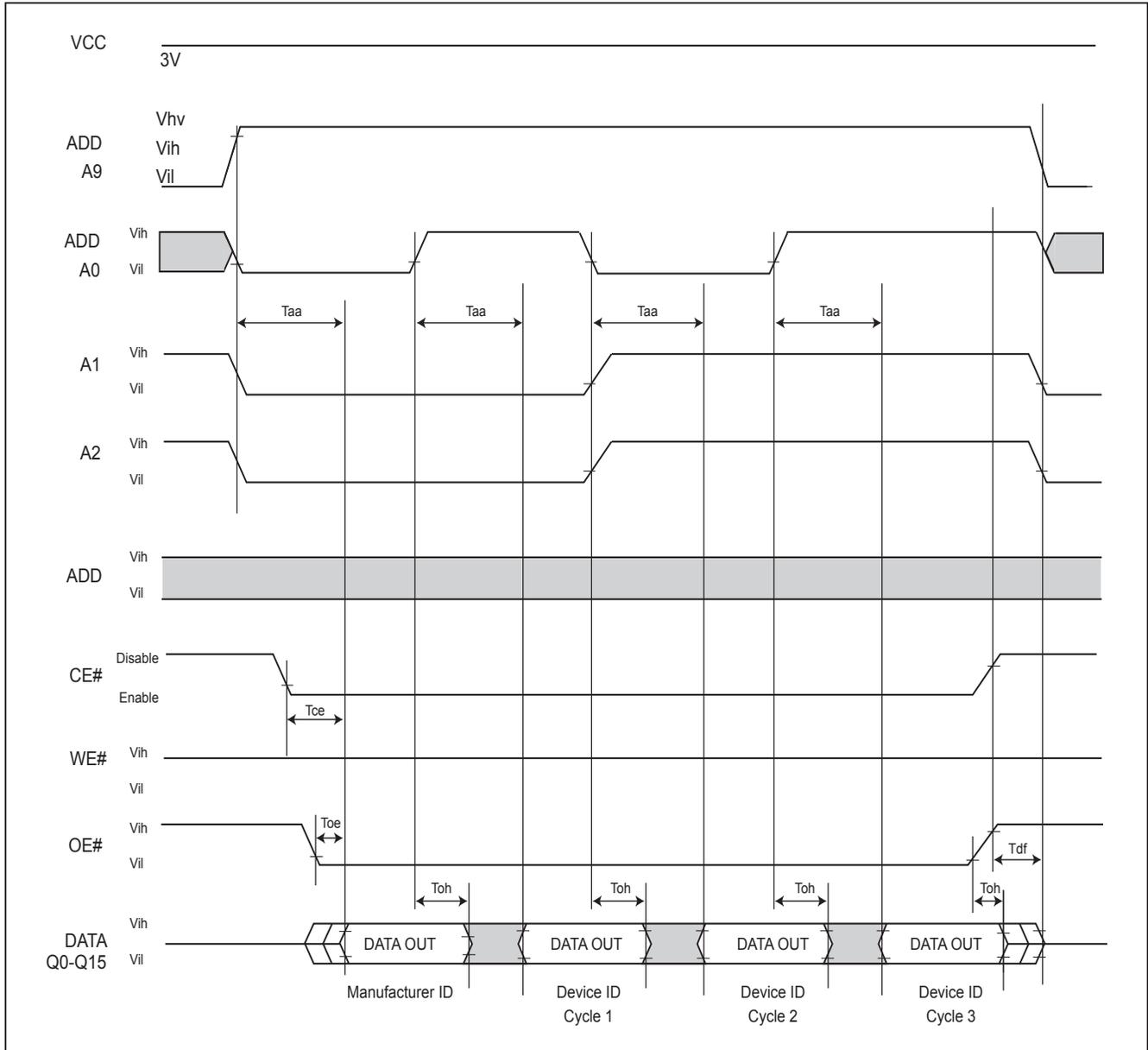
WRITE OPERATION STATUS

Figure 14. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)
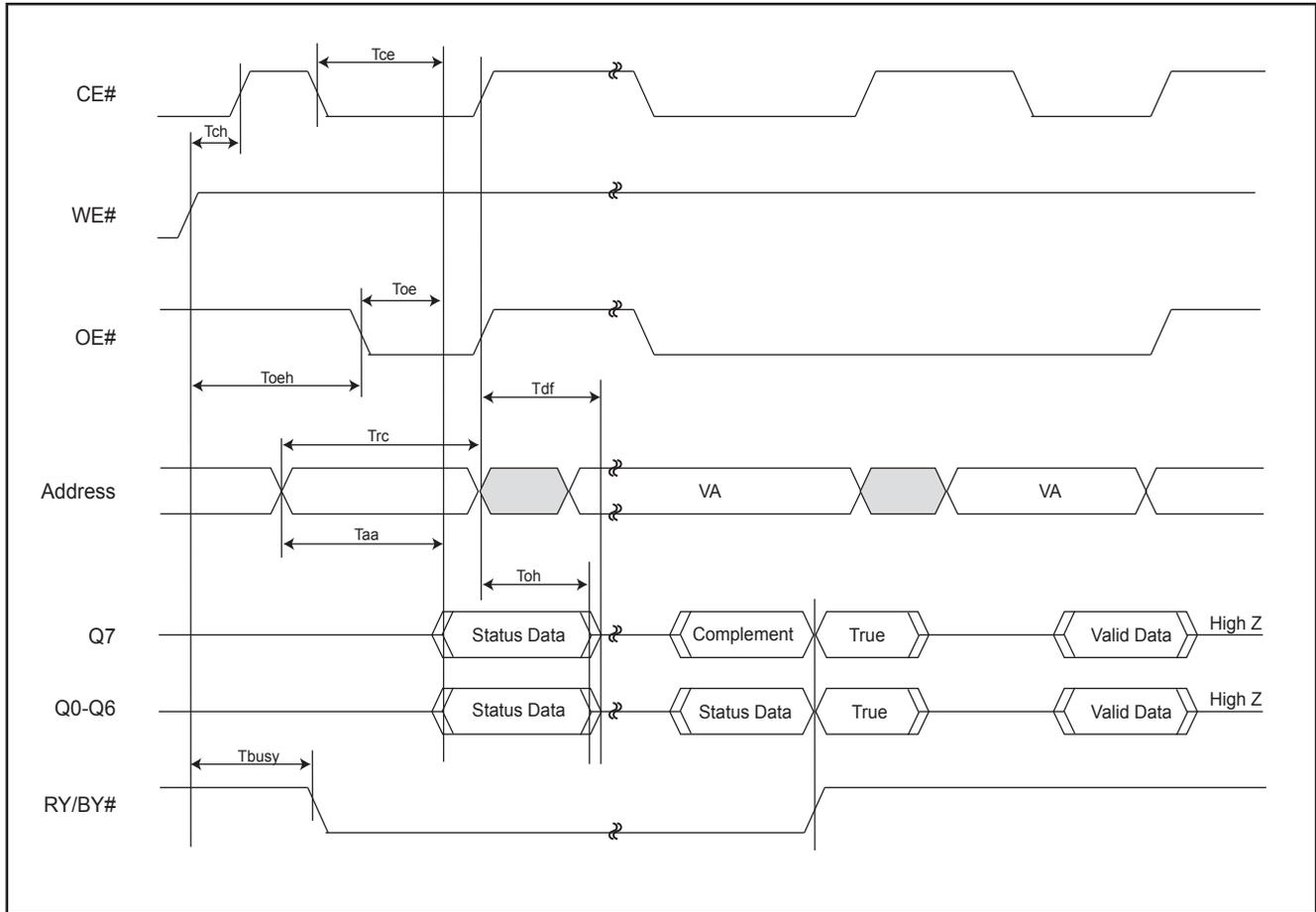
Figure 15. STATUS POLLING FOR WORD PROGRAM/ERASE
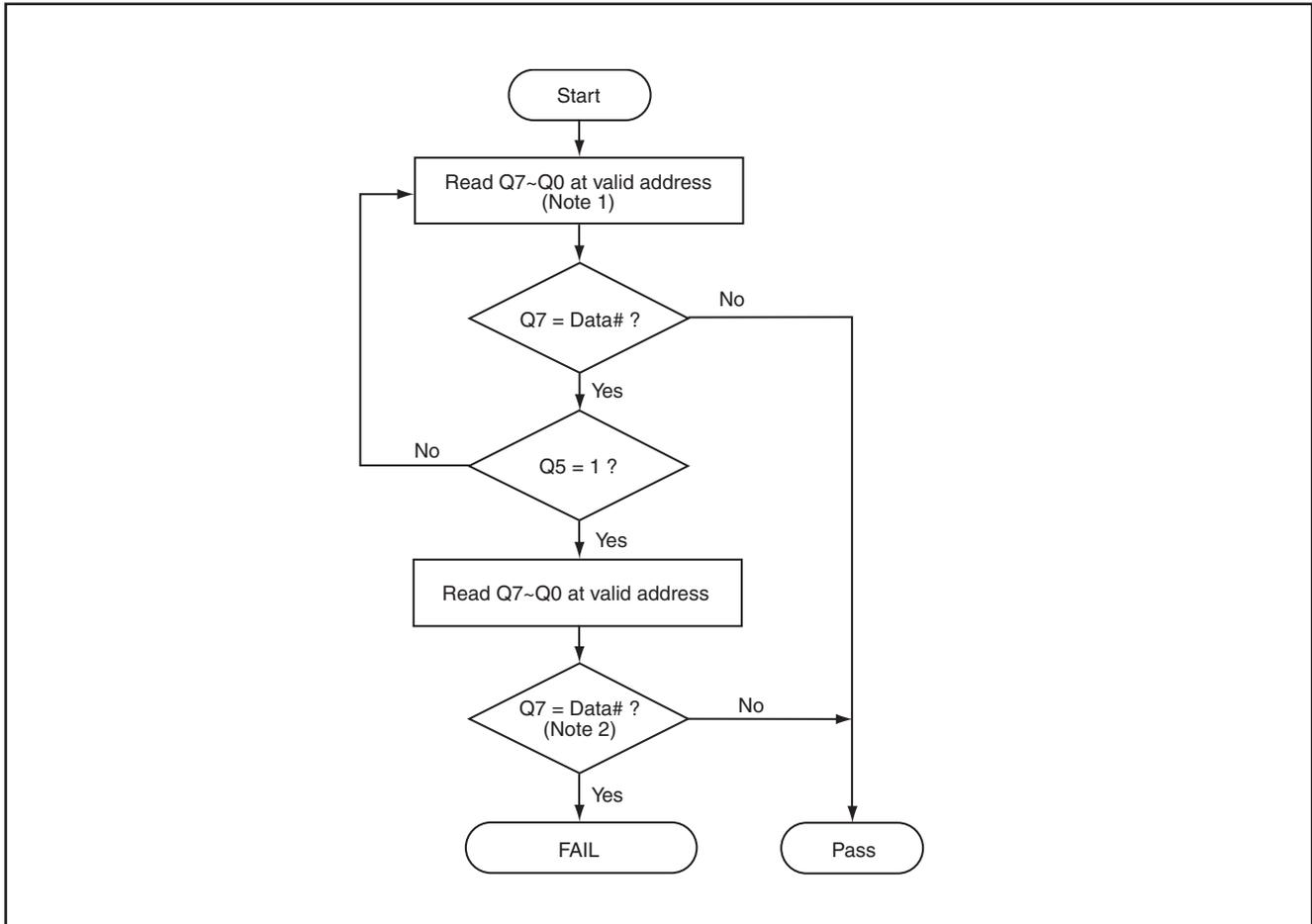
Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 16. STATUS POLLING FOR WRITE BUFFER PROGRAM
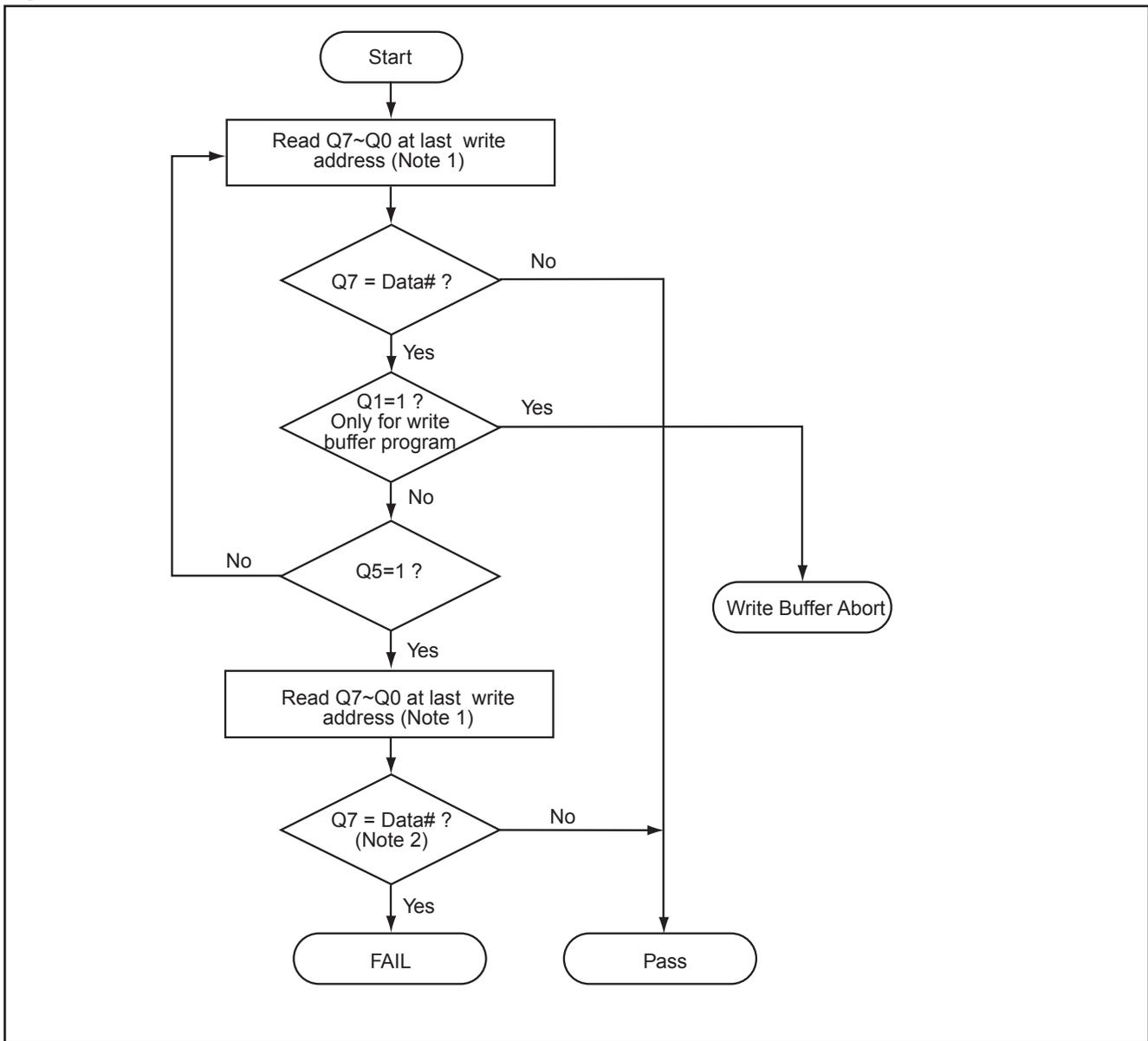
Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 17. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

VA : Valid Address
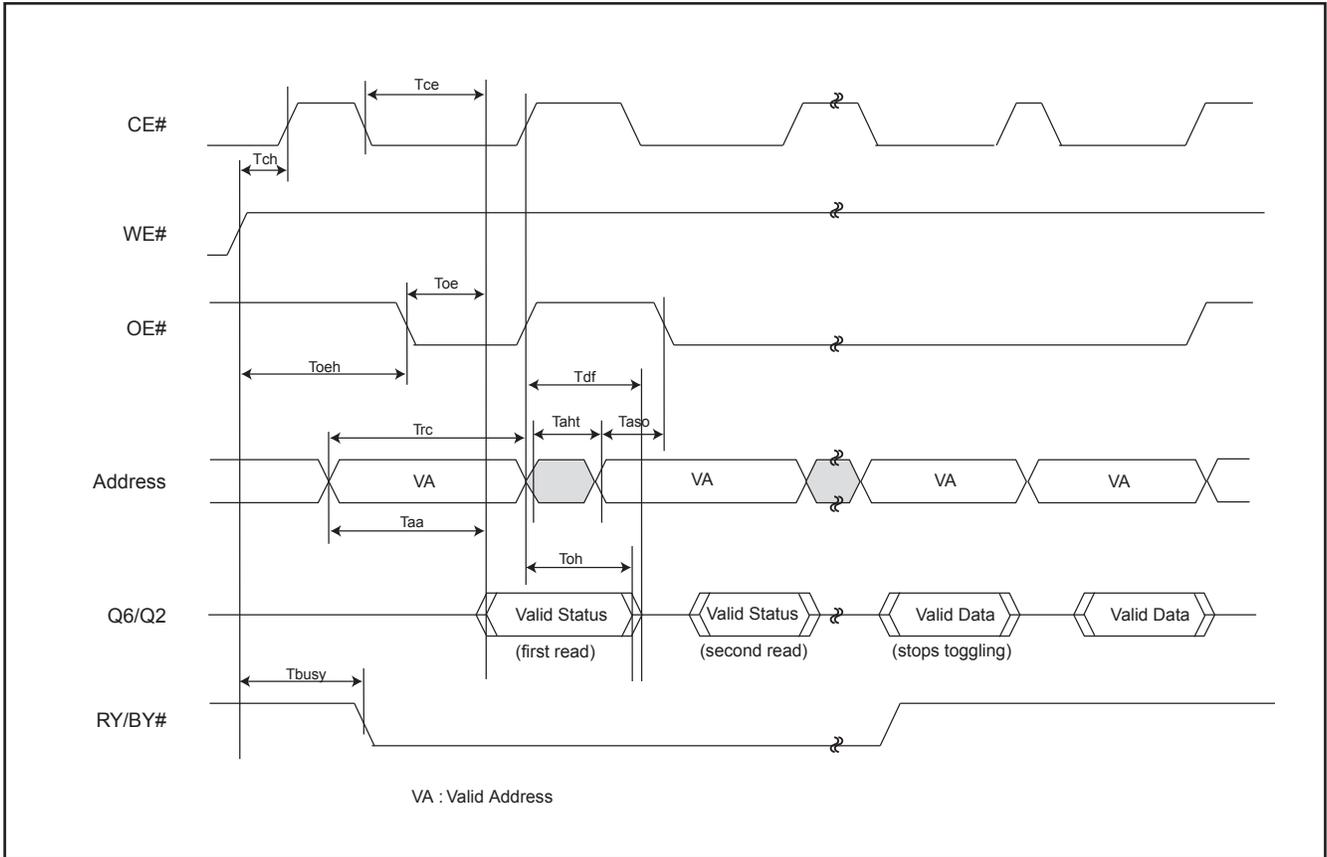
Figure 18. TOGGLE BIT ALGORITHM
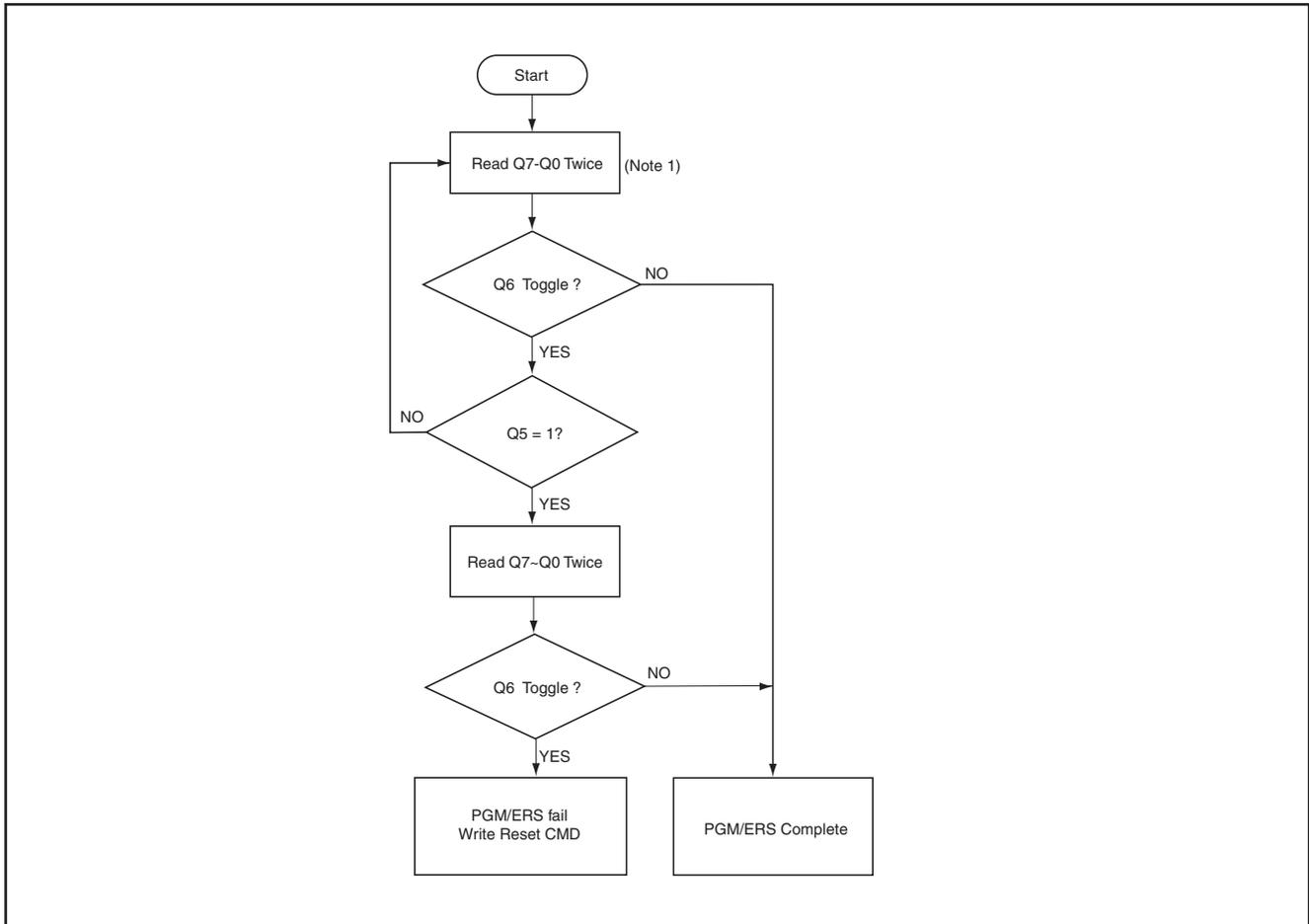
Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 19. PAGE READ TIMING WAVEFORM

Note: CE#, OE# are enable.
Page size is 8 words.
Address are A2~A0.
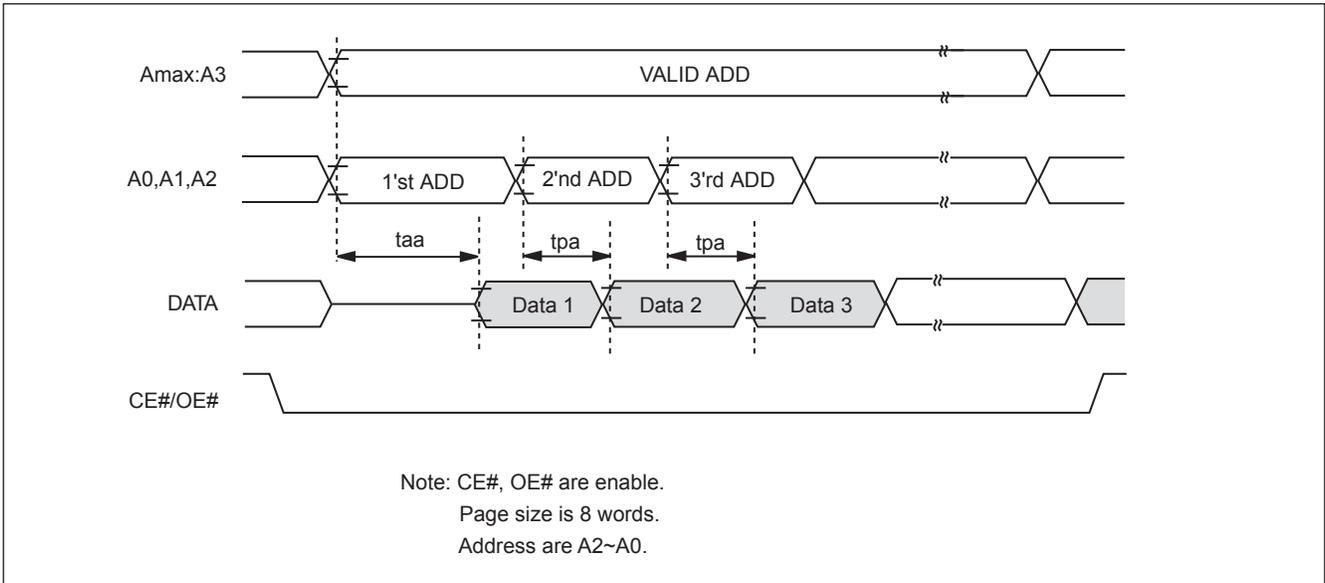
AC CHARACTERISTICS

ITEM		TYP	MAX
WEB high to release from deep power down mode	tRDP	100us	200us
WEB high to deep power down mode	tDP	10us	20us

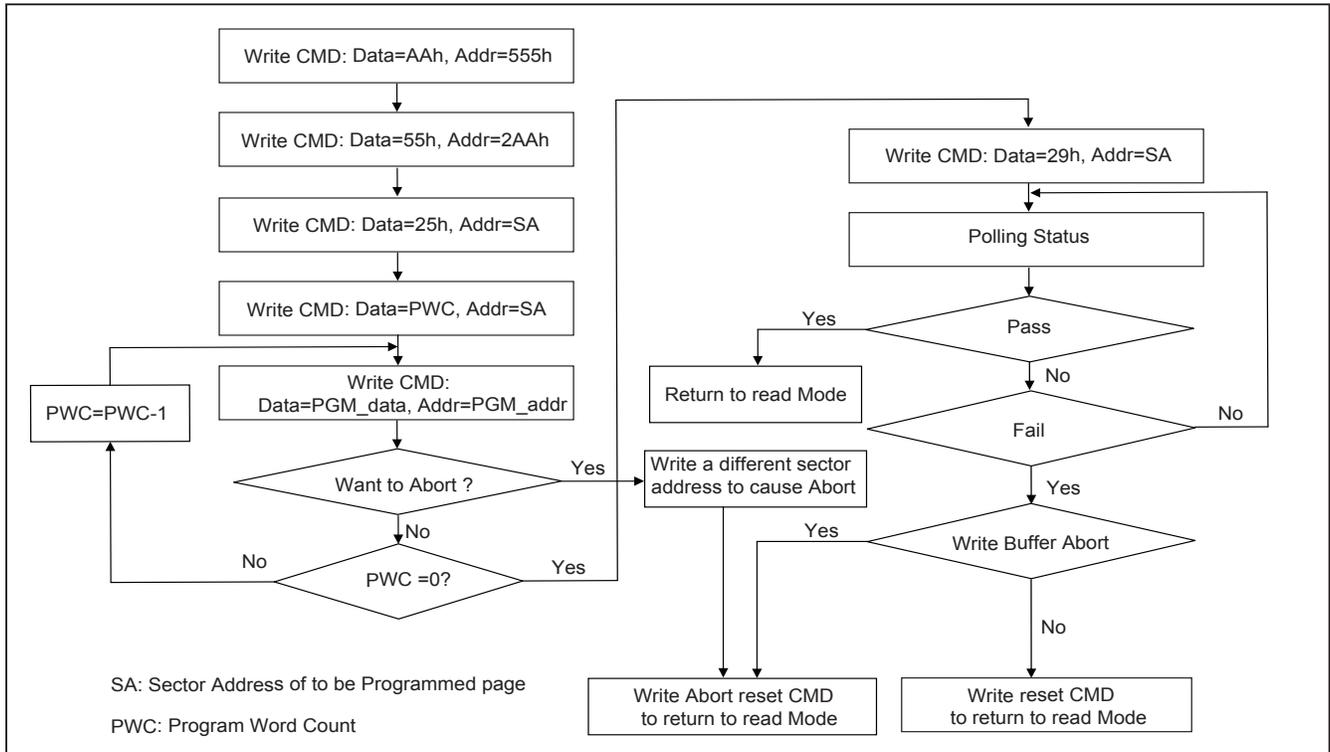**Figure 20. DEEP POWER DOWN MODE WAVEFORM**
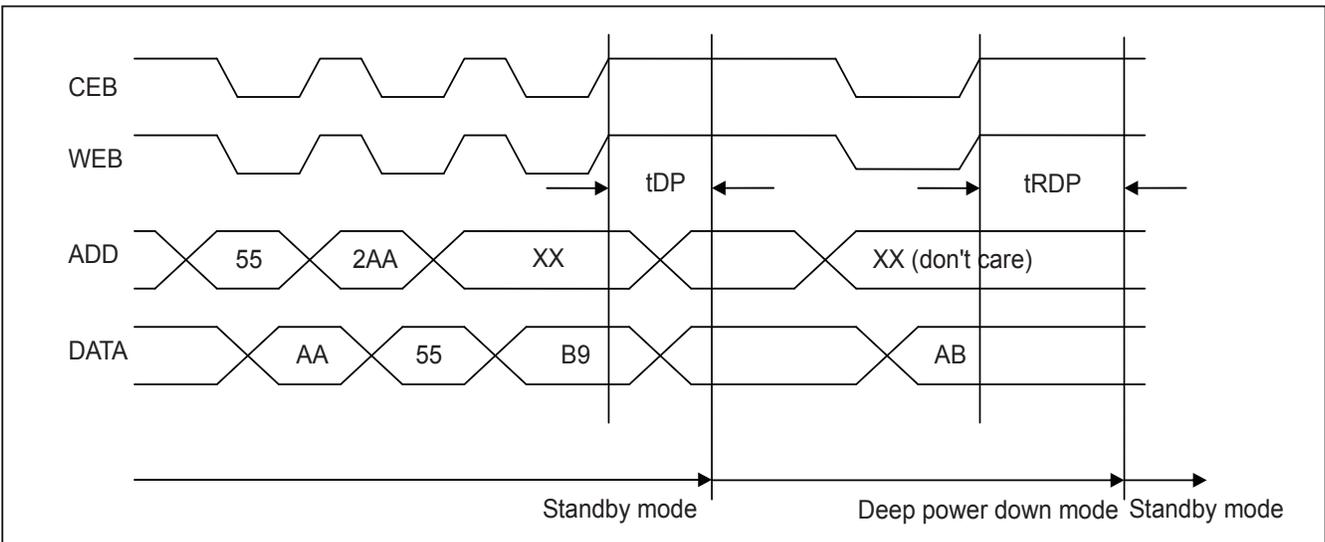
Figure 21. WRITE BUFFER PROGRAM FLOWCHART

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V
Tvcs	Vcc Setup Time	200		us

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		LIMITS			UNITS
		MIN.	TYP. (1)	MAX. (2)	
Chip Erase Time	128Mb		64	150	sec
	256Mb		128	300	sec
Sector Erase Time			0.6	5	sec
Chip Programming Time	128Mb		50	180	sec
	256Mb		100	350	sec
Word Program Time			11	360	us
Total Write Buffer Time			200		us
ACC Total Write Buffer Time			100		us
Erase/Program Cycles			100,000		Cycles

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.
4. Exclude 00h program before erase operation.

DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55°C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage voltage difference with GND on WP#/ACC, A9	-1.0V	10.5V
Input Voltage voltage difference with GND on all normal pins input	-1.0V	1.5Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

128Mb

MX29GA129E C/F			
PART NO.	ACCESS TIME (ns)	PACKAGE	Remark
MX29GA129ECXCI-90G	90	64 FBGA	Pb-free
MX29GA129EFXCI-90G	90	64 FBGA	Pb-free

256Mb

MX29GA257E C/F			
PART NO.	ACCESS TIME (ns)	PACKAGE	Remark
MX29GA257ECXCI-90Q	90	64 FBGA	Pb-free (Note 1)
MX29GA257EFXCI-90Q	90	64 FBGA	Pb-free (Note 1)

Note :
1. 90Q covers 2.7V~3.6V for 100ns and 3.0V~3.6V for 90ns.

PART NAME DESCRIPTION

MX   29   GA   129   E   C   XC   I   -   90   Q

OPTION:
G: Lead-free with Vcc: 2.7V~3.6V
Q: Lead-free with restricted Vcc: 3.0V~3.6V (Note 1)

SPEED:
90: 90ns

TEMPERATURE RANGE:
I: Industrial (-40° C to 85° C)

PACKAGE:
XC: FBGA (10mm x 13mm)

BOOT BLOCK TYPE:
C: Highest Address Sector Protected, with Read Protection
F: Lowest Address Sector Protected, with Read Protection

REVISION:
E

DENSITY & MODE:
129: 128Mb x16 Uniform Block
257: 256Mb x16 Uniform Block

TYPE:
GA: 3V Security Flash

DEVICE:
29:Flash

Note 1: 90Q covers 2.7V~3.6V for 100ns and 3.0V~3.6V for 90ns

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PACKAGE INFORMATION

Title: Package Outline for CSP 64BALL(10X13X1.2MM,BALL PITCH 1.00MM,BALL DIAMETER 0.4MM)

TOP VIEW

BOTTOM VIEW

SEATING PLANE

$\bigcirc$ | 0.10 | C
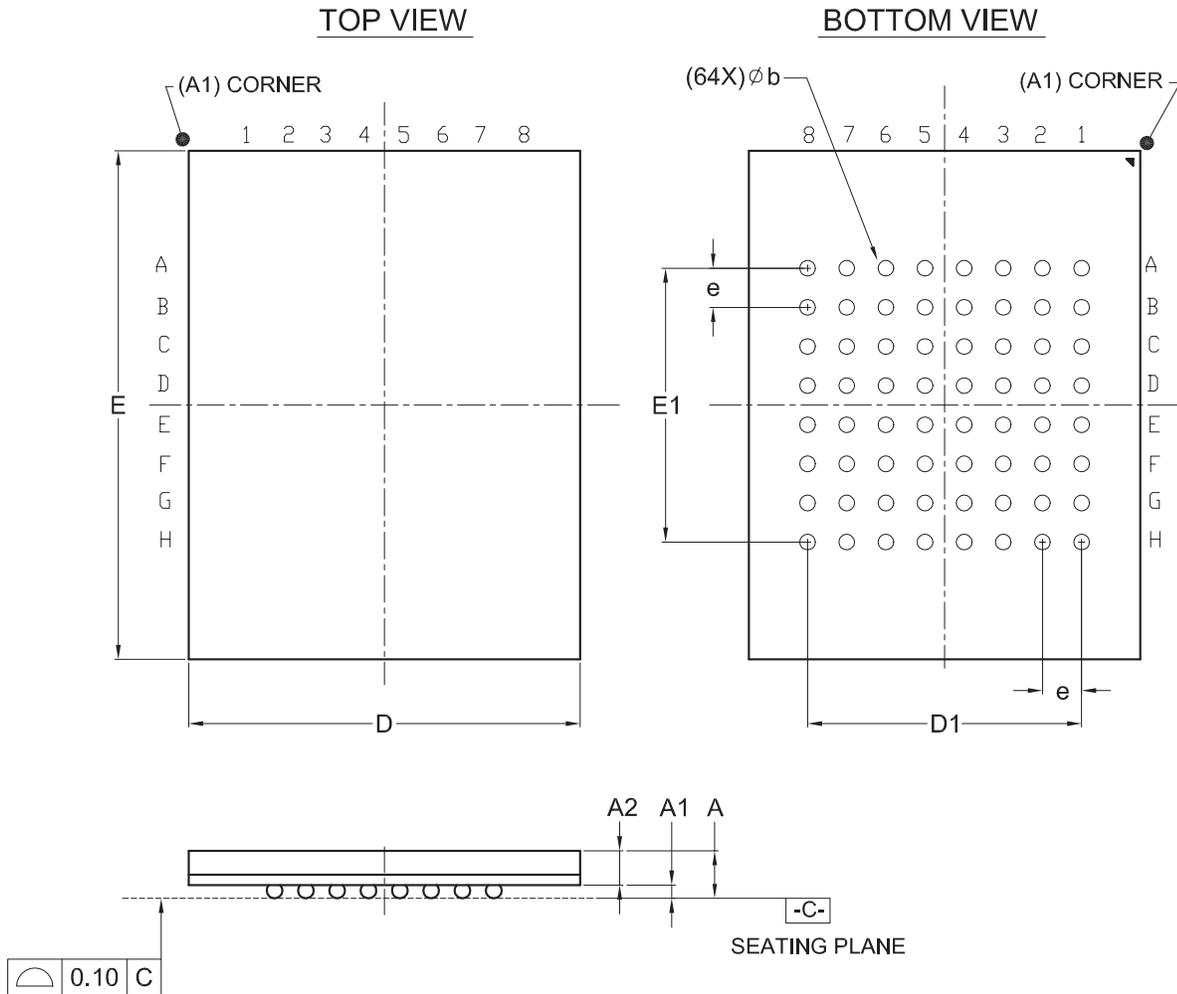
Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	9.90		12.90		
	Nom.	---	0.30	---	0.40	10.00	7.00	13.00	7.00	1.00
	Max.	1.20	0.35	---	0.45	10.10		13.10		
Inch	Min.	--	0.010	0.026	0.014	0.390		0.508		
	Nom.	--	0.012	---	0.016	0.394	0.276	0.512	0.276	0.039
	Max.	0.047	0.014	---	0.018	0.398		0.516		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4220	3	MO-216			12-15-'03

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Added Read Protection function application example flow chart and Read Protection mode unclock criteria description	P71~72	AUG/10/2009
	2. Modified Multual Authentication wave form description	P79	
	3. Modified Read Unlock command	P82	
	4. Changed data retention from 10-years to 20-years	P2	
	5. Added Icr2 into DC Characteristics	P35	
	6. Modified Tsrw(min.) from 20ns to 35ns	P37,38	
	7. Added figure 16. status polling for write buffer program	P53	

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