SoftAMC™ Audio Modem Codec

AMC '97 Audio Modem Codec with Host-Processed (HSF) V.90/K56flex™ Modem and Host-based Audio Software with AC-link Interface

The Conexant™ SoftAMC™ Audio Modem Codec (AMC) combines two coder/decoder functions, compliant with Intel Audio Codec '97 2.1 Extensions for a combo audio modem codec (AMC'97), into a single 64-pin TQFP.

The SoftAMC can operate with Conexant RipTide™ Audio Communications Controllers or Conexant-qualified AC'97-compliant core logic chip sets.

The SoftAMC supports one telephone line and is supplied with Conexant MMX-based HSF (SoftK56™) V.90/K56flex™ modem software. In ITU-T V.90/K56flex data mode, the modem can receive data at speeds up to 56 kbps from a digitally connected V.90 or K56flex-compatible central site modem and can send data at V.34 rates. In V.34 data mode, the modem operates at line speeds up to 33.6 kbps. When applicable, error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput. Non-error-correcting mode is also supported. Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

The SoftAMC is also supplied with either basic or enhanced audio software (Table 1).

A simplified block diagram of the SoftAMC is shown in Figure 1.

Distinguishing Features

- Combined Audio/Modem Codec (AMC)
  - AC '97 Codec V2.1 compliant (AMC '97)
- Advanced Power Management
- Audio
  - Stereo Full-Duplex Codec with 18-bit resolution
  - Six Audio Analog Input Channels
  - Three Audio Analog Output Channels
  - 3D Spatialization
  - Delta-Sigma Converter for enhanced performance
- Modem
  - Full-Duplex Codec with 16-bit resolution
  - 1-Line Telephone Line Interface
  - Dedicated Handset ADC/DAC
  - Dedicated Microphone ADC
  - Caller ID Decode and Storage
  - Analog On Hold and Call Progress
  - External audio amplifier on/off control
- 9 GPIO Lines
- Standard 64-pin TQFP package

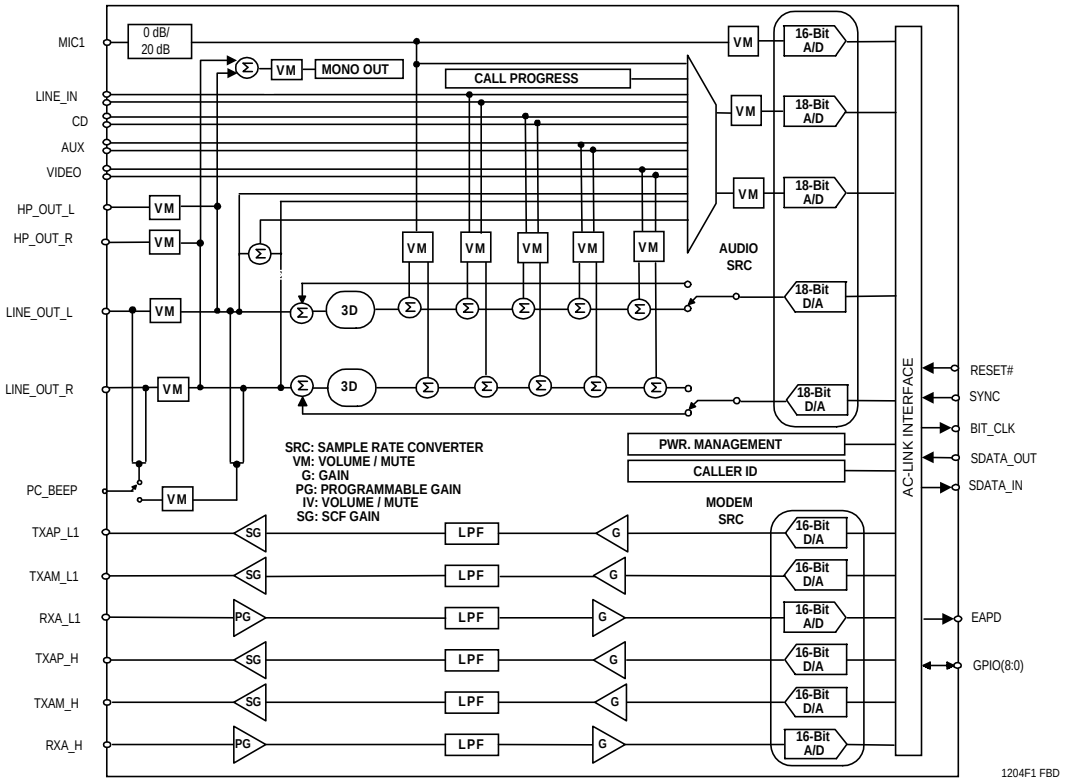


Figure 1. SoftAMC Functional Block Diagram

Ordering Information

Table 1. SoftAMC Models and Options

		Supplied Software		
Marketing Model No.	Part Number	SoftK56 Modem Software	Basic Audio Software	Enhanced Audio Software
RAMC021	20432-32	Y	Y	—
RAMC021	20432-32	Y	—	Y

Notes:
Supported functions (Y = Supported; – = Not supported):

System Description

System Solution

A block diagram of a typical PCI Audio/Communications System is shown in Figure 2.

Audio Modem Codec (AMC)

The AMC supports one telephone line.

The AMC communicates to the Conexant RipTide Audio/Communications Controller (ACC) or other Conexant-qualified AC'97-compatible core logic device set through a digital serial link (AC-link). All digital data audio stream, modem data (telephone stream, handset, and microphone), GPIO data, and codec command/status information is transferred between the controller and the codec over this point-to-point serial channel.

NOTE: The term, "controller" used in this document, refers to a Conexant RipTide Audio/Communications Controller (ACC) or Conexant-qualified AC '97-compatible core logic device set.

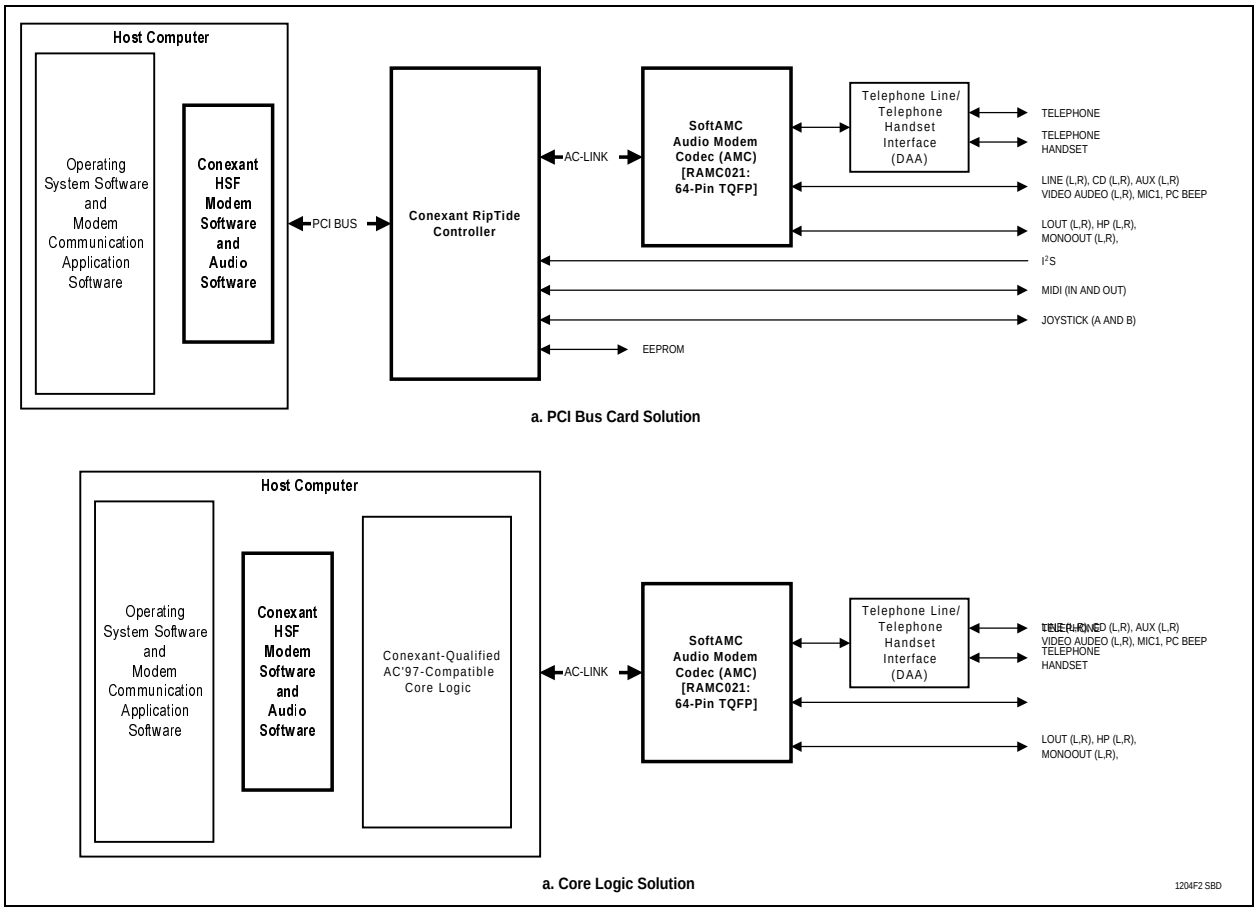


Figure 2. Typical SoftAMC System Block Diagram

Reference Information

The Conexant RipTide LP Audio/Comm System (Integrated Audio/Communications System Device Family with Host-Processed (HSF) V.90/K56flex™ Modem and PCI Bus Interface) features the D7300 Controller packaged in a 128-pin TQFP. See Product Description Order No. 1200.

The Conexant RipTide PCI Audio/Comm Device Family features the D7400 Controller packaged in a 176-pin TQFP. See Product Description Order No. 1167.

AMC Hardware Interface

AMC 64-Pin TQFP Pin Assignments

The pin assignments for the AMC in 64-pin TQFP are shown in Figure 3 and are listed in Table 2.

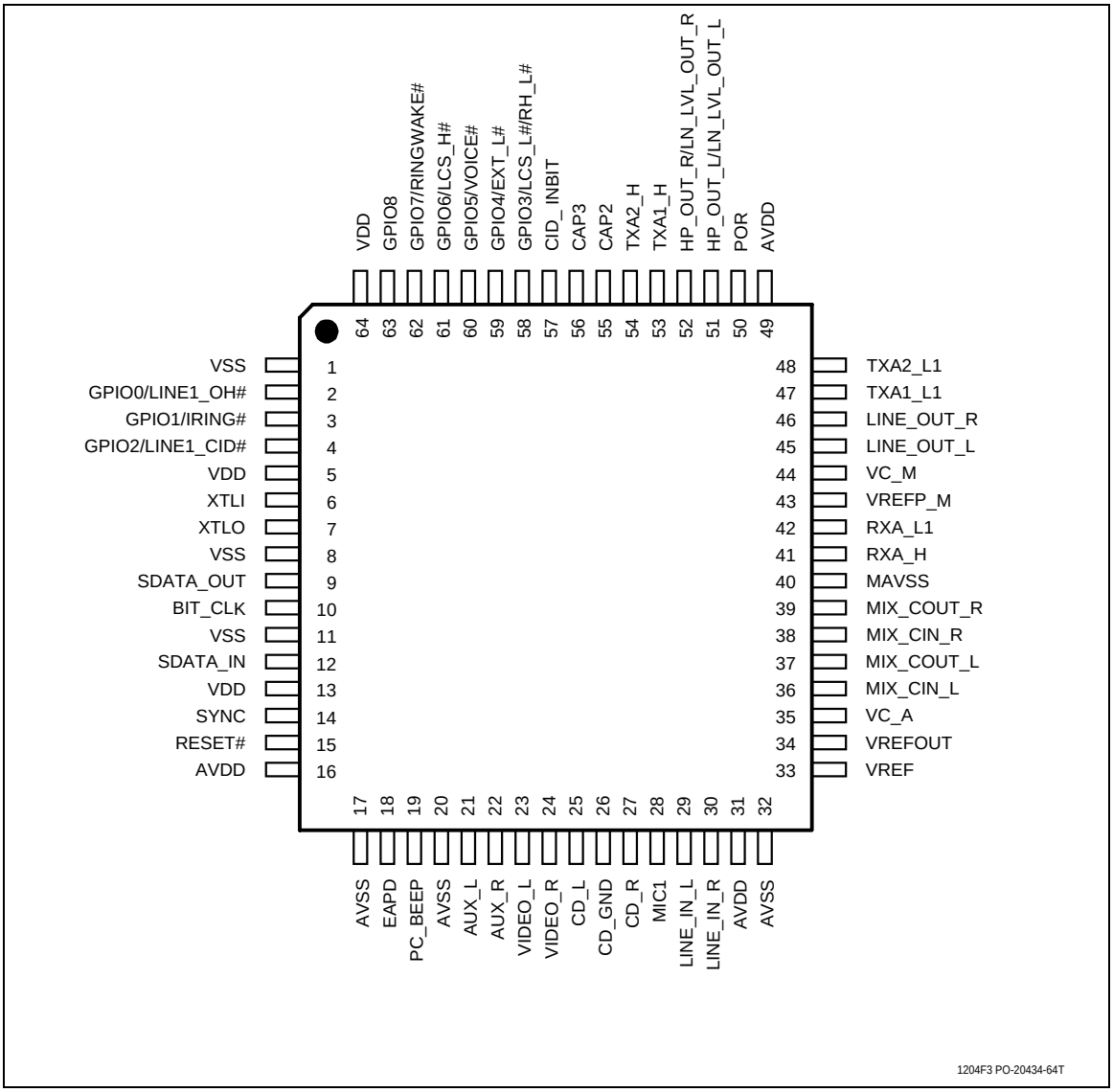


Figure 3. SoftAMC Pin Assignments - 64-Pin TQFP

Table 2. SoftAMC Pin Assignments - 64-Pin TQFP

Pin	Signal Label	I/O Type[1]	Interface[2]	Pin	Signal Label	I/O Type	Interface
1	VSS	GND	GND	33	VREF	REF	AGND through 10 uF and 0.1 uF
2	GPIO0/LINE1_OH#	Ot2	LTI: Line 1 Off-Hook Relay	34	VREFOUT	REF	AGND through 10 uF and 0.1 uF
3	GPIO1/IRING#	It	LTI: Ring Detect Circuit	35	VC_A	REF	AGND through 10 uF and 0.1 uF
4	GPIO2/LINE1_CID#	Ot2	LTI: Line 1Caller ID Relay	36	MIX_CIN_L	Ia	AI: MIX_COUTL through 1 uF
5	VDD	PWR	+5V or +3.3V	37	MIX_COUT_L	Oa	AI: MIX_CIN_L through 1 uF
6	XTLI	Ix	24.576 MHz Crystal Circuit or Oscillator	38	MIX_CIN_R	Ia	AI: MIX_COUT_R through 1 uF
7	XTLO	Ox	24.576 MHz Crystal Circuit or open (XTLI connected to Oscillator	39	MIX_COUT_R	Oa	AI: MIX_CIN_R through 1 uF
8	VSS	GND	GND	40	MAVSS	MAGND	MAGND
9	SDATA_OUT	Iac	AC-link: SDATA_OUT	41	RXA_H	Ia	LTI: Handset Receive Analog
10	BIT_CLK	Oac	AC-link: BIT_CLK	42	RXA_L1	Ia	LTI: Line 1 Receive Analog
11	VSS	GND	GND	43	VREFP_M	REF	MAGND through 10 uF and 0.1 uF
12	SDATA_IN	Oac	AC-link: SDATA_IN	44	VC_M	REF	MAGND through 10 uF and 0.1 uF
13	VDD	PWR	+5V or +3.3V	45	LINE_OUT_L	Oa	AI: Line Out Left Channel
14	SYNC	Iac	AC-link: SYNC	46	LINE_OUT_R	Oa	AI: Line Out Right Channel
15	RESET#	Iac	AC-link: RESET#	47	TXA1_L1	Oa	LTI: Line 1 Transmit Analog Plus
16	AVDD	PWR	+5VA	48	TXA2_L1	Oa	LTI: Line 1 Transmit Analog Minus
17	AVSS	AGND	AGND	49	AVDD	PWR	+5VA
18	EAPD	Ot2	AI: Ext. Audio Amplifier Control	50	POR	CAP	AGND through 1 uF
19	PC_BEEP	Ia	AI: PC Speaker beep pass through	51	HP_OUT_L/ LN_LVL_OUT_L	Oa	AI: Headphone Out Left Channel Line Level Out Left Channel
20	AVSS	AGND	AGND	52	HP_OUT_R/ LN_LVL_OUT_R	Oa	AI: Headphone Right Channel Line Level Out Right Channel
21	AUX_L	Ia	AI: Aux Audio Left Channel	53	TXA1_H	Oa	LTI: Handset Transmit Analog Plus
22	AUX_R	Ia	AI: Aux Audio Right Channel	54	TXA2_H	Oa	NC
23	VIDEO_L	Ia	AI: Video Audio Left Channel	55	CAP2	CAP	CAP3 through 12 nF
24	VIDEO_R	Ia	AI: Video Audio Right Channel	56	CAP3	CAP	AGND through 47 nF
25	CD_L	Ia	AI: CD Audio Left Channel	57	CID_INBIT	It	LTI: Caller ID Detect Circuit
26	CD_GND	GND	AI: CD Audio analog ground	58	GPIO3/LCS_L#/RH_L#	It	LTI: Line Cur Sense/Rem Hangup
27	CD_R	Ia	AI: CD Audio Right Channel	59	GPIO4/EXT_L#	It	LTI: Extension Pickup
28	MIC1	Ia	AI: Desktop Microphone Input	60	GPIO5/VOICE#	Ot2	LTI: Voice Relay
29	LINE_IN_L	Ia	AI: Line In Left Channel	61	GPIO6/LCS_H#	It	LTI: Handset Loop Current Sense
30	LINE_IN_R	Ia	AI: Line In Right Channel	62	GPIO7/RINGWAKE#	It	LTI: Ring Detect Circuit
31	AVDD	PWR	+5VA	63	GPIO8	It/Ot2	General purpose I/O
32	AVSS	AGND	AGND	64	VDD	PWR	+5V or +3.3V

1. I/O types:

Ia	Analog input (see Table 7)
Iac	Digital input, AC-link-compatible, C_{IN} = 50 pF (see Table 6)
It	Digital input, TTL (see Table 6)
Ix	Digital input crystal/clock
It/Ot2	Digital input, TTL/Digital output, TTL, 2 mA, 50 pF (see Table 6)
Oa	Analog output (see Table 7)
Oac	Digital output, AC-link-compatible (see Table 6)
Ot2	Digital output, TTL, 2 mA, 50 pF (see Table 6)
Ox	Digital output, crystal
REF	Reference voltage
CAP	Filter capacitor

2. Interface:

AI	Audio interface
LTI	Line/telephone interface

3. All GPIO lines have It/Ot2 capability. I/O Type listed corresponds to application signal.

SoftAMC Pin Signal Descriptions

System

Signal Name	Pin	I/O Type	Description
XTLI	6	Ix	Input from 24.576 MHz crystal circuit, or clock oscillator circuit.
XTLO	7	Ox	Output to 24.576 MHz crystal circuit, or NC if XTLI is connected to a clock oscillator.
POR	49	CAP	**Power-On Reset.** Connect to AGND through 1 uF.

AC-link Interface

Signal Name	Pin	I/O Type	Description
BIT_CLK	10	Oac	**Bit Clock.** 12.288 MHz AC-link bit clock. Connect to Controller BIT_CLK input.
SYNC	14	Iac	**Frame Sync.** 48 kHz fixed rate sample AC-link sync. Connect to Controller SYNC output.
SDATA_IN	12	Oac	**Serial Data Input.** Serial, time division multiplexed, AC-link input data stream. Connect to Controller SDATA_IN input.
SDATA_OUT	9	Iac	**Serial Data Output.** Serial, time division multiplexed, AC-link output stream. Connect to Controller SDATA_OUT output.
RESET#	15	Iac	**Reset.** Active low reset input. Connect to Controller RESET# output.

Modem Telephone Line and Telephone Handset Digital Signals

Signal Name	Pin	I/O Type	Application Description
CID_INBIT	57	Ia	**Caller ID Signal.** Caller ID input data stream.
GPIO0/LINE1_OH#	2	Ot2	**Line 1 Off-Hook Relay Control.** Active low output used to control the normally open off-hook relay. Connect to DAA #OH input.
GPIO1/IRING#	3	It	**Ring Indicate.** A low-going edge used to initiate presence of a ring frequency. Typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be high. Connect to DAA IRING# output and to +3.3V through 100 KΩ.
GPIO2/LINE1_CID#	4	Ot2	**Line 1 Caller ID Relay Control.** Active low output used to control the optional normally open Caller ID relay which is used to connect CID_INBIT input to the telephone line between first and second rings to receive the caller ID signal. Connect to DAA CID# input.
GPIO3/LCS_L#/RH_L#	58	It	**Line Current Sense/ Remote Hang-up.** Active low input used to indicate hang-up of the remote modem or telephone, i.e., the remote modem/telephone has released the line (gone on-hook). Connect to DAA LCS_L#/RH_L# output and to +3.3V through 100 KΩ.
GPIO4/EXT_L#	59	It	**Extension Off-Hook.** Active low input used to indicate the telephone line is in use. Connect to DAA EXT_L# output and to +3.3V through 100 KΩ.
GPIO5/VOICE#	60	Ot2	**Voice Relay Control.** Active low output used to control the Voice relay. When inactive. (Default.), the handset is connected to the line. When active, the handset is disconnected from the line and connected to a DC supply on the application board and the handset is connected to the Codec for voice record and playback. Connect to DAA VOICE# input.
GPIO6/LCS_H#	61	It	**Line Current Sense Handset.** Active low input used to indicate local modem handset off-hook status and to detect remote hang-up. Connect to DAA VOICE# INPUT and to +3.3V through 100 KΩ.
GPIO7/RINGWAKE#	62	It	**RingWake.** Active low input used to indicate that a valid ring signal has been detected. When RINGWAKE# is asserted, the PME# output is asserted. Used for Caller ID support.
GPIO8	63	It	**General Purpose Input/Out.** Reserved.

Audio Analog Signals

These signals connect the AC '97 component to analog sources and sinks, including microphones and speakers.

Signal Name	Pin	I/O Type	Description
EAPD	18	Ot2	**External Audio Amplifier Power Down.** Active low output used to enable the external power amplifier. EAPD is low on power-on, enabling the external power amplifier.
PC_BEEP	19	Ia	**PC Speaker Beep Pass through. When** RESET# is asserted, PC_BEEP is directly routed to the Line Out (LINE_OUT_L and LINE_OUT_R) through an internal 300 ohm resistor to allow the user to hear system startup beeps in the event of PC system errors. PC_BEEP is **not** routed to Line Level Output (HP_OUT_L and HP_OUT_R).
MIC1	28	Ia	**Microphone 1 Input.** Connect to MIC1.
AUX_L	21	Ia	**Aux Audio Left Channel.** Connect to AUX_L.
AUX_R	22	Ia	**Aux Audio Right Channel.** Connect to AUX_R.
VIDEO_L	23	Ia	**Video Audio Left Channel.** Connect to VIDEO_L.
VIDEO_R	24	Ia	**Video Audio Right Channel.** Connect to VIDEO _R.
CD_L	25	Ia	**CD Audio Left Channel.** Connect to CD_L.
CD_GND	26	Ia	**CD Audio Analog Ground.** Connect to AGND through 1 uF.
CD_R	27	Ia	**CD Audio Right Channel.** Connect to CD_R.
LINE_IN_L	29	Ia	**Line In Left Channel.** Connect to LINEIN_L.
LINE_IN_R	30	Ia	**Line In Right Channel.** Connect to LINEIN_R.
LINE_OUT_L	45	Oa	**Line Out Left Channel.** Connect to LOUT_L.
LINE_OUT_R	46	Oa	**Line Out Right Channel.** Connect to LOUT_R.
HP_OUT_L/ LN_LVL_OUT_L	51	Oa	**Headphone Out/Line Level Out Left Channel.** Connect to HPOUT_L.
HP_OUT_R/ LN_LVL_OUT_R	52	Oa	**Headphone Out/Line Level Out Right Channel.** Connect to HPOUT_R.

Modem Analog Signals

These signals connect the Codec to telephone line and telephone handset analog signals.

Signal Name	Pin	I/O Type	Description
TXA1_L1	47	Oa	**Line 1 Transmit Analog Plus.** Plus level of differential analog output signal output to telephone line 1.
TXA2_L1	48	Oa	**Line 1 Transmit Analog Minus.** Minus level of differential analog output signal output to telephone line 1.
RXA_L1	42	Ia	**Line 1 Receive Analog.** Single-ended analog receive input signal from telephone line 1.
TXA1_H	53	Oa	**Handset Transmit Analog Plus.** Plus level of differential analog output signal output to the handset speaker.
TXA2_H	54	Oa	**Handset Transmit Analog Minus.** Minus level of differential analog output signal output to the handset speaker. Not used. Leave open.
RXA_H	41	Ia	**Handset Receive Analog.** Single-ended analog receive input signal from the handset microphone.

Filter and Reference Voltage Connections

Signal Name	Pin	I/O Type	Description
VREF	33	REF	**Audio Reference Voltage**. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
VREFOUT	34	REF	**Reference Voltage Out.** Intended for mic bias, if needed. Connect, through 200 Ω, to 10 uF (polarized) and 0.1 uF (ceramic) connected in parallel to AGND. Connect also to DAA VREFOUT input through the 200 Ω resistor. .
VC_A	35	REF	**Audio Reference Voltage.** Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
MIX_CIN_L	36	Ia	**Mixer Common In Left.** Connect to MIX_COUT_L through 1 uF.
MIX_COUT_L	37	Oa	**Mixer Common Out Left.** Connect to MIX_CIN_L through 1 uF.
MIX_CIN_R	38	Ia	**Mixer Common In Right.** Connect to MIX_COUT_R through 1 uF.
MIX_COUT_R	39	Oa	**Mixer Common Out Right.** Connect to MIX_CIN_R through 1 uF.
VREFP_M	43	REF	**Modem Reference Voltage.** Connect to MAGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
VC_M	44	REF	**Modem Reference Voltage.** Connect to MAGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
CAP2	55	CAP	**Generic Cap.** Connect to CAP3 through 12 nF.
CAP3	56	CAP	**Generic Cap.** Connect to AGND through 47 nF.

Power and Ground

Signal Name	Pin	I/O Type	Description
VDD	5, 13, 64	PWR	**Digital Circuit Power.** Connect to + 5V or +3.3V.
AVDD	16, 31, 49	PWR	**Digital Portion of Analog Circuit Power.** Connect to +5VA.
VSS	1, 8, 11	GND	**Digital Ground.** Connect to GND.
AVSS	17, 20, 32	GND	**Analog Ground.** Connect to AGND.
MAVSS	40	GND	**Modem Analog Ground.** Connect to MAGND. Connect MAGND to AGND through a zero ohm resistor to allow insertion of a ferrite bead if needed for noise suppression.

Specifications

Operating Conditions

Table 3. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage VDD = +3.3V VDD = +5V	VDD	 +3.0 to +3.6 +4.75 to +5.25	V
I/O Voltage	AVDD	+4.75 to +5.25	V
Operating Temperature Range	T_A	0 to +70	°C

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage VDD = +3.3V VDD = +5V	VDD	 -0.3 to +4.0 -0.3 to +6.0	V
Digital Input Voltage	V_{IN}	-0.3 to (VDD +0.3)	V
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Input Voltage	V_{IN}	-0.3 to (AVDD + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.3 to (VDD + 0.3)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±300	mA

Current and Power Requirements

Table 5. Current and Power Requirements

Mode (State)	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	Notes
Normal Mode (D0)	15.50	-	52	-	VDD = +3.3V
Power Down Mode (D3hot)	.02	-	0.066	-	VDD = +3.3V
Sleep Mode (D3cold)	.02	-	0.066	-	VDD = +3.3V
Normal Mode (D0)	52 (idle)	-	260	-	VDD = +5V
Power Down Mode (D3hot)	9	-	45	-	VDD = +5V
Sleep Mode (D3cold)	NA	NA	NA	NA	VDD = +5V

Notes:

1. Test conditions for VDD = +3.3V: VDD = +3.3V for typical values; VDD = +3.6V for maximum values.
2. Test conditions for VDD = +5V: VDD = +5.0V for typical values; VDD = +5.25V for maximum values.
3. Input Ripple ≤ 0.1 Vpeak-peak.
4. f = Internal frequency.
5. Sleep Mode configured for wakeup.

DC Electrical Characteristics

Table 6. Digital Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Voltage	V_{in}	-0.30	-	3.60	V	VDD = +3.6V
Input Voltage	V_{in}	-0.30	-	5.25	V	VDD = +5.25V
Input Voltage Low	V_{il}	-0.30	-	0.25*VDD	V	
Input Voltage High	V_{ih}	0.65*VDD	-	VDD + 0.3	V	
Output Voltage Low	V_{ol}	0	-	0.1*VDD	V	
Output Voltage High	V_{oh}	0.85*VDD	-	VDD	V	
GPIO Output sink current at 0.4 V maximum	-	2.4	-	-	mA	
GPIO Output source current at 2.97 V minimum	-	2.4	-	-	mA	
GPIO rise/fall time		20		100	ns	

Notes:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC or 5.0V ± 5% VDC; T_A = 0°C to 70°C; external load = 50 pF

AC Performance Characteristics

Table 7. Analog Performance Characteristics

Parameter	Min	Typical	Max	Units
Full Scale Input Voltage				
LINE_IN	-	1.0	-	Vrms
MIC (+20 dB Boost on)	-	0.1	-	Vrms
MIC (+20 dB Boost off)	-	1.0	-	Vrms
Full Scale Output Voltage				
LINE_OUT	-	1.0	-	Vrms
HP_OUT	-	-	1.41	Vrms
Analog S/N				
CD to LINE_OUT, HP_OUT, or MONO_OUT	90	-	-	dB
Other to LINE_OUT, HP_OUT, or MONO_OUT	-	85	-	dB
Analog Frequency Response (±1 dB limits)	20	-	20,000	Hz
Digital S/N[1]				
D/A	85	90	-	dB
A/D	75	80	-	dB
Total Harmonic Distortion:				
LINE_OUT (0 dB gain, 20 kHz BW, 48 kHz Sample Frequency)	-	-	0.02	%
HP_OUT (+3 dB output into 32 Ω load)	-	-	1.0	%
D/A and A/D Frequency Response (±0.25 dB limits)	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[2]	-74	-	-	dB
Out-of-Band Rejection[3]	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk between Input channels	-	-	-70	dB
Crosstalk between headphone channels	-	-	-70	dB
Crosstalk between line ADC/DAC and any other channel	-	-	-80	dB
Isolation between audio and modem sections	80	-	-	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size (except for PC Beep)	-	1.5	-	dB
Interchannel Gain Mismatch (Difference between errors)	-0.5	-	0.5	dB
Absolute Gain Step Error at any given setting	-	-	0.75	dB
Input Resistance	10	-	-	Kohm
Input Capacitance	-	7.5	-	pF
Vrefout	-	2.25-2.75	-	V
DC Offset				
Audio ADCs	-	±10	±50	mV
Other ADCs	-	-	±100	mV
Audio DACs	-	±5	±25	mV
Other DACs	-	-	±100	mV

Table 6. Analog Performance Characteristics (Cont'd)

Parameter	Min	Preliminary	Max	Units
Modem Line				
DAC to Line Driver output SNR at -10 dBm, 1200 Ω	77	-	80	dB
Line Input to ADC SNR at -6 dBm	77	-	80	dB
Handset				
DAC to Line Driver output SNR at -10 dBm, 1200 Ω	77	-	80	dB
Line Input to ADC SNR at -6 dBm	77	-	80	dB
Mic ADC				
Line Input to ADC SNR at -6 dBm without 20 dB boost	77	-	80	dB
Line Input to ADC SNR at -6 dBm with 20 dB boost	-	65	-	dB

Notes:

1. The ratio of the rms output level with 1kHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20Hz to a 20kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
2. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
3. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 VRMS DAC output.

Standard test conditions unless otherwise noted:

Temperature	25 °C	
Analog Supply (AVDD)	5.0 V ±5%	
Digital Supply(VDD)	3.3 V ±0.3V	
Input Voltage Levels:	VDD = +5 V	VDD = +3.3 V
Logic Low	0.8 V	1.0 V
Logic High	2.4 V	2.97 V
Input signal	1 kHz sine wave	
Sample Frequency(FS)	48 kHz	

0 dBV = 1 Vrms

10 kohm/50 pF load

Testbench Characterization BW:

Pass Band	20 Hz - 20 kHz
Attenuation	0 dB
Gain on inputs	0 dB

AC Timing Characteristics

AC Link Clocks

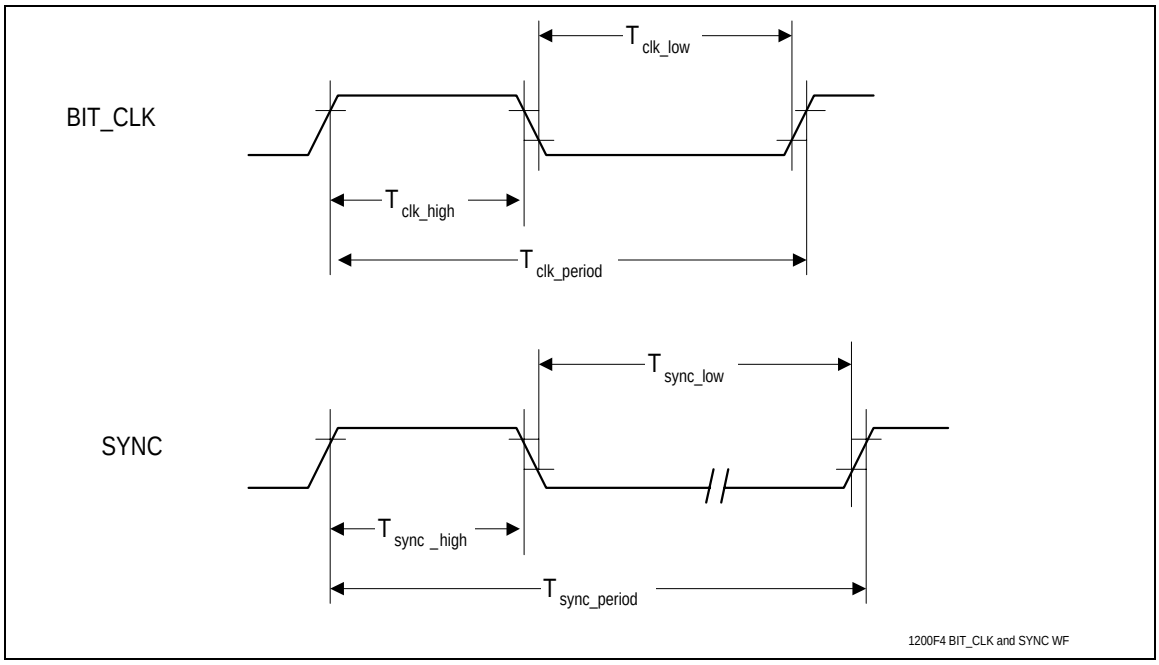


Figure 4. BIT_CLK and SYNC Timing Waveforms

Table 8. BIT_CLK and SYNC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (Note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs

Notes:
1. Worst case duty cycle restricted to 45/55.
2. 47.5 pF - 70 pF external load.

Data Output and Input

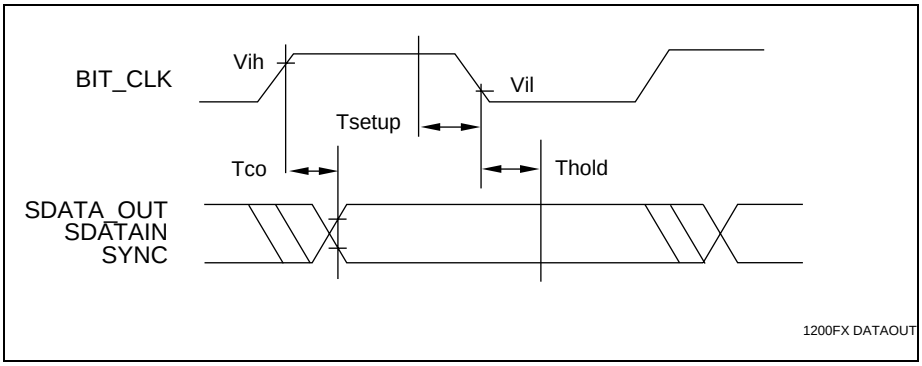


Figure 5. Data Output and Input Timing Waveforms

Table 9. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	Tco	-	-	15	ns
Notes: 1. Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. 2. 50 pF external load.					

Table 10. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	T_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	T_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC inputs with respect to BIT_CLK at the device latching the input					

Table 11. AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note: Maximum combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					

Signal Rise and Fall Times

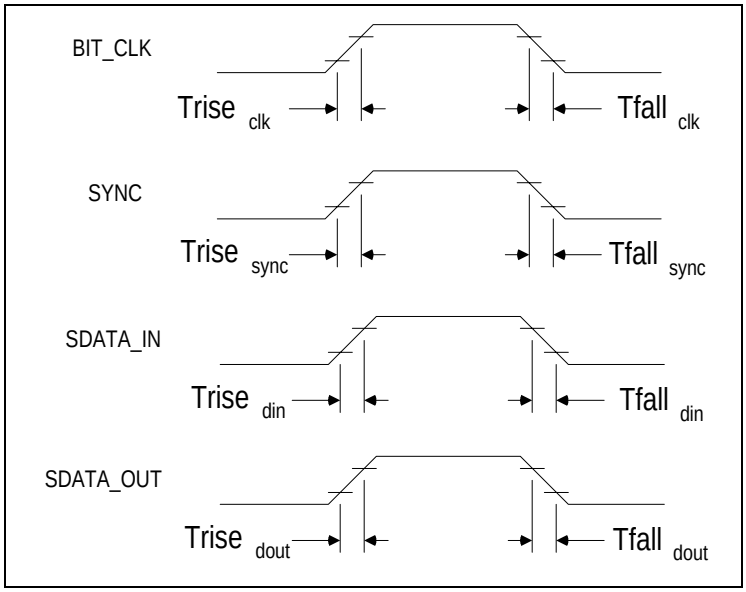


Figure 6. Signal Rise and Fall Time Timing Waveforms

Table 12. Signal Rise and Fall Time Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns

Notes:
1. 50 pF external load; from 10% to 90% of VDD.
2. Rise is from 10% to 90% of VDD (Vol to Voh).
3. Fall is from 90% to 10% of VDD (Voh to Vol).

RESET# (Cold Reset)

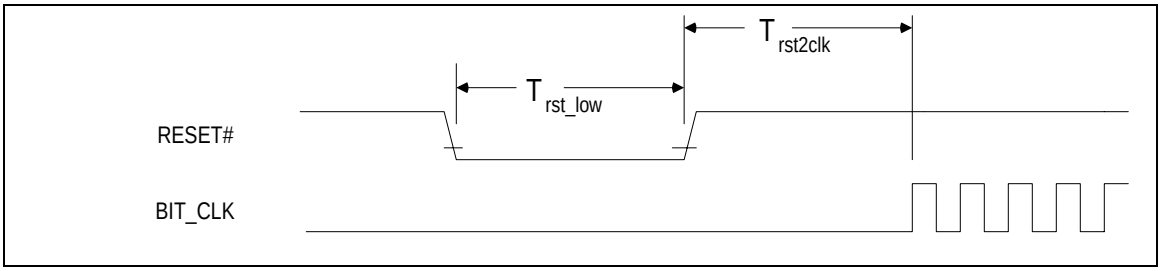


Figure 7. Cold Reset Timing Waveforms

Table 13. Cold Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

RESET# (Warm Reset)

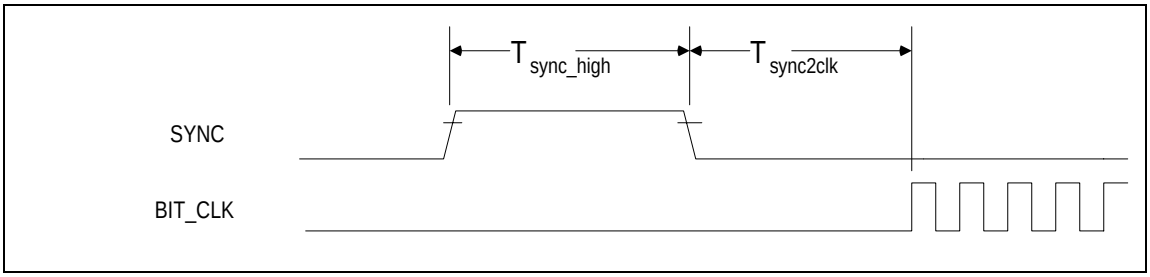


Figure 8. Warm Reset Timing Waveforms

Table 14. Warm Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns
Note: The minimum SYNC pulse width pertains to warm reset only, during normal operation, SYNC is asserted for the entire tag phase (16 BIT_CLK times).					

AC-link Low Power Mode Timing

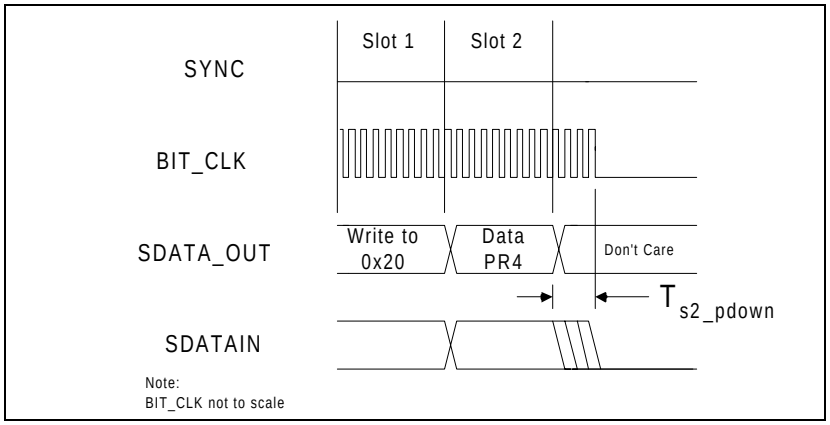


Figure 9. AC-link Low Power Mode Timing Waveforms

Table 15. AC-link Low Power Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

ATE Test Mode Timing

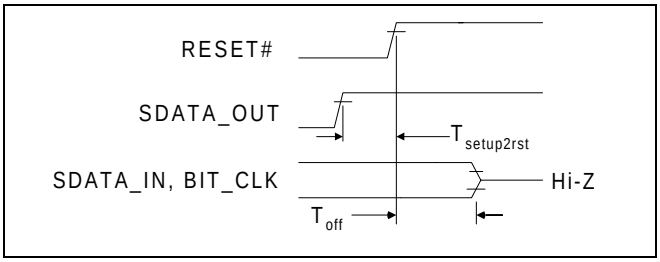


Figure 10. ATE Test Mode Timing Waveforms

Table 16. ATE Test Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

Crystal Specification

Table 17 lists the required crystal parameters.

Table 17. Crystal Specification

Parameter	Range
Frequency	24.576 MHz
Oscillation Mode	Fundamental
Resonance	Parallel
Load Capacitance	22 pF
Frequency Tolerance	± 40 ppm @ 25 °C
Temperature Stability	± 45 ppm, 0-70 °C
Operating Temperature	0 -70 °C
Shunt Capacitance	< 7 pF
Equivalent Series Resistance	< 35 ohms @ 20 nW Drive Level
Drive Level	100 μW Correlation, 300 μW Max
Aging	± 15 ppm over 5 years
Storage Temperature Range	-40 to +85°C

General Description

Digital Interface

The codec communicates with the controller via a digital serial link (AC-link). All digital audio streams, modem line codec stream, handset, GPIO, and command/status information is transferred between the controller and the codec over this point to point serial channel. The AC-link interface signals are shown in Figure 11 and are described in Table 18.

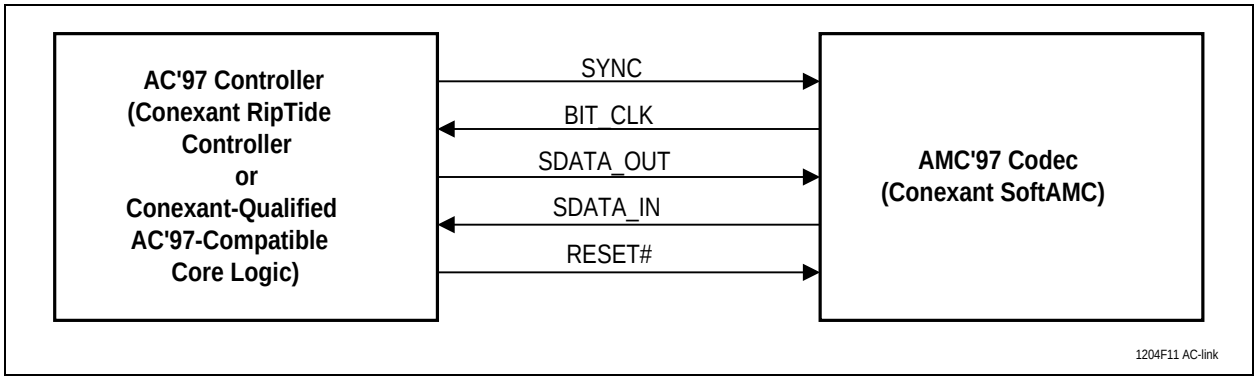


Figure 11. AC-link Serial Interface

Table 18. AC-link Serial Interface Signals

Signal Name	I/O	Description
SYNC	I	48 kHz fixed rate sample synchronization from the controller.
BIT_CLK	O	12.288 MHz serial data clock from the codec.
SDATA_IN	O	Serial data stream from the codec to the controller.
SDATA_OUT	I	Serial data stream from the controller to the codec.
RESET#	I	Master hardware reset from the controller

The control and status slots allow writing and reading of registers internal to the AC ’97 codec. These registers are defined as 16 bit and are addressed at word aligned byte addresses 0x00, 0x02, 0x04, …, 0x7e. Registers 0x00 - 0x58 are predefined, 0x5a - 0x7a are reserved for the vendor, 0x7c and 0x7e are for the vendor ID.

Because provisions exist for the modem and other sample rates to be less than 48 kHz, the TAG slot contains bits which indicate the validity of each slot in the serial stream.

The AMC ’97 specification also defines slot request bits that allow the codec to request samples from the controller. These bit definitions (active low) are implemented as defined in that specification.

When a slot is valid for the outgoing stream, the controller places a one in the corresponding bit position in the TAG slot. For all slots other than the PCM left and right slots, the codec ignores the data present in the slot when the slot’s tag bit is a 0 for that particular data phase. This allows the controller to simply repeat the current sample if desired. However, the controller must respond properly to the SLOTREQ bits. For the PCM left and right slots, the codec assumes every slot is valid. If the slot is invalid, the controller must send 0’s for the data.

When a slot is valid for the incoming stream, the codec places a one in the corresponding bit position in the TAG slot. The controller must ignore the data present in the slot when the slot’s tag bit is a 0 for that particular data phase. The Codec puts zeros in the slot when the slot is invalid.

The AC-link request for status always returns in the next frame. The request is, therefore, always delayed by one frame time. A write request in the current frame will not affect the status that is returned in that particular write frame. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the controller.

For fixed 48 kHz sample rate operation, the SLOTREQ bits are always set active and a sample is transferred each frame.

For optional multiple sample rate input, the tag bit for each input slot indicates whether valid data is present or not. The SoftAMC Codec, configured for fixed 48 kHz operation, is compatible with Conexant RipTide controllers and Conexant-qualified AC'97 core logic chip sets.

Thus, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame that should be set or reset by the controller.

Any protocol violation in the AC-link, e.g., less than 256 BIT_CLKs in a SYNC frame, will result in a warm reset of the codec.

Conexant AMC '97 Codec

The Conexant AMC '97 codec (AMC) is implemented only as a primary codec. The time slots supported by the AMC are listed in Table 19.

Table 19. AMC '97 Slot Assignments

Slot Number	SDATAOUT (Controller to Codec)	SDATAIN (Codec to Controller)
0	TAG	TAG
1	Command Address Port	Status Address Port
2	Command Data Port	Status Data Port
3	PCM Playback Left Channel	PCM Record Left Channel
4	PCM Playback Right Channel	PCM Record Right Channel
5	Modem Line 1 DAC Input Data	Modem Line 1 ADC Output Data
6	Not Supported	Mic ADC Output Data
7	Not Supported	Not Supported
8	Not Supported	Not Supported
9	Not Supported	Not Supported
10	Not Supported	Not Supported
11	Handset DAC Input Data	Handset ADC Output Data
12	GPIO Control	GPIO Status

SDATA_IN (Codec to Controller) Slot Definitions

Input Slot 1: Status Address Port / SLOTREQ Bits

Slot 1, the Status Address Port, delivers codec control register read address *and* variable sample rate slot request flags for all output slots. Bits 11 to 2 are defined as data request flags for output Slots 3-12.

Input Slot 1: Status Address Port	
Bit	**Description**
19	**Reserved.** Set to 0 by the codec.
18:12	**Control Register Index.** Echo of register index for which data is being returned. Set to 0s if tagged “invalid” by the controller.
11:2	**“On Demand” Data Request Flags (next output frame).** 0 = Send data, 1 = Do not send data.
11	**Slot 3 Request.** PCM Left Channel.
10	**Slot 4 Request.** PCM Right Channel.
9	**Slot 5 Request.** Modem Line 1.
8	**Slot 6 Request.** Not used. Set to 0 by the codec.
7	**Slot 7 Request.** Not used. Set to 0 by the codec.
6	**Slot 8 Request.** Not used. Set to 0 by the codec.
5	**Slot 9 Request.** Not used. Set to 0 by the codec.
4	**Slot 10 Request.** Not used. Set to 0 by the codec.
3	**Slot 11 Request.** Handset.
2	**Slot 12 Request.** GPIO.
1:0	**Reserved.** Set to 0 by the codec.

The Slot 1 tag bit is independent of the bit 11:2 slot request field, and **only** indicates valid Status Address Port data (Control Register Index). The AMC sets SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to "1" when returning valid data from a previous register read. They are otherwise set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots are driven with 0s for maximum compatibility with the original AC '97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit is forced to “1” in the interval between when the powerdown bit for its associated channel is turned off and when its channel is ready to accept samples. The controller can take advantage of this scheme to eliminate the need to poll the AMC status registers.

To power down a channel, the controller needs only to:

1. Disable the source of DAC samples in controller.
2. Set the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.

To power up a channel, the controller needs only to:

1. Clear the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.
2. Enable the source of DAC samples in controller.

Variable Sample Rate Signaling Protocol

For variable sample rate output, the codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame signal which *active output slots* require data from the controller in the next audio output frame. An *active output slot* is defined as any slot supported by the codec that is not in a powerdown state. For fixed 48 kHz operation, the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

Upon reset, the audio sample rate registers default to 48 kHz.

The VRM bit controls the optional MIC ADC behavior. SLOTREQ bits for active modem DACs are always treated as valid (data on demand).

Input Slot 2: Status Data Port

Input Slot 2, the Status Data Port, port delivers 16-bit control register read data.

Input Slot 2: Status Data Port	
Bit	**Description**
19:4	**Control Register Read Data.** Stuffed with 0's if tagged "invalid" by the codec.
11:0	**Reserved.** Stuffed with 0's by the codec.

Input Slot 3: PCM Left Record Data

Input Slot 3 contains the 18-bit PCM left channel ADC output data.

Input Slot 3: PCM Left Channel ADC Output Data	
Bit	**Description**
19:2	**PCM Left Channel ADC Output Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 4: PCM Right Record Data

Input Slot 4 contains the 18-bit PCM right channel ADC output data.

Input Slot 4: PCM Right Channel ADC Output Data	
Bit	**Description**
19:2	**PCM Right Channel ADC Output Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 5: Modem Line 1 ADC Output Data

Input Slot 5 contains the 16-bit Modem Line 1 ADC output data.

Input Slot 5: Modem Line 1 ADC Output Data	
Bit	**Description**
19:4	**Modem Line 1 ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 6: Microphone ADC Output Data

Input Slot 6 contains the 16-bit Microphone ADC output data.

Input Slot 6: Microphone ADC Output Data	
Bit	**Description**
19:4	**Microphone ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

Input Slots 7-10: Reserved

Input Slots 7-10 are reserved.

Input Slot 7-10: Reserved	
Bit	**Description**
19:0	**Microphone ADC Output Data.** Stuffed to 0's by the codec.

Input Slot 11: Handset ADC Output Data

Input Slot 11 contains the 16-bit Handset ADC output data.

Input Slot 11: Handset ADC Output Data	
Bit	**Description**
19:4	**Handset ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

Input Slot 12: GPIO Control

Input Slot 12 contains the GPIO status bits. The codec constantly updates the status slot based upon the logic level detected at each GPIO configured for input. The controller must debounce the reported states as required for the 48 kHz sample rate.

Input Slot 12: GPIO Status	
Bit	**Description**
19:4	**GPIO[15:0] Status.** 1 = High level detected at input pin; 0 = Low level detected at input pin. Bits corresponding to GPIO outputs reflect the command level.
19	**GPIO15 Status.** Application assigned. Not supported.
18	**GPIO14 Status.** Application assigned. Not supported.
17	**GPIO13 Status.** Application assigned. Not supported.
16	**GPIO12 Status.** Application assigned. Not supported.
15	**GPIO11 Status.** Application assigned. Not supported.
14	**GPIO10 Status.** Application assigned. Not supported.
13	**GPIO9 Status.** Application assigned. Not supported.
12	**GPIO8 Status.** Application assigned.
11	**GPIO7 Status.** Application assigned (RINGWAKE#).
10	**GPIO6 Status.** Application assigned (LCS_H#).
9	**GPIO5 Status.** Application assigned (VOICE#).
8	**GPIO4 Status.** Application assigned (EXT_L#).
7	**GPIO3 Status.** Application assigned (LCS_L#/RH_L#).
6	**GPIO2 Status.** Application assigned (LINE1_CID#).
5	**GPIO1 Status.** Application assigned (IRING#).
4	**GPIO0 Status.** Application assigned (LINE1_OH#).
3:0	**Not Used.** Stuffed to 0's by the codec.

SDATA_OUT (Controller to Codec) Slot Definitions

Output Slot 1: Command Address Port

Output Slot 1, the Command Address Port, is used to control features and monitor status (see Input Slots 1 and 2) for codec functions such as mixer settings and power management.

Output Slot 1: Command Address Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 2: Command Data Port

Output Slot 2, the Command Data Port, is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19). If the current command port operation is a read, then the entire slot time must be stuffed with 0's by the controller.

Output Slot 2: Command Data Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 3: PCM Left Playback Data

Output Slot 3 contains the 18-bit PCM left channel DAC input data.

Output Slot 3: PCM Left Channel DAC Input Data	
Bit	**Description**
19:2	**PCM Left Channel DAC Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

Output Slot 4: PCM Right Playback Data

Output Slot 4 contains the 18-bit PCM right channel DAC input data.

Output Slot 4: PCM Right Channel DAC Input Data	
Bit	**Description**
19:2	**PCM Right Channel DAC Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

Output Slot 5: Modem Line 1 DAC Input Data

Output Slot 5 contains the 16-bit Modem Line 1 DAC input data.

Output Slot 5: Modem Line 1 DAC Input Data	
Bit	**Description**
19:4	**Modem Line 1 DAC Input Data.** 16-bit sample (bit 19 = MSD; bit 4 = LSD)
3:0	**Not Used.** Stuffed to 0's by the controller.

Output put Slots 6-10: Reserved

Output Slots 6-10 are reserved.

Output Slot 6-10: Reserved	
Bit	**Description**
19:0	**Reserved.** Stuffed to 0's by the controller.

Output Slot 11: Handset DAC Input Data

Output Slot 11 contains the 16-bit Handset DAC input data.

Output Slot 11: Handset DAC Input Data	
Bit	**Description**
19:4	**Handset DAC Input Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the controller.

Output Slot 12: GPIO Status

Output Slot 12 contains the GPIO control bits. The codec constantly sets the GPIOs that are configured for output based upon the value of the corresponding bit position of the control slot.

Output Slot 12: GPIO Control	
Bit	**Description**
19:4	**GPIO[15:0] Control.** 1 = High level at the codec output pin.; 0 = Low level at the codec output pin. Bits corresponding to GPIO inputs are set to 0 by the controller.
19	**GPIO15 Control.** Application assigned. Not supported.
18	**GPIO14 Control.** Application assigned. Not supported.
17	**GPIO13 Control.** Application assigned. Not supported.
16	**GPIO12 Control.** Application assigned. Not supported.
15	**GPIO11 Control.** Application assigned. Not supported.
14	**GPIO10 Control.** Application assigned. Not supported.
13	**GPIO9 Control.** Application assigned. Not supported.
12	**GPIO8 Control.** Application assigned.
11	**GPIO7 Control.** Application assigned (used for input).
10	**GPIO6 Control.** Application assigned (used for input).
9	**GPIO5 Control.** Application assigned (VOICE#).
8	**GPIO4 Control.** Application assigned (used for input).
7	**GPIO3 Control.** Application assigned (used for input).
6	**GPIO2 Control.** Application assigned (LINE1_CID#).
5	**GPIO1 Control.** Application assigned (used for input).
4	**GPIO0 Control.** Application assigned (LINE1_OH#).
3:0	**Not Used.** Stuffed to 0's by the controller.

General Purpose Inputs/Outputs

The Codec contains a number of General Purpose Input/Outputs suitable for easy connection with minimal parts to a DAA circuit. The controller must configure any GPIOs as outputs on power-up.

When configured as an input, a GPIO performs as a CMOS Schmitt triggered input for a 3.3V power supply. The board designers are responsible for connecting unused pins to VDD or VSS. However, to prevent excess power loss due to floating conditions during an extended reset period, all GPIOs, when RESET# is asserted, are pulled down.

The GPIOs are tristated to a high impedance state on power-on or a cold reset. The controller must first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs have slow rise and fall times. Typical values should be 40 ns. In addition, the device sinks 2.4 mA at a maximum level of 0.4V and sources 2.4 mA at a minimum level of 2.97V.

Upon a warm reset, the GPIOs that are configured for outputs maintain their output values. As long as the controller does not tag the GPIO control slot as valid, the outputs will not change.

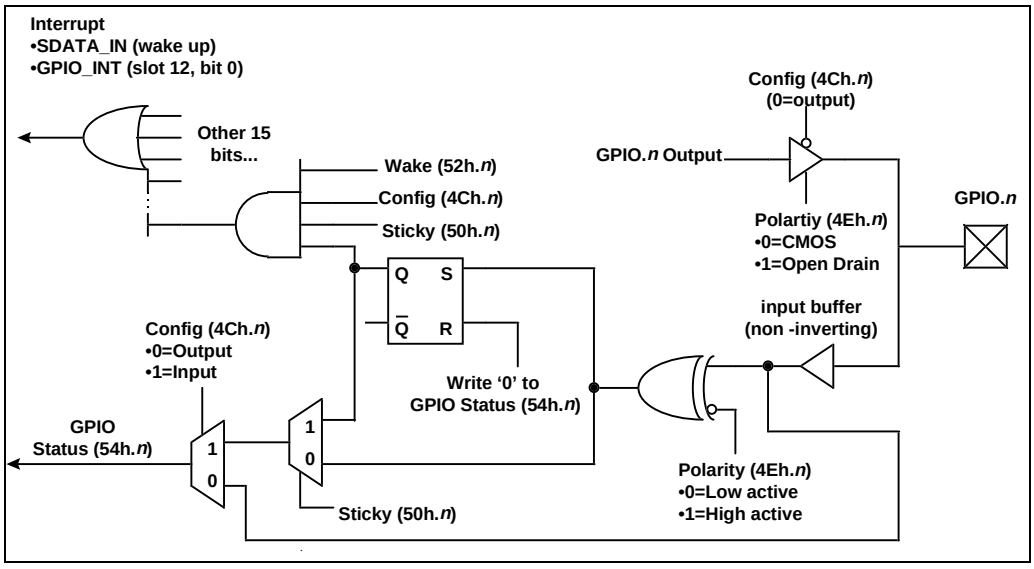


Figure 12. Conceptual GPIO Configuration

Low Power Modes

The Codec is a fully static design, i.e., when the clock is stopped to any subsection of the device, that subsection maintains its value.

The low power modes specified in Section 7 of the AC '97 Specification are supported in full, i.e., the modem ADC/DAC, the handset ADC/DAC, and the mic ADC can be individually powered down and up. See the appropriate registers for control, which are the Powerdown Control/Status and the Modem Powerdown Control/Status.

Loop Back Modes

Several loopback modes are defined for the ADC/DAC pairs as well as the microphone ADC. These loopback modes are for diagnostic and test purposes. These modes are described in this section; however, the positions of the controlling bits are detailed in the Mixer Register definition section.

Because the dedicated microphone ADC has no associated DAC, it must “borrow” a DAC from another source. Somewhat randomly, the source chosen is the handset DAC. Therefore, when referring to the microphone ADC loopback paths, the handset DAC is meant.

In keeping with proper AC-link terminology, AC-link Outgoing streams go INTO the AMC ’97 audio modem codec, while AC-link Incoming streams go OUT of the codec.

Note that the DAC outputs are squelched automatically when the loopback modes are used.

Modem/Handset/Microphone Loop Back Definitions

The following definitions apply to the modem line 1, handset, and dedicated microphone ADC/DAC pairs. To conserve register space, implementation of the modes are done by combinations of bits, rather than by individual bits, with the exception of the one-bit output bit.

ADC Loop Back

The ADC Loop Back travels from the Line input signal through internal filtering, the delta-sigma ADC, another internal filter, and then to the Line output.

Line In -> Filter -> ADC -> Filter -> Line Out.

Local Analog Loop Back

Otherwise known as Loop3, the digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the delta-sigma DAC, an internal filter, routed back through the delta-sigma ADC, another internal filter, and then out onto the appropriate incoming stream slot of the AC -link.

AC-link Out Stream -> DAC -> Filter -> ADC -> Filter -> AC-link In Stream

DAC Digital Loop Back

The DAC Digital Loop Back is a purely digital loopback. The digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the delta-sigma DAC, to an internal filter, and then out onto the appropriate incoming stream slot of the AC-link.

AC-link Out Stream -> DAC -> Filter ->AC-link In Stream

Remote Analog Loop Back

Otherwise known as Loop4, the Line input signal is passed through an internal filter and routed directly back to the Line output.

Line In -> Filter -> Line Out

ADC and DAC Loop Back Combined

This mode provides the option to perform both of the ADC and DAC loopbacks at the same time since they use separate blocks of the codec.

Audio ADC/DAC Loop Back Definitions

The following definitions apply to the audio ADC/DAC pairs. To conserve register space and to provide backward compatibility to AC ’97, implementation of the modes are done by both a combination of bits and individual bits. Some have been defined previously by the AC ’97 spec.

ADC to DAC Loop Back

The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. This will provide both left and right loopbacks to occur simultaneously for backward compatibility. Individual bits are required to allow for left ADC to left DAC and right ADC to right DAC independently of each other.

DAC to ADC Loop Back

The DAC to ADC Loop Back is a purely digital loopback. The digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the delta-sigma DAC, to an internal filter, and then out onto the appropriate incoming stream slot of the AC-link.

AC-link Out Stream -> DAC -> Internal Filter -> AC-link In Stream

Caller ID Operation in Low Power Mode

Caller ID operation when the system is in regular operation is performed via the modem data lines and drivers. However, when the system is in low-power mode, Caller ID is supported in the codec using circuitry that is not effected by the low-power mode.

Operation of the codec Caller ID circuitry when the system is powered down is controlled and monitored using the Caller ID Control and Status Register (Register 62h).

Analog On Hold and Call Progress

Two mixers, the Analog On Hold Mixer and the Call Progress Mixer, support analog on hold (e.g., music-on-hold) and call progress features, respectively.

Analog On Hold

Analog on hold allows the user to place a handset or speakerphone caller on hold (Figure 13). In this mode, the MONOOUT audio signal is routed back into the handset while simultaneously muting the PCM Handset and PCM Modem TX1 output signals.

When bit AOHME (Register 64h bit 7) is asserted, the input to the Handset line is sourced by the MONO_OUT analog audio output rather than the handset microphone

Likewise, by asserting AOHME, the Modem TX1 is sourced by the sum of MONO_OUT and the regular PCM Modem TX1 (enabled by T1AME = 1). This configuration allows speakerphone applications to either source the on-hold music by MONO_OUT analog audio or by supplying the music digitally via PCM Modem TX1.

In addition, regular speakerphone calls have the option of playing music from MONO_OUT to listeners by asserting AOHME and T1AME (Register 64h bit 6). Codec users have the option of playing music during a modem speakerphone call.

Note that the call progress power down (PDMX) must be 0 in order to get music out of a speakerphone call.

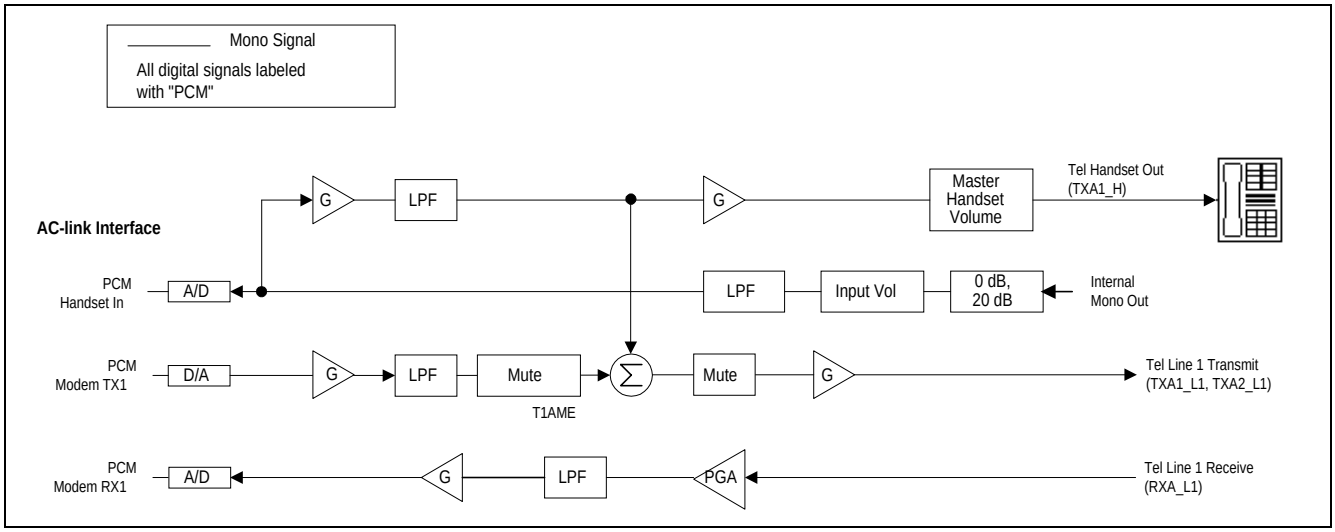


Figure 13. Analog On Hold Mixer

Call Progress

Register 64h has control bits that allow the controller to monitor call progress. Analog signals on Modem RX1, Modem TX1, Handset RX, and Handset TX can all be summed via the call progress mixer. Figure 14 shows the call progress signal routing and control signals. 6dB gain can be added to both handset and modem receive signals in order to compensate for signal loss in the analog line.

The PDMX bit (Register 64h bit 8) must be cleared to enable Call Progress Mixer operation.

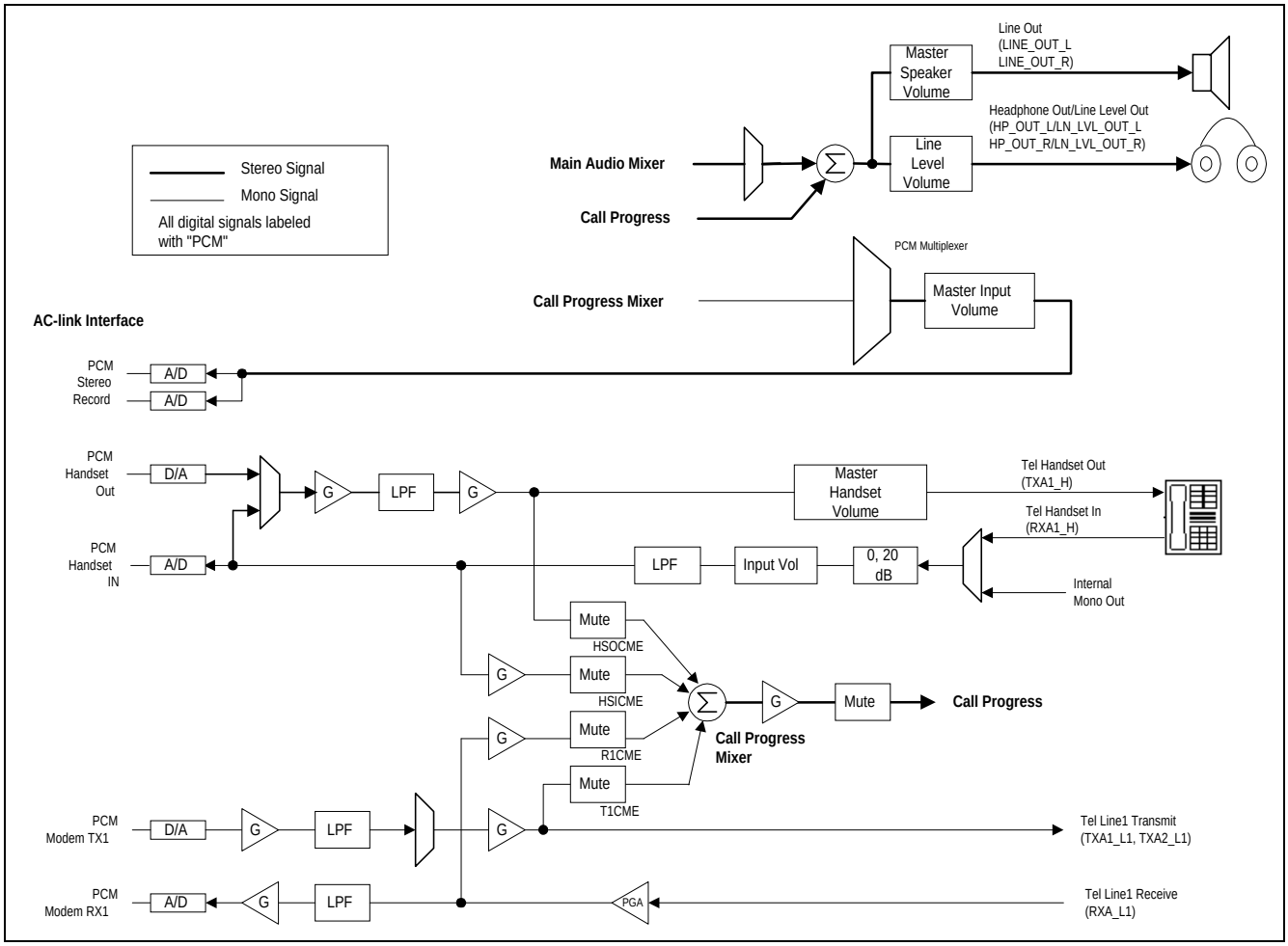


Figure 14. Call Progress Mixer

Interface Registers

Table 20 identifies the AMC registers and bits.

Table 20. Audio Modem Codec (AMC) Registers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	x	**SE4**	**SE3**	**SE2**	**SE1**	**SE0**	**ID9**	**ID8**	**ID7**	**ID6**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**	7173h
02h	Play Master Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Master Volume	Mute	x	x	x	x	x	x	x	x	x	x	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV2	PV0	x	0000h
0Ch	Phone Volume	Mute	x	x	x	x	x	x	x	x	x	x	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	x	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	x	x	x	x	x	x	x	x	x	x	x	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	POP	ST	3D	LD	x	x	MIX	MS	LPBK	x	PCMS	x	x	x	x	x	0000h
22h	3D Control	x	x	x	x	CR3	CR2	CR1	CR0	x	x	x	x	DP3	DP2	DP1	DP0	0300h
26h	Powerdown Control/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	PDM	PDA	MDM	**REF**	**ANL**	**DAC**	**ADC**	000xh
28h	Extended Audio ID	**ID1**	**ID0**	x	x	x	x	x	x	x	x	x	x	**VRM**	x	x	**VRA**	0009h
2Ah	Extended Audio Status/Control	x	PRL	PRK	PRJ	PRI	x	**MADC**	**LDAC**	**SDAC**	**CDA**	x	x	VRM	x	DRA	VRA	4x00h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	x	CID1	HSET	x	LIN1	000Dh~
3Eh	Extended Modem Status/Control	PRH	PRG	x	x	PRD	PRC	PRB	PRA	**HDAC**	**HADC**	x	x	**DAC1**	**ADC1**	**MREF**	**GPIO**	FFxxh
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
46h	Line 1 DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset DAC/ADC Level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ch	GPIO Pin Configuration	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wake up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	0xxxh
56h	Misc Modem AFE Status/Control	x	**CID1**	**CIDR**	MLNK	x	HSB2	HSB1	HSB0	x	x	x	x	x	L1B2	L1B1	L1B0	6000h
5Ah	Mixer Volume	x	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h
5Ch	Miscellaneous Audio	P3D	USEM	USEL	USER	CALM	CALL	CALR	DM	x	x	FAIM	FAIL	FAIR	DONM	DONL	DONR	0000h
5Eh-60h	Conexant Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0000h
62h	Caller ID Control and Status	x	x	x	x	x	x	x	x	**CIDRDY**	x	x	CIDBYP	CIDEN	CIDCLR	CIDCC	CIDCC1	0000h
64h	Monitor Call Progress	x	x	x	x	x	x	x	PDMX	AOHME	T1AME	HSOCME	HSICME	T1CME	R1CME	HSGEN	R1GEN	0000h
66h-7Ah	Conexant Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	xxxxh
7Ch	Vendor ID1	**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	4358h
7Eh	Vendor ID2	**T7**	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**	**REV7**	**REV6**	**REV5**	**REV4**	**REV3**	**REV2**	**REV1**	**REV0**	54xxh

Bold: Read-only inputs to AC-link.

Register Definitions

Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code identifying supported functions and a code identifying the 3D Stereo Enhancement supplier.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	x	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	7173h

Bit	Label	R/W	Description
15			**Reserved.** Set to 0.
14:10	SE[4:0]	R	**3D Stereo Enhancement Vendor ID.** Identifies the Conexant 3D Stereo Enhancement (11100b).
9	ID9	R	**20-Bit ADC Supported Status.** 0 = Not Supported.
8	ID8	R	**18-Bit ADC Supported Status.** 1 = Supported.
7	ID7	R	**20-Bit DAC Supported Status.** 0 = Not Supported.
6	ID6	R	**18-Bit DAC Supported Status.** 1 = Supported.
5	ID5	R	**Loudness (Bass Boost) Supported Status.** 0 = Not Supported.
4	ID4	R	**Headphone Out Supported Status.** 1 = Supported.
3	ID3	R	**Simulated Stereo (Mono to Stereo) Supported Status.** 0 = Not Supported.
2	ID2	R	**Bass and Treble Control Supported Status.** 0 = Not Supported.
1	ID1	R	**Modem Line Codec Supported Status.** 1 = Supported.
0	ID0	R	**Dedicated Mic PCM in Channel Supported Status.** 1 = Supported.

Play Master Volume Registers (Index 02h)

This register controls the Play Master output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Play Master Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Master Volume Mute.** 1 = The channel is muted. (Default.) 0 = Channel volume is controlled by the ML[4:0] and MR[4:0] bits).
14:13			**Reserved.**
12:8	ML[4:0]	R/W	**Left Master Volume Control Attenuation.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] / ML[4:0] / Attenuation** 0 / 00000 / 0 dB (Default) 0 / 00001 / 1.5 dB 0 / 11111 / 46.5 dB 1 / xxxxx / ∞ dB (Mute)
7:5			**Reserved.**
4:0	MR[4:0]	R/W	**Right Master Volume Control Attenuation.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] / MR[4:0] / Attenuation** 0 / 00000 / 0 dB (Default) 0 / 00001 / 1.5 dB 0 / 11111 / 46.5 dB 1 / xxxxx / ∞ dB (Mute)

Headphone Volume Register (Index 04h)

This register controls the Headphone output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphone Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Headphone Master Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the ML[4:0] and MR[4:0] bits.
14:13			**Reserved.**
12:8	ML[4:0]	R/W	**Headphone Left Master Volume Control.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] / ML[4:0] / Attenuation** 0 / 00000 / 0 dB (Default) 0 / 00001 / 1.5 dB 0 / 11111 / 46.5 dB 1 / xxxxx / ∞ dB (Mute)
7:5			**Reserved.**
4:0	MR[4:0]	R/W	**Headphone Right Master Volume Control.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] / MR[4:0] / Attenuation** 0 / 00000 / 0 dB (Default) 0 / 00001 / 1.5 dB 0 / 11111 / 46.5 dB 1 / xxxxx / ∞ dB (Mute)

Mono Master Volume Register (Index 06h)

This register controls the Mono Master output Volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Mono Master Volume	Mute	x	x	x	x	x	x	x	x	x	MM5	MM4	MM3	MM2	MM1	MM0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Mono Master Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the MM[4:0] bits.
14:5			**Reserved.**
4:0	MM[4:0]	R/W	**Mono Master Volume Control.** This field controls the Mono Master Volume Control output attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] / MM[4:0] / Attenuation** 0 / 00000 / 0 dB (Default) 0 / 00001 / 1.5 dB 0 / 11111 / 46.5 dB 1 / xxxxx / ∞ dB (Mute)

PC Beep Register (Index 0Ah)

This register controls the PC Beep input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV2	PV0	x	0000h

Bit	Label	R/W	Description
15	Mute	R/W	**PC Beep Volume Mute.** 1 = The channel is muted. 0 = The channel volume is controlled by the PV[3:0] bits. (Default.) Because the PC Beep signal input to the audio mixer is used primarily for system diagnostic purposes, the default value for the PC Beep Volume is unmuted.
14:5			**Reserved.**
4:1	PV[3:0]	R/W	**PC Beep Volume Control.** This field controls the PC Beep output attenuation from 0 dB to 46.5 dB in approximately 3 dB steps. **Mute [bit 15] / PV[3:0] / Attenuation** 0 / 0000 / 0 dB (Default) 0 / 0001 / 3 dB 0 / 1111 / 45 dB 1 / xxxx / ∞ dB (Mute)
0			**Reserved.**

Phone Volume Register (Index 0Ch)

This register controls the Phone input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	Phone Volume	Mute	x	x	x	x	x	x	x	x	x	x	GN4	GN3	GN2	GN1	GN0	8008h

Bit	Label	R/W	Description
15	Mute	R/W	**Phone Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GN[4:0] bits.
14:5			**Reserved.**
4:0	GN[4:0]	R/W	**Phone Volume**. This field controls Phone volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GN[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / -∞ dB (Mute)

Mic Volume Register (Index 0Eh)

This register controls the Mic input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	x	GN4	GN3	GN2	GN1	GN0	8008h

Bit	Label	R/W	Description
15	Mute	R/W	**Mic Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GN[4:0] bits.
14:7			**Reserved.**
6	20dB	R/W	**Mic 20 dB Gain Enable.** 1 = Enable the Mic 20 dB boost. 0 = Disable the Mic 20 dB boost. (Default.)
5			**Reserved.**
4:0	GN[4:0]	R/W	**Mic Volume.** This field controls the Mic volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GN[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

Line In Volume Register (Index 10h)

This register controls the Line In input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**Line In Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left Line In Volume.** This field controls the Left Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / -∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right Line In Volume**. This field controls the Right Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / -∞ dB (Mute)

CD Volume Register (Index 12h)

This register controls the CD input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**CD Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left CD Volume.** This field controls the Left CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right CD Volume**. This field controls the Right CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

Video Volume Register (Index 14h)

This register controls the CD input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	Video Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**Video Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left Video Volume.** This field controls the Left Video Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right Video Volume**. This field controls the Right Video Volume from +12 dB to -34.5 dB in approximately 1.5 dB steps. The default value is 0 dB. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

Aux Volume Register (Index 16h)

This register controls the Aux input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	Aux Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**Aux Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left Aux Volume.** This field controls the Left Aux Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right Aux Volume**. This field controls the Right Aux Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

PCM Out Volume Register (Index 18h)

This register controls the PCM Out output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**PCM Out Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left PCM Out Volume.** This field controls the Left PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right PCM Out Volume**. This field controls the Right PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

Record Select Register (Index 1Ah)

This register selects the record source.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h

Bit	Label	R/W	Description
15:11			**Reserved.**
10:8	SL[2:0]	R/W	**Left Record Select.** This field selects the record source for the left channel. **SL[2:0] — Left Record Source** 000 — Mic (Default) 001 — Left CD In 010 — Left Video In 011 — Left Aux In 100 — Left Line In 101 — Left Stereo Mix 110 — Mono Mix 111 — Phone (implemented internally)
7:3			**Reserved.**
2:0	SR[2:0]	R/W	**Right Record Select.** This field selects the record source for the right channel. **SR[2:0] — Right Record Source** 000 — Mic (Default) 001 — Right CD In 010 — Right Video In 011 — Right Aux In 100 — Right Line In 101 — Right Stereo Mix 110 — Mono Mix 111 — Phone (implemented internally)

Record Gain Register (Index 1Ch)

This register controls the input record gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Input Record Gain Mute.** 1 = The channel is muted. (Default.) 0 = Record gain is controlled by the GL[3:0] and GR[3:0] bits.
14:12			**Reserved.**
11:8	GL[3:0]	R/W	**Left Input Record Gain.** This field controls the Left Input Record Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. **Mute [bit 15] — GL[3:0] — Gain** 0 — 1111 — +22.5 dB 0 — 0000 — 0 dB (Default) 1 — xxxxx — –∞ dB (Mute)
7:4			**Reserved.**
3:0	GR[3:0]	R/W	**Right Input Record Gain.** This field controls the Right Input Record Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. **Mute [bit 15] — GR[3:0] — Gain** 0 — 1111 — +22.5 dB 0 — 0000 — 0 dB (Default) 1 — xxxxx — –∞ dB (Mute)

Record Gain Mic Register (Index 1Eh)

This register controls the input record gain mic.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Eh	Record Gain Mic	Mute	x	x	x	x	x	x	x	x	x	x	x	GM3	GM2	GM1	GM0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Input Record Gain Mic Mute.** 1 = The channel is muted. (Default.) 0 = Record gain is controlled by the GM[3:0] bits.
14:4			**Reserved.**
3:0	GM[3:0]	R/W	**Input Record Gain Mic.** This field controls the Record Gain Mic from 0 dB to +22.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GM[3:0] / Gain** 0 / 1111 / +22.5 dB 0 / 0000 / 0 dB (Default) 1 / xxxxx / –∞ dB

General Purpose Register (Index 20h)

This register controls several miscellaneous codec functions. This register should be read before writing, to generate a mask for only the bit(s) that need to be changed. The default value is 0000h which is all off.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	POP	ST	3D	LD	x	x	MIX	MS	LPBK	x	PCMS	AMC	x	x	x	x	0000h

Bit	Label	R/W	Description
15	POP	R/W	**PCM Output Path Select.** This bit controls the optional PCM out 3D bypass path and Mute (the pre and post 3D PCM out paths are mutually exclusive). 1 = Post 3D. 0 = Pre 3D. (Default.)
14	ST	R/W	**Simulated Stereo Enhancement.** Not supported. Must be 0. Defaults to 0.
13	3D	R/W	**3D Stereo Enhancement On/Off Control.** 1 = 3D Stereo Enhancement on. 0 = 3D Stereo Enhancement off. (Default.)
12	LD	R/W	**Loudness (Bass Boost) On/Off Control.** Not supported. Must be 0. Defaults to 0.
11:10			**Reserved.**
9	MIX	R/W	**Mono Output Select.** 1 = Mic input 0 = Input Mixer output. (Default.)
8	MS	R/W	**Microphone Input Select.** 1 = Mic 2 (not supported) 0 = Mic 1. (Default.)
7	LPBK	R/W	**ADC/DAC Loopback Mode Enable.** 1 = Enable loopback of the stereo ADC output to the stereo DAC input (left-to-left, right-to-right) without involving the AC-link, allowing for full system performance measurements. 0 = Disable loopback. (Default.)
6			**Reserved.**
5	PCMS	R/W	**PCM Output Selection.** 0 = result of bit 15; 1 = PCM DAC Out to no Mix, Main Analog Out = PCM Stereo. See Figure 15. **POP (Bit 15) / PCMS (Bit 5) / Description** 0 / 0 — Normal operation occurs, with the PCM stereo DAC output going into the audio mixer, going through the 3D block (if enabled), and then out the speaker. This output can then be recorded if the record mux is selected properly. 1 / 0 — The PCM stereo DAC output is summed after the 3D block. Again, the output can be record if the record mux is selected properly. 1 / 1 — The PCM stereo DAC goes directly out to the speaker. What can be recorded is post 3D without the PCM stereo DAC. 0 / 1 — The speaker, headphone, and mono output (if mic as input is not selected) are muted.
4:0			**Reserved.**

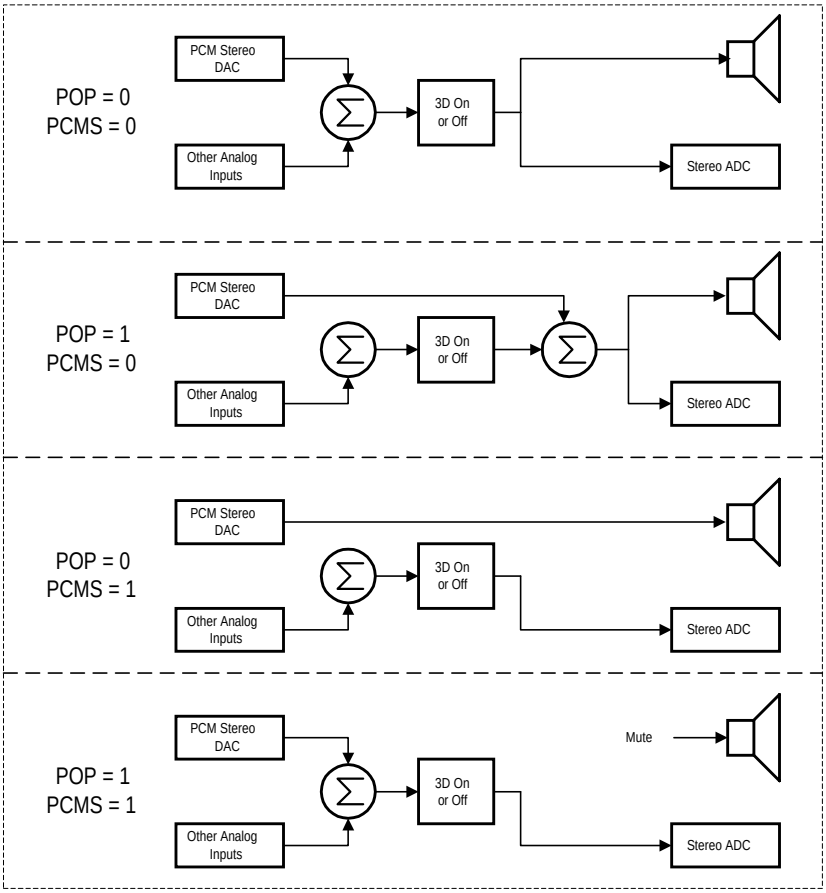


Figure 15. PCM Output Select: 3-Way Mux Options

3D Control Register (Index 22h)

This register controls the 3D Stereo Enhancement Gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	x	x	x	x	CR3	CR2	CR1	CR0	x	x	x	x	DP3	DP2	DP1	DP0	0300h

Bit	Label	R/W	Description
15:12			**Reserved.**
11:8	CR[3:0]	R/W	**3D Stereo Enhancement Gain A.** This field controls the 3D Stereo Enhancement Gain A from -32 dB, -12 dB to 9 dB in 1.5 dB steps. **CR[3:0] Gain** 0000 -32 dB (Default) 0001 -12 dB …. …. 1111 9 dB
7:4			**Reserved.**
3:0	DP[3:0]	R/W	**3D Stereo Enhancement Gain B.** This field controls the 3D Stereo Enhancement Gain B from -32 dB, -12 dB to 9 dB in 1.5 dB steps. **DP[3:0] Gain** 0000 -32 dB (Default) 0001 -12 dB …. …. 1111 9 dB

Powerdown Control/Status Register (Index 26h)

This register controls powerdown states and monitors subsystem readiness. The lower four bits are read-only status with a "1" indicating that the subsection is "ready". Ready indicates the subsection is able to perform in its nominal state. When this register is written, the bit values that come in on AC-link have no effect on read only bits 4-0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Powerdown Control/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	PDM	PDA	MDM	REF	ANL	DAC	ADC	000xh

Bit	Label	R/W	Description
15	EAPD	R/W	**External Amplifier Power Down.** 0 = Do not powerdown External Amplifier; causes pin 18 (EAPD) to be low. (Default.) 1 = Powerdown External Amplifier; causes pin 18 (EAPD) to be high.
14	PR6	R/W	**Powerdown Headphone Amplifier.** 0 = Do not powerdown Headphone Amplifier. (Default.) 1 = Powerdown Headphone Amplifier.
13	PR5	R/W	**Powerdown Internal Clock Circuit.** 0 = Do not powerdown internal clock circuit. (Default.) 1 = Powerdown internal clock circuit.
12	PR4	R/W	**Powerdown Digital Interface.** 0 = Do not powerdown digital AC-link interface. (Default.) 1 = Powerdown digital AC-link interface.
11	PR3	R/W	**Powerdown Analog Mixer with Vref Off.** PR3 can be used in combination with PR2 or by itself. 0 = Do not powerdown Analog Mixer. (Default.) 1 = Powerdown Analog Mixer and turn Vref off.
10	PR2	R/W	**Powerdown Analog Mixer with Vref On.** 0 = Do not powerdown Analog Mixer. (Default.) 1 = Powerdown Analog Mixer but leave Vref on.
9	PR1	R/W	**Powerdown PCM Output DACs.** 0 = Do not powerdown PCM Output DACs. (Default.) 1 = Powerdown PCM Output DACs.
8	PR0	R/W	**Powerdown PCM Input ADCs and Input Mux.** 0 = Do not powerdown PCM Input ADCs and Input Mux. (Default.) 1 = Powerdown PCM Input ADCs and Input Mux.
7	PRZ	R/W	**Powerdown Clock Interface Except BIT_CLK.** 0 = Do not powerdown Clock Interface. (Default.) 1 = Powerdown Clock Interface except BIT_CLK output. This turns off all digital power to clock interface except BIT_CLK so the ASIC controller can monitor GPIOs.
6	PDM	R/W	**Powerdown Mono Amplifier.** 0 = Do not powerdown Mono output amplifier. (Default.) 1 = Powerdown Mono output amplifier.
5	PDA	R/W	**Powerdown Line Out Amplifiers.** 0 = Do not powerdown stereo Line Out output amplifiers. (Default.) 1 = Powerdown stereo Line Out output amplifiers (left and right).
4	MDM	R	**Modem Ready Status.** Not supported, always 0. (Default.) See Register 3Eh.
3	REF	R	**Audio Reference Voltages Ready Status.** 0 = Audio reference voltages (Vrefs) not ready. 1 = Audio reference voltages (Vrefs) ready (at nominal level).
2	ANL	R	**Analog Mixers Ready Status.** 0 = Analog mixers not ready. 1 = Analog mixers ready.
1	DAC	R	**DAC Ready Status.** 0 = Stereo playback DAC not ready to accept data. 1 = Stereo playback DAC ready to accept data.
0	ADC	R	**ADC Ready Status.** 0 = Stereo record ADC not ready to transmit data. 1 = Stereo record ADC ready to transmit data.

Extended Audio ID Register (Index 28h)

The read-only Extended Audio ID register identifies which extended audio features are supported (in addition to the original AC '97 features identified by reading the Reset register at Index 0h). A 1 indicates the extended audio feature is supported.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	**ID1**	**ID0**	x	x	x	x	x	x	x	x	x	x	**VRM**	x	x	**VRA**	0009h

Bit	Label	R/W	Description
15:14	ID[1:0]	R	**Codec Configuration Identifier.** This 2-bit field identifies the codec configuration. 00 = Primary codec configuration supported.
13:4			**Reserved.**
3	VRM	R	**Variable Rate Mic Supported.** 1 = Supported.
2:1			**Reserved.**
0	VRA	R	**Variable Rate PCM Audio Supported.** 1 = Supported.

Extended Audio Status and Control Register (Index 2Ah)

The Extended Audio Status and Control Register provides status and control of the extended audio features.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Extended Audio Status/Control	x	PRL	PRK	PRJ	PRI	x	**MADC**	**LDAC**	**SDAC**	**CDA**	x	x	VRM	x	DRA	VRA	4x00h

Bit	Label	R/W	Description
15			**Reserved.**
14	PRL	R/W	**Power Down Mic ADC.** 0 = Do not turn off the Mic ADC. 1 = Turn off the Mic ADC (Mic ADC operation is independent of PR0 in address 26h). (Default.)
13	PRK	R/W	**Power Down PCM LFE DACs.** Not supported. Defaults to 1.
12	PRJ	R/W	**Power Down PCM Surround DAC.** Not supported. Defaults to 1.
11	PRI	R/W	**Power Down PCM Center DAC.** Not supported. Defaults to 1.
10			**Reserved.**
9	MADC	R	**Mic ADC Ready Status.** 0 = Mic ADC is not ready. (Default.) 1 = Mic ADC is ready.
8	LDAC	R	**PCM LFE DAC Ready Status**. Not supported. Defaults to 0.
7	SDAC	R	**PCM Surround DAC Ready Status.** Not supported. Defaults to 0.
6	CDAC	R	**PCM Center DAC Ready Status**. Not supported. Defaults to 0.
5:4			**Reserved.**
3	VRM	R/W	**Variable Rate Mic Input Enable.** 0 = Disables Variable Rate Audio mode for the dedicated Mic ADC. (Default.) 1 = Enables Variable Rate Audio mode for the dedicated Mic ADC.
2			**Reserved.**
1	DRA	R/W	**Double-Rate PCM Audio Mode Enable.** Not supported. Defaults to 0.
0	VRA	R/W	**Variable Rate PCM Audio Mode Enable.** 0 = Disables Variable Rate PCM Audio Mode. (Default.) 1 = Enables Variable Rate PCM Audio Mode.

PCM Front DAC Rate Control Registers (Index 2Ch)

Registers 2Ch (PCM Front DAC Rate), 32h (PCM LR ADC Rate), and 34h (MIC ADC Rate) operate in a similar manner. Writing to these audio sample rate control registers alters the DAC and ADC rate for those channels. They are read/write registers.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**PCM Front DAC Sample Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2B11 — 11.025 kHz 2EE0 — 12 kHz 3E80 — 16 kHz 5622 — 22.050 kHz 5DC0 — 24 kHz AC44 — 44.1 kHz 7D00 — 32 kHz BB80 — 48 kHz

PCM LR ADC Rate Control Registers (Index 32h)

This register controls the PCM LR ADC Sample rate.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**PCM LR ADC Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2B11 — 11.025 kHz 2EE0 — 12 kHz 3E80 — 16 kHz 5622 — 22.050 kHz 5DC0 — 24 kHz AC44 — 44.1 kHz 7D00 — 32 kHz BB80 — 48 kHz

MIC ADC Rate Control Registers (Index 34h)

This register controls the Mic ADC Sample rate.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**Mic ADC Sample Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2580 — 9.6 kHz 3592 — 13.71428 kHz 3E80 — 16 kHz 4B00 — 19.2 kHz 5DC0 — 24 kHz BB80 — 48 kHz

Extended Modem ID Register (Index 3Ch)

The extended modem ID is a read/write register that primarily identifies the codec's modem AFE capabilities. Writing any value to this register performs a warm modem AFE reset (register range 3C-56h), including GPIO (register range 4C-54h). The warm reset causes all affected registers to revert to their default values.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	x	CID1	HSET	x	LIN1	000Dh~

Bit	Label	R/W	Description
15:14	ID[1:0]	R/W	**Codec Configuration Identifier.** This 2-bit field identifies the codec configuration: 00 = Primary codec configuration
13:4			**Reserved.**
3	CID1	R	**Caller ID Decode for Line 1 Supported.** 1 = Supported.
2	HSET	R	**Handset DAC Supported.** 1 = Supported.
1			**Reserved.**
0	LIN1	R	**Line 1 Supported.** 1 = Supported.

Extended Modem Status and Control Register (Index 3Eh)

This register controls modem and handset powerdown and reports modem and handset ready status. This register functions similarly to the Powerdown Control/Status Register (Index 26h), however, bit MDM in register 26h is not supported and replaced by extended functions in this register. Bits 15-8 are read/write and control modem subsystem powerdown. Bits 7-0 are read-only and indicate modem subsystem readiness.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Eh	Extended Modem Status/Control	PRH	PRG	x	x	PRD	PRC	PRB	PRA	HDAC	HADC	x	x	DAC1	ADC1	MREF	GPIO	FFxxh

Bit	Label	R/W	Description
15	PRH	R/W	**Powerdown Handset DAC.** 0 = Do not powerdown DAC. 1 = Powerdown DAC. (Default.)
14	PRG	R/W	**Powerdown Handset ADC.** 0 = Do not powerdown ADC. 1 = Powerdown ADC. (Default.)
13:12			**Reserved.**
11	PRD	R/W	**Powerdown Modem Line 1 DAC.** 0 = Do not powerdown DAC. 1 = Powerdown DAC. (Default.)
10	PRC	R/W	**Powerdown Modem Line 1 ADC.** 0 = Do not powerdown ADC. 1 = Powerdown ADC. (Default.)
9	PRB	R/W	**Powerdown Modem Vref.** 0 = Do not powerdown Modem Vref. 1 = Powerdown Modem Vref. (Default.)
8	PRA	R/W	**Powerdown GPIO.** 0 = Do not powerdown GPIO. 1 = Powerdown GPIO. (Default.) **NOTE:** When the GPIO section is powered down, all outputs are tri-stated and input slot 12 is marked invalid when the AC-link is active.
7	HDAC	R	**Handset DAC Ready Status.** 0 = Not ready. (Default.) 1 = Ready.
6	HADC	R	**Handset ADC Ready Status.** 0 = Not ready. (Default.) 1 = Ready.
5:4			**Reserved.**
3	DAC1	R	**Modem Line 1 DAC Ready Status.** 0 = Not ready. (Default.) 1 = Ready.
2	ADC1	R	**Modem Line 1 ADC Ready Status.** 0 = Not ready. (Default.) 1 = Ready.
1	MREF	R	**Modem Reference Voltage (Vrefs) Ready Status.** 0 = Not ready. (Default.) 1 = Ready.
0	GPIO	R	**GPIO Ready Status.** 0 = Not ready. (Default.) 1 = Ready.

Modem Line 1 DAC/ADC Rate Control Register (Index 40h)

These registers control the sample rate the modem line 1 ADC/DAC uses sending/receiving samples to/from the controller.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**Line 1 DAC/ADC Sample Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2580 — 9.6 kHz 3592 — 13.71428 kHz 3E80 — 16 kHz 4B00 — 19.2 kHz 5DC0 — 24 kHz BB80 — 48 kHz The default values are loaded after a cold reset or a controller-write to register 3Eh.

Handset DAC/ADC Rate Control Register (Index 44h)

These registers control the sample rate the handset ADC/DAC uses for sending/receiving samples to/from the controller.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**Handset DAC/ADC Sample Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2580 — 9.6 kHz 3592 — 13.71428 kHz 3E80 — 16 kHz 4B00 — 19.2 kHz 5DC0 — 24 kHz BB80 — 48 kHz The default values are loaded after a cold reset or a controller-write to register 3Eh.

Modem Line 1 DAC/ADC Level Control Registers (Index 46h)

This read/write register controls the modem line 1 DAC and ADC levels.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	Line 1 DAC/ADC level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h

Bit	Label	R/W	Description
15	Mute	R/W	**Modem Line 1 Output Mute.** 0 = The Modem Line 1 output level is controlled by the DAC[3:0] bits. 1 = The Modem Line 1 output is muted. (Default.)
14:12			**Reserved.**
11-8	DAC[3:0]	R/W	**Modem Line 1 Output Attenuation.** This field controls the Modem Line 1 Output Attenuation from 0 dB to -45 dB in 3 dB steps when the Modem Line 1 Output Mute bit is cleared. **Mute[bit 15] DAC[3:0] Attenuation** 0 0000 0 dB 0 0001 3 dB (Default) 1 1111 –45 dB (Mute)
7	Mute	R/W	**Modem Line 1 Input Mute.** 0 = The Modem Line 1 Input level is controlled by the ADC[3:0] bits. 1 = The Modem Line 1 Input is muted. (Default.)
6			**Modem Line 1 Input 20 dB Attenuation Enable.** 0 = Disable 20 dB attenuation. (Default.) 1 = Enable 20 dB attenuation.
5:4			**Reserved.**
3:0	ADC[3:0]	R/W	**Modem Line 1 Input Gain.** This field controls the Modem Line 1 Input Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps when the Modem Line 1 Input Mute bit is cleared. **Mute [bit 7] ADC[3:0] Gain** 0 1111 +22.5 dB 0 0000 0 dB (Default) 1 xxxx –∞ dB (Mute)

Handset DAC/ADC Level Control Registers (Index 4Ah)

This register controls the handset output volume and mute when the handset is connected to TXA_H via relay control as well as the handset input volume and mute.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ah	Handset DAC/ADC level	Mute	x	x	x	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h

Bit	Label	R/W	Description
15	Mute	R/W	**Handset Output Mute.** 0 = The channel attenuation is controlled by the DAC[4:0] bits. 1 = The channel is muted. (Default.)
14:12			**Reserved.**
11-8	DAC[3:0]	R/W	**Handset Output Attenuation.** This field controls the Handset Output Attenuation from 0 dB to -45 dB in 3 dB steps when the Handset Output Mute bit is cleared. **Mute[bit 15] DAC[3:0] Attenuation** 0 0000 0 dB 0 0001 3 dB (Default) 1 1111 –45 dB (Mute)
7	Mute	R/W	**Handset Input Mute.** 0 = The channel gain is controlled by the ADC[3:0] bits. 1 = The channel is muted. (Default.)
6			**Handset 20 dB Attenuation Enable.** 1 = Enable 20 dB attenuation. 0 = Disable 20 dB attenuation. (Default.)
5:4			**Reserved.**
3:0	ADC[3:0]	R/W	**Handset Input Gain.** This field controls the Handset Input Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps when the Handset Input Mute bit is cleared.. **Mute [bit 7] ADC[3:0] Gain** 0 1111 +22.5 dB 0 0000 0 dB (Default) 1 xxxx –∞ dB (Mute)

GPIO Pin Configuration Register (Index 4Ch)

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

On cold reset or a controller write to register 3Ch, all pins are configured as inputs.

NOTE: A warm reset will **not** reconfigure all outputs as inputs. The status of all implemented GPIO pins will initially read back "1" (via Slot 12 or register 54h), unimplemented GPIO pins (GPIO9-GPIO15) will always read back "0". This scheme informs software as to how many GPIO pins have been implemented. The controller must send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ch	GPIO Pin Configuration	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh

GPIO Pin Polarity/Type Register (Index 4Eh)

The GPIO Pin Polarity/Type is a read/write register that defines:

- GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an input.
- GPIO Output Type (0=CMOS, 1=Open-drain) when a GPIO pin is configured as an output.

On cold reset or a controller write to register 3Ch, this register defaults to all 1's.

NOTE: A warm reset will **not** cause this register to default to all 1's.

Unimplemented GPIO pins (GPIO9-GPIO15) always return 1's.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh

GPIO Pin Sticky Register (Index 50h)

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0=Not Sticky, 1=Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a “0” to the corresponding bit of the GPIO Pin Status register 54h (see below), and by reset. Sticky is defined as Edge sensitive, Non-Sticky as Level-sensitive.

On cold reset or a controller write to register 3Ch, this register defaults to all "0’s" specifying Non-Sticky.

NOTE: A warm reset will **not** cause this register to default to all 0's.

Unimplemented GPIO pins (GPIO9-GPIO15) always return "0’s".

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h

GPIO Pin Wake up Mask Register (Index 52h)

The GPIO Pin Wake up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake up or GPIO_INT (0=No interrupt, 1=Yes interrupt). When the AC-Link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wake up event will trigger the assertion of SDATA_IN (the AC-Link wake up protocol is defined in Appendix C). When AC-link is powered up, a wake up event will appear as GPIO_INT=1 on bit 0 of input slot 12.

An AC-Link wake up Interrupt is defined as a "0" to "1" transition on SDATA_IN when the AC-Link is Powered down (Register 26h PR4="1"). GPIO bits that have been programmed as Inputs, Sticky and Pin Wake up, upon transition (either high-to-low or low-to-high depending on pin polarity), will cause an AC-Link wake up event (transition of SDATA_IN from "0" to "1"), only if the AC-Link was powered down.

On cold reset or a controller write to register 3Ch this register defaults to all "0's" specifying no wake up event.

NOTE: A warm reset will **not** cause this register to default to all 0's.

Unimplemented GPIO pins (GPIO9-GPIO15) always returns "0's".

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
52h	GPIO Pin Wake up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h

GPIO Pin Status Register (Index 54h)

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a “0” to the corresponding bit of this register.

Bits corresponding to unimplemented GPIO pins (GPIO15-GPIO8) should be forced to zero in this register and input slot 12.

Reset does not affect the value read. It is always the state of the GPIO pin. GPIO bits that have been programmed as Inputs and Sticky, upon transition (either high-to-low or low-to-high depending on pin polarity), will cause the individual GI bit to go asserted "1", and remain asserted until a write of "0" to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	0xxxh

Miscellaneous Modem Register (Index 56h)

This read/write register defines the loopback modes available for the modem line and handset ADCs/DACs and Caller ID bits.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Misc Modem AFE Status/Control	x	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	x	x	x	x	L1B2	L1B1	L1B0	6000h

Bit	Label	R/W	Description
15			**Reserved.**
14	CID1	R	**Caller ID Decode for Line 1 Supported.** 1 = Caller ID Decode for Line 1 is supported.
13	CIDR	R	**Caller ID Data is Raw.** 0 = Caller ID data is not raw (i.e., Caller ID data is demodulated and decoded).
12	MLNK	R/W	**MC '97 Link.** Controls MC '97 AC-link status. 0 = AC-link is on. (Default.) 1 = AC-link is off (sleep).
11			**Reserved.**
10:8	HSB[2:0]	R/W	**Handset Loopback Enable.** **HSB[2:0] Function** 000 = Disabled (Default) 001 = ADC loopback 010 = Local Analog loopback 011 = DAC loopback 100 = Remote Analog loopback 101 = ADC and DAC loopback combined 110 = Reserved 111 = Reserved
7:3			**Reserved.**
2:0	L1B[2:0]	R/W	**Modem Line 1 Loopback Enable.** **L2B[2:0] Function** 000 = Disabled (Default) 001 = ADC Loopback 010 = Local analog loopback 011 = DAC Loopback 100 = Remote analog loopback 101 = ADC and DAC loopback combined 110 = Reserved 111 = Reserved

Mixer Volume Register (Index 5Ah)

This register controls the attenuation on each of the signals coming into the main mixer so as to prevent clipping of the final signal. The step size is 1.5 dB and the range is 0 to -21.0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah	Mixer Volume	x	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h

Bit	Label	R/W	Description
15:12			**Reserved.**
11:8	MXL[3:0]	R/W	**Left Mixer Volume Attenuation**. This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. **Mute** **MXL[3:0]** **Attenuation** 0 0000 0 dB (Default) 0 0001 1.5 dB 0 …. …. 0 1110 21.0 dB
7:4			**Reserved.**
3:0	MXR[3:0]	R/W	**Right Mixer Volume Attenuation.** This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. **Mute** **MXR[3:0]** **Attenuation** 0 0000 0 dB (Default) 0 0001 1.5 dB 0 …. …. 0 1110 21.0 dB

Miscellaneous Audio Register (Index 5Ch)

This register allocates bits to control and provide status of the ADC DC offset calibration. It also has bits to enable dithering of the ADC output. All bits are defaulted 0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ch	Miscellaneous Audio	P3D	USEM	USEL	USER	CALM	CALL	CALR	DM	x	x	FAIM	FAIL	FAIR	DONM	DONL	DONR	0000h

Bit	Label	R/W	Description
15	P3D	R/W	**3D Block Power Down Control.** 0 = Do not powerdown 3D block. (Default.) 1 = Powerdown 3D block.
14	USEM	R/W	**DC Offset Calibration Use, Dedicated Mic ADC.** 0 = Do not calibrate. (Default.) 1 = Calibrate.
13	USEL	R/W	**DC Offset Calibration Use, Left Channel of Audio ADC.** 0 = Do not calibrate. (Default.) 1 = Calibrate.
12	USER	R/W	**DC Offset Calibration Use, Right Channel of Audio ADC.** 0 = Do not calibrate. (Default.) 1 = Calibrate.
11	CALM	R/W	**DC Offset Calibration Start, Dedicated Mic ADC.** 0 = Do not start calibration. (Default.) 1 = Start calibration.
10	CALL	R/W	**DC Offset Calibration Start, Left Channel of Audio ADC.** 0 = Do not start calibration. (Default.) 1 = Start calibration.
9	CALR	R/W	**DC Offset Calibration Start, Right Channel of Audio ADC.** 0 = Do not start calibration. (Default.) 1 = Start calibration.
8	DM	R/W	**Dither Disable for Dedicated Mic ADC.** 0 = Enable dither. (Default.) 1 = Disable dither.
7:6			**Reserved.**
5	FAIM	R	**DC Offset Calibration Fail, Dedicated Mic ADC.** 0 = Calibration did not fail. 1 = Calibration failed.
4	FAIL	R	**DC Offset Calibration Fail, Left Channel of Audio ADC.** 0 = Calibration did not fail. 1 = Calibration failed.
3	FAIR	R	**DC Offset Calibration Fail, Right Channel of Audio ADC.** 0 = Calibration did not fail. 1 = Calibration failed.
2	DONM	R	**DC Offset Calibration Done, Dedicated Mic ADC.** 0 = Calibration not complete. 1 = Calibration complete.
1	DONL	R	**DC Offset Calibration Done, Left Channel of Audio ADC.** 0 = Calibration not complete. 1 = Calibration complete.
0	DONR	R	**DC Offset Calibration Done, Right Channel of Audio ADC.** 0 = Calibration not complete. 1 = Calibration complete.

Caller ID (Index 62h)

This register provides control and status bits to support Caller ID operation during system low power mode.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
62h	Caller ID Control and Status	x	x	x	x	x	x	x	x	CIDRDY	x	x	CIDBYP	CIDEN	CIDCLR	CIDCC	CIDCC1	0000h

Bit	Label	R/W	Description
15:8			**Reserved.**
7	CIDRDY	R	**Caller ID Data Ready.** Status bit reporting when Caller ID information is available. 0 = Caller ID information obtained in Low-Power mode is not available. (Default.) 1 = Caller ID information obtained in Low-Power mode is available (ready).
6:5			**Reserved.**
4	CIDBYP	R/W	**Caller ID Internal Filter Bypass.** Control bit used to route the Caller ID signal around the internal filter (assuming an external filter is provided). 0 = The Caller ID signal does not bypass the internal filter. (Default.) 1 = The Caller ID signal bypasses the internal filter.
3	CIDEN	R/W	**Caller ID Enable.** Control bit used to clear Caller ID low-power storage register once the controller has obtained data. 0 = Disable Caller ID feature. (Default.) 1 = Enable Caller ID feature.
2	CIDCLR	R/W	**Caller ID Clear.** Control bit used to clear Caller ID internal RAM once the controller has obtained data. 0 = Do not clear Caller ID internal RAM. (Default.) 1 = Clear Caller ID internal RAM.
1:0	CIDCC[1:0]	R/W	**Caller ID Country Code.** This control field specifies the Caller ID Type. **CIDCC[1:0] Type** 00 = United States (Default) 01 = British 10 = France 11 = Japan

Monitor Call Progress (Index 64h)

This register is used to control analog modem call progress and analog on hold mixers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
64h	Monitor Call Progress	x	x	x	x	x	x	x	PDMX	AOHME	T1AME	HSOCME	HSICME	T1CME	R1CME	HSGEN	R1GEN	0000h

Bit	Label	R/W	Description
15:9			**Reserved.**
8	PDMX	R/W	**Power Down Call Progress Mixer and Analog on Hold Mixer.** 0 = Do not power down Call Progress Mixer and Analog On Hold Mixer. (Default.) 1 = Power down Monitor Call Progress Mixer and Analog On Hold Mixer.
7	AOHME	R/W	**Analog On Hold Mixer Enable.** 0 = No receive signal input signal into mixer. (Default.) 1 = RXA modem input is taken from MONOOUT; TXA_L1 is fed transmit data from TXA_H.
6	T1AME	R/W	**Transmit Line 1 Input to Analog On Hold Mixer Enable.** 0 = Disable Transmit Line signal input to the Analog On Hold Mixer (when LBF = 1, Line 1 is transmitted out on TXA_L1). (Default.) 1 = Enable Transmit Line signal input to the Analog On Hold Mixer (when LBF = 1, Line 1 and Handset transmit are added together and transmitted out on TXA_L1).
5	HSOCME	R/W	**Handset Out (Transmit Line 1) Input to Call Progress Mixer Enable.** 0 = Disable Handset Out signal input to the Call Progress Mixer. (Default.) 1 = Enable Handset Out signal input to the Call Progress Mixer.
4	HSICME	R/W	**Handset In (Receive Line 1) Input to Call Progress Mixer Enable.** 0 = Disable Handset In (MONOOUT) signal input to the Call Progress Mixer. (Default.) 1 = Enable Handset In (MONOOUT) signal input to the Call Progress Mixer.
3	T1CME	R/W	**Transmit Line 1 Input to Call Progress Mixer Enable.** 0 = Disable Transmit Line 1 signal input to the Call Progress Mixer. (Default.) 1 = Enable Transmit Line 1 signal input to the Call Progress Mixer.
2	R1CME	R/W	**Receive Line 1 Input to Call Progress Mixer Enable.** 0 = Disable Receive Line 1 signal input to the Call Progress Mixer. (Default.) 1 = Enable Receive Line 1 signal input to the Call Progress Mixer.
1	HSGEN	R/W	**Handset Amplifier Gain Enable.** 0 = Disable 6 dB gain in the Handset In path to the Call Progress Mixer. (Default.) 1 = Enable 6 dB gain in the Handset In path to the Call Progress Mixer.
0	R1GEN	R/W	**Receive Line 1 Amplifier Gain Enable.** 0 = Disable 6 dB gain in the Receive Line 1 path to the Call Progress Mixer. (Default.) 1 = Enable 6 dB gain in the Receive Line 1 path to the Call Progress Mixer.

Vendor ID Registers 1 and 2 (Indexes 7Ch, 7Eh)

These registers contain the vendor identification code and revision numbers.

The vendor identification code is reported in the F[7:0], S[7:0], and T[7:0] fields. The ID method is Microsoft's Plug and Play Vendor ID code.

The vendor revision number is reported in the REV[7:0] field.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4358h

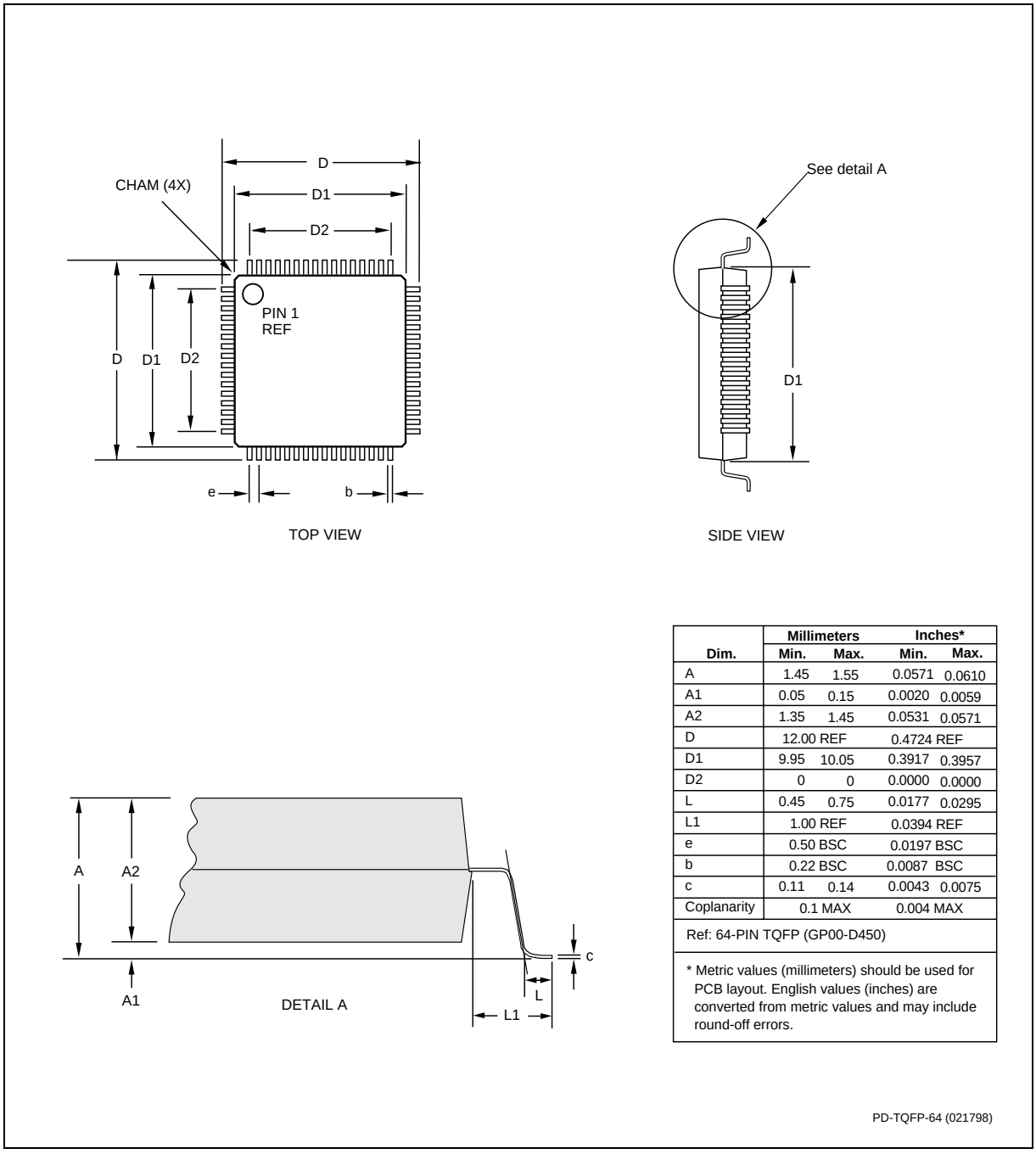
Bit	Label	R/W	Description
15:8	F[7:0]	R	**Vendor ID Code Character 1.** Conexant ID code character 1: ASCII "C" (43h).
7:0	S[7:0]	R	**Vendor ID Code Character 2.** Conexant ID code character 2: ASCII "X" (58h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	54xxh

Bit	Label	R/W	Description
15:8	T[7:0]	R	**Vendor ID Code Character 3.** Conexant ID code character 3: ASCII "T" (54h).
7:0	REV[7:0]	R	**Vendor Revision Number**. Conexant revision number.

Package Dimensions

The 64-pin TQFP package dimensions are shown in Figure 16.



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.45	1.55	0.0571	0.0610
A1	0.05	0.15	0.0020	0.0059
A2	1.35	1.45	0.0531	0.0571
D	12.00 REF		0.4724 REF	
D1	9.95	10.05	0.3917	0.3957
D2	0	0	0.0000	0.0000
L	0.45	0.75	0.0177	0.0295
L1	1.00 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.22 BSC		0.0087 BSC	
c	0.11	0.14	0.0043	0.0075
Coplanarity	0.1 MAX		0.004 MAX	

Ref: 64-PIN TQFP (GP00-D450)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-64 (021798)

Figure 16. 64-Pin TQFP package dimensions

Application Connection Circuits

Typical SoftAMC Interface Connections and Supporting Components

Figure 17 shows typical SoftAMC interface connections in an application circuit with required supporting components. Recommended supporting components are listed in Table 21.

Table 21. Typical SoftAMC Interface Components

Pin Name	Connection Description
VDD	Connect to GND through 0.1 uF ceramic capacitors
AVDD	Connect to AGND through 0.1 uF ceramic and 10 uF capacitors in parallel with each other. One pair for each AVDD.
POR	Connect to GND through 1 uF ceramic capacitor
XTLI	39 pF to GND
XTLO	39 pF to GND
PC_BEEP	1 uF AC-coupling capacitor
AUX_L	1 uF AC-coupling capacitor
AUX_R	1 uF AC-coupling capacitor
VIDEO_L	1 uF AC-coupling capacitor
VIDEO_R	1 uF AC-coupling capacitor
CD_L	1 uF AC-coupling capacitor
CD_R	1 uF AC-coupling capacitor
MIC1	1 uF AC-coupling capacitor
LINE_IN_L	1 uF AC-coupling capacitor
LINE_IN_R	1 uF AC-coupling capacitor
VREF	10 uF Tantalum in parallel with 0.1 uF ceramic to AGND
VREFOUT	200 ohm in series with 10 uF Tantalum in parallel with 0.1 uF ceramic to AGND
VC_A	10 uF Tantalum in parallel with 0.1 uF ceramic to MAGND
MIX_CIN_L	1 uF ceramic to MIX_COUT_L
MIX_CIN_R	1 uF ceramic to MIX_COUT_R
VREFP_M	10 uF Tantalum in parallel with 0.1 uF ceramic to MAGND
VC_M	10 uF Tantalum in parallel with 0.1 uF ceramic to MAGND
LINE_OUT_L	1 uF AC-coupling capacitor. Also attach a 47 kΩ resistor if the DC level is desired to be 0V
LINE_OUT_R	1 uF AC-coupling capacitor. Also attach a 47 kΩ resistor if the DC level is desired to be 0V
CAP2	12 nF between CAP2 and CAP3.
CAP3	47 nF to AGND

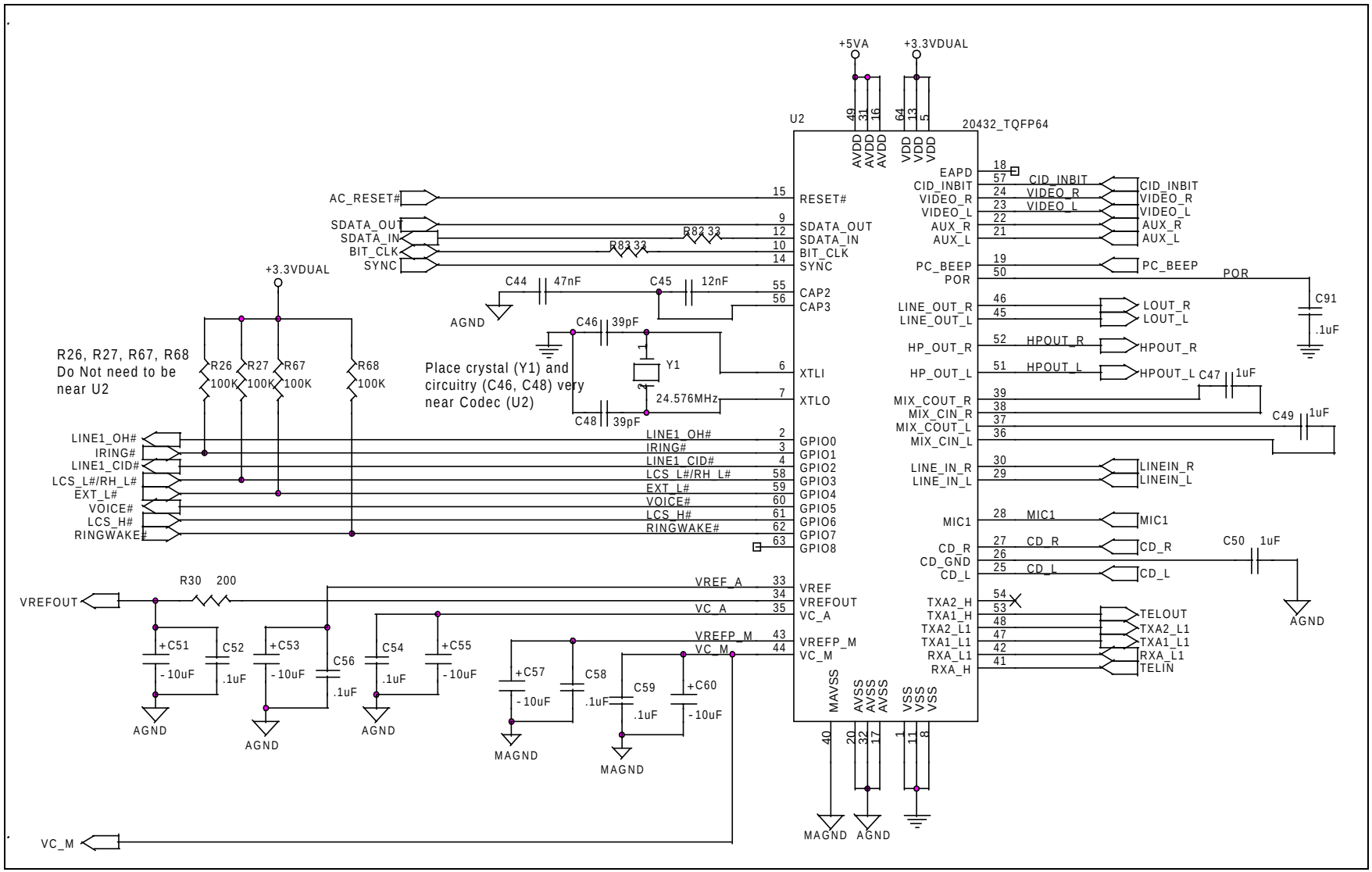


Figure 17. Typical SoftAMC Interface Schematic

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