6AM15

Silicon N/P Channel MOS FET
High Speed Power Switching

HITACHI

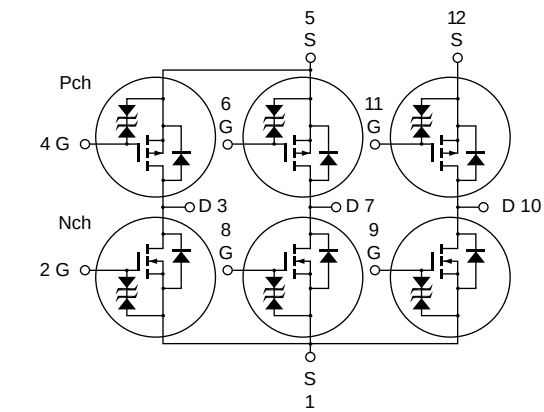
ADE-208-719 (Z)
1st. Edition
Feb. 1999

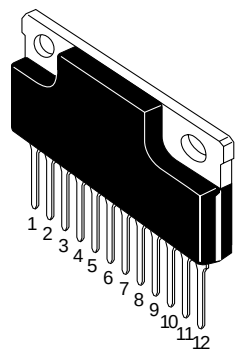
Features

- Low on-resistance
  N Channel : $R_{DS(on)}$ = 0.045 Ω typ.
  P Channel : $R_{DS(on)}$ = 0.085 Ω typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source
- High density mounting

Outline

SP-12TA





1. Nch Source
2, 8, 9 Nch Gate
3, 7, 10 Nch Drain
Pch Drain
4, 6, 11 Pch Gate
5, 12. Pch Source

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	10	–10	A
Drain peak current	$I_{D(pulse)}$ Note1	40	–40	A
Body-drain diode reverse drain current	I_{DR}	10	–10	A
Avalanche current	I_{AP} Note3	10	–10	A
Avalanche energy	E_{AR} Note3	8.5		mJ
Channel dissipation	Pch (Tc = 25°C) Note2	42		W
Channel dissipation	Pch Note2	4.8		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 6 Devices operation
3. Value at Ta = 25°C, Rg ≥ 50

Electrical Characteristics (N Channel) (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.045	0.060	Ω	I_D = 5 A, V_{GS} = 10 V [Note5]
	$R_{DS(on)}$	—	0.070	0.115	Ω	I_D = 5 A, V_{GS} = 4 V [Note5]
Forward transfer admittance	$\|y_{fs}\|$	5.5	9	—	S	I_D = 5 A, V_{DS} = 10 V [Note5]
Input capacitance	Ciss	—	500	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	110	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} =10 V, I_D = 5 A
Rise time	t_r	—	50	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	
Fall time	t_f	—	100	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F =10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	52	—	ns	I_F =10 A, V_{GS} = 0 diF/ dt = 50A/ µs

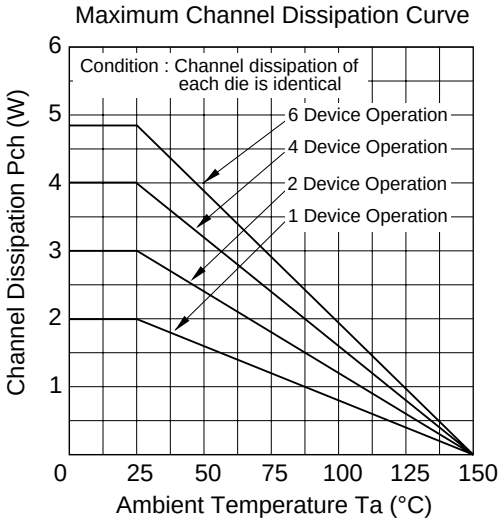
Note: 5. Pulse test

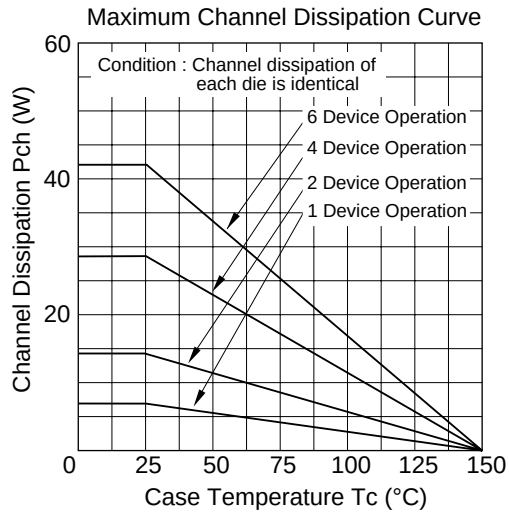
Electrical Characteristics (P Channel) (Ta = 25°C)

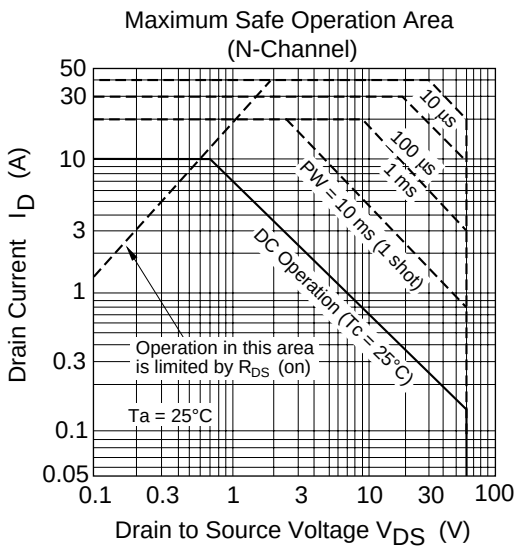
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.085	0.105	Ω	I_D = –5 A, V_{GS} = –10 V [Note5]
	$R_{DS(on)}$	—	0.115	0.165	Ω	I_D = –5 A, V_{GS} = –4 V [Note5]
Forward transfer admittance	$\|y_{fs}\|$	5.5	9	—	S	I_D = –5 A, V_{DS} = –10 V [Note5]
Input capacitance	Ciss	—	850	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	420	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	110	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	V_{GS} = –10 V, I_D = –5 A
Rise time	t_r	—	55	—	ns	R_L = 6 Ω
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	
Fall time	t_f	—	70	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.95	—	V	I_F = –10 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	65	—	ns	I_F = –10 A, V_{GS} = 0 diF/ dt = 50 A/ µs

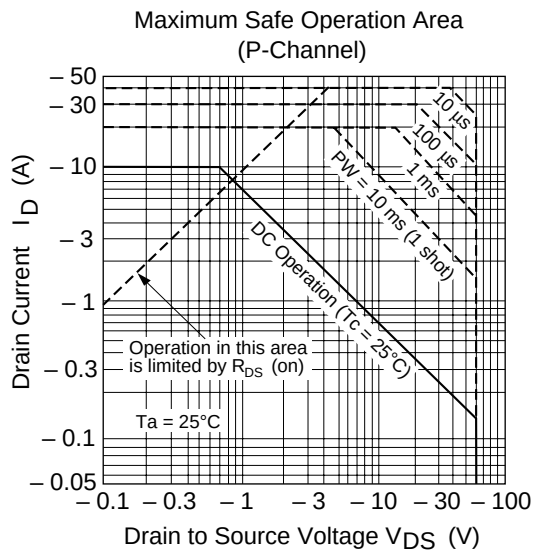
Note: 5. Pulse test

Main Characteristics



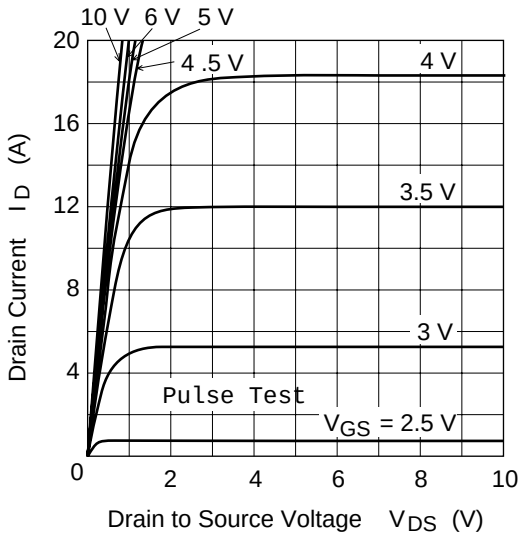




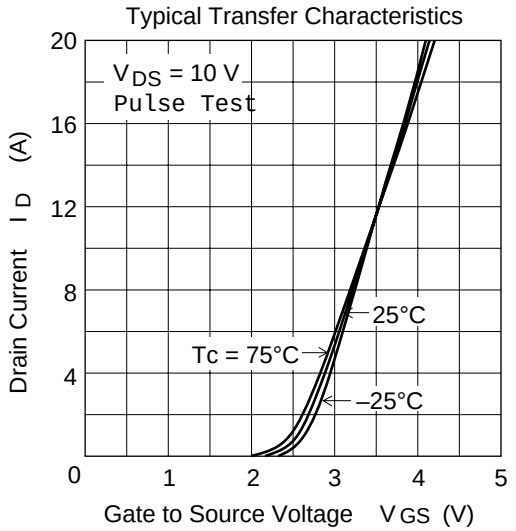


Main Characteristics (N Channel)

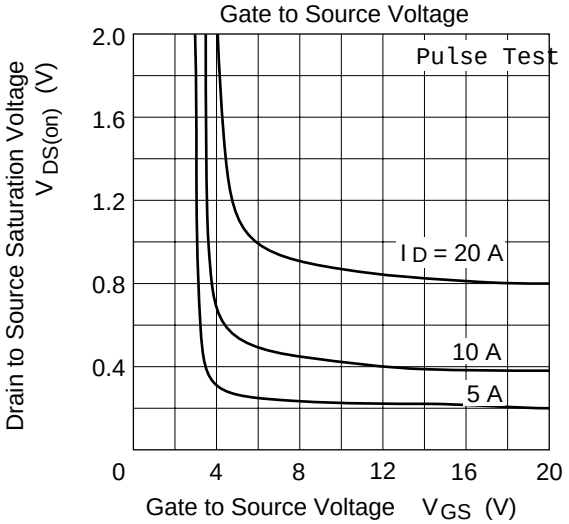
Typical Output Characteristics



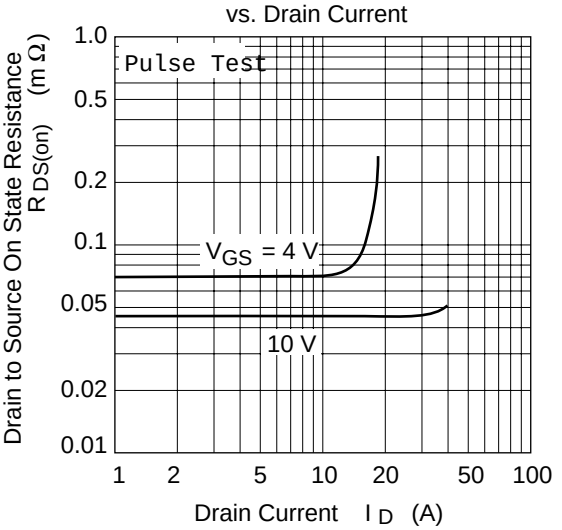
Typical Transfer Characteristics



Drain to Source Saturation Voltage vs. Gate to Source Voltage

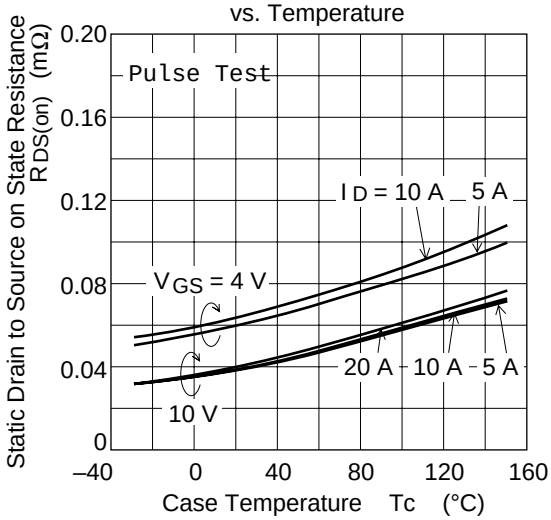


Static Drain to Source on State Resistance vs. Drain Current

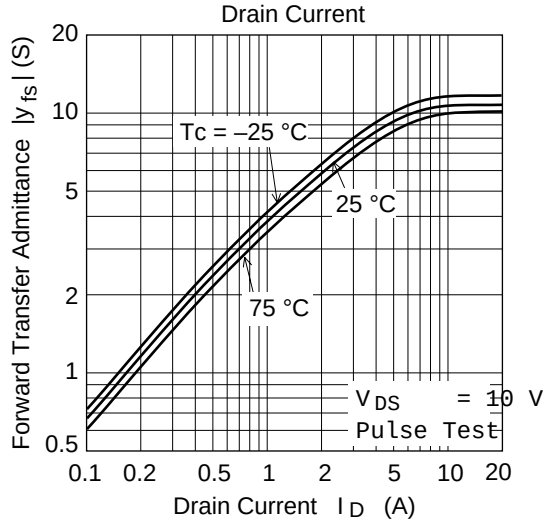


Main Characteristics (N Channel)

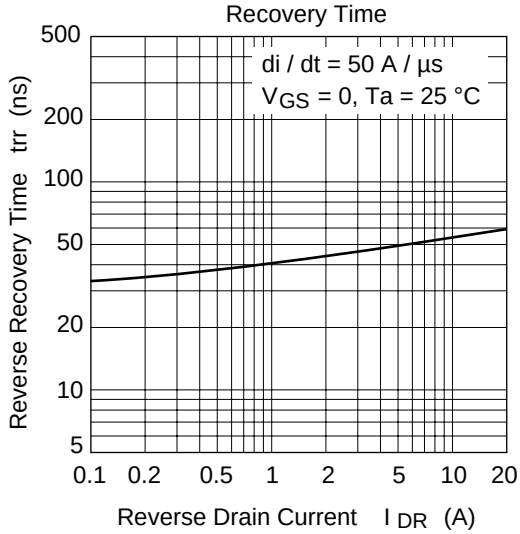
Static Drain to Source on State Resistance vs. Temperature



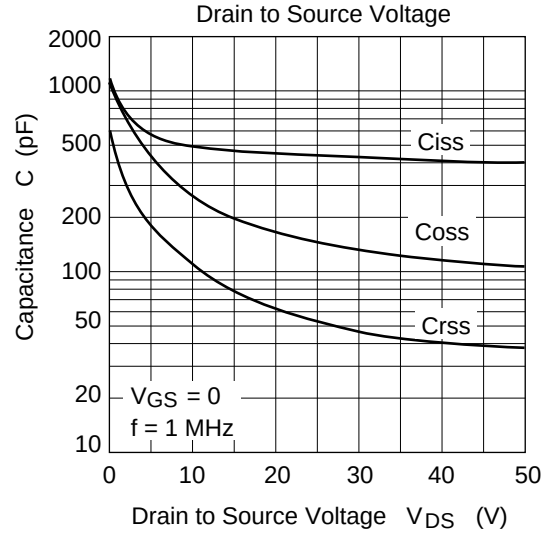
Forward Transfer Admittance vs. Drain Current



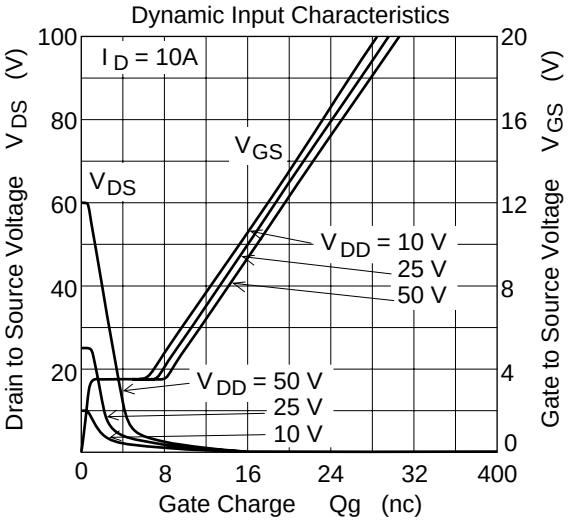
Body–Drain Diode Reverse Recovery Time

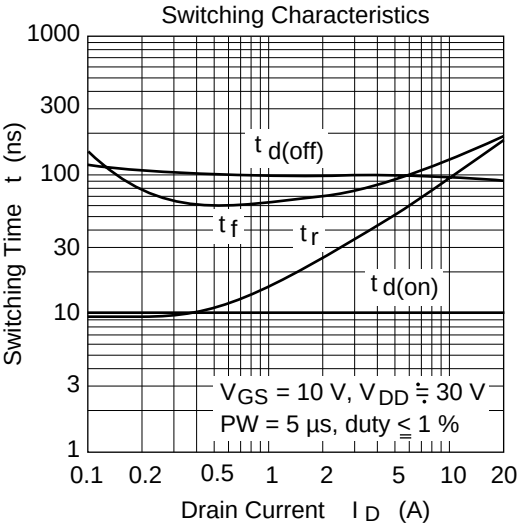


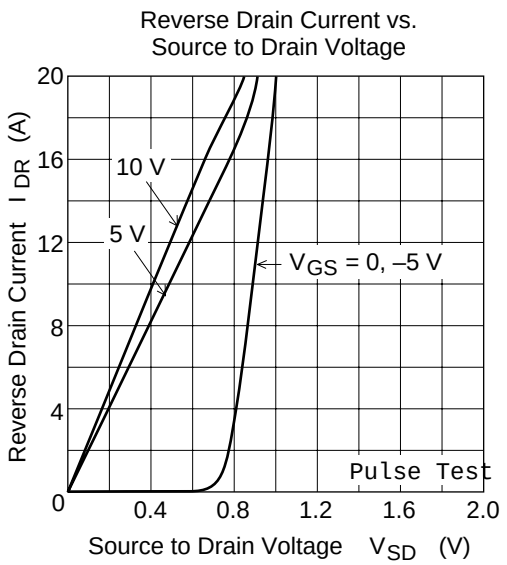
Typical Capacitance vs. Drain to Source Voltage

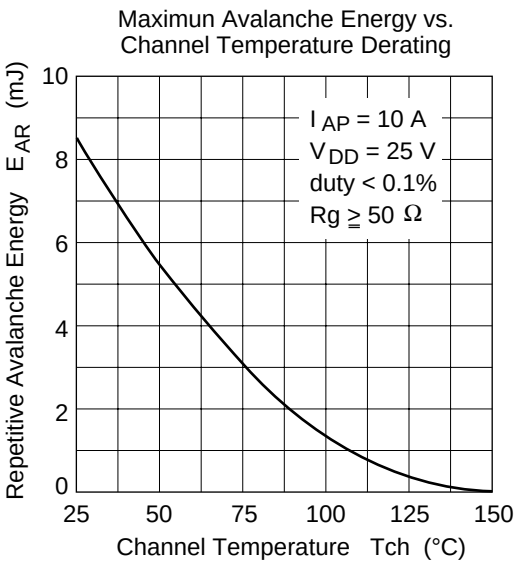


Main Characteristics (N Channel)



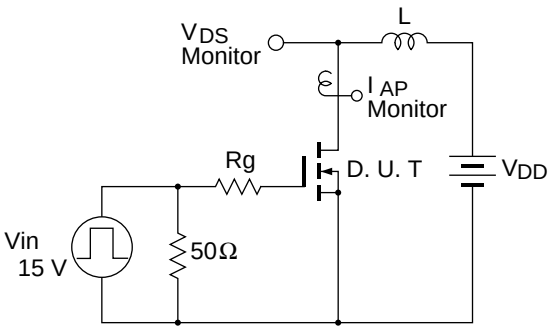






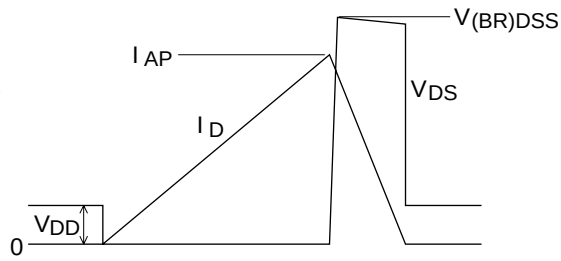
Main Characteristics (N Channel)

Avalanche Test Circuit

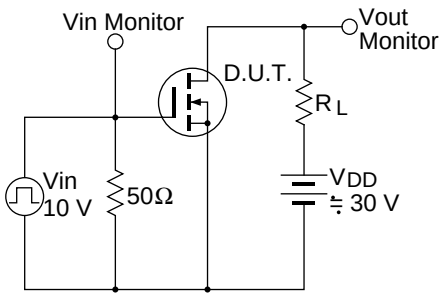


Avalanche Waveform

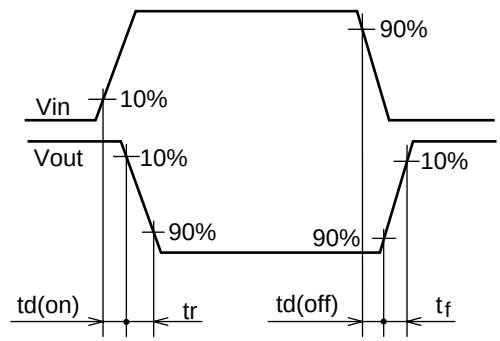
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



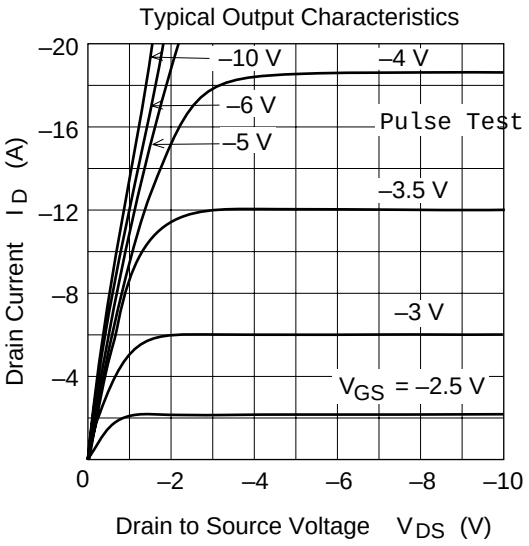
Switching Time Test Circuit

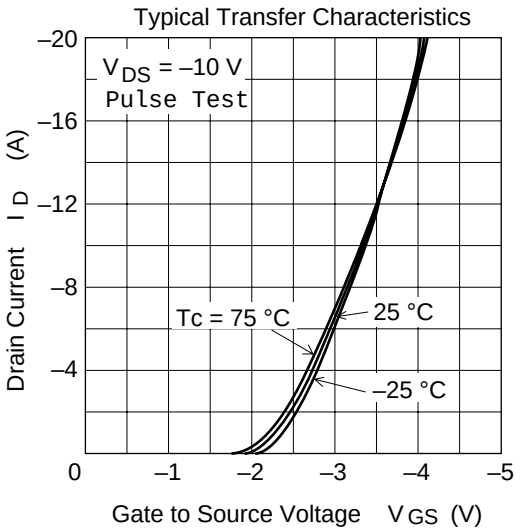


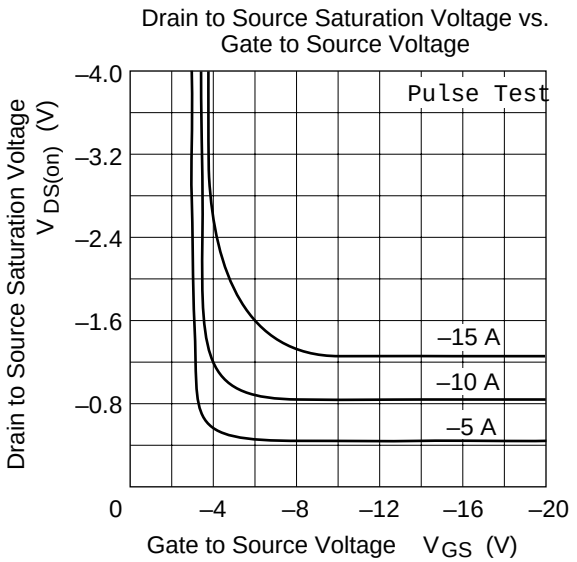
Waveform

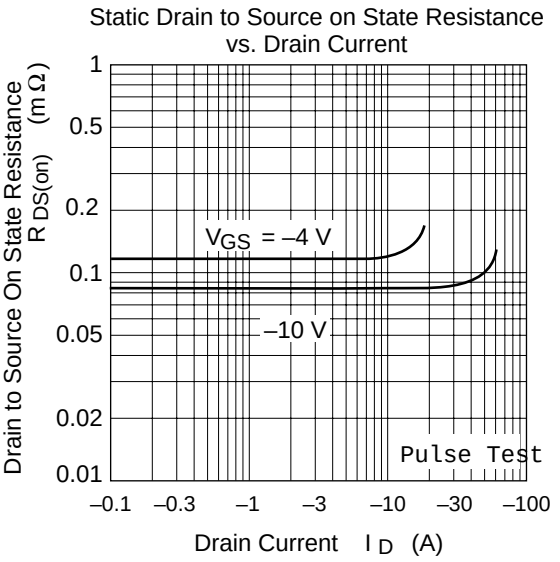


Main Characteristics (P Channel)



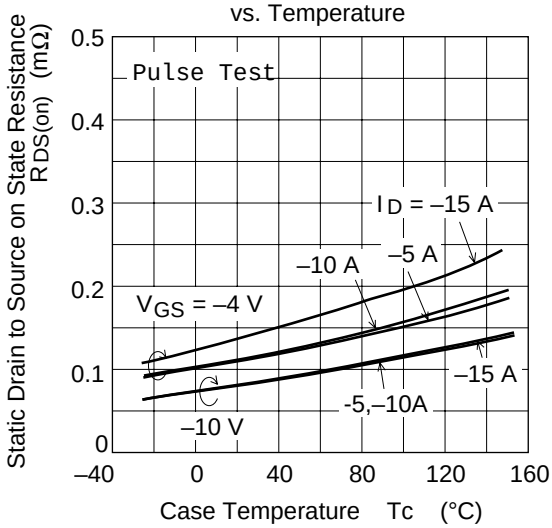




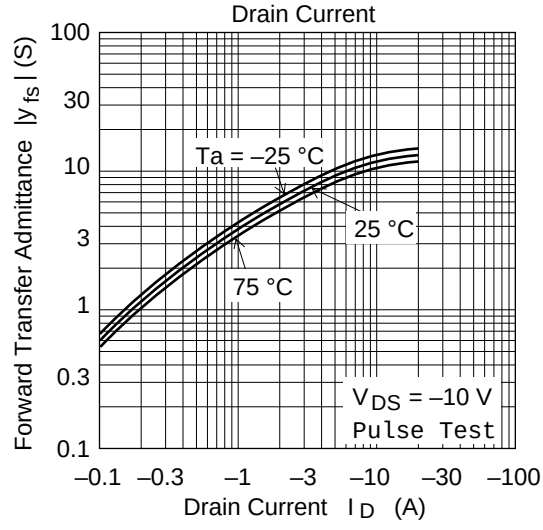


Main Characteristics (P Channel)

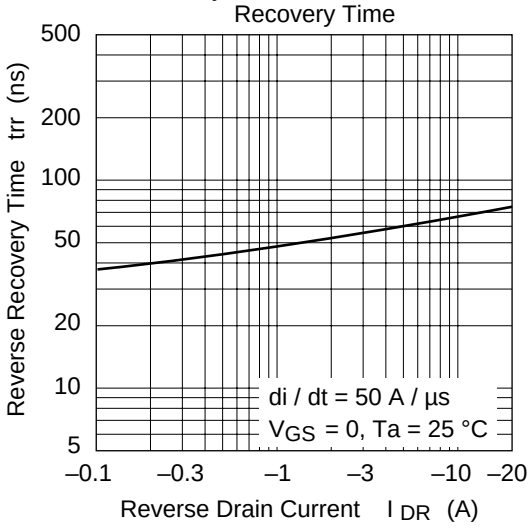
Static Drain to Source on State Resistance vs. Temperature



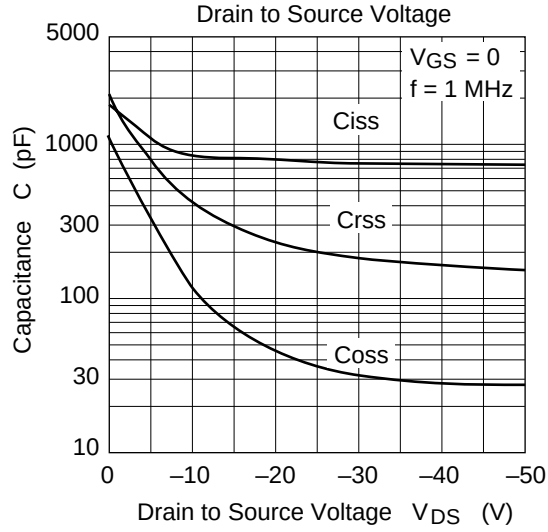
Forward Transfer Admittance vs. Drain Current



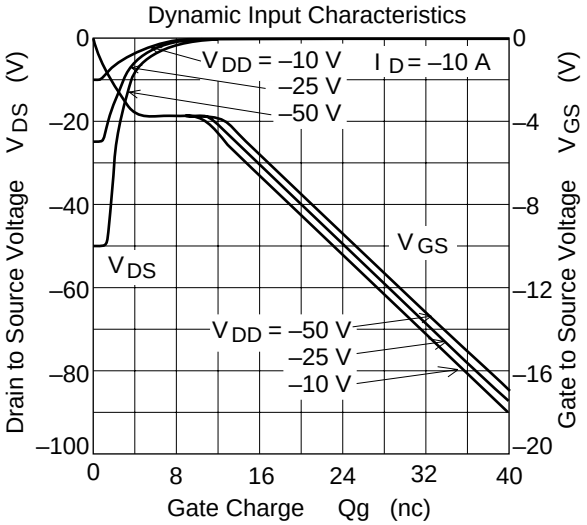
Body–Drain Diode Reverse Recovery Time

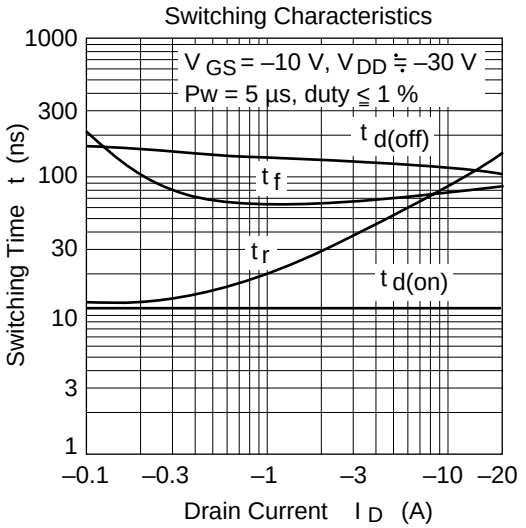


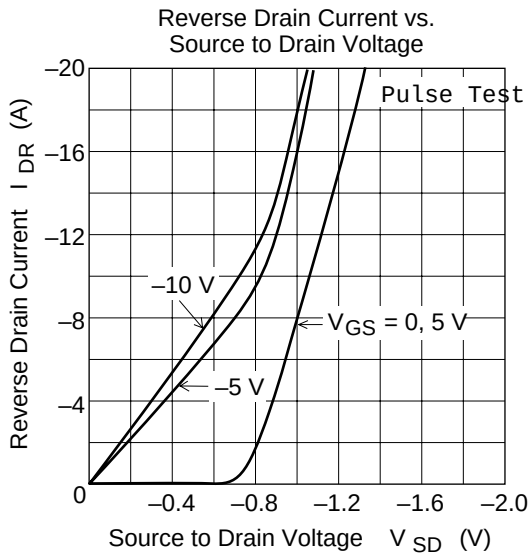
Typical Capacitance vs. Drain to Source Voltage

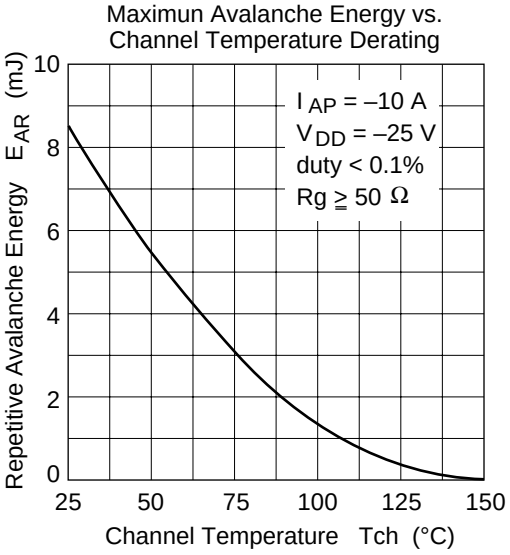


Main Characteristics (P Channel)



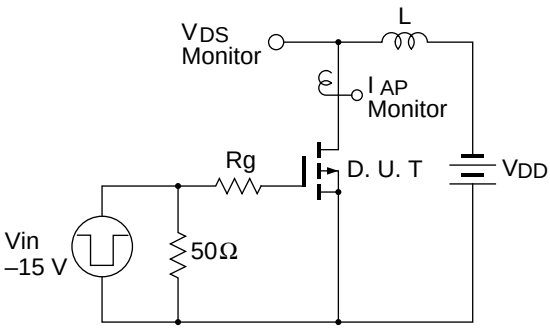






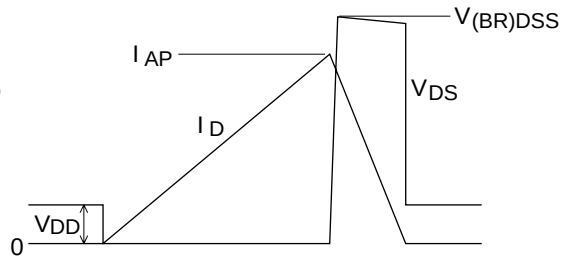
Main Characteristics (P Channel)

Avalanche Test Circuit

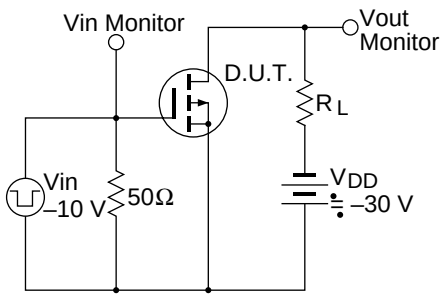


Avalanche Waveform

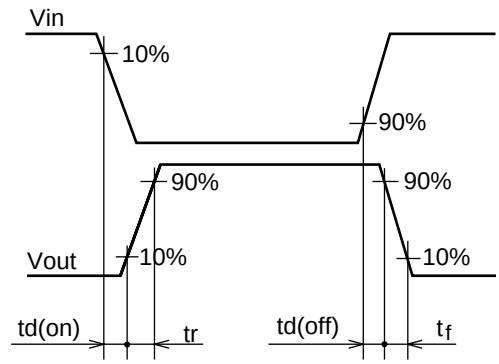
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

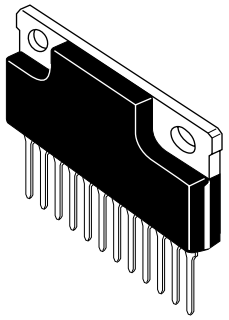


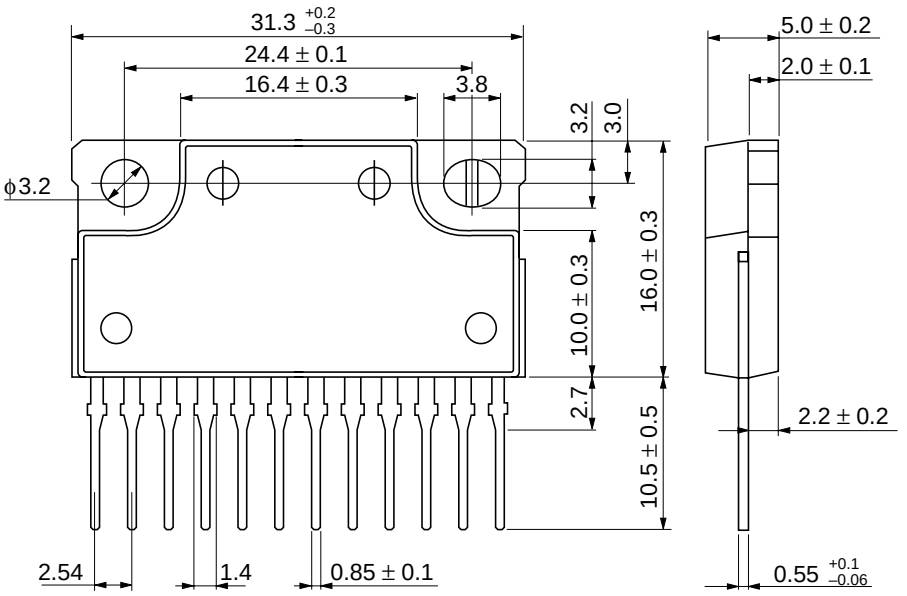
Waveform

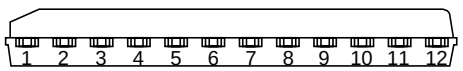


Package Dimensions

As of January, 2001
Unit: mm







Hitachi Code	SP-12TA
JEDEC	—
EIAJ	—
Mass (reference value)	6.1 g

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