

# 74HCT534

5 V octal D-type flip-flop; positive-edge trigger; inverting;  
3-state

Rev. 03 — 18 October 2004

Product data sheet

## 1. General description

The 74HCT534 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HCT534 is specified in compliance with JEDEC standard no. 7A.

The 74HCT534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74HCT534 is functionally identical to the 74HCT374, but has inverted outputs.

## 2. Features

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input.

## 3. Quick reference data

**Table 1: Quick reference data**  
*GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay CP to $\overline{Q}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	-	13	-	ns
f <sub>max</sub>	maximum clock frequency	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	-	40	-	MHz
C <sub>I</sub>	input capacitance		-	3.5	-	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 4.5 V	<a href="#">[1]</a> <a href="#">[2]</a>	19	-	pF

[1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

**PHILIPS**

$V_{CC}$  = supply voltage in Volts;  
 N = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2] The condition is  $V_I = GND$  to  $V_{CC} - 1.5 V$ .

### 4. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HCT534N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT534D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

### 5. Functional diagram

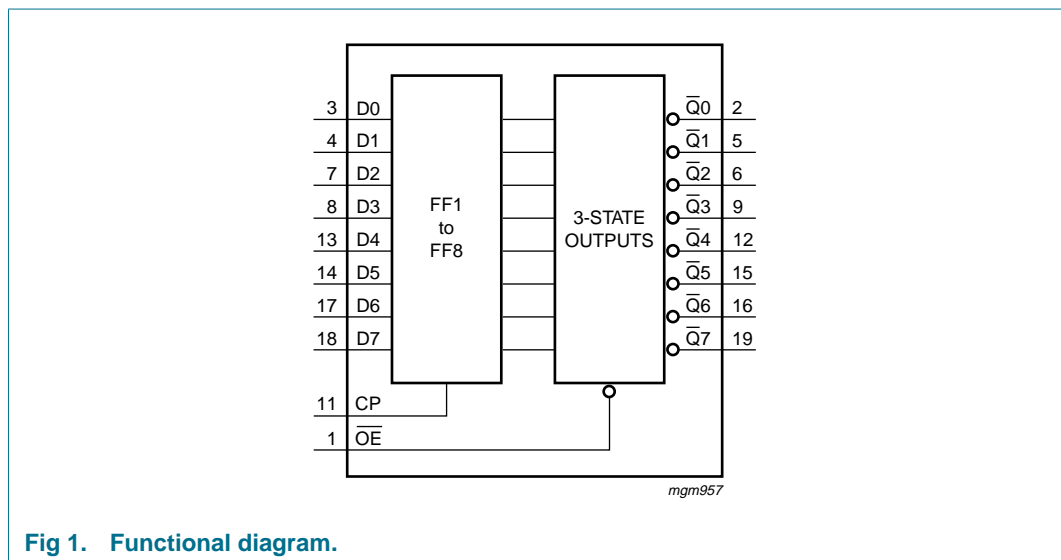


Fig 1. Functional diagram.

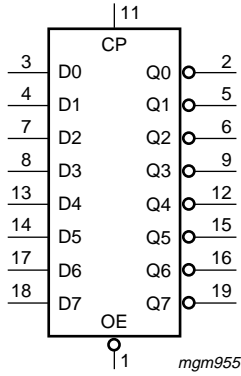


Fig 2. Logic symbol.

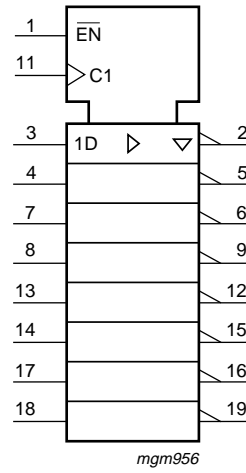


Fig 3. IEC logic symbol.

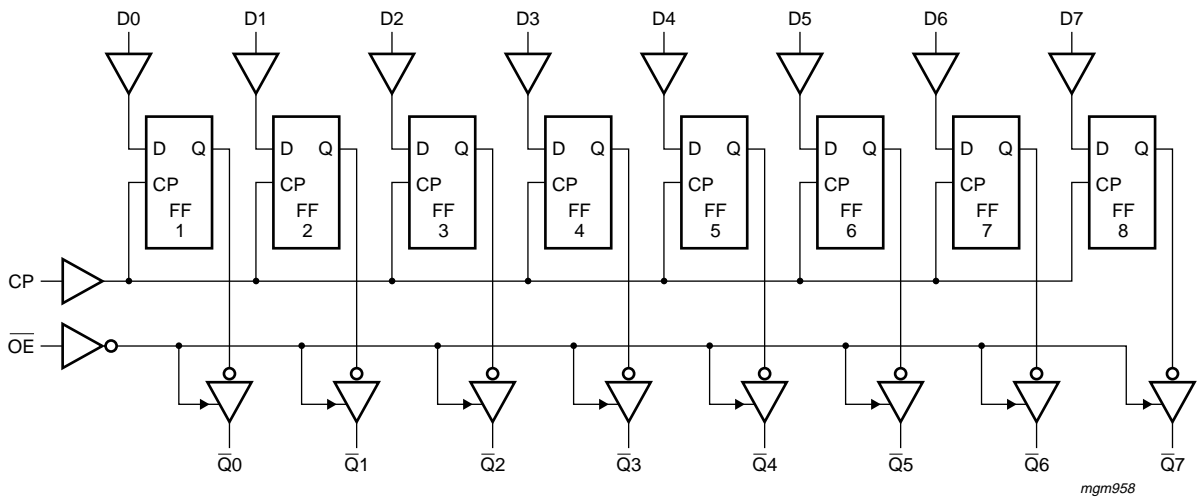
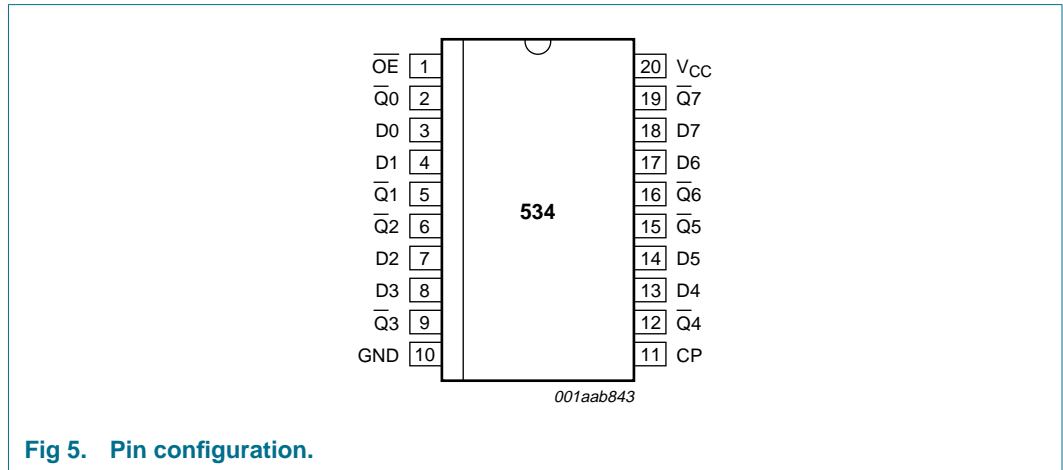


Fig 4. Logic diagram.

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
$\overline{Q0}$	2	3-state output
D0	3	data input
D1	4	data input
$\overline{Q1}$	5	3-state output
$\overline{Q2}$	6	3-state output
D2	7	data input
D3	8	data input
$\overline{Q3}$	9	3-state output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
$\overline{Q4}$	12	3-state output
D4	13	data input
D5	14	data input
$\overline{Q5}$	15	3-state output
$\overline{Q6}$	16	3-state output
D6	17	data input
D7	18	data input
$\overline{Q7}$	19	3-state output
V <sub>CC</sub>	20	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Internal flip-flops	Output $\bar{Q}_n$
	$\overline{OE}$	CP	Dn		
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	±20	mA
$I_O$	output source or sink current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±35	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±70	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation				
	DIP20 package		[1] -	750	mW
	SO20 package		[2] -	500	mW

[1] Above 70 °C:  $P_{tot}$  derates linearly with 12 mW/K.

[2] Above 70 °C:  $P_{tot}$  derates linearly with 8 mW/K.

## 9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V

Table 6: Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_O$	output voltage		0	-	$V_{CC}$	V
$t_r, t_f$	input rise and fall times	$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
$T_{amb}$	ambient temperature	see <a href="#">Section 10</a> and <a href="#">11</a>	-40	-	+125	°C

## 10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$				
		$I_O = -20\text{ }\mu\text{A}$	4.4	4.5	-	V
		$I_O = -6\text{ mA}$	3.98	4.32	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$				
		$I_O = 20\text{ }\mu\text{A}$	-	0	0.1	V
		$I_O = 6.0\text{ mA}$	-	0.16	0.26	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{OZ}$	3-state OFF current	$V_I = V_{IH}$ or $V_{IL}$ ; other inputs $V_{CC}$ or GND; $V_O = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	-	$\pm 0.5$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$ ; $V_{CC} = 5.5\text{ V}$	-	-	8.0	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1\text{ V}$ ; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; $I_O = 0\text{ A}$				
		pin $\overline{OE}$	-	125	450	$\mu\text{A}$
		pin CP	-	90	325	$\mu\text{A}$
		pins Dn	-	35	125	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$				
		$I_O = -20\text{ }\mu\text{A}$	4.4	-	-	V
		$I_O = -6\text{ mA}$	3.84	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$				
		$I_O = 20\text{ }\mu\text{A}$	-	-	0.1	V
		$I_O = 6.0\text{ mA}$	-	-	0.33	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OZ}$	3-state OFF current	$V_I = V_{IH}$ or $V_{IL}$ ; other inputs $V_{CC}$ or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	$\pm 5$	$\mu A$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	$\mu A$
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pin $\overline{OE}$	-	-	560	$\mu A$
		pin CP	-	-	405	$\mu A$
		pins Dn	-	-	155	$\mu A$
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = -20$ $\mu A$	4.4	-	-	V
		$I_O = -6$ mA	3.7	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V				
		$I_O = 20$ $\mu A$	-	-	0.1	V
		$I_O = 6.0$ mA	-	-	0.4	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	$\pm 1.0$	$\mu A$
$I_{OZ}$	3-state OFF current	$V_I = V_{IH}$ or $V_{IL}$ ; other inputs $V_{CC}$ or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	$\pm 10$	$\mu A$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	$\mu A$
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pin $\overline{OE}$	-	-	610	$\mu A$
		pin CP	-	-	440	$\mu A$
		pins Dn	-	-	170	$\mu A$

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**GND = 0 V;  $V_{CC} = 4.5$  V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 9](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25</math> °C</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to $\overline{Qn}$	see <a href="#">Figure 6</a>				
		$C_L = 50$ pF; $V_{CC} = 4.5$ V	-	16	30	ns
		$C_L = 15$ pF; $V_{CC} = 5$ V	-	13	-	
$t_{PZH}$ , $t_{PZL}$	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	16	30	ns

**Table 8: Dynamic characteristics ...continued**  
 GND = 0 V; V<sub>CC</sub> = 4.5 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF; see [Figure 9](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	18	30	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 6</a>	-	5	12	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>	23	14	-	ns
t <sub>su</sub>	set-up time Dn to CP	see <a href="#">Figure 8</a>	12	4	-	ns
t <sub>h</sub>	hold time Dn to CP	see <a href="#">Figure 8</a>	5	-1	-	ns
f <sub>max</sub>	maximum clock pulse frequency	see <a href="#">Figure 6</a>				
		C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 4.5 V	22	36	-	MHz
		C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	-	40	-	MHz
C <sub>PD</sub>	power dissipation capacitance per flip-flop		[1][2]	19	-	pF

#### T<sub>amb</sub> = -40 °C to +85 °C

t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay CP to $\overline{Qn}$	see <a href="#">Figure 6</a>	-	-	38	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	-	38	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	-	38	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 6</a>	-	-	15	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>	29	-	-	ns
t <sub>su</sub>	set-up time Dn to CP	see <a href="#">Figure 8</a>	15	-	-	ns
t <sub>h</sub>	hold time Dn to CP	see <a href="#">Figure 8</a>	5	-	-	ns
f <sub>max</sub>	maximum clock pulse frequency	see <a href="#">Figure 6</a>	18	-	-	MHz

#### T<sub>amb</sub> = -40 °C to +125 °C

t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay CP to $\overline{Qn}$	see <a href="#">Figure 6</a>	-	-	45	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	-	45	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see <a href="#">Figure 7</a>	-	-	45	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 6</a>	-	-	18	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>	35	-	-	ns
t <sub>su</sub>	set-up time Dn to CP	see <a href="#">Figure 8</a>	18	-	-	ns
t <sub>h</sub>	hold time Dn to CP	see <a href="#">Figure 8</a>	5	-	-	ns
f <sub>max</sub>	maximum clock pulse frequency	see <a href="#">Figure 6</a>	15	-	-	MHz

[1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts;

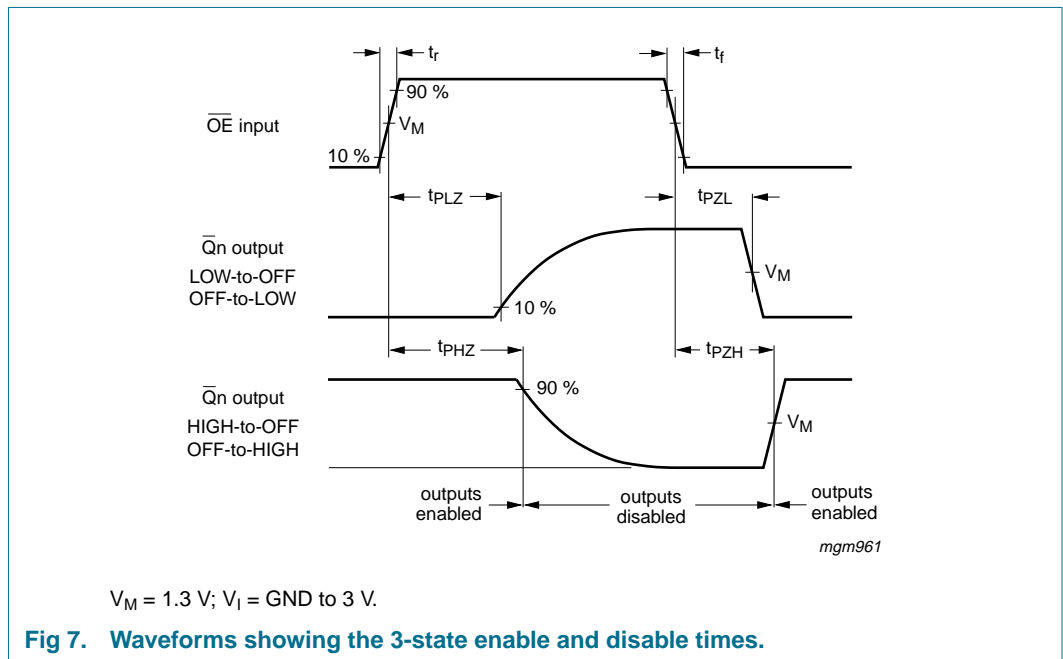
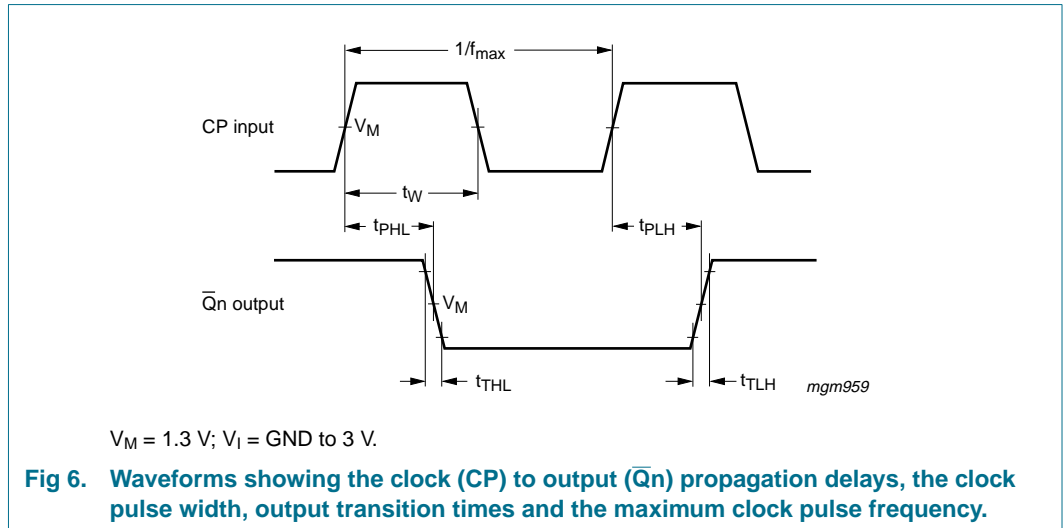
N = number of inputs switching;

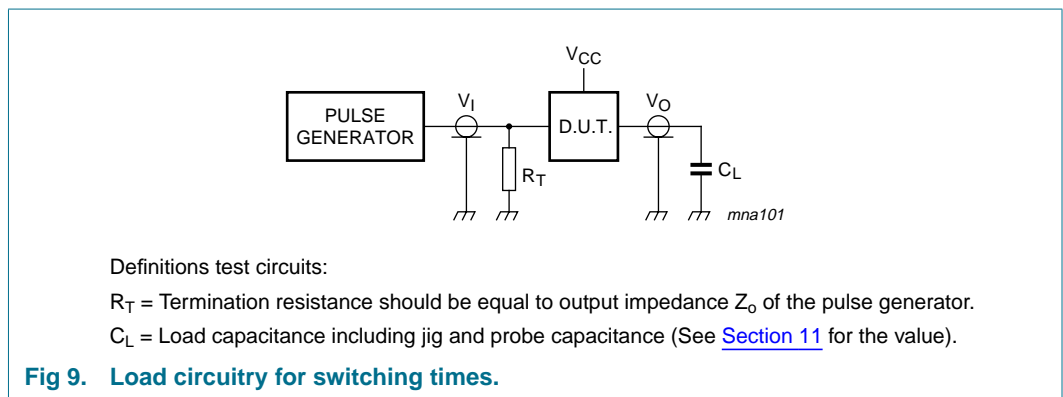
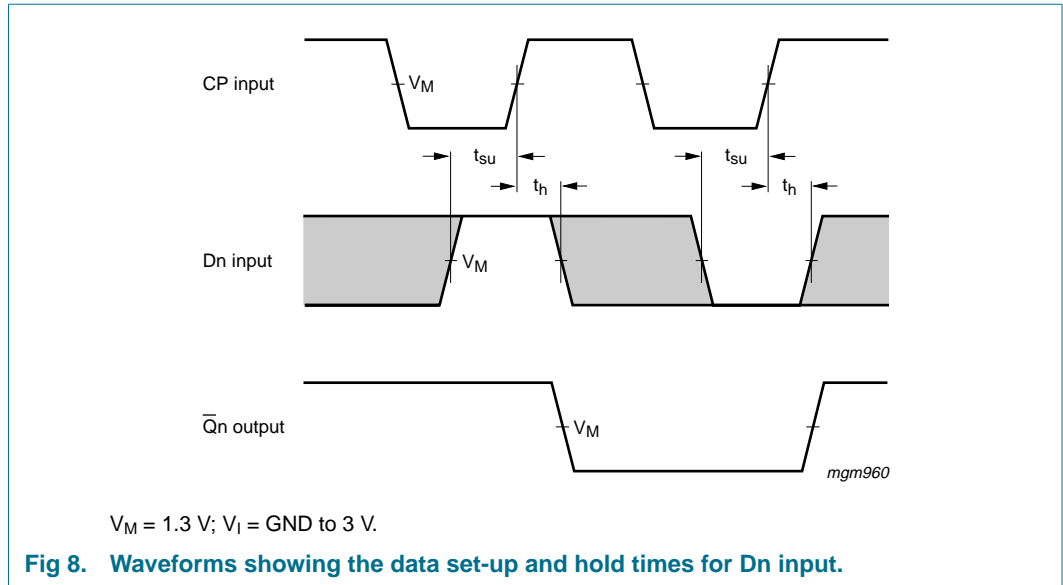
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

[2] The condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V.



12. Waveforms





13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

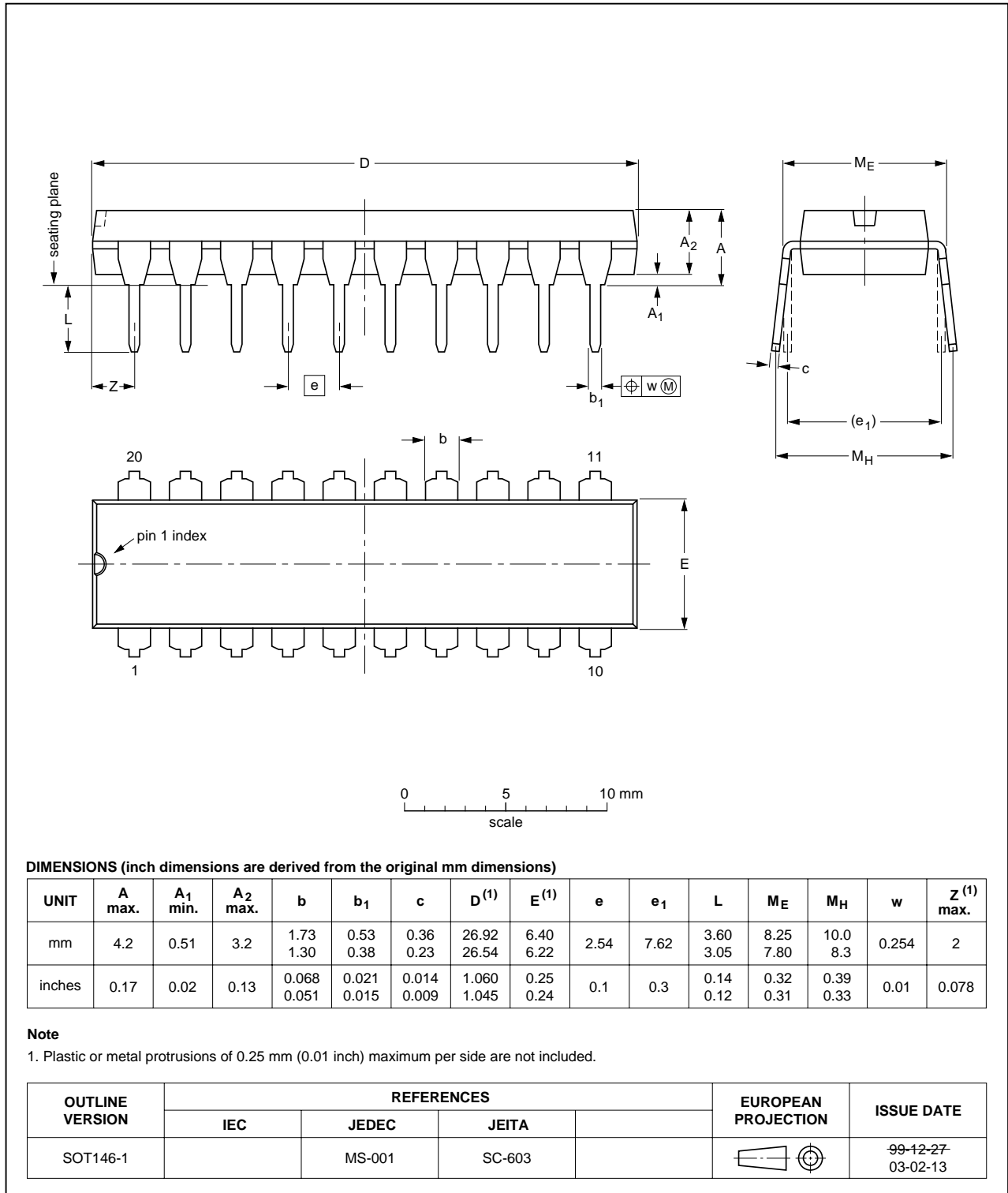


Fig 10. Package outline SOT146 (DIP20).

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

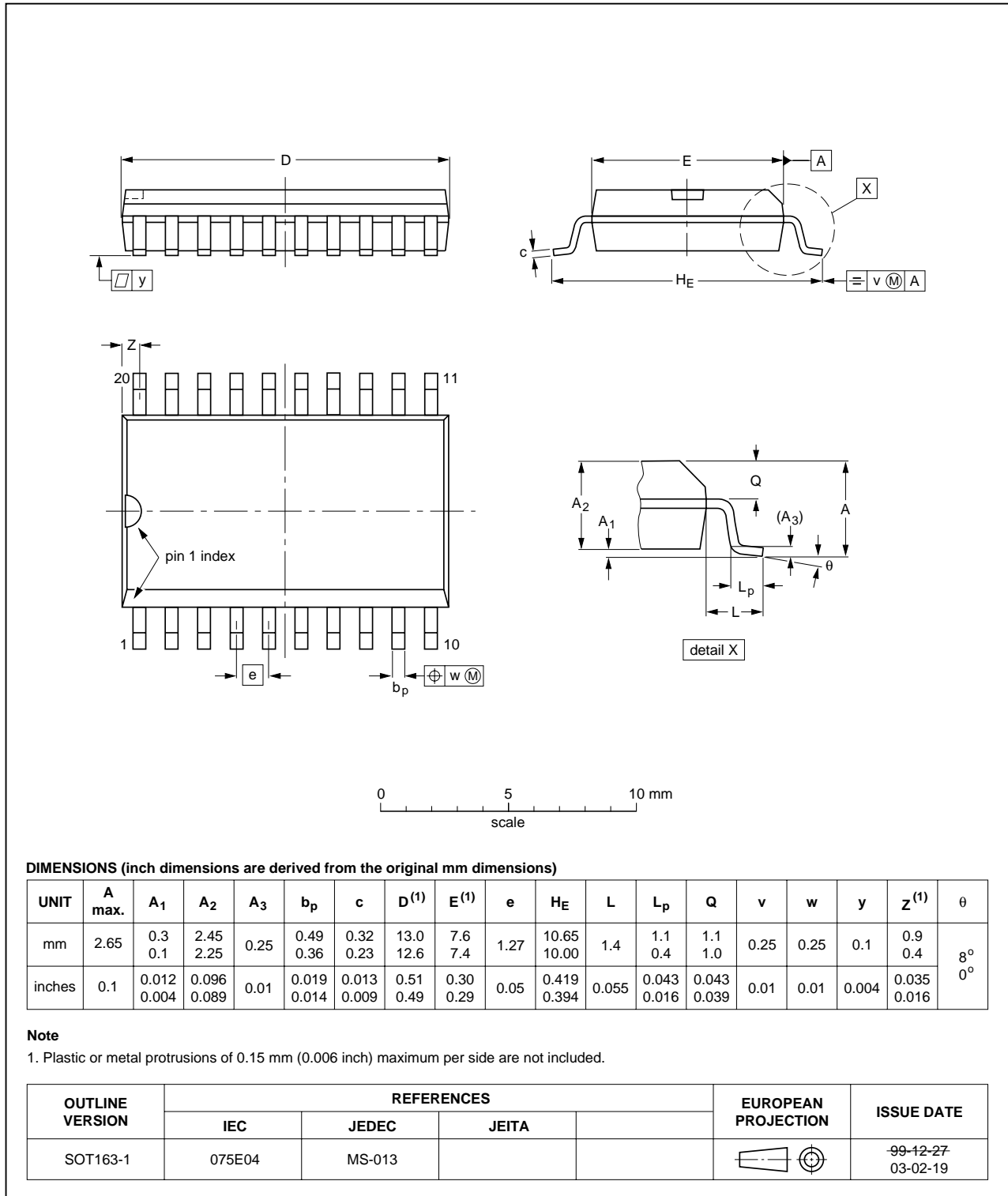


Fig 11. Package outline SOT163 (SO20).

## 14. Revision history

**Table 9: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HCT534_3	20041018	Product data sheet	-	9397 750 13817	74HC_HCT534_CNV_2
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors</li><li>• Information related to 74HC534 type is deleted</li><li>• Reference to family specifications is replaced by the actual information.</li></ul>
74HC_HCT534_CNV_2	19980410	Product specification	-	-	74HC_HCT534_1

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 16. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 17. Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## 18. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

## 19. Contents

1	General description . . . . .	1
2	Features . . . . .	1
3	Quick reference data . . . . .	1
4	Ordering information . . . . .	2
5	Functional diagram . . . . .	2
6	Pinning information . . . . .	4
6.1	Pinning . . . . .	4
6.2	Pin description . . . . .	4
7	Functional description . . . . .	5
7.1	Function table . . . . .	5
8	Limiting values . . . . .	5
9	Recommended operating conditions . . . . .	5
10	Static characteristics . . . . .	6
11	Dynamic characteristics . . . . .	7
12	Waveforms . . . . .	9
13	Package outline . . . . .	11
14	Revision history . . . . .	13
15	Data sheet status . . . . .	14
16	Definitions . . . . .	14
17	Disclaimers . . . . .	14
18	Contact information . . . . .	14



© Koninklijke Philips Electronics N.V. 2004

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 18 October 2004  
Document number: 9397 750 13817

Published in The Netherlands