AN3922NK, AN3922NS

FM Audio Signal Processing Circuit for VTRs

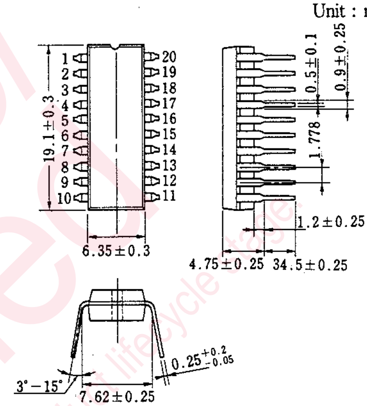
■ Outline

The AN3922NK and The AN3922NS are integrated circuits designed for the FM audio modulation and demodulation for a VTR.

■ Features

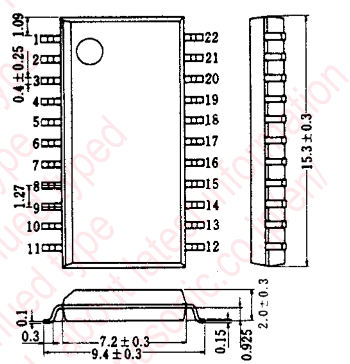
- Built—in switching noise reduction circuit
- Erase oscillation (3MHz) possible
- Supply voltage: 5V

Unit : mm



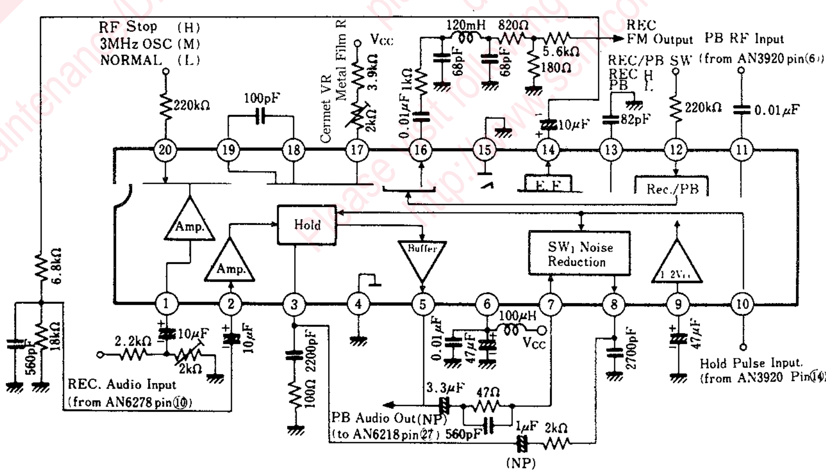
20-Lead Shrunk DIL Plastic Package

Unit : mm



22-Lead PANAFLAT Package (SO-22D)

■ Block Diagram



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■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Audio Signal Input on Rec. Mode	11	RF Signal Input on PB Mode
2	Holc Amp. Input Terminal	12	Rec/PB Control
3	Hold Control	13	FM Demodulation Control
4	GND (Audio)	14	FM Demodulation Output
5	Hold Output Terminal	15	GND (RF)
6	V_{CC}	16	FM Modulation Output
7	Switching Noise Reduction Input Terminal	17	VCO Frequency Adjustment
8	Switching Noise Reduction Output Terminal	18	VCO Capacitance
9	$1/2V_{CC}$	19	VCO Capacitance
10	Hold Pulse Input Terminal	20	VCO Oscillation Control

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6.0	V
Power Dissipation	P_D	200	mW
Operating Ambient Temperature	T_{opr}	−20～+70	℃
Storage Temperature	T_{stg}	−55～+125	℃

■ Electrical Characteristics (Vcc= 5 V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Current on Rec. Mode	$I_{CC\text{-}Rec}$	1		6.7		14.3	mA
Supply Current on PB Mode	$I_{CC\text{-}PB}$	1		12.3		25.6	mA
Rec. Holding Voltage	$V_{12\text{-}Rec}$	2		3.3		5	V
PB Holding Voltage	$V_{12\text{-}PB}$	2		0		1.6	V
VCO Control(1)(FM Modulation)	$V_{20\text{-}L}$	3		0		0.8	V
VCO Control(2) (Insert Oscillation)	$V_{20\text{-}C}$	3		1.8		3.1	V
VCO Free Run Frequency	$V_{20\text{-}H}$	3		4.3		5	V
Output Amplitude on Rec.Mode	f_{OSC}	4		1.1		1.7	MHz
VCO Control(2) (Insert Oscillation)	V_{16}	4		0.32		0.49	V_{P-P}
VCO Insert Oscillation Frequency	f_{INS}	4		2.6		3.4	MHz
VCO Control Sensitivity	β	4		0.8		1.2	MHz
VCO Frequency Shift(+)	$f_{DEV(+)}$	5	$\Delta V_1=+0.113V$	35		65	kHz
VCO Frequency Shift(−)	$f_{DEV(-)}$	5	$\Delta V_1=-0.113V$	35		65	kHz
FM Demodulation Output Amplitude	V_{14}	6	$f_C=1.4MHz$, $V_C=70mV_{P-P}$ $f_m=1kHz$, $DEV=\pm50kHz$ 6dB down of the Pin output	38		65	kHz
FM Demodulation Distortion Rate	THD_{14}	6	$f_C=1.4MHz$, $V_C=70mV_{P-P}$ $f_m=1kHz$, $DEV=\pm50kHz$		0.15	0.3	%
Hold Control Voltage (ON)	$V_{10\text{-}H}$	7		3.09		5	V
Hold Control Voltage (OFF)	$V_{10\text{-}L}$	7		0		1.5	V
Hold Amplifier Output Amplitude	V_5	8	Pin ② Input 1kHz Sine Wave	430		580	mV_{P-P}

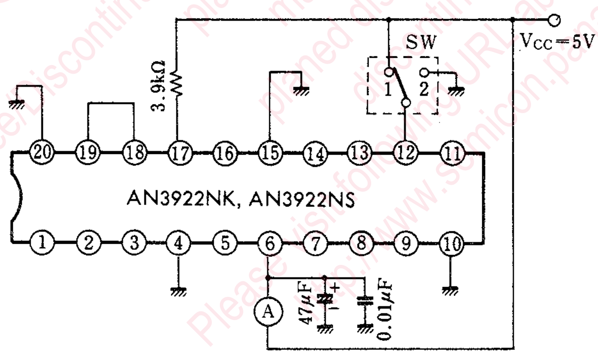
■ Electrical Characteristics (Vcc=5V, Ta=25℃) (Con'd)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Hold Amplifier Distortion	THD_5	8	Pin ② Input 1kHz Sine Wave 50mV_{P-P}		0.05	0.3	%
Differentiating Circuit Output Oscillation	V_8	9	Pin ② Input 10kHz Sine Wave 50mV_{P-P}	650		1150	mV_{P-P}
Hold Amplifier Maximum Output	$v_{5max.}$	10		2			V
Supply Current on Rec. Mode	I_{CC-REC}*	1			10		mA
Supply Current on PB Mode	I_{CC-PB}*	1			19		mA
VCO Free Run Frequency	f_{OSC}*	4			1.4		MHz
Output Amplitude on Rec. Mode	v_{16}*	4			0.4		V_{P-P}
VCO Insert Oscillation Frequency	f_{INS}*	4			3		MHz
VCO Control Sensitivity	β*	4			1		MHz
VCO Frequency Shift(+)	$f_{DEV(+)}$*	5	$\Delta V_1=+0.113V$		50		kHz
VCO Frequency Shift(−)	$f_{DEV(-)}$*	5	$\Delta V_1=-0.113V$		50		kHz
FM Demodulation Output Amplitude	v_{14}*	6	f_C=1.4MHz, V_C=70mV_{P-P} f_m=1kHz, DEV=±50kHz Measure 6dB down of the Pin output		50		mV_{P-P}
Hold Amplifier Output Amplitude	v_5*	8	Pin ② Input 1kHz Sine Wave 50mV_{P-P}		500		mV_{P-P}
Differentiating Circuit Output Oscillation	v_8*	9	Pin ② Input 10kHz Sine Wave 50mV_{P-P}		900		mV_{P-P}
FM Demodulation Output S/N	$S/N_{(D)}$*	6	f_C=1.4MHz, V_C=70mV_{P-P} f_m=1kHz, Dev.=±50kHz	45	55		dB
Hold Amplifier Output S/N	$S/N_{(H)}$*	8	Pin ② Input 1kHz Sine Wave 50mV_{P-P}	55	65		dB

Note) Range of the Operating Supply Voltage : $V_{CC(opr)}$=4.5 to 5.5V

* These are reference values for designing and not a guaranteed ones.

Test Circuit 1 (I_{CC-Rec}, I_{CC-PB})



Symbol	SW
I_{CC-Rec}	1 (V_{CC})
I_{CC-PB}	2 (GND)

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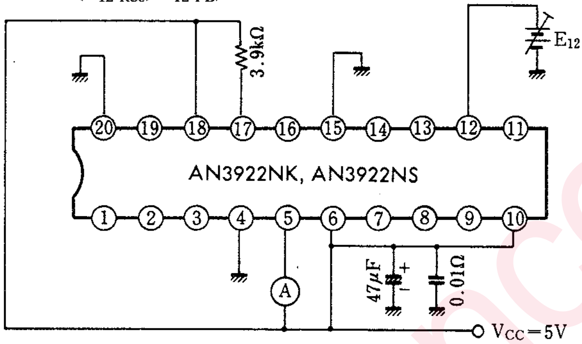
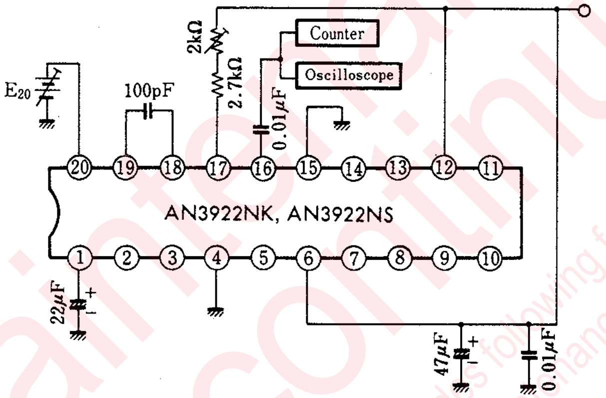
Test Circuit 2 ($V_{12\text{-Rec}}$, $V_{12\text{-PB}}$)



- V_{12-PB}
The voltage range in which ammeter values are over 250μA by increasing E_{12} from 0V.
- V_{12-REC}
The voltage range in which ammeter values are 250μA or less by increasing E_{12} still further.

Test Circuit 3 ($V_{20\text{-L}}$, $V_{20\text{-C}}$, $V_{20\text{-H}}$)

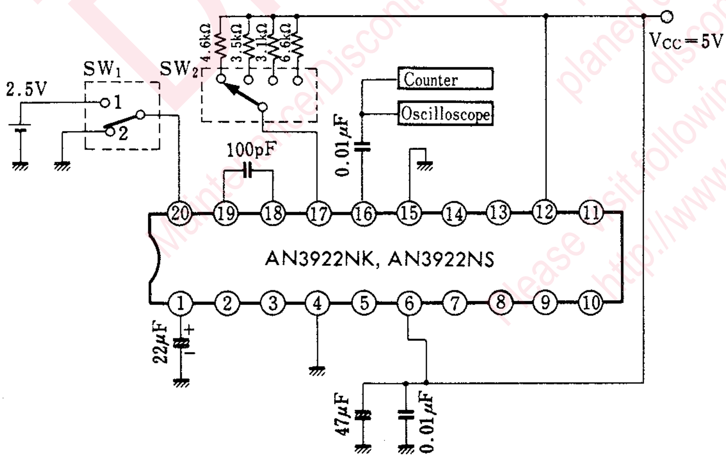


Note) The capacitance between Pin⑱ and Pin⑲ must be that of NPO and the percentage of errors must be within ±0.2%. A metal film resistance and a cermet volume must be used for the Pin⑰ resistance.

Let E_{20}=0V. resistor= 2 kΩ and f_0=1.8 MHz.

- V_{20-L}
The voltage range in which the circuit is oscillating when f is 1.8MHz by increasing E_{20} from 0V.
- V_{20-C}
The voltage range in which the circuit is oscillating when f is 3MHz±200KHz by increasing E_{20} still further.
- V_{20-H}
The voltage range in which oscillation waveforms are not output by increasing E_{20} still further.

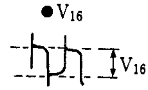
Test Circuit 4 (V_{16}, f_{OSC}, f_{INS}, β)



Note) The capacitance between Pin⑱ and Pin⑲ must be that of NPO and the percentage of errors must be within ±0.2%. A metal film resistance must be used for the Pin⑰ resistance and the percentage of errors must be within ±0.2%.

Item \ Condition	SW1	SW2
f_{OSC}	2	1 (4.6K)
V_{16}	2	1 (4.6K)
f_{INS}	1	2 (3.5K)
β	2	3 (3.1K) 4 (6.6K)

- V_{16}



- β
The difference between the Pin⑯ output frequency in the case where the Pin⑰ resistor is 3.1kΩ and that in the case where the resistor is 6.6kΩ.
$\beta = f_{16}(6.6\,k\Omega) - f_{16}(3.1\,k\Omega)$

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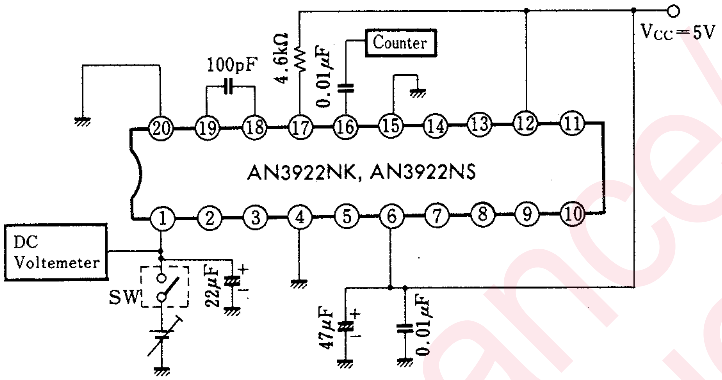
Test Circuit 5 ($f_{DEV(+)}$, $f_{DEV(-)}$)



• $f_{DEV(+)}$

After measuring the Pin① voltage V_1 and the Pin⑯ output frequency f_0 when the Pin① SW is OFF, measure the Pin⑯ output frequency $f_{(+113)}$ by applying(V_1+0.113V) to Pin①.

$f_{DEV(+)}$ is defined as follows.

$f_{DEV(+)}=f_{(+113)}-f_0$

• $f_{DEV(-)}$

Measure the Pin⑯ output $f_{(-113)}$ by applying (V_1−0.113V) to Pin① in the same way as in $f_{DEV(+)}$.

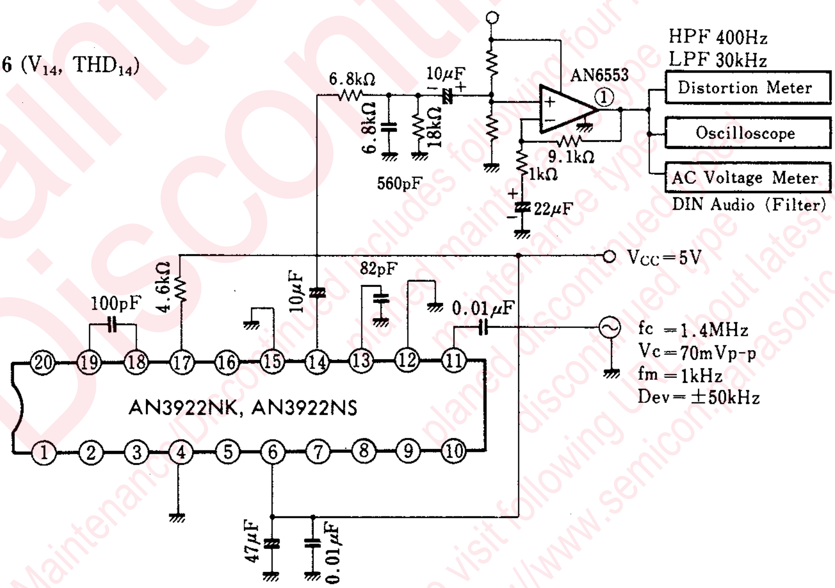
$f_{DEV(-)}$ is defined as follows.

$f_{DEV(-)}=f_0-f_{(-113)}$

Note) The capacitance between Pin⑱ and Pin⑲ must be that of NPO and the percentage of errors must be within ±0.2%.

A metal film resistance must be used for the Pin⑰ resistance and the percentage of errors must be within ±0.2%.

Test Circuit 6 (V_{14}, THD_{14})



• V_{14}

Amplification is performed ten times as much with the OP-amp. in the above figure, V_{14} is one-tenth of the OP-amp. output.

Note) The capacitance between Pin⑱ and Pin⑲ must be that of NPO and the percentage of errors must be within±0.2%.

A metal film resistance must be used for the Pin⑰ resistance and the percentage of errors must be within±0.2%.

The percentage of the precision of other external parts must be within±0.2%.

• S/N_D

The ratio of the AC voltage at point A in the case where an FM modulated wave is input to Pin⑪ to that in the case where only a carrier is input to Pin⑪ in the above figure.

• THD_{14}

Range of the harmonic: Measure from the second to the tenth harmonics

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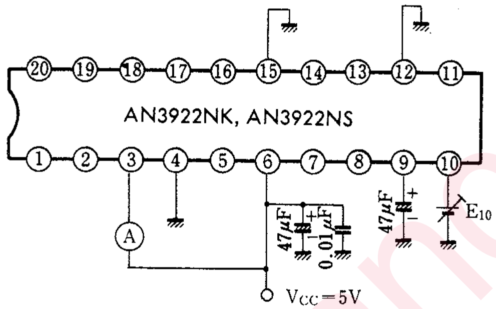
Test Circuit 7 ($V_{10\text{-}H}$, $V_{10\text{-}L}$)



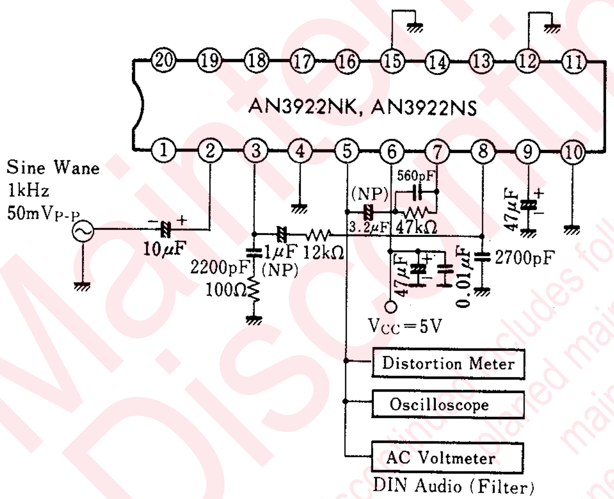
- V_{10-L}

The Pin⑩ voltage range in which Pin③ ammeter values are 200 μA or over by increasing E_{10} from 0V.

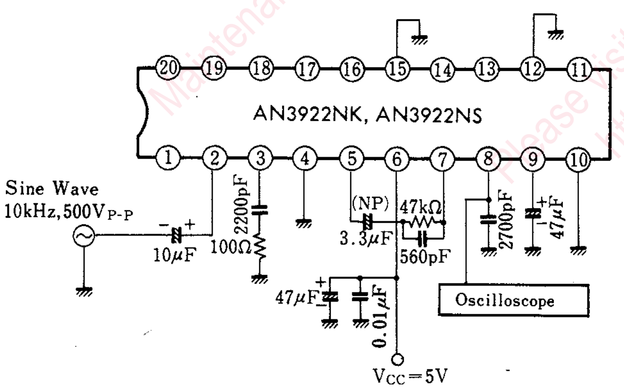
- V_{10-H}

The Pin⑩ voltage range in which Pin③ ammeter values are 200 μA or less by increasing E_{10} still further.

Test Circuit 8 (V_5, THD_5)



Test Circuit 9 (V_8)



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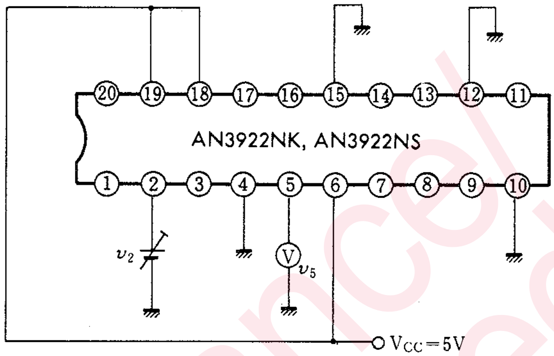
Test Circuit 10 ($v_{5max.}$)



● V_{5max}

• Measure the Pin⑤ output voltage V_5 (V_2=1V) in the case where (V_2=1V) is applied and the Pin⑤ output voltage V_5 (V_2=4V) in the case where(V_2=4V) is applied, and find the difference between them

$V_{5max}=V_5(V_2=4V)-V_5(V_2=1V)$

Waveforms of Pins

Pin No.	Function	DC 電圧 (V)	Waveform	Impedance (Ω)	Pin No.	Function	DC Voltage (V)	Waveform	Impedance (Ω)
①	AUDIO IN	2.5	−22dBV	10k	⑪	PB RF iN I	3.2	70mVP.P	6k
②	HOLD IN	3.2	50mVP.P	10k	⑫	REC/PB CONT	5V/0V	—	H
③	HOLD	2.5	Hold Interval −15dBV	—	⑬	EM DEMOD	3.2		10k
④	GND (AUDIO)	0	—	—	⑭	FM DEMOD OUT	2.5		E.F.
⑤	HOLD OUT	2.5	−15dBV	E.F.	⑮	GND (RF)	0	—	—
⑥	V_{CC}	5.0	—	—	⑯	FM OUT	—	400mVP.P	E.F.
⑦	SW NOISE REDUCTION IN	2.5	−15dBV	47k	⑰	VCO fo ADJ	3.85	—	—
⑧	SW NOISE REDUCTION OUT	2.5	—	—	⑱	VCO	—		—
⑨	$\frac{1}{2}V_{CC}$	2.55	—	—	⑲	VCO	—		—
⑩	HOLD PULSE IN	—	0V	H	⑳	VCO CONT	5V 2.5V 0V	RF STOP 3MHz OSC. Normal	H

Note) The above values are standard ones and fluctuate depending on the use conditions and the unevenness of an integrated circuit (V_{cc} is 5V)

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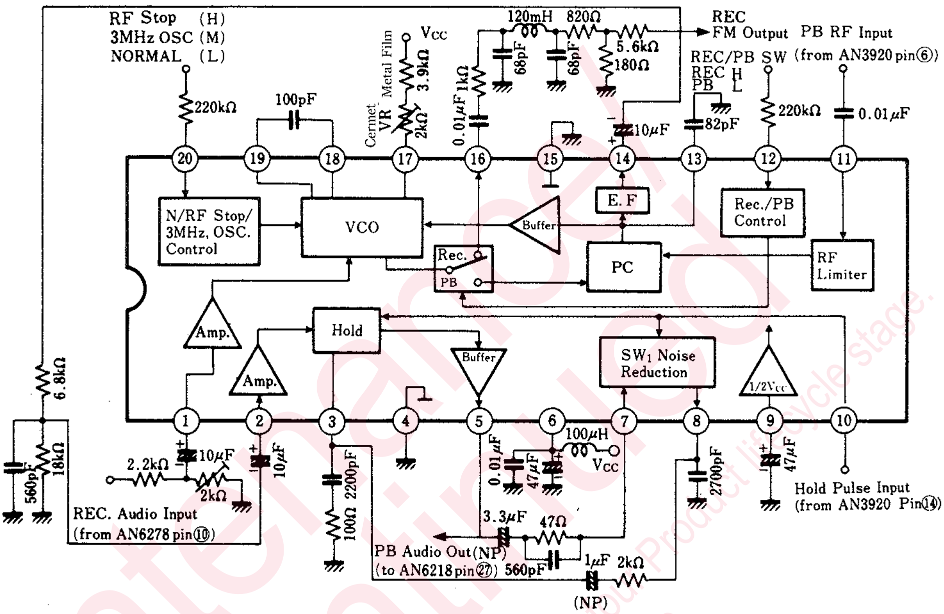
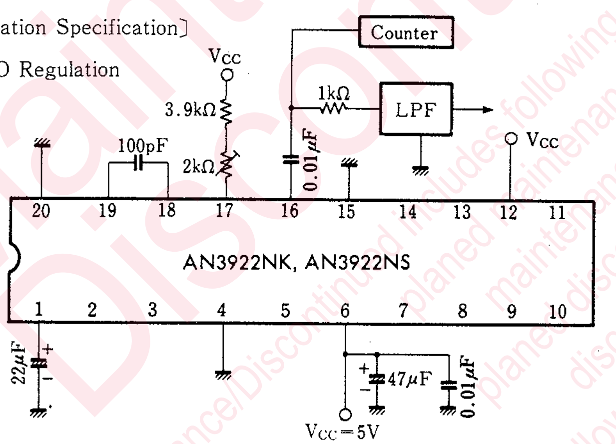
■ Application Circuit



〔Regulation Specification〕

(1)VCO Regulation



- Pin⑫: In the REC. mode (3V to 5V)
- Pin⑳: In the Normal mode (0V to 1V)

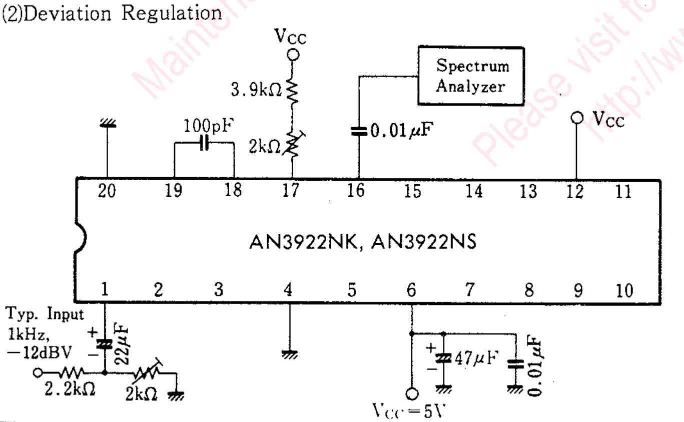
Note 1) Use the Pin⑰ external fixed resistances with the following characteristics

※Pin ⑰ External Fixed Resistance

	R-ch		L-ch	
	Frequency	Resistance	Frequency	Resistance
NTSC	1.7MHz	2700Ω	1.3MHz	3900Ω
PAL	1.8MHz	2700Ω	1.4MHz	3900Ω

Note 2) The Pin⑰ variable resistance must be regulated so that the Pin⑯ frequency will be within ±5KHz of the foregoing frequencies.

(2)Deviation Regulation



Regulate the Pin① input variable resistance so that the FM modulation deviation of the Pin⑯ output will be ±50±2kHz by the standard input (1kHz, −12dBV).
(The Pin① input is a standard value of −22dBV.)

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[Instructions before Use]

(1) Parts

- The capacitance between Pin⑱ and Pin⑲ must be that of NPO in order to diminish the temperature change of the carrier frequency of the FM modulation. In addition, a metal film resistance and a cermet volume must be used for the Pin⑰ external resistance and the variable resistance respectively.
- The low precision of the capacitance between Pin⑱ and Pin⑲ causes fluctuations of the frequency of the 3MHz fixed OSC (ex. PAL: 1.8MHz→3MHz NTSC: 1.7MHz→2.9MHz) and the decline of S/N will result.

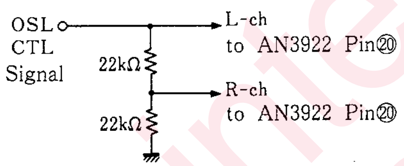
(2) Power supply

- In the case where voltage or a current is applied to each control pin of the signal processing unit with a microcomputer, etc. without applying supply voltage to this integrated circuit when the power supply is OFF, attach protective resistances to Pin⑫ and Pin⑳.

[Operating Instructions]

(1) VCO control

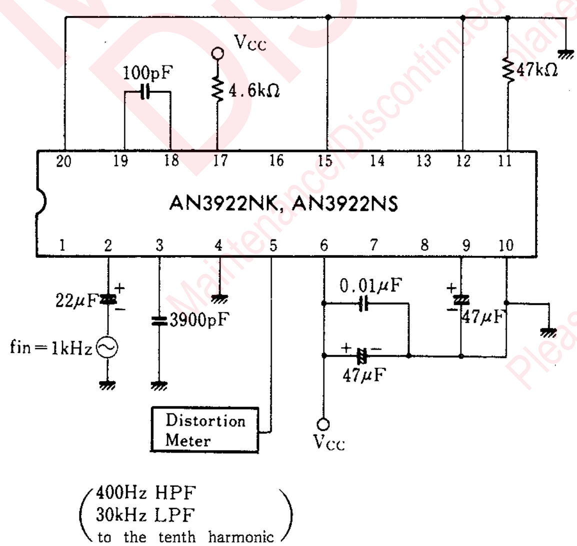
The audio Head is temporarily used for the erase and the recording is performed without the FM modulation in performing the insert on the REC. mode. For this purpose, the oscillation of NTSC(1.3MHz) and PAL(1.4MHz) of the L−ch. is halted and NTSC(1.7MHz) and PAL(1.8MHz) of the R−ch. are regulated so that they will be close to 3MHz(NTSC: 2.9MHz, PAL: 3MHz).



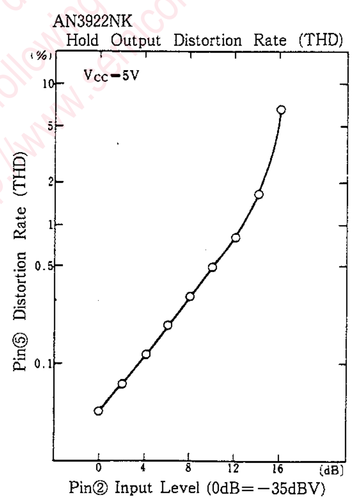
(2) SW Noise Reduction

The differentiation just before the Hold Pulse period is performed to the output for the improvement of the S/N ratio by inputting the Pin⑤ output to the differentiating circuit Pin⑦ in which the high frequency gain is increased and by the feedback from Pin⑧ to Pin③.

(3) Hold Output Distortion Rate



The Hold output distortion rate measured in the measuring circuit in the left figure is shown graphically below. The below graph shows the standard characteristic and the values fluctuate depending on the use conditions and the unevenness of an integrated circuit.



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