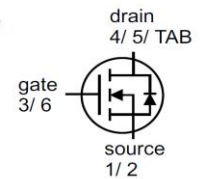


**OptiMOS™ Power-MOSFET**
**Features**

- Optimized for high performance Buck converter
- Monolithic integrated Schottky like diode
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	1.2	mΩ
$I_D$	50	A
$Q_{OSS}$	33	nC
$Q_G(0V..10V)$	56	nC

**LG-USON-6-1**


Type	Package	Marking
BSN012N03LSI	LG-USON-6-1	012N03LI

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	50	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	50	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	50	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$	36	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	50	
Avalanche energy, single pulse	$E_{AS}$	$I_D=50\text{ A}, R_{GS}=25\text{ Ω}$	145	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	78	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=50\text{ K/W}^2$	2.5	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	-	1.6	K/W
		top	-	-	1	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=1\text{ mA}$	30	-	-	V
Breakdown voltage temperature coefficient	$\frac{dV_{(\text{BR})\text{DSS}}}{dT_j}$	$I_{\text{D}}=10\text{ mA}$ , referenced to 25 °C	-	15	-	mV/K
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	V
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=20\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	-	0.5	mA
		$V_{\text{DS}}=20\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	3	-	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}$ , $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$ , $I_{\text{D}}=30\text{ A}$	-	1.3	1.6	mΩ
		$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=30\text{ A}$	-	1.0	1.2	
Gate resistance	$R_{\text{G}}$		0.3	0.5	1.0	Ω
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=30\text{ A}$	80	160	-	S

<sup>3)</sup> See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=12\text{ V}, f=1\text{ MHz}$	-	3600	4800	pF
Output capacitance	$C_{oss}$		-	1600	2200	
Reverse transfer capacitance	$C_{rss}$		-	220	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=12\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	3.9	-	ns
Rise time	$t_r$		-	7.8	-	
Turn-off delay time	$t_{d(off)}$		-	27	-	
Fall time	$t_f$		-	5.2	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=12\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	8.6	11	nC
Gate charge at threshold	$Q_{g(th)}$		-	5.7	-	
Gate to drain charge	$Q_{gd}$		-	8.2	11	
Switching charge	$Q_{sw}$		-	11	-	
Gate charge total	$Q_g$		-	28	37	
Gate plateau voltage	$V_{plateau}$		-	2.4	-	V
Gate charge total	$Q_g$	$V_{DD}=12\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	56	74	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }4.5\text{ V}$	-	23	-	
Output charge	$Q_{oss}$	$V_{DD}=12\text{ V}, V_{GS}=0\text{ V}$	-	33	44	

**Reverse Diode**

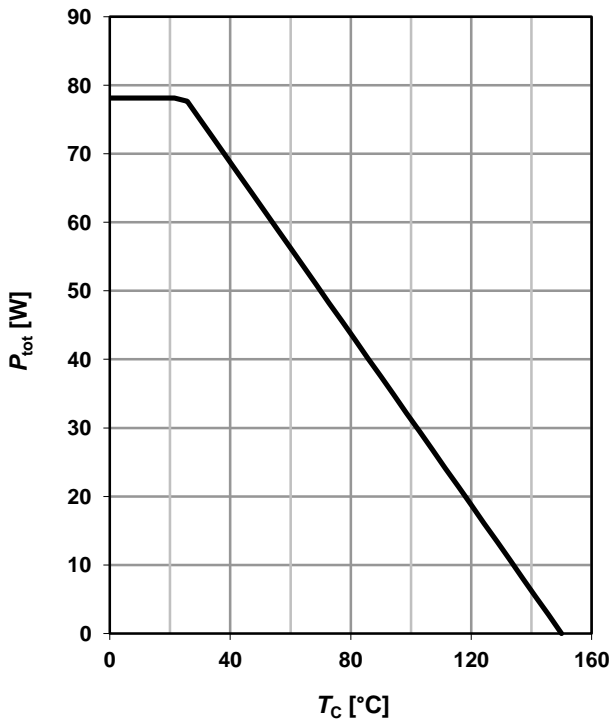
Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	96	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=12\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.58	-	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=12\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$	-	5	-	nC

<sup>4)</sup> See figure 13 for more detailed information

<sup>5)</sup> See figure 16 for gate charge parameter definition

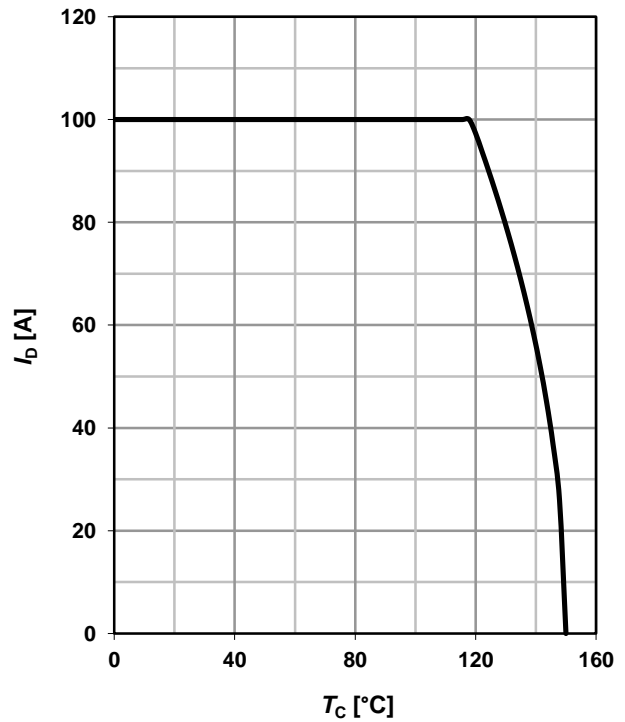
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

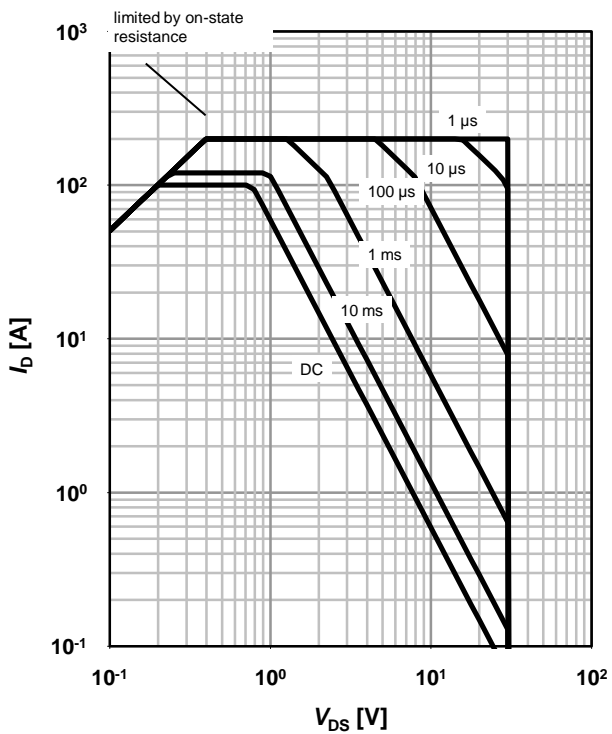
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

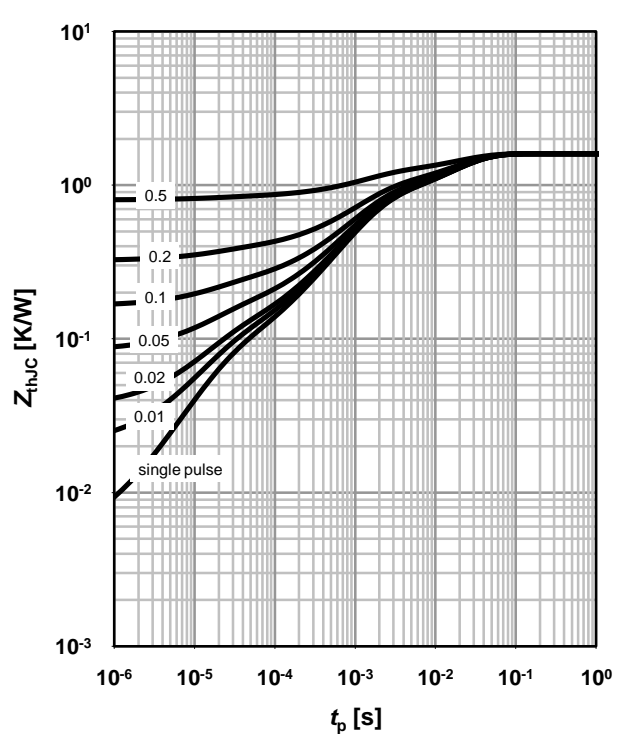
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

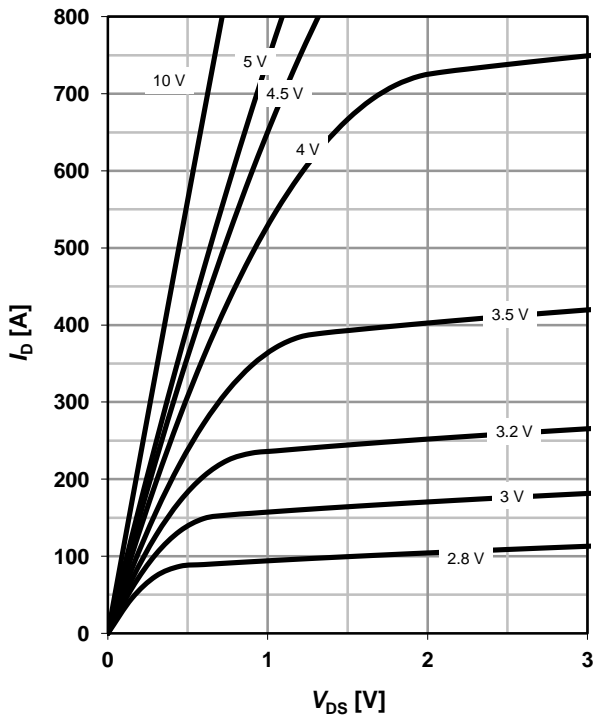
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

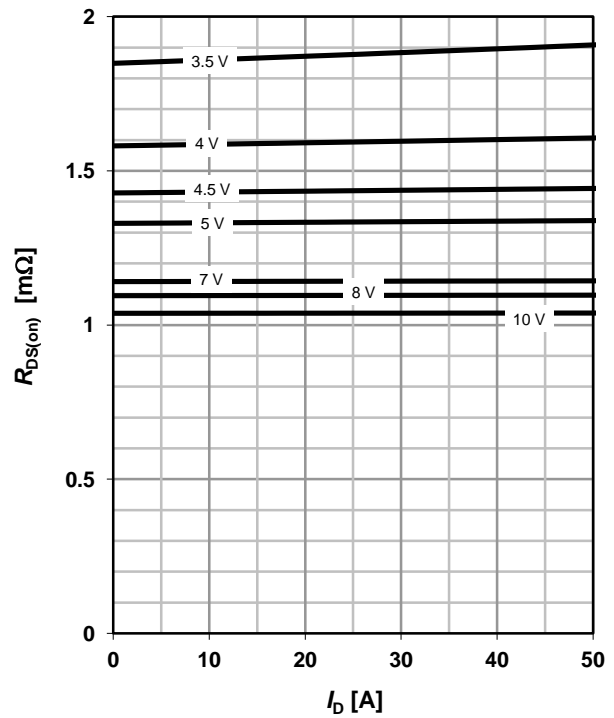
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

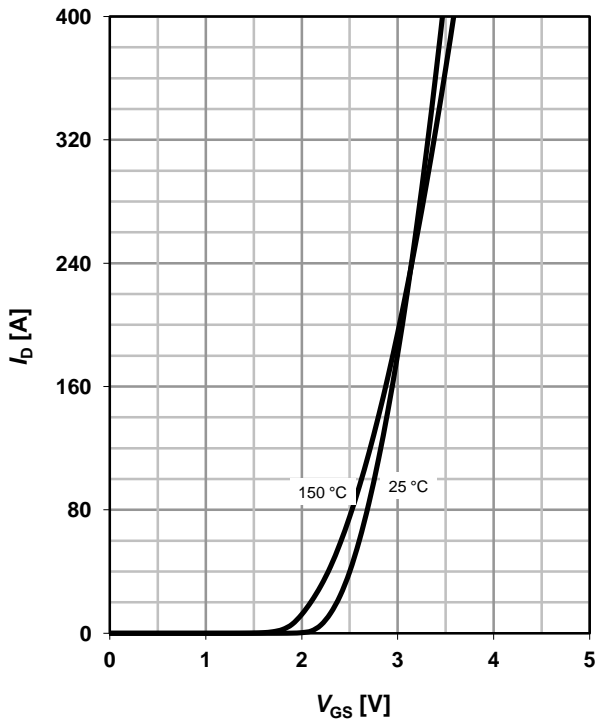
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

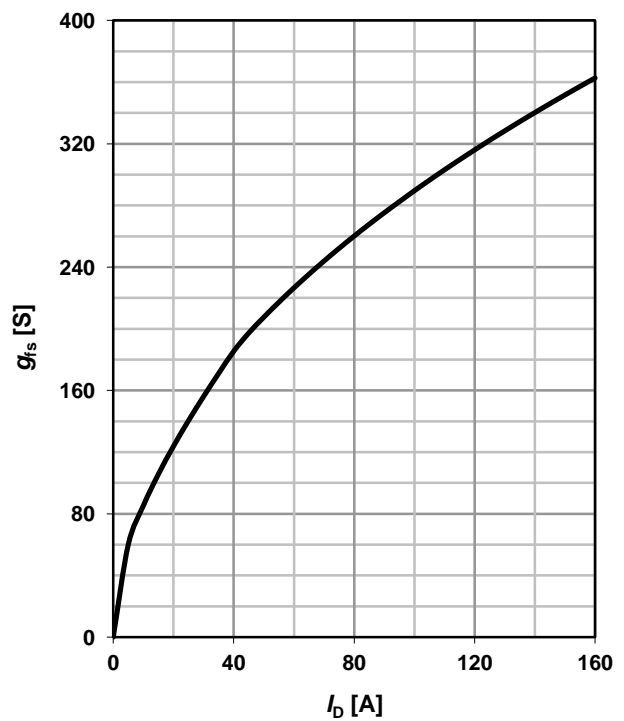
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$

parameter:  $T_j$



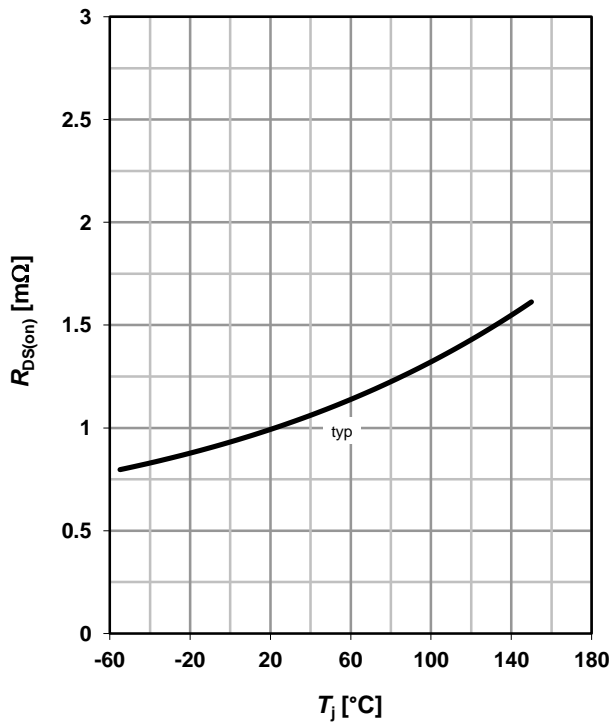
**8 Typ. forward transconductance**

$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$



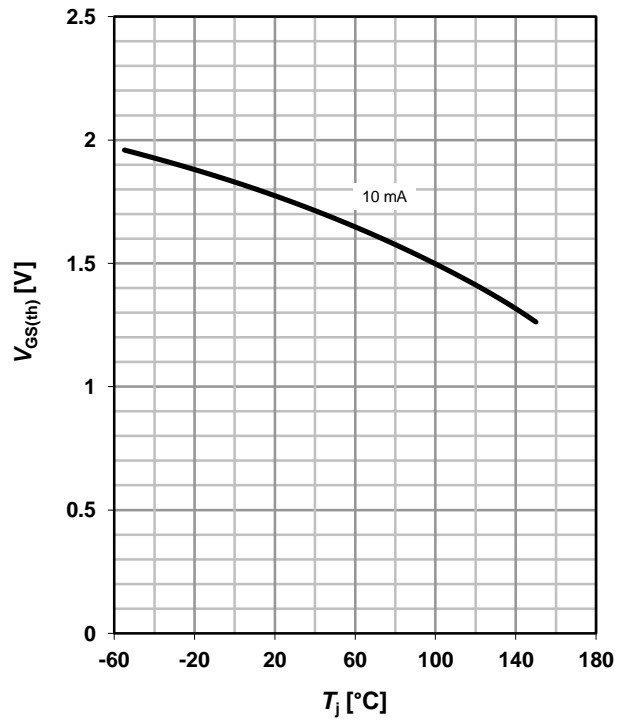
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$



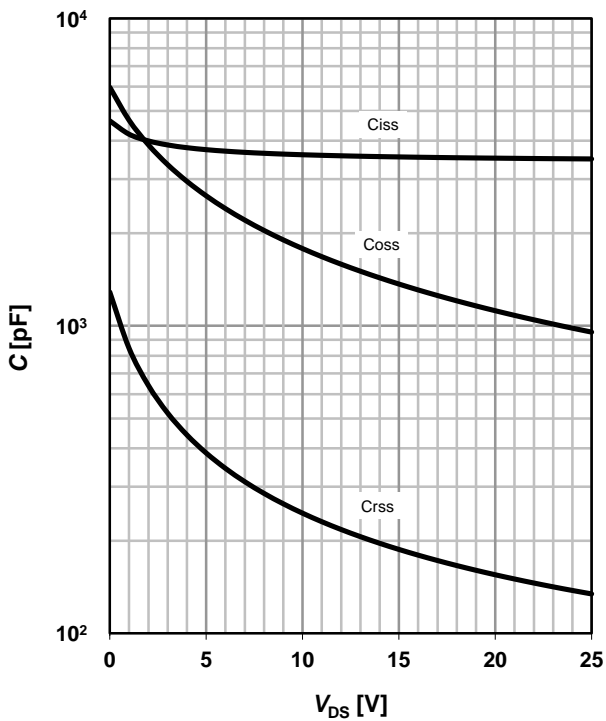
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$



**11 Typ. capacitances**

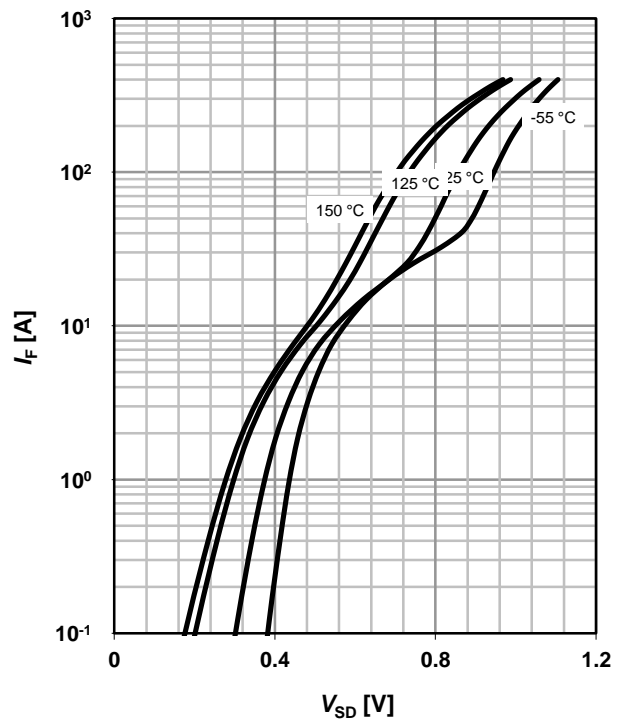
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

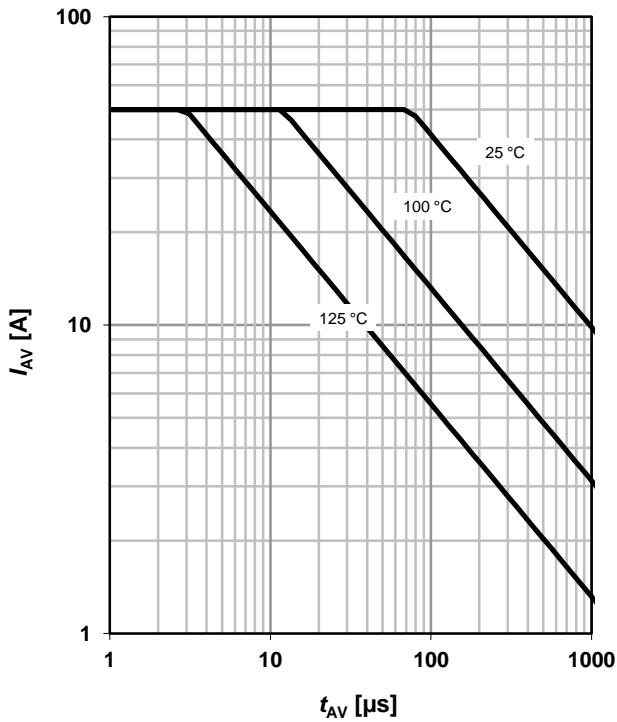
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

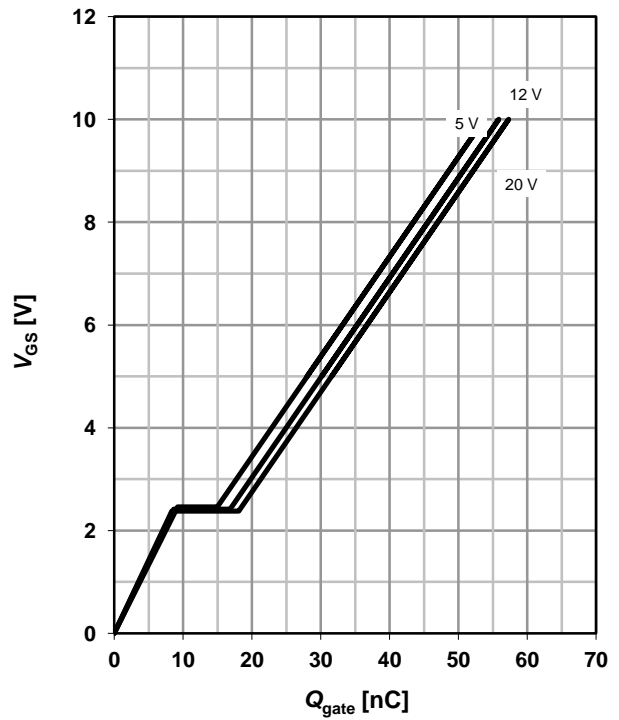
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$

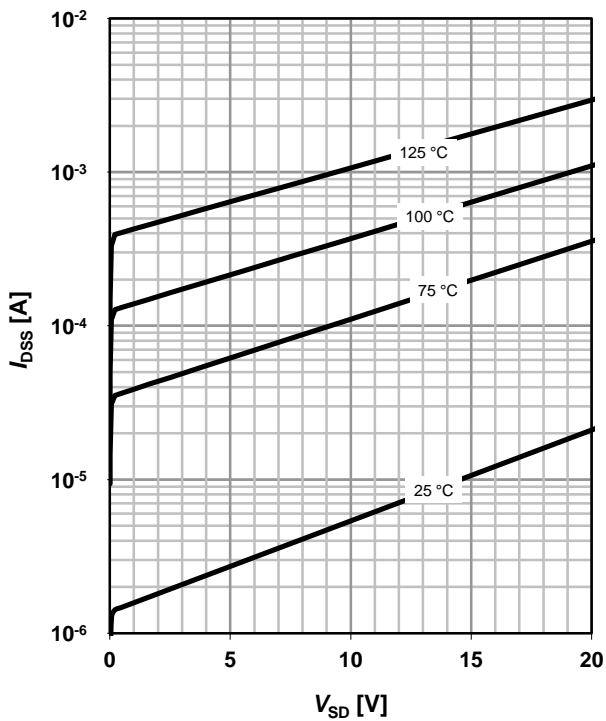
parameter:  $V_{DD}$



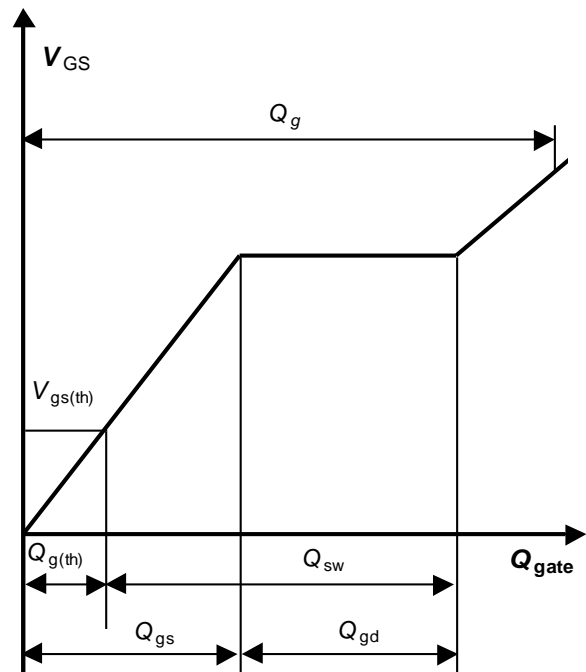
**15 Typ. drain-source leakage current**

$I_{DSS}=f(V_{DS}); V_{GS}=0 \text{ V}$

parameter:  $T_j$



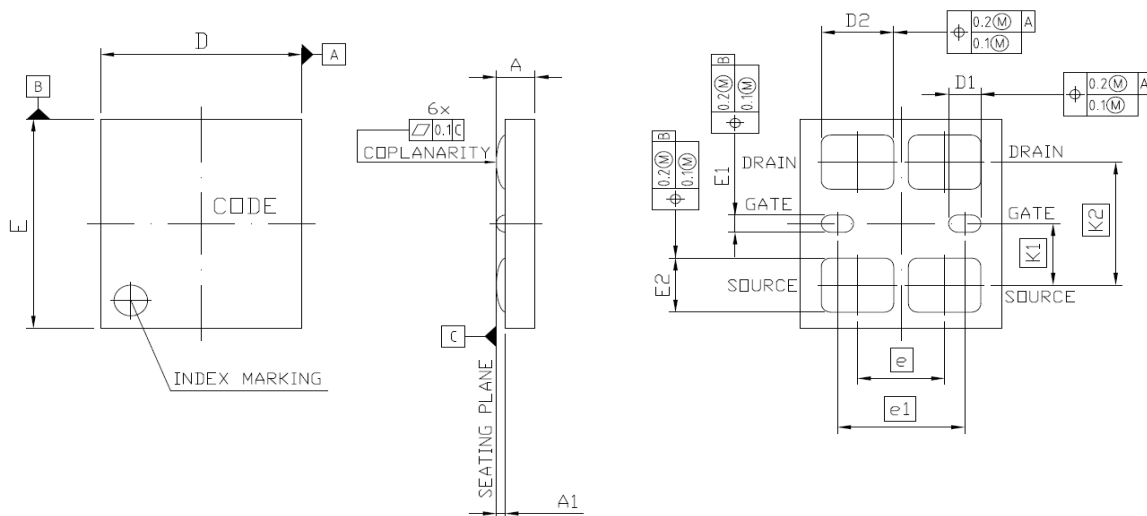
**16 Gate charge waveforms**



Package Outline

LG-USON-6-1

LG-USON-6-1: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	0.65	-	0.026
A1	0.08	-	0.003	-
D	2.90	3.10	0.114	0.122
D1	0.38	0.58	0.015	0.023
D2	0.98	1.18	0.039	0.046
e	1.30		0.051	
e1	1.90		0.075	
E	3.30	3.50	0.130	0.138
E1	0.18	0.38	0.007	0.015
E2	0.78	0.98	0.031	0.039
K1	1.00		0.039	
K2	2.00		0.079	

**DOCUMENT NO.**  
Z8B00170449

**SCALE**

**EUROPEAN PROJECTION**

**ISSUE DATE**  
03.09.2013

**REVISION**  
01



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**  
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