**Philips Components–Signetics**

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# NE502A
## Ethernet encoder/decoder

### DESCRIPTION

The NE502A is an Ethernet™ encoder/decoder designed to meet all the requirements of the IEEE 802.3 and Ethernet/Thin Ethernet specification and fabricated with high-speed ECL and Schottky TTL technology.

The encoder converts serial binary data into complementary Manchester code. The decoder converts Manchester code into binary data and synchronous clock signals. The decoding method is a digital phase locked loop with dual bandwidth which allows both fast lock-on and low jitter. Typical acquisition is eight bits or better. A key feature of the decoder design is its capability to recover distorted input signals. The NE502A is packaged in a standard 24-pin ceramic DIP.

The NE502A is normally part of a 3-chip set that implements a complete Ethernet/Thin Ethernet interface for a DTE. The other chips are an Ethernet Data Link Controller (EDLC) such as the NE86950 and a coaxial transceiver interface (CTI) such as the NE8392A.

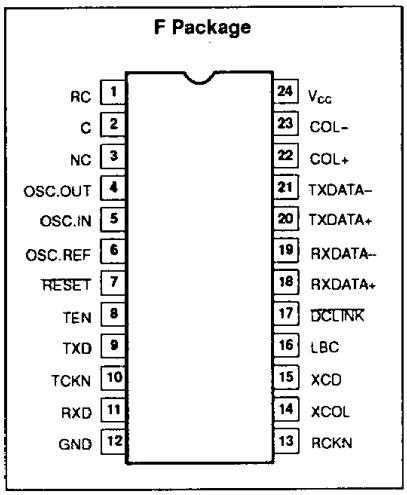
### FEATURES

- Full Ethernet II, IEEE 802.3 10base5 and 10base2 compatibility
- Manchester encode and decode
- Level conversion: transceiver level to/from TTL level
- Carrier detection
- Large distortion recovery: ±20ns
- Dual bandwidth phase locked loop: allows fast acquisition
- Loopback "CONFIDENCE" test feature
- Built-in clock generator
- Small external parts count:
- High-speed ECL and Schottky TTL technology
- Single power supply: +5V
- Low power dissipation: 750mW typ.
- 24-pin standard dual in-line ceramic package

### APPLICATION

- Workstations
- Terminals
- File servers
- Print servers

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 24-Pin Ceramic DIP | 0°C to 70°C | NE502AF |

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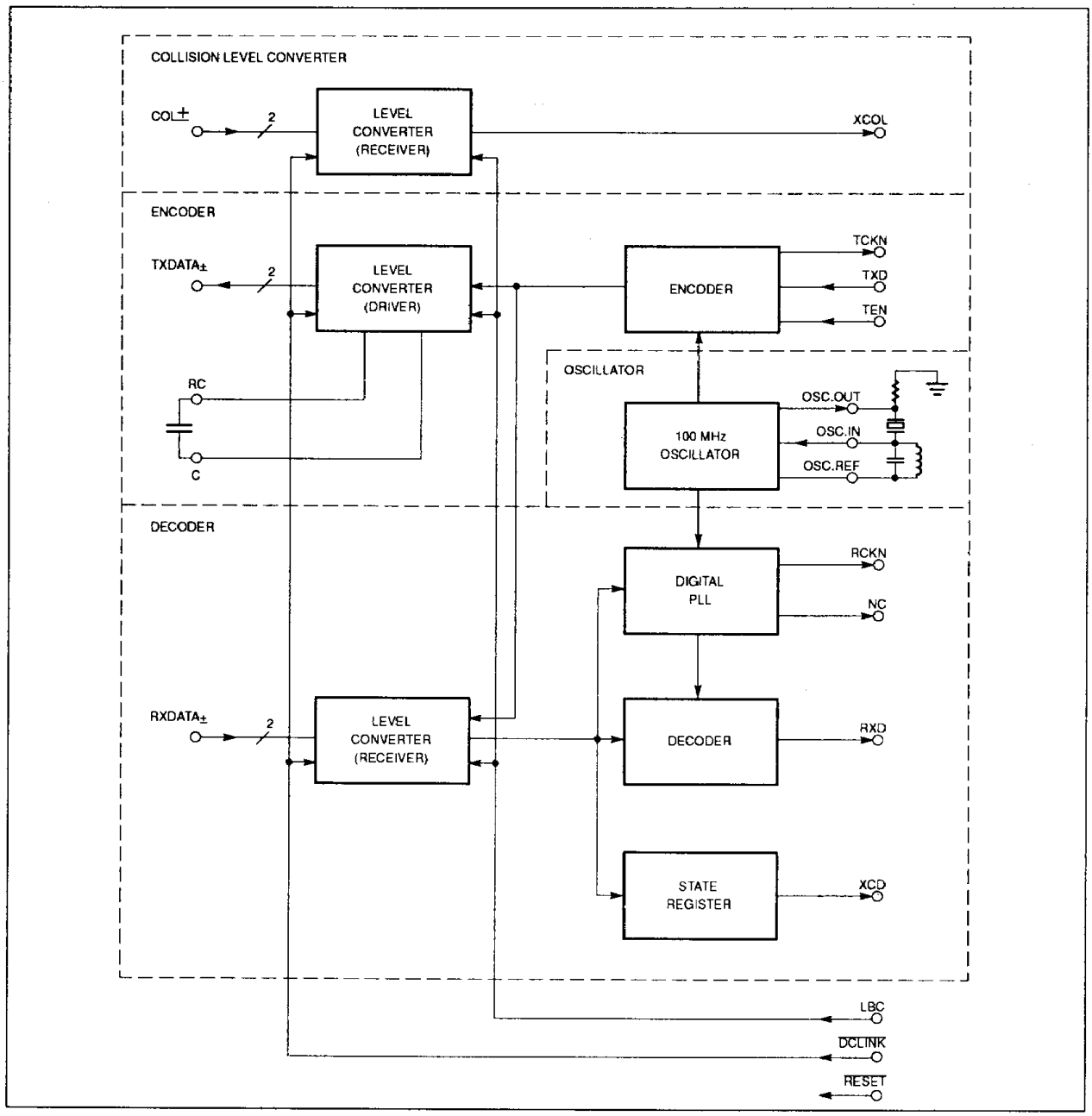
# Ethernet encoder/decoder | NE502A

## BLOCK DIAGRAM



## PIN ASSIGNMENT TABLE

| PIN NO. | SYMBOL | PIN NAME | I/O | LEVEL | FUNCTION |
|---|---|---|---|---|---|
| **Power Group** | | | | | |
| 12 | GND | Power supply | I | — | Ground |
| 24 | $V_{CC}$ | Power supply | I | — | +5V DC power Supply |
| **Cable Group** | | | | | |
| 18<br>19 | RXDATA+<br>RXDATA– | Receive data pair | I<br>I | ECL differential | Interfacing to receive pair of the transceiver. |
| 20<br>21 | TXDATA+<br>TXDATA– | Transmit data pair | O<br>O | ECL differential | Interfacing to transmit pair of the transceiver. |
| 22<br>23 | COL+<br>COL– | Collision presence pair | I<br>I | ECL differential | Interfacing to collision presence pair of the transceiver. |
| **EDLC Group** | | | | | |
| 8 | TEN | Transmit encode enable | I | TTL | Input for encoding and TXDATA± enable. |
| 9 | TXD | Transmit serial data | I | TTL | Input for transmit data to be encoded onto the Ethernet coax. |
| 10 | TCKN | Transmit data clock | O | TTL | Stable 10MHz clock output for transmit bit stream. |
| 11 | RXD | Receive serial data | O | TTL | Output of received and decoded bit stream. |
| 13 | RCKN | Receive data clock | O | TTL | Clock output to strobe RXD. |
| 14 | XCOL | Collision presence | O | TTL | Duplication of the collision presence pair (COL±). |
| 15 | XCD | Receive carrier detect | O | TTL | Carrier detect function of the decoder. |
| 16 | LBC | Loopback command | I | TTL | Input to command the NE502A to operate in loopback mode. |
| **Oscillator Group** | | | | | |
| 4<br>5<br>6 | OSC. OUT<br>OSC. IN<br>OSC. REF | Oscillator pins | O<br>I<br>O | ECL | Pins for direct connection of discrete oscillator components. |
| **Others** | | | | | |
| 1<br>2 | RC<br>C | Capacitor pins | —<br>— | ECL<br>— | Pins for direct connection of a capacitor. |
| 3 | NC | Non-connection (PLL test) | O | ECL | Output pin for PLL testing purpose only. |
| 7 | RESET | FF test | I | TTL | Input pin to initialize flip-flops for testing purpose only. |
| 17 | DCLINK | DC/AC coupling select for transceiver pairs | I | TTL | Input to select DC/AC coupling of transceiver cable pairs. |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 to 7.0 | V |
| $V_{ITTL}$ | TTL Level Input Voltage | –0.3 to 7.0 | V |
| $V_{IR}$ | Receiver Input Voltage | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_{ODV}$ | Driver Output Voltage | $V_{CC}$ (max) | V |
| $I_{ODV}$ | Driver Output Current | –40.0 to 0 | mA |
| $V_{IOSC}$ | Oscillator Input Voltage | $V_{CC}$–4 to $V_{CC}$ and < –0.3 | V |
| $I_{OOSC}$ | Oscillator Output Current | –20.0 to 0 | mA |
| $T_{OP}$ | Operating Temperature | –25 to 100 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 125 | °C |

**NOTE:**
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 5.0V ± 5% | 0°C to +70°C |
| $I_{OH}$ | TTL High Level Output Current | | –0.4mA to 0mA | |
| $I_{OL}$ | TTL Low Level Output Current | | 0mA to 8mA | |
| $V_{IR}$ | Receiver Input Voltage | | 0V to $V_{CC}$ | |
| $R_{LD}$ | Driver Terminator | | 270Ω | |
| $R_{DLD}$ | Differential Load | | 78Ω | |
| $R_{LOSC}$ | Oscillator Terminator | | 330Ω and 33pF parallel[1] | |
| $f_{XTAL}$ | Crystal for Oscillator | | 100MHz ± 0.01%[2] | |
| $C_{TX}$ | Capacitor placed between C and RC pins | | 470pF | |
| $L_{OSC}$ | LC Tank Constant | Inductance | 0.15μH | |
| $C_{OSC}$ | | Capacitance | 33pF[1] | |

**NOTES:**
1. The values of the oscillator capacitors may have to be tuned for a particular components layout. Both capacitors should be adjusted for maximum voltage at OSC.IN. However, once the correct values are determined for that layout, any more tuning will not be necessary for each board.
2. 5th overtone series resonant.

## DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| SYMBOL | PARAMETER | CONDITION | $V_{CC}$ (V) | VALUE | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IH}$ | High level input voltage[1] | | | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage[1] | | | | | 0.8 | V |
| $V_{IC}$ | Input clamp voltage[1] | $I_{IL}$ = –18mA | 4.75 | –1.5 | | | V |
| $V_{OH}$ | High level output voltage[2] | $I_{OH}$ = –0.4mA | 4.75 | 2.7 | | | V |
| $V_{OL}$ | Low level output voltage[2] | $I_{OL}$ = 8mA | 4.75 | | | 0.5 | V |
| $I_{IH}$ | High level input current[1] | $V_{IH}$ = 2.7V | 5.25 | | | 20 | µA |
| $I_{IL}$ | Low level input current[1] | $V_{IL}$ = 0.4V | 5.25 | –100 | | | µA |
| $I_{OS}$ | Output short current[2] | $V_O$ = 0V | 5.25 | –100 | | –20 | mA |
| $V_{IHD}$ | High level differential input voltage[3] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V | | 0.2 | | | V |
| $V_{ILD}$ | Low level differential input voltage[3] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V | | | | –0.2 | V |
| $V_{IHD}$ | High level differential input voltage[4] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V | | –0.05 | | | V |
| $V_{ILD}$ | Low level differential input voltage[4] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V | | | | –0.4 | V |
| $V_{IHD}$ | High level differential input voltage[5] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V | | 0.2 | | | V |
| $V_{ILD}$ | Low level differential input voltage[5] | $V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V | | | | –0.2 | V |
| $I_{IHR}$ | High level input current[3] | $V_{IR}$ = 5.25V, $\overline{DCLINK}$ = 0V | 5.25 | | | 0.7 | mA |
| $I_{ILR}$ | Low level input current[3] | $V_{IR}$ = 0V, $\overline{DCLINK}$ = 0V | 5.25 | –1.5 | | | mA |
| $V_{OHTX}$ | High level output voltage[6] | | 5.0 | | 4.1 | | V |
| $V_{OLTX}$ | Low level output voltage[6] | | 5.0 | | 3.3 | | V |
| $V_{OHD}$ | High level differential output voltage[6] | $V_{O+} - V_{O-}$, $\overline{DCLINK}$ = 0V | | 0.55 | | 1.0 | |
| $V_{OLD}$ | Low level differential output voltage[6] | $V_{O+} - V_{O-}$, $\overline{DCLINK}$ = 0V | | –1.0 | | –0.55 | |
| $V_{BB}$ | Oscillator reference voltage[7] | | 5.0 | | 3.7 | | V |
| $I_{IHO}$ | High level input current[8] | $V_{IH}$ = 4.1V | 5.0 | | | 150 | µA |
| $V_{OHO}$ | High level output voltage[9] | OSC.IN is open | 5.0 | | 4.15 | | V |
| $V_{OLO}$ | Low level output voltage[9] | $V_{IOSC}$ = 4.1V | 5.0 | | 3.3 | | V |
| $R_{RC}$ | RC internal resistor | $V_{RC}$ = 0.5V | 0.5 | 25 | 50 | 100 | kΩ |
| $I_{CC}$ | Power supply current | All signal pins are open. | 5.25 | | | 220 | mA |

NOTES:
1. Applicable to TTL input pins. (TEN, TXD, LBC, $\overline{DCLINK}$ and $\overline{RESET}$)
2. Applicable to TTL output pins. (TCKN, RXD, RCKN, XCOL and XCD)
3. Applicable to COL± and RXDATA±.
4. Applicable to RXDATA± while XCD output is low (idle state) and COL±.
5. Applicable to RXDATA± while XCD output is high.
6. Applicable to TXDATA±. These pins are connected to ground through 270Ω resistors. A 78Ω resistor is placed between these pins.
7. Applicable to OSC.REF.
8. Applicable to OSC.IN.
9. Applicable to OSC.OUT. This pin is connected to ground through a 330Ω resistor.

**AC CHARACTERISTICS** Recommended operating conditions unless otherwise noted. $V_{CC}$ = 5.0V. Transmit Timing (Figure 22)

| SYMBOL | PARAMETER | CONDITION | VALUE | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Transmit timing (Figure 1)** | | | | | | |
| $t_{CTTC}$ | TCKN cycle time | (Figures 2,3) | 99.99 | 100.00 | 100.01 | ns |
| $t_{WLTC}$ | TCKN low time | (Figures 2,3) | 40 | 50 | | ns |
| $t_{WHTC}$ | TCKN high time | (Figures 2,3) | 40 | 50 | | ns |
| $t_{PDTX}$ | TXDATA± encode time | (Figures 2,3) | | 95 | | ns |
| $t_{RTX}$ | TXDATA± output rise time | (Figures 5,6) | | 2.0 | | ns |
| $t_{FTX}$ | TADATA± output fall time | (Figures 5,6) | | 2.0 | | ns |
| $t_{LTX}$ | TXDATA– low level hold time | $C_{TX}$ = 470pF $\overline{DCLINK}$ = $V_{CC}$ (Figures 5,6) | | 3 | | µs |
| $t_{RLTX}$ | TXDATA– idling rise time | $C_{TX}$ = 470pF, (20% ~ 80%), $\overline{DCLINK}$ = $V_{CC}$ (Figures 5,6) | | 0.8 | | µs |
| $t_{SUTX}$ | TXD, TEN setup time | (Figures 4) | 20 | | | ns |
| $t_{HDTX}$ | TXD, TEN hold time | (Figures 4) | 0 | | | ns |
| **Receive timing (Figures 2, 3)** | | | | | | |
| $t_{CTRC}$ | RCKN cycle time in idle | (Figures 2,3) | 99.99 | 100.00 | 100.01 | ns |
| $t_{WLRC}$ | RCKN low time | (Figures 2,3) | 35 | 50 | | ns |
| $t_{WHRC}$ | RCKN high time | (Figures 2,3) | 35 | 50 | | ns |
| $t_{PHLRC}$ | RCKN delay time | (Figures 2,3,7) | | 120 | | ns |
| $t_{PLHCD}$ | XCD ON delay time | (Figures 2,3,7) | | 80 | 110 | ns |
| $t_{PHLCD}$ | XCD OFF delay time | (Figures 2,3,7) | | 230 | | ns |
| $t_{HDLCD}$ | XCD low hold time | (Figures 2,3) | 0 | 10 | | ns |
| $t_{HDHCD}$ | XCD high hold time | (Figures 2,3) | | 120 | | ns |
| $t_{SULCD}$ | XCD Low setup time | (Figures 2,3) | | 80 | | ns |
| $t_{SURXD}$ | RXD setup time | (Figures 2,3) | 20 | 60 | | ns |
| $t_{HDRXD}$ | RXD hold time | (Figures 2,3) | 10 | 20 | | ns |
| **Loopback timing[1] (Figure 4)** | | | | | | |
| $t_{PGLBC}$ | LBC receiving data purge time | (Figures 2,3,4) | | 230 | | ns |
| $t_{ACLBC}$ | LBC receiving data accept time | (Figures 2,3,4) | | 80 | | ns |
| $t_{PHLTRU}$ | DATA through time | (Figures 2,3,4) | | 280 | | ns |
| $t_{WTEN}$ | TEN wait time | (Figures 2,3,4) | 0 | | | ns |
| **Collision timing (Figure 5)** | | | | | | |
| $t_{PLH}$ | COL to XCOL Propagation Delay Time | $\overline{DCLINK}$ = 0V, (Figures 2,3,7) | | 9 | 30 | ns |
| $t_{PHL}$ | COL to XCOL Propagation Delay Time | $\overline{DCLINK}$ = 0V, (Figures 2,3,7) | | 11 | 30 | ns |

**NOTE:**

1. In Loopback mode operation, $COL_{\pm}$ and $RXDATA_{\pm}$ inputs are ignored, TXDATA+ and XCOL are high level, and XCD, RCKN and RXD functions are in the same manner as a normal receive operation.

# Ethernet encoder/decoder | NE502A

## FUNCTIONAL DESCRIPTION

The NE502A has five major functions: encode, decode, collision signal conversion, master clock generation and loopback.

### Encode

The encoder section of the NE502A is a simple circuit which performs an appropriate exclusive-OR between the transmit clock and transmit data using latches to reduce the skew of TXDATA± outputs. The encoder sends the transmit clock (TCKN) to an Ethernet Data Link controller (EDLC) such as the NE86950. An encode enable signal (TEN) and data (TXD) are then returned from the EDLC.

### Decode

The decoder performs three functions. First, it decodes data arriving at the RXDATA± inputs and passes it to the EDLC via the RXD output. Second, it signals to the EDLC that receive carrier is present by asserting the XCD output. Third, the receive clock is recovered and passed to the EDLC via the RCKN output. The RCKN is inhibited for 6 or 7 cycles during PLL acquisition, but, upon restarting, has the correct phase relationship with the recovered data.

The decoder PLL is a digital phase locked loop with excellent distortion handling capability. It is designed to recover data from ±20ns of jitter.

### Collision

In the event of a collision, the 10MHz collision signal sent from the transceiver to the COL+ inputs is converted to a TTL 10MHz signal at the XCOL pin. The latching and timing functions for this signal are provided in the EDLC (NE86950).

### Master Clock Generation

The oscillator generates a 100MHz master clock for the encoder and decoder.

Discrete oscillator components and a crystal are directly connected to the provided oscillator pins. The oscillation frequency must be 100MHz with a tolerance of less than ±0.01% to meet the IEEE 802.3 specification because one tenth of the oscillation frequency is the transmit bit rate.

### Loopback

A loopback input (LBC) is provided to allow all encoding and decoding functions to be exercised without using the transceiver cable. During loopback operation, the encoded data is routed internally to the decoder, while transmit outputs remain idle and the receive and collision inputs are ignored.

## SIGNAL PIN DESCRIPTION

### Cable Group

**RXDATA±** (receive serial data pair, inputs): These are the inputs to the decoder. They receive Manchester coded signals from the transceiver. The input circuit is a differential receiver and with a common mode voltage range of 0 to $V_{CC}$. The differential receiver has two modes of operation: DC coupled operation and AC coupled operation, which are selected by the $\overline{\text{DCLINK}}$ input.

In DC coupled operation ($\overline{\text{DCLINK}}$ is low), the differential squelch threshold is typically –0V.

In AC coupled operation ($\overline{\text{DCLINK}}$ is high), the differential squelch threshold is typically –0.2V. This is the operating mode for coaxial Ethernet where an isolation transformer is used between the encoder/decoder and the transceiver.

In both DC and AC coupled operation, the differential zero crossing threshold for the received signal is 0V in order to minimize receive distortion. When RXDATA± are idle, the RXD output is a TTL high.

**TXDATA±** (transmit data pair, outputs): These are the outputs of the encoder. They transmit Manchester coded signals to the transceiver.

The driver output circuits are emitter followers and require pull-down resistors of 270Ω. They can drive a transceiver cable with differential impedance of 78Ω.

The differential transmitter outputs TXDATA± are normally connected directly to the primary of an isolating pulse transformer. In idle state they have a low offset voltage in order to minimize DC current through the transformer. When entering the idle state, at the end of a transmit packet, the transmitter outputs gradually return to a differential voltage of 0V across the transformer primary in order to prevent undershoot glitches at the transformer secondary. The returning time constant is determined by an external capacitor connected between the RC and C pins.

**COL±** (collision presence pair, inputs): This pair of inputs receive a 10MHz signal from the transceiver when a collision is detected.

The input circuit has the same common mode voltage range as the RXDATA± inputs. It also operates in DC or AC coupled modes, depending on whether $\overline{\text{DCLINK}}$ is low or high respectively, with the same differential squelch thresholds of 0V or –0.2V, respectively.

Unlike the RXDATA± inputs, the zero crossing threshold is –0.2V even when COL± are receiving a collision present signal.

When COL± are idle, the XCOL output is a TTL high.

### EDLC Group

**TEN** (transmit encode enable, input): This is an input to the on-chip Manchester encoder and enables the TXDATA± pair. An input high enables the TXDATA± pair; an input low makes the TXDATA± pair idle (high).

**TXD** (transmit serial data, input): This is an input to the on-chip Manchester encoder and provides the data to be encoded.

Serial binary data must be supplied to this input synchronously with the falling edge of TCKN (transmit data clock).

This input is enabled when TEN (transmit encode enable) is high.

**TCKN** (transmit data clock, output): A 10MHz clock output for the transmit serial binary data. This is a stable clock of one-tenth of the master clock frequency. See TXD (transmit serial data) description.

**RXD** (receive serial data, output): This is an output of the on-chip Manchester decoder and provides decoded data to the EDLC.

This output is synchronous with the falling edge of RCKN (receive data clock).

**RCKN** (receive data clock, output): Clock output to strobe RXD (receive serial data). See RXD (receive serial data) description.

At the beginning of a packet, RCKN is inhibited for 6 or 7 clock cycles to allow the PLL to gain acquisition. At the end of a packet, RCKN is inhibited for 1 clock cycle.

During idle state, this output generates a 10MHz clock signal.

**XCOL** (collision presence, output): This is a TTL duplication of the collision signal at COL±. The transceiver connected to the Ethernet coax supplies a high level or differential voltage of 0V to COL± when a collision is not present on the coax. It supplies a 10MHz square wave signal to COL± when a collision is detected. Accordingly, XCOL outputs a high level when collision is not see and outputs a 10MHz square wave signal during collision presence.

**XCD** (receive carrier detect, output): This output provides the carrier detect function of the Manchester decoder. This signal is used by the receive section of the Data Link controller as a data acquisition enable signal and by the transmit section as transmission permission information.

Output is low when the Ethernet coax is idle.

**LBC** (loopback command, input): A high level input to this pin dictates loopback mode operation. During the loopback mode operation, XCOL output is a high level, TXDATA± outputs are high level, RXDATA± inputs are ignored. The data supplied to TXD (transmit serial data) when TEN (transmit encode enable) is high is encoded, internally routed back to the Manchester decoder and output from RXD (receive serial data), RCKN (receive data clock) and XCD (receive carrier detect).

## Oscillator Group

**OSC.OUT, OSC.IN,** and **OSC.REF** (oscillator pins): A 100MHz crystal is placed between OSC.IN and OSC.OUT.

An LC tank circuit is placed between OSC.IN and OSC.REF to assure start-up at the proper harmonic of the crystal.

OSC.OUT is an emitter-follower output and requires a pull-down resistor (330Ω typ.). A phase adjusting capacitor is placed in parallel with the pull-down resistor to make the delay through the oscillator close to 10ns to increase the efficiency of the crystal.

As a design recommendation, connection wires should be as short as possible.

## Others

**RC** and **C** (capacitor pins): A capacitor placed between these pins provides the timing for the active-to-idle time of the TXDATA± pair.

In AC coupled operation ($\overline{\text{DCLINK}}$ is high), after data transmission, TXDATA– goes high with rise time determined by the time-constant of the internal resistor and the connected capacitor. When a 470pF capacitor is connected, the rise time of TXDATA– is typically 0.8µs (20% to 80%).

Because pin C is connected to $V_{CC}$ on chip, DC voltage must never be supplied to this pin.

**$\overline{\text{DCLINK}}$** (DC/AC coupling select for transceiver pair): This input is to select DC/AC coupling of the transceiver cable pairs. A low level selects DC coupling; a high level selects AC coupling and makes both TXDATA± high during idle state to prevent the transformer core from saturating. See CABLE GROUP description.

This pin must be connected to a TTL high or low. It may be connected directly to $V_{CC}$ or ground.

**$\overline{\text{RESET}}$** (FF testing purpose only): This input pin is used to initialize flip-flops for testing purposes only and must be connected to $V_{CC}$ or a TTL high level in a normal operation.

**NC** (non-connection): This output pin is for testing purposes only and must be left open in a normal operation.

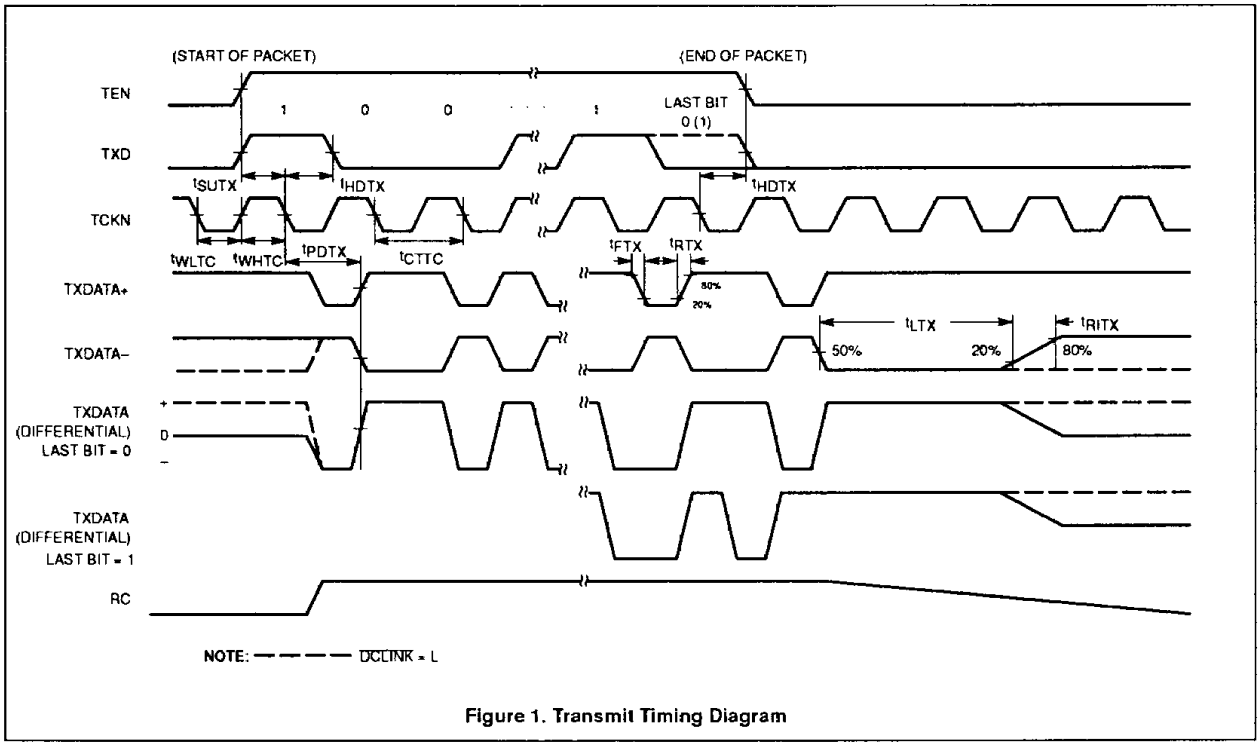



**Figure 1. Transmit Timing Diagram**

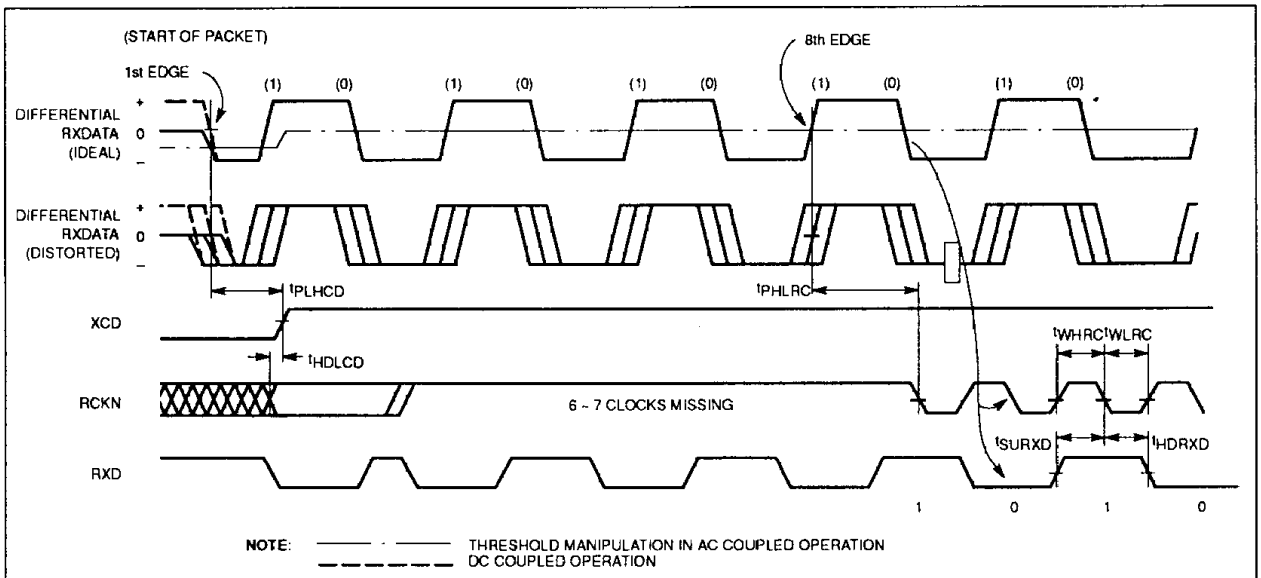



**Figure 2. Receive Timing Diagram, Start of Packet**

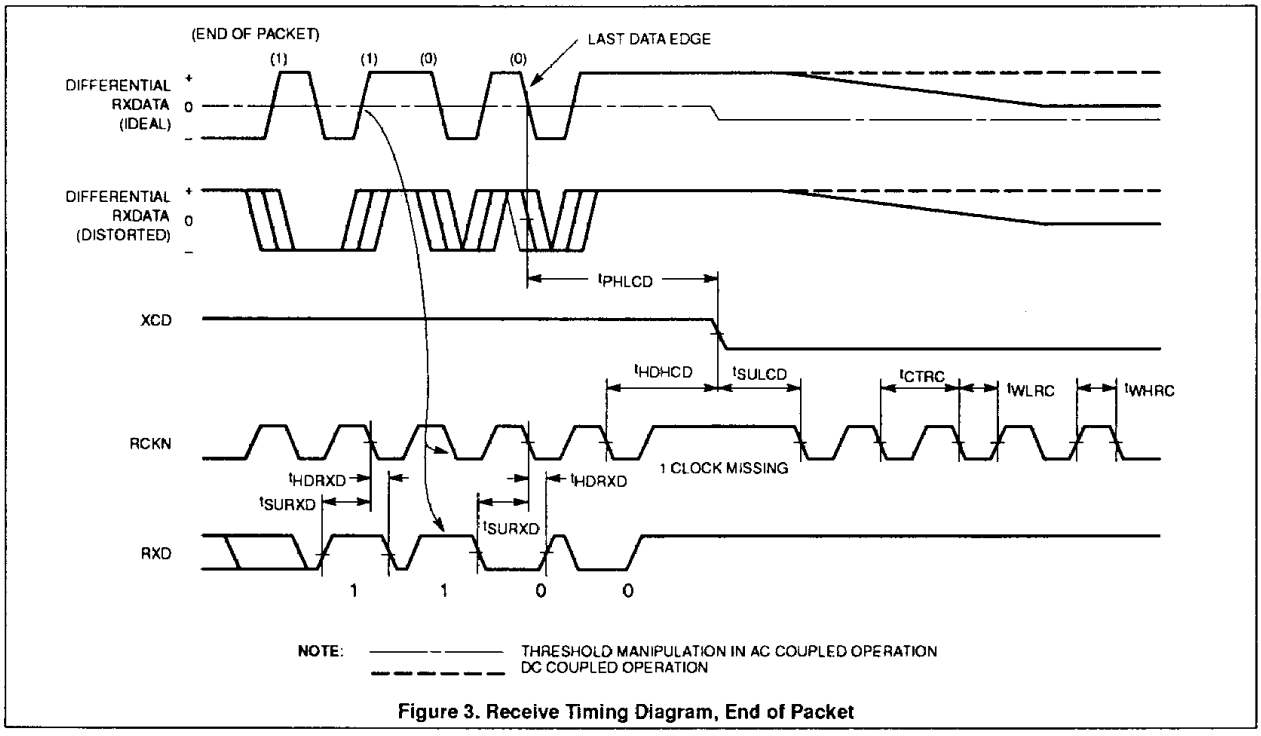
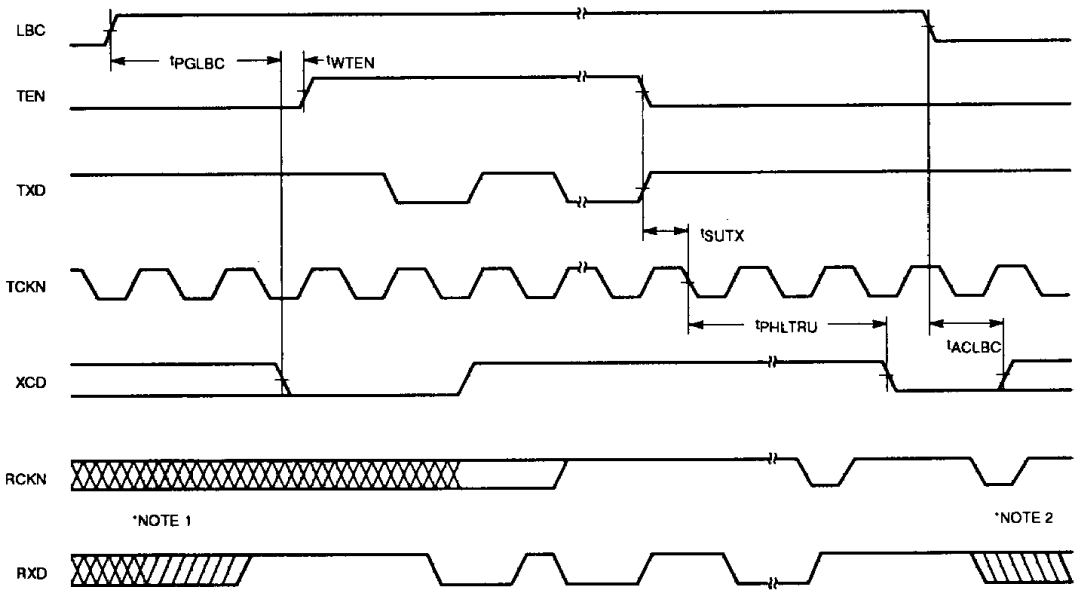



**Figure 3. Receive Timing Diagram, End of Packet**




NOTE 1: WHEN RXDATA± ARE RECEIVING A PACKET AT LBC RISING, THE RECEIVED DATA IS NOT COMPLETE.
NOTE 2: WHEN RXDATA± ARE RECEIVING AT LBC FALLING, THE PACKET MAY NOT BE DECODED CORRECTLY.

**Figure 4. Loopback Timing Diagram**

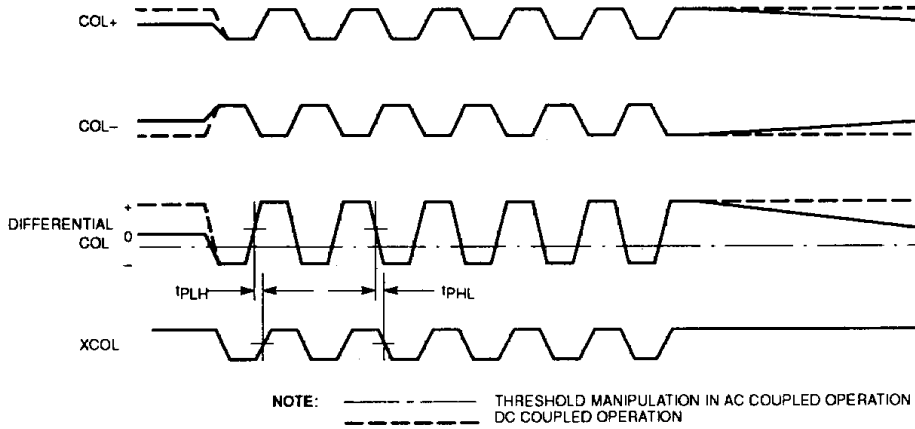



**Figure 5. Collision Timing Diagram**

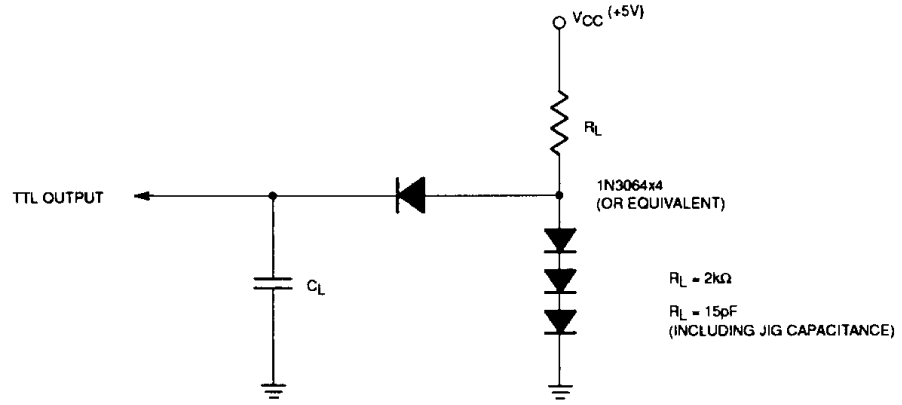



**Figure 6. TTL Output Load Circuit**

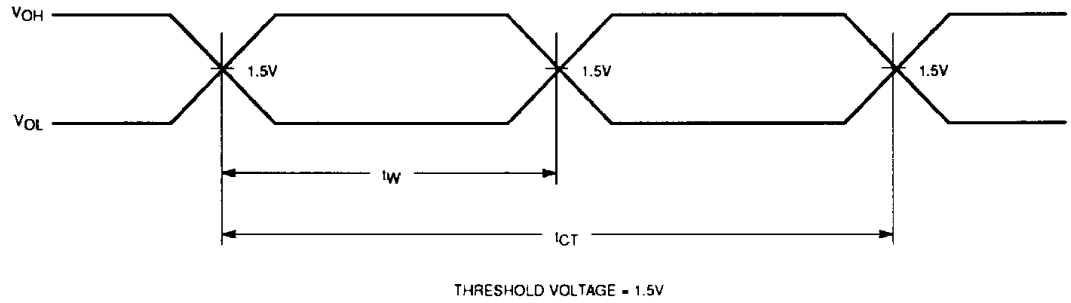



**Figure 7. TTL Output Waveform**

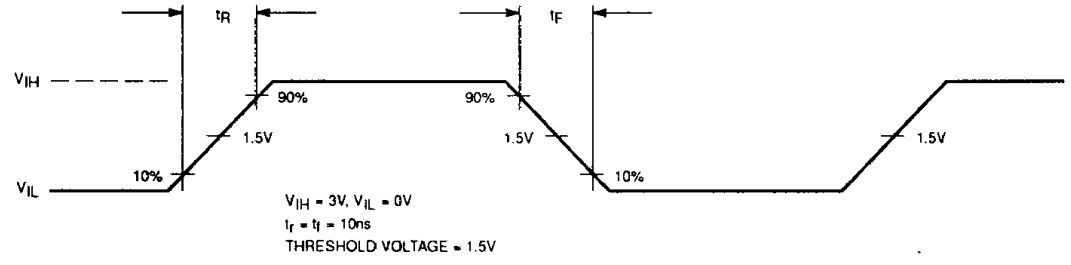



**Figure 8. TTL Input Waveform**

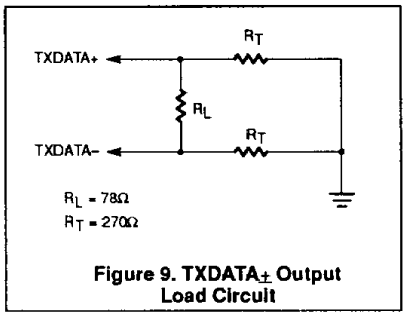



**Figure 9. TXDATA± Output Load Circuit**

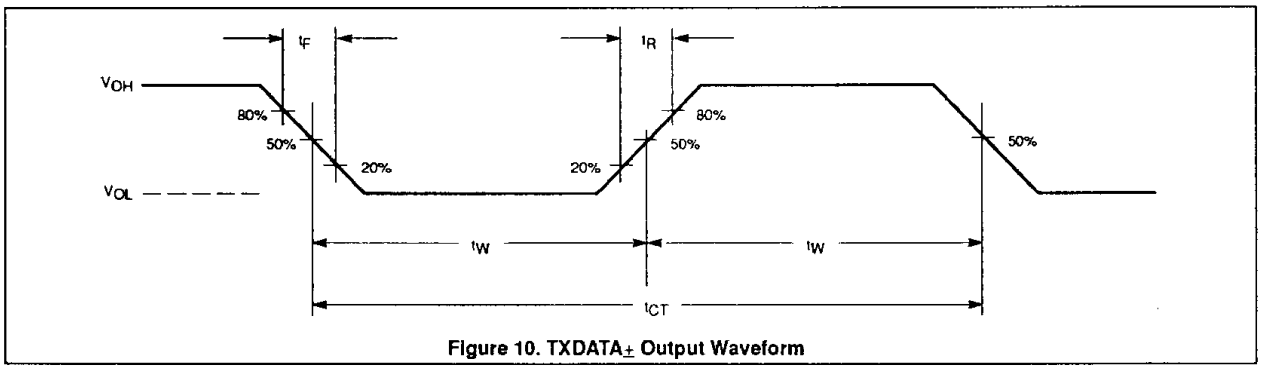



**Figure 10. TXDATA± Output Waveform**

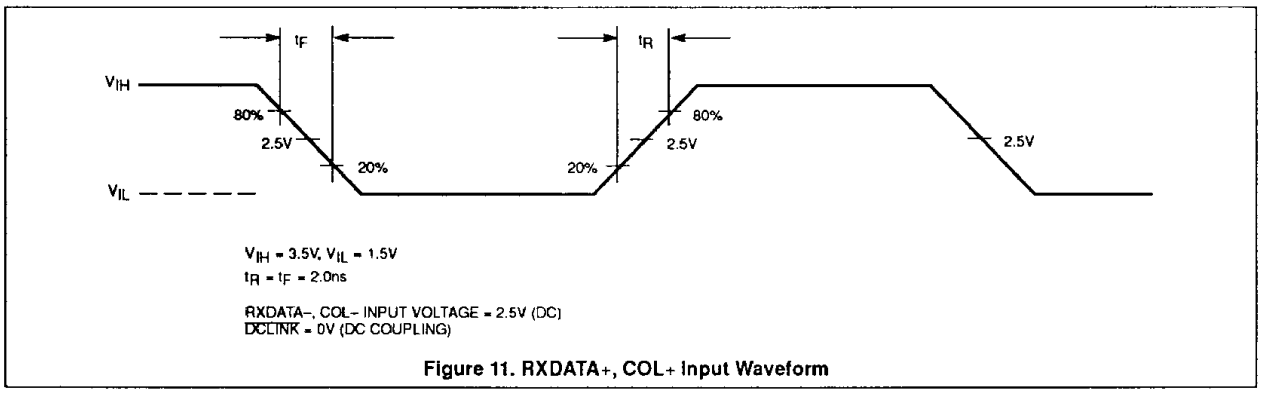



**Figure 11. RXDATA+, COL+ Input Waveform**

## TYPICAL TIMING CHARACTERISTICS

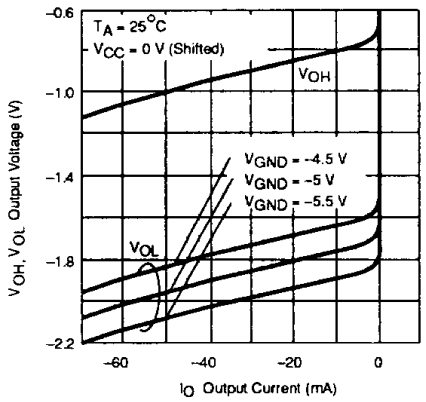



**Figure 12. TXDATA± Output Voltage vs Output Current**

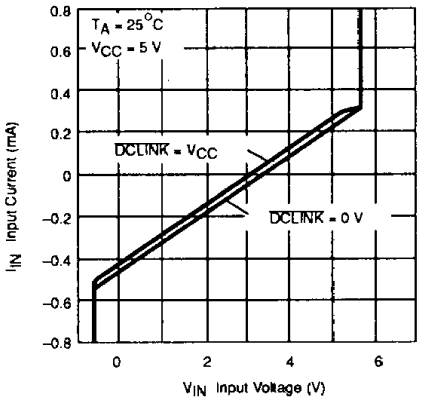



**Figure 13. RXDATA±, COL± Input Current vs Input Voltage**

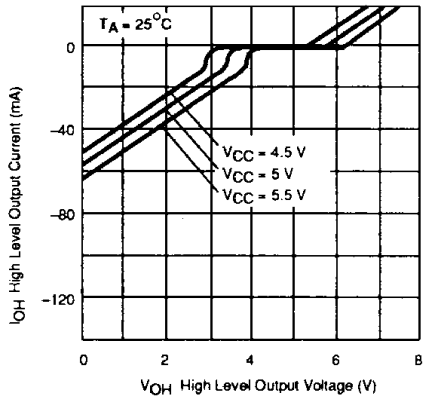



**Figure 14. TTL-OUTPUT High Level Output Current vs High Level Output Voltage**

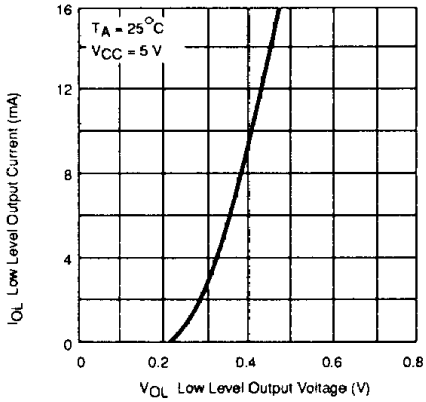



**Figure 15. TTL-OUTPUT Low Level Output Current vs Low Level Output Voltage**

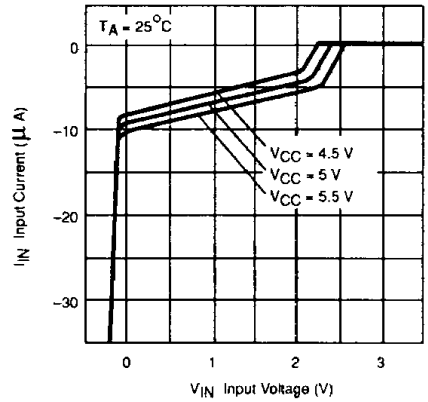



**Figure 16. TTL-INPUT Input Current vs Input Voltage**

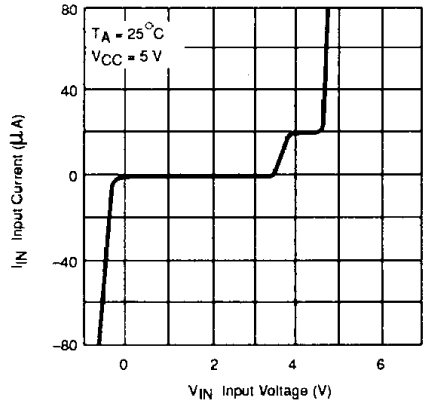



**Figure 17. OSC.IN Input Current vs Input Voltage**

## TYPICAL TIMING CHARACTERISTICS

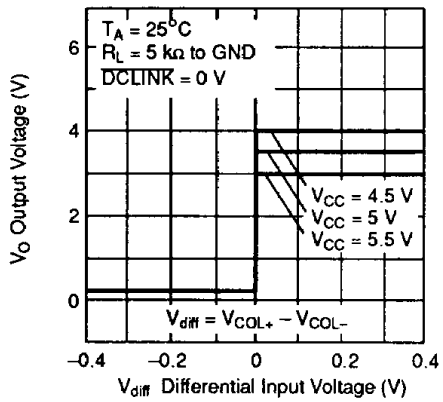



**Figure 18. COL± to XCOL TRANSFER (Receiver Threshold) Output Voltage vs Differential Input Voltage**

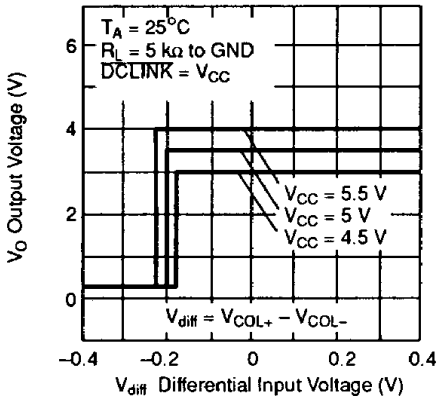



**Figure 19. COL± to XCOL TRANSFER (Receiver Threshold) Output Voltage vs Differential Input Voltage**

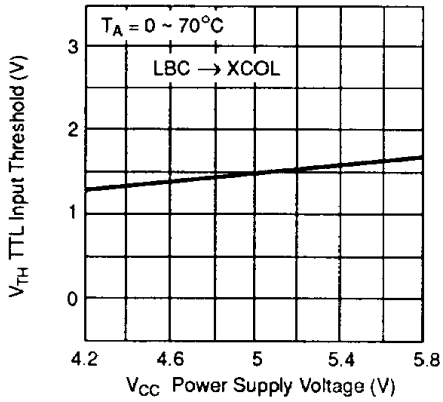



**Figure 20. TTL-INPUT THRESHOLD TTL Input Threshold vs Power Supply Voltage**

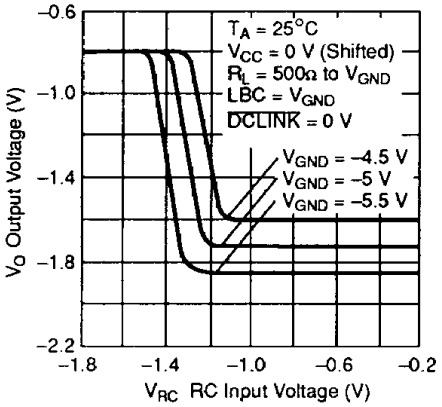



**Figure 21. RC to TXDATA– TRANSFER Output Voltage vs RC Input Voltage**

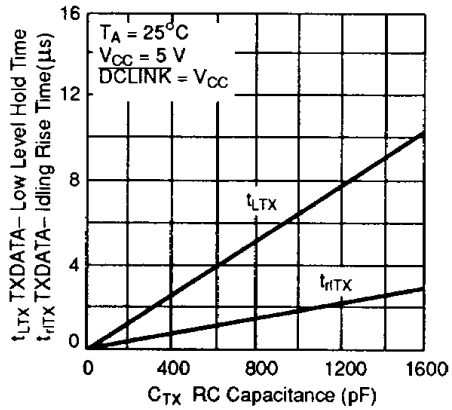



**Figure 22. TXDATA– LOW LEVEL HOLD TIME TXDATA– Low Level Hold Time TXDATA– Idling Rise Time vs RC Capacitance**

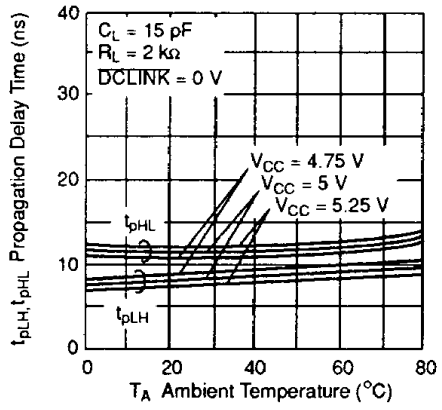
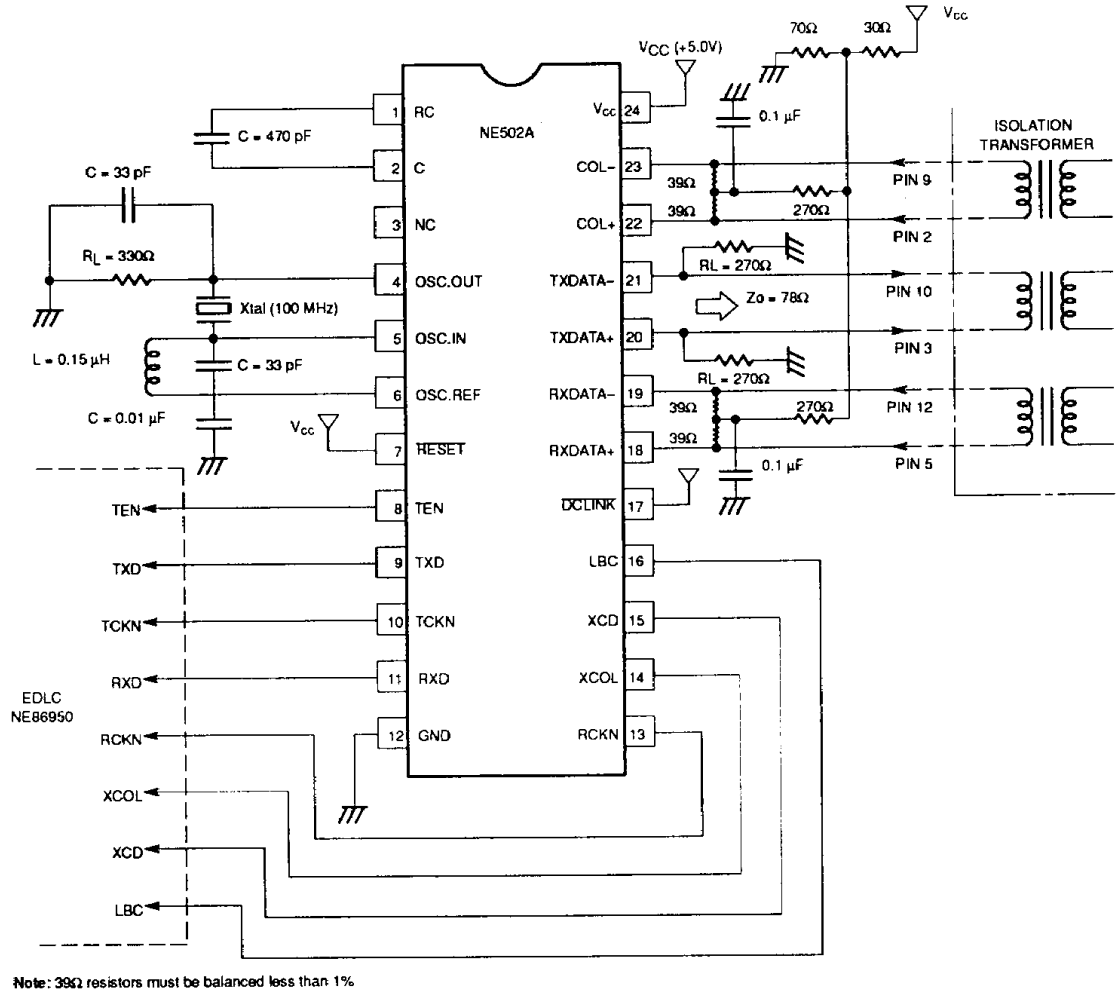



**Figure 23. COL± to XCOL PROPAGATION DELAY TIME Propagation Delay Time vs Ambient Temperature**




Note: 39Ω resistors must be balanced less than 1%

**Figure 24. Typical Application Circuit**

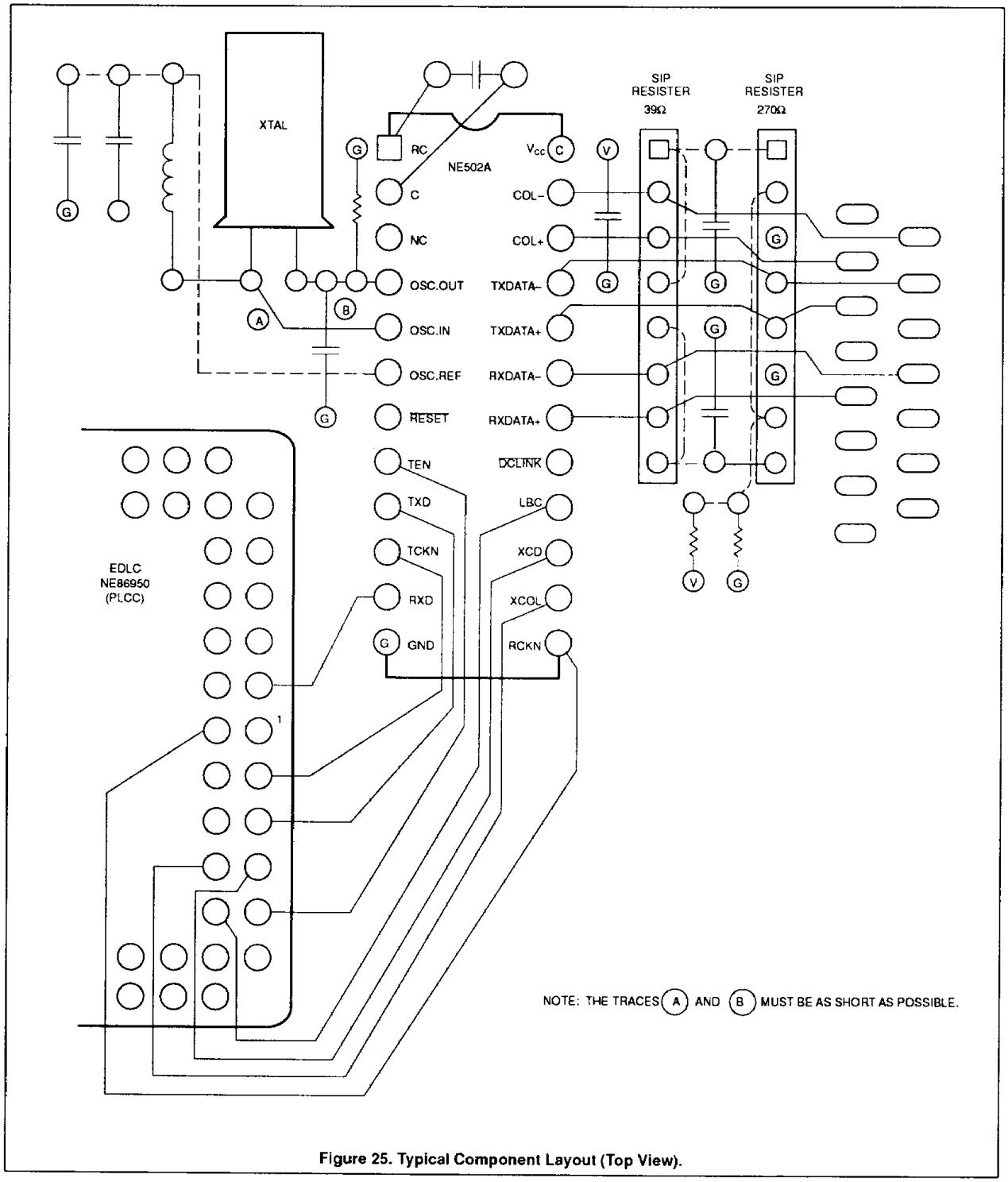



**Figure 25. Typical Component Layout (Top View).**