ICs for Communications

Octal Transceiver for U_{PN} Interfaces
OCTAT-P

PEB 2096 Version 2.1

Data Sheet 04.99

DS 2

PEB 2096 Revision History:		Current Version: 04.99
Previous Releases:		Data Sheet 01.96
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
9	9	Pin Configuration (correction pin 17 and 18)
-	19	Data rate on IOM-2 interface: up to 8192 kbit/s
21	22	Revision number for V2.1
40	42	Correction of State Diagram
45	46	Correction of Activation and Deactivation Example
-	49	Delay measurement
53	56	Correction of AC Characteristics
60	63	New Figure on Upn Frame Relation to FSC

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1 Overview

The new Infineon Technologies generation of highly integrated ISDN circuits enables design engineers to decrease board size and thus PBX size and its production costs.

Figure 1-1 shows an example of a PBX for 16 ISDN and 16 analog subscribers with 4 trunk lines realized with a few highly integrated chips of the new Infineon Technologies family of PBX and Line Card ICs: DOC, SICOFI-4, OCTAT-P and QUAT-S.

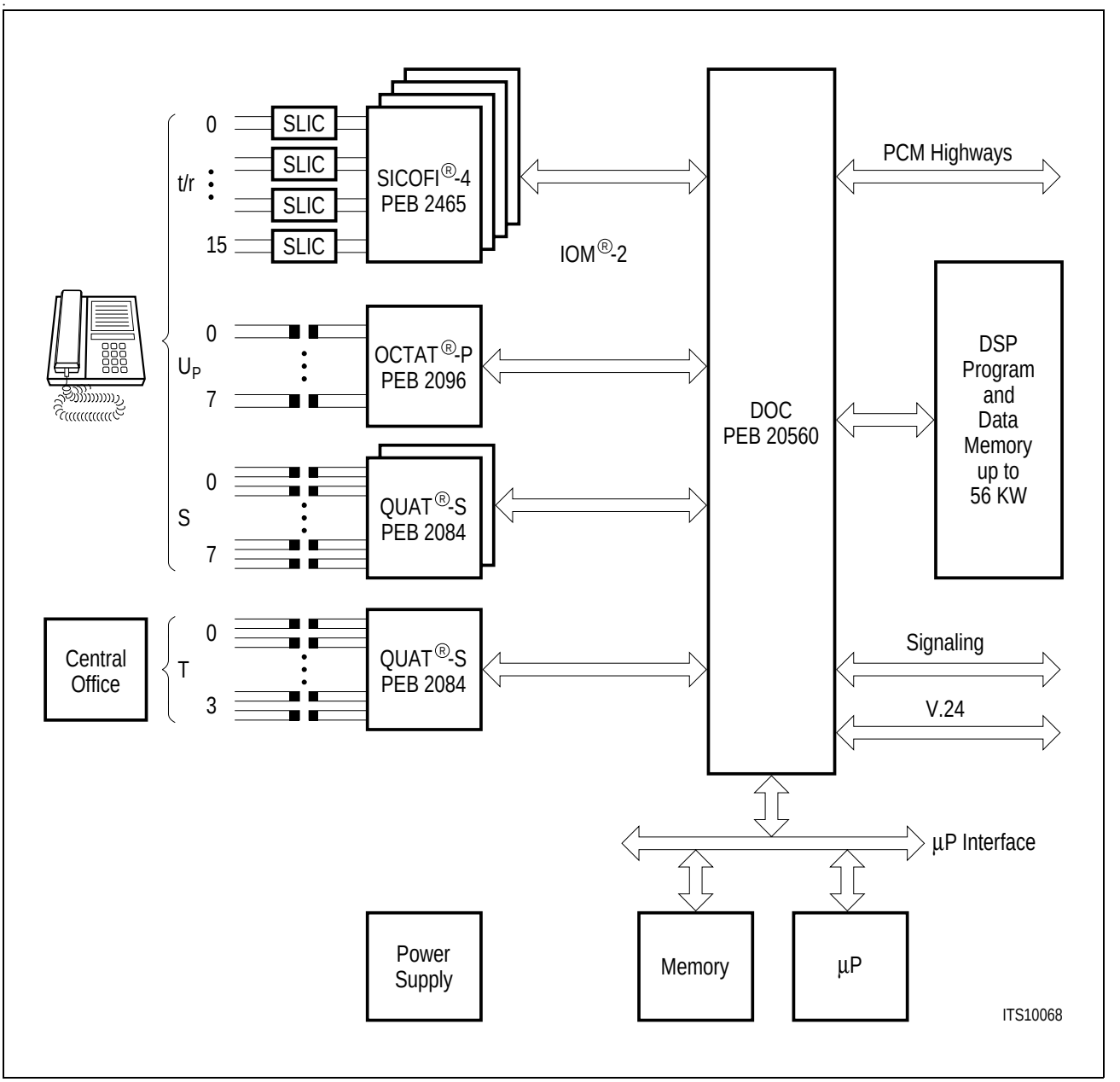


Figure 1-1 Application Example
PBX for 32 Subscribers with 4 Trunk Lines using one DOC

DOC, DSP Oriented PBX Controller, PEB 20560. The DOC integrates many different functional blocks on a single chip for building small PBXs or PBX Line Cards: Two ELICs,

Enhanced Line Card Controller (PEB 20550), one SIDEC, 4-channel signaling controller (LAPD), multiple IOM-2 and PCM interfaces, one up to 40 MIPS DSP with on-chip emulation and a Mailbox, one PCM-DSP interface for fast DSP access, one UART, Interrupt Controller, …
The DOC is a CMOS device offered in a P-MQFP-160 package.

QUAT®-S, Quadruple Transceiver for S/T Interfaces, PEB 2084, implements 4 four-wire S/T interfaces to link voice/data digital terminals to PBX subscriber lines and PBX trunk lines to the public ISDN. It can handle up to four S/T interfaces simultaneously in accordance with CCITT I.430, ETSI 300.012, and ANSI T1.605 standards.
The QUAT-S is a CMOS device offered in a P-MQFP-44 package.

OCTAT®-P, Octal Transceiver for U_{PN} Interfaces, PEB 2096, implements the two-wire U_{PN} interface used to link voice/data digital terminals to PBX subscriber lines. The OCTAT-P is an optimized device for LT applications and can handle up to eight U_{PN} interfaces simultaneously. It handles the U_{PN} interfaces in accordance with the U_{P0} interface specification except for the reduced loop length.
The OCTAT-P is a CMOS device offered in a P-MQFP-44 package.

SICOFI®-4, Programmable Signaling and CODEC Filter with 4 channels, PEB 2465, implements 4 t/r (a/b) interfaces to link analog voice terminals to PBX subscriber lines and analog PBX trunk lines to public switches. An integrated Digital Signal Processor handles all the algorithms necessary e.g. transhybrid-loss adaption, gain, frequency response, impedance matching. The IOM-2 Interface handles digital voice transmission, SICOFI-4 feature control and transparent access to the SICOFI-4 command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on-chip coefficient RAM. Thus it is possible to use the same line card in different countries.
The SICOFI-4 is a CMOS device offered in P-MQFP-64 package.

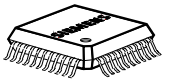
ISDN-Oriented Modular Interface (IOM®-2)

The “Group of Four”, ALCATEL, Siemens, Plessey and ITALTEL systems houses, originally defined a General Circuit Interface (GCI) with the aim of specifying a comprehensive interface which would allow various telecommunication devices to communicate in an efficient manner. The IOM-2 interface is a four-wire interface. It became a standard interface for interchip communication in ISDN applications. All above ICs are compatible and operate from a single 5 V power supply.

Octal Transceiver for U_{PN} Interfaces **PEB 2096**
OCTAT-P

Version 2.1 **CMOS**

1.1 Features



P-MQFP-44

- Eight full duplex 2B+D U_{PN} interface transceivers, each equipped with the following functions:
  - –Conversion from/to binary to/from pseudo-ternary code
  - –Receive timing recovery
  - –Activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO received from the line (e.g. detection of INFO 1)
  - –Line Delay Measurement
  - –Execution of test loops
  - –Analog line transceiver for up to 16 dB line attenuation
  - –U_{PN} interface functions compatible to PEB 2095, IBC, and PEB 20950, ISAC-P (except for looplength)
  - –U_{PN} interface fully compatible to PSB 2196, ISAC-P TE, PSB 2197, SmartLink-P, SCOUT
- IOM-2 interface
- Support for JTAG boundary scan test
- 1µ CMOS technology with low power consumption
- P-MQFP-44 package

Note: U_{PN} refers to a version of the standard interface U_{P0} (according to ZVEI standard) with a reduced loop length (up to 1.3 km).

Type	Package
PEB 2096	P-MQFP-44

1.2 Logic Symbol

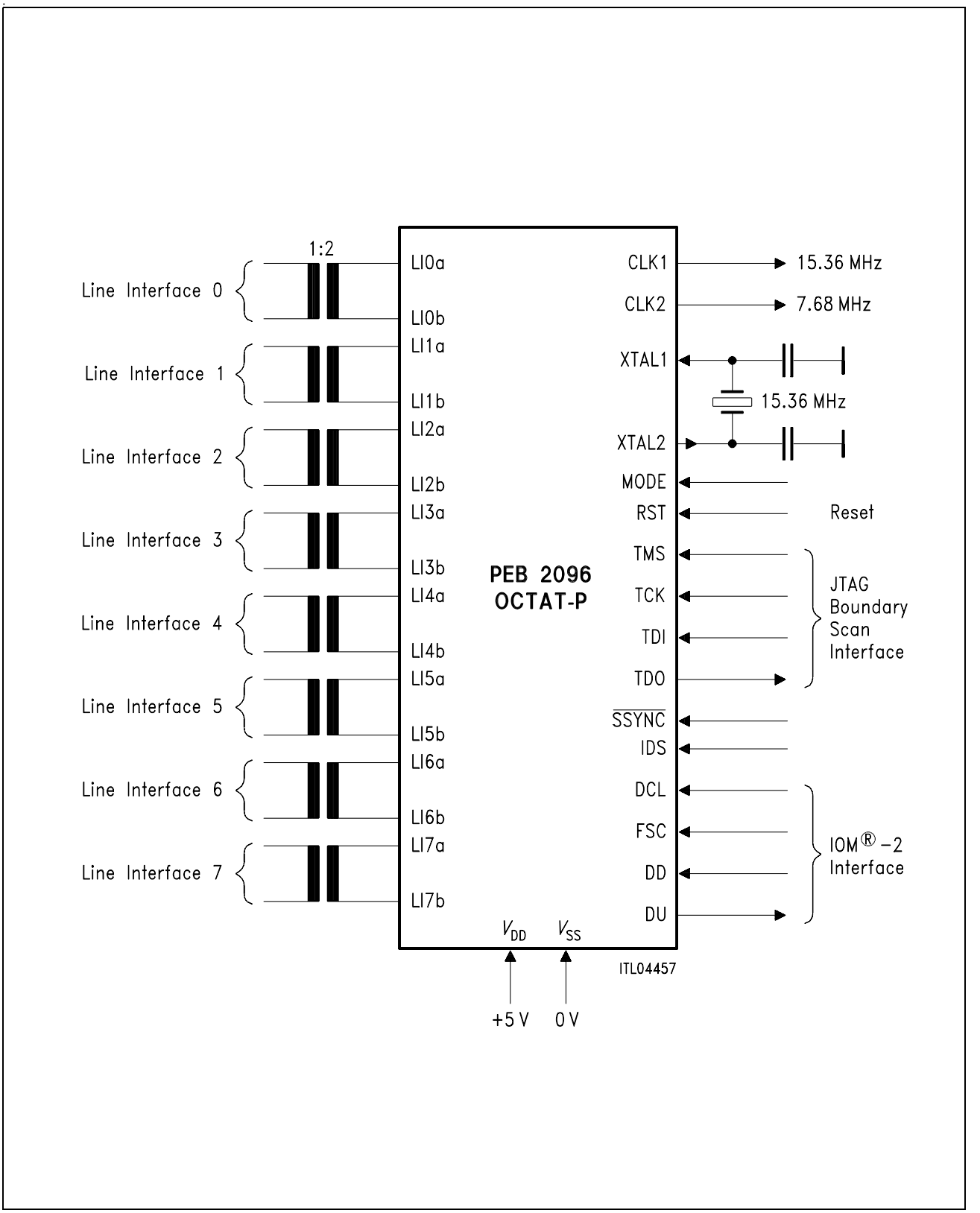


Figure 1-2 Logic Symbol

1.3 Pin Configuration

(top view)

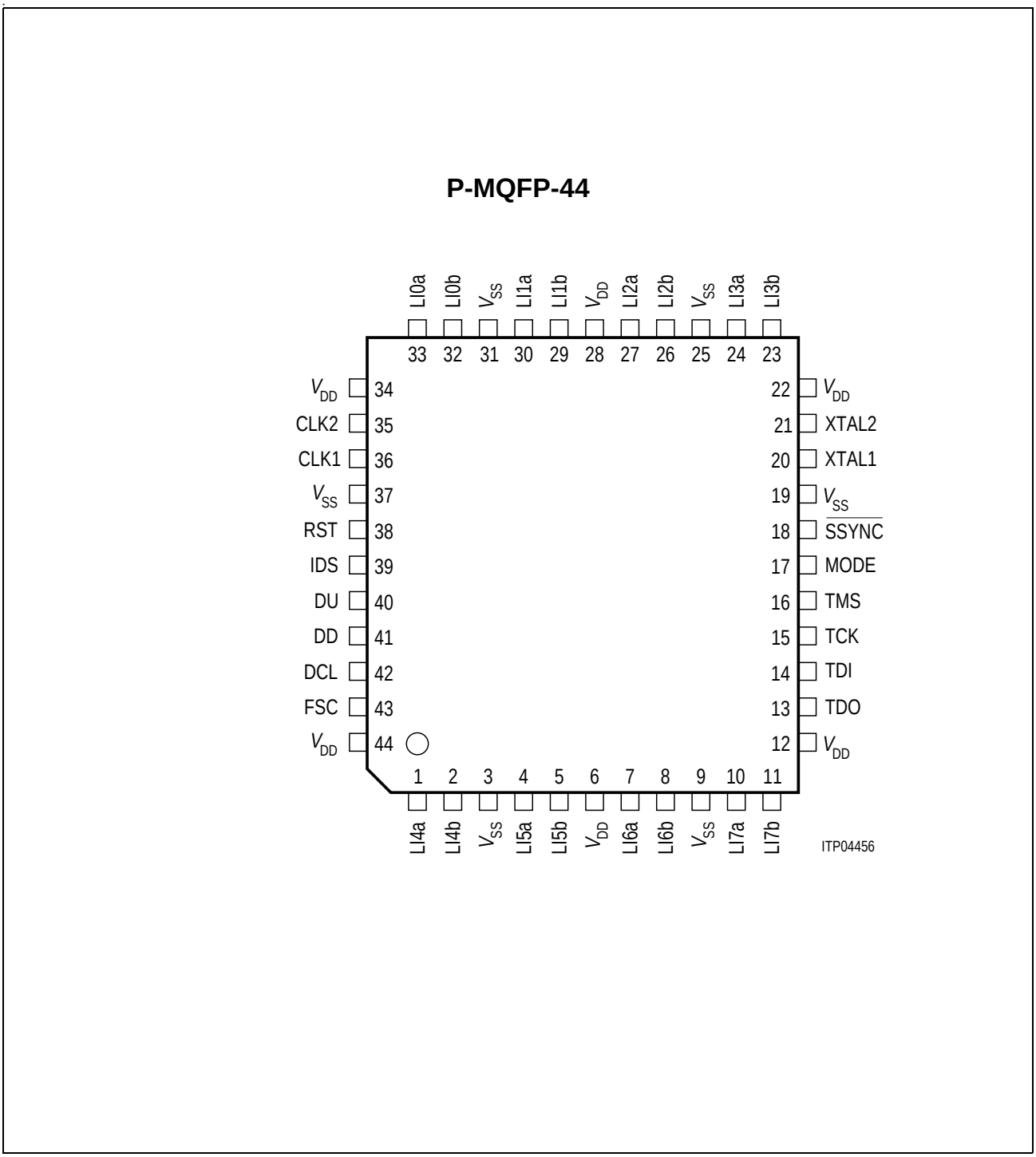


Figure 1-3 Pin Configuration

1.4 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
6, 12, 22, 28, 34, 44	V_{DD}	I	+ 5 V power supply
3, 9, 19, 25, 31, 37	V_{SS}	I	Reference ground
			U_{PN} Line Interfaces a,b
33, 32	LI0a,b	I/O	No. 0: differential input / output
30, 29	LI1a,b	I/O	No. 1: differential input / output
27, 26	LI2a,b	I/O	No. 2: differential input / output
24, 23	LI3a,b	I/O	No. 3: differential input / output
1, 2	LI4a,b	I/O	No. 4: differential input / output
4, 5	LI5a,b	I/O	No. 5: differential input / output
7, 8	LI6a,b	I/O	No. 6: differential input / output
10, 11	LI7a,b	I/O	No. 7: differential input / output
			IOM®-2 Interface
43	FSC	I	Frame Synchronization Clock: 8 kHz
42	DCL	I	Data Clock
41	DD	I	Data Downstream (data input)
40	DU	O	Data Upstream (data output)
39	IDS	I	Interface Data rate Select (static pin-strapped): 0: double DCL (normal IOM interface) 1: single DCL
			JTAG Boundary Scan Interface
16	TMS	I	Test Mode Select, internal pull-up resistor
15	TCK	I	Test Clock
14	TDI	I	Test Data Input, internal pull-up resistor
13	TDO	O	Test Data Output
20	XTAL1	I	Oscillator or 15.36 MHz clock input
21	XTAL2	O	Oscillator output
36	CLK1	O	Clock output 15.36 MHz (i.e. to drive other OCTAT-P)
35	CLK2	O	Clock output 7.68 MHz (i.e. to drive ISAC-S or QUAT-S)
38	RST	I	Reset, active high

1.4 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
18	$\overline{\text{SSYNC}}$	I	Superframe synchronization
17	MODE	I	This pin selects the initial values of the General Configuration Register and in the Configuration Register for U_{PN} Line Interfaces as described in **Chapter 4.2** and **Chapter 4.4**. It also enables Push-Pull Sensing on pin DU as described in **Chapter 3.4**.

1.5 Block Diagram

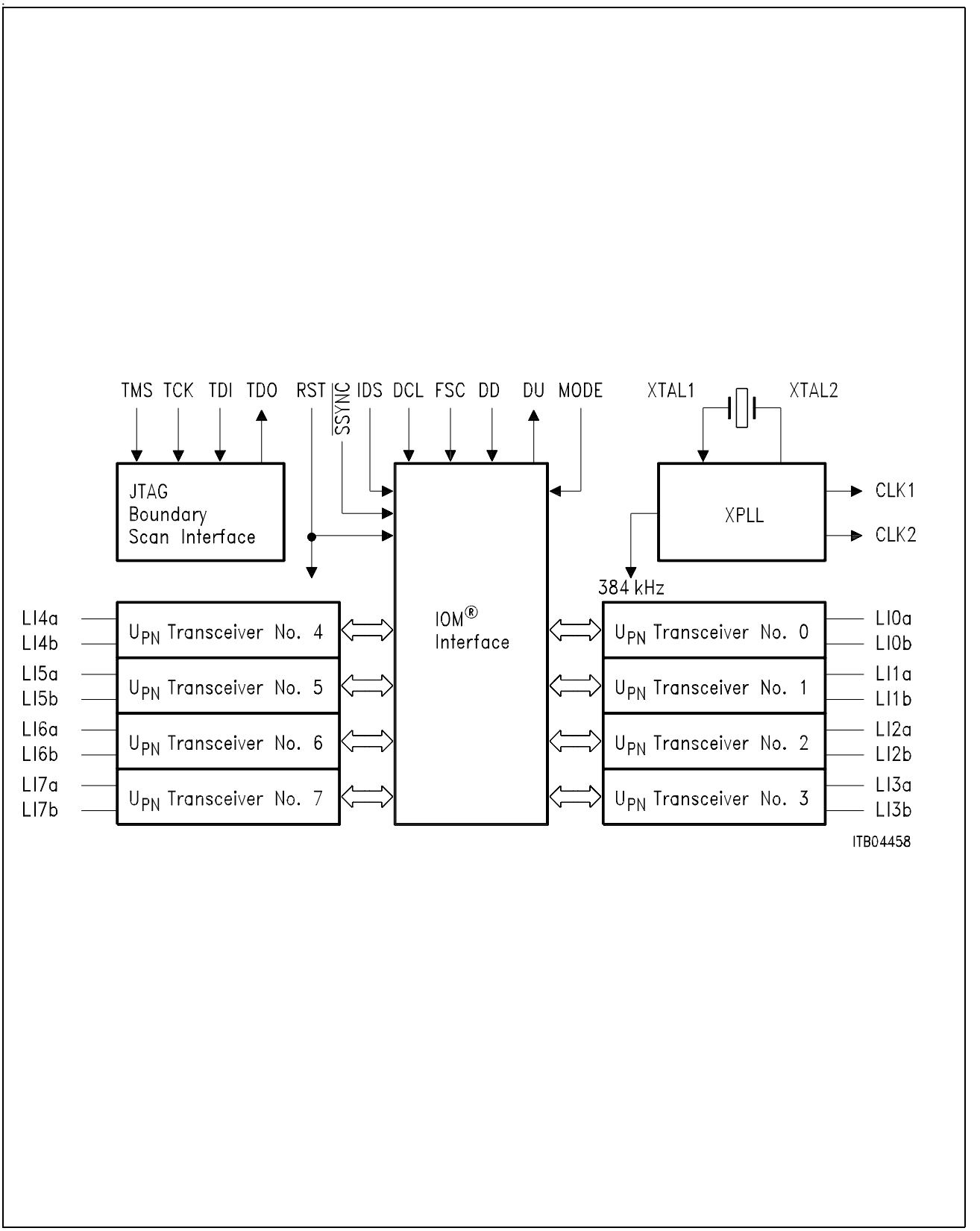


Figure 1-4 Block Diagram

2 Functional Description

The PEB 2096, OCTAT-P, performs the layer-1 functions of the ISDN basic access for eight U_{PN} interfaces at the LT side of the PBX.

2.1 Device Architecture

The OCTAT-P contains the following functional blocks: Refer to **Figure 1-4**

- Eight line transceivers for the U_{PN} interfaces
- One IOM-2 interface
- Frame structure converter between the IOM-2 interface and the U_{PN} interfaces
- JTAG Boundary scan interface
- Clocking, reset and initialization block

2.2 Interfaces

2.2.1 General Principle of the U_{PN} Interface

A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay (t_d). Refer to **Figure 2-1**. The terminal equipment waits a minimum guard time (t_g = 5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange begins a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and a PT (Private Termination) follows exactly the same procedure.

Note that the guard time in TE is always defined with respect to the M-bit.

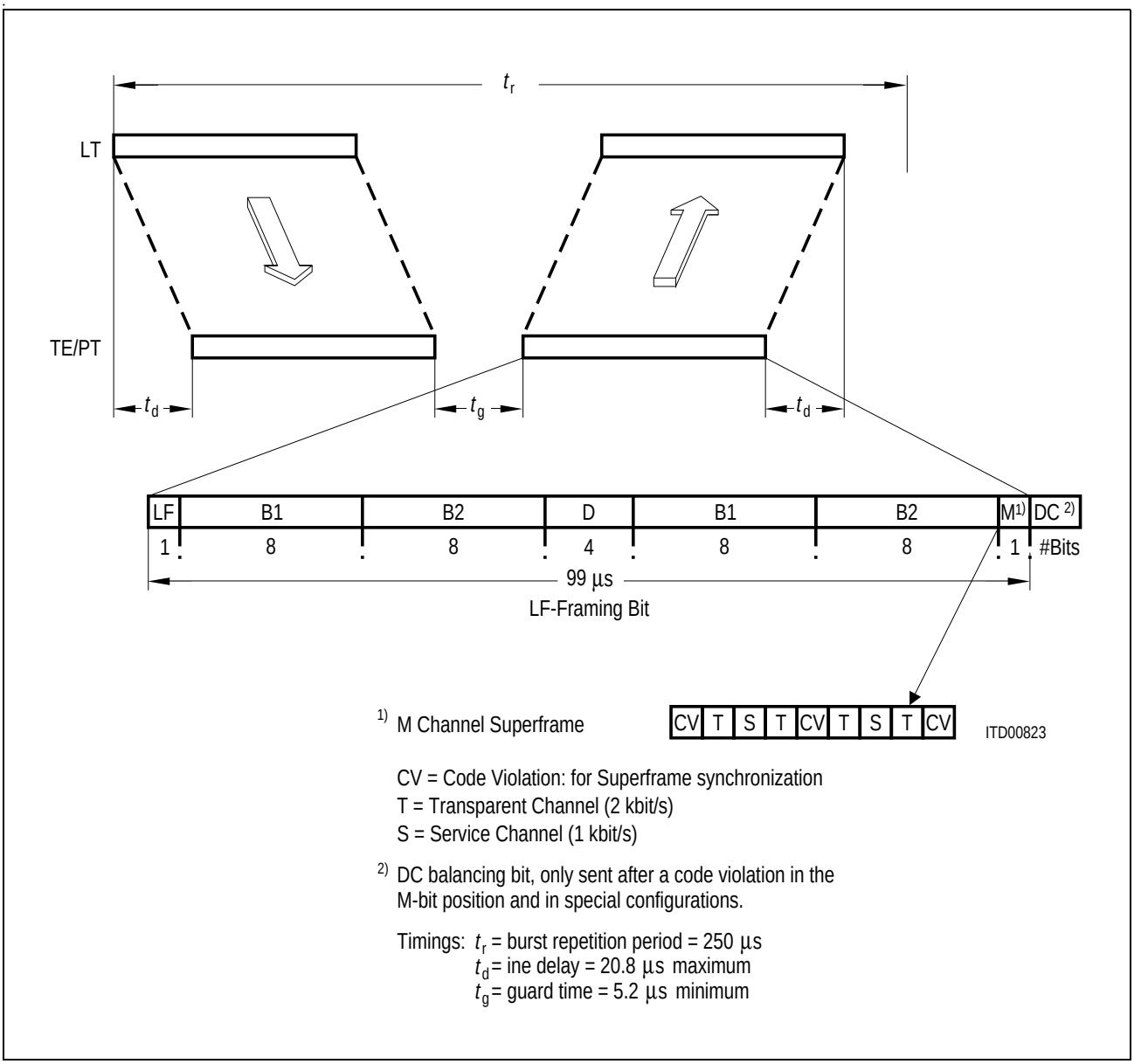


Figure 2-1 U_{P0} Interface Frame Structure (= U_{PN})

Within a burst, the data rate is 384 kbit/s. The 38-bit frame structure is as shown in **Figure 2-1**. The framing bit (LF) is always logical ‘1’. The frame also contains the user channels (2B + D).

It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This results in an effective full duplex data rate of 16 kbit/s for the D channel and 64 kbit/s for each B channel.

The final bit of the frame is called the M bit. Its data rate is 4 kbit/s. Four successive M bits, from four successive U frames, constitute a superframe. Three signals are carried in this superframe. Every fourth M bit is a code violation (CV) and is used for superframe synchronization. This can be regarded as the first bit of the superframe. From this reference (CV = bit 1), bit 3 of the superframe is the service channel bit S. This

S-channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S channel has a data rate of 1 kbit/s. It conveys test loop control information from the LT to the TE/PT and reports of transmission errors from the TE/PT to the LT. Bit 2 and bit 4 of the superframe are the T bits. This 2 kbit/s channel is accessible via the C/I channel and may be used to carry the “available”/“blocked” information sent by the D-channel arbiter of the PEB 20550, ELIC.

It is allowed to add a DC balancing bit to the burst, in order to decrease DC offset voltage on the line after transmission of a CV in the M-bit position. The OCTAT-P transmits this DC balancing bit when transmitting INFO 4 and when line characteristics indicate potential decrease in performance.

The OCTAT-P scrambles B-channel data on the U_{PN} interface in order to ensure that the downstream receiver (e.g. ISAC-P TE) gets enough pulses for a reliable clock extraction (flat continuous power density spectrum is provided) and no periodic patterns appear on the line.

The scrambling is in accordance with CCITT V.27.

The coding technique used on the U interface is a half-bauded AMI code (with a 50 % pulse width). A logical ‘0’ corresponds to a neutral level, logical ‘1s’ are coded as alternate positive and negative pulses. Code violation (CV) is caused by two successive pulses with the same polarity.

See **Figure 2-2**. The AMI coding includes always the data bits going on the U_{PN} interface in one direction. Thus there is a separate AMI coding unit for data downstream and one for data upstream.

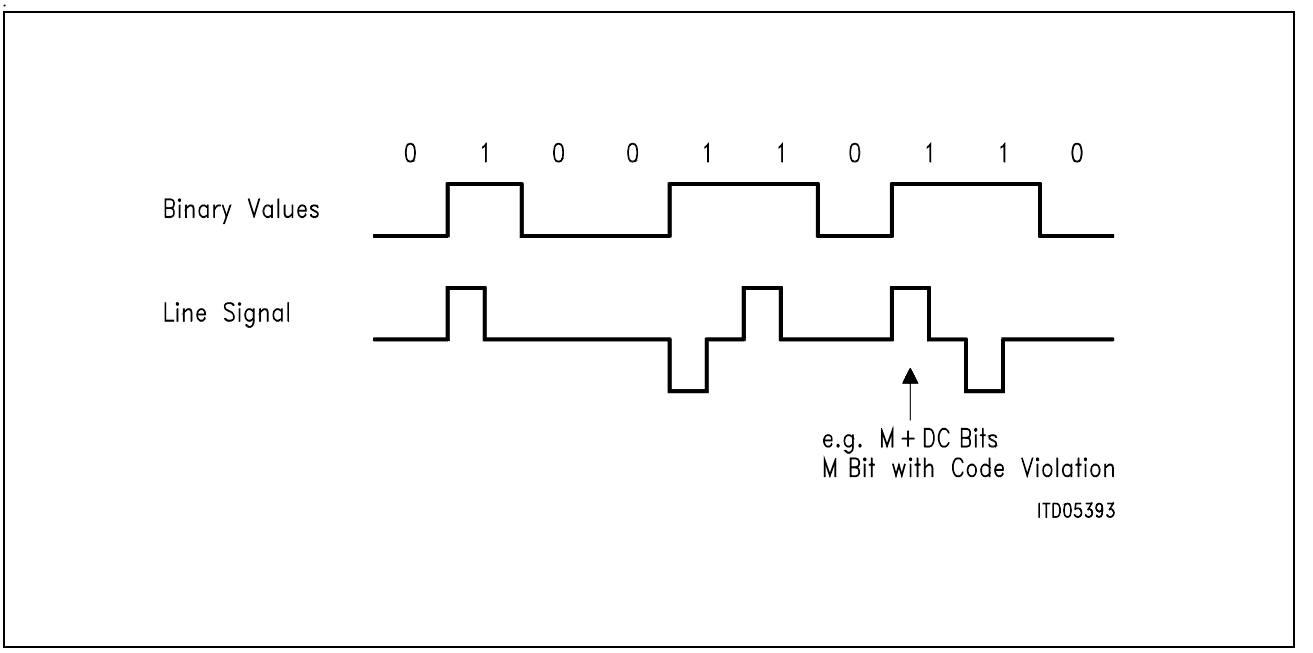


Figure 2-2 AMI Coding on the U_{PN} Interface

2.2.2 IOM®-2 System Interface

The PEB 2096, OCTAT-P, is equipped with a digital ISDN Oriented Modular (IOM-2) interface, for communication with upper layer functions, such as IDEC (PEB 2075), EPIC (PEB 2055) and ELIC (PEB 20550). EPIC and ELIC represent the first switching stage towards the exchange system. Refer to **Figure 2-3**.

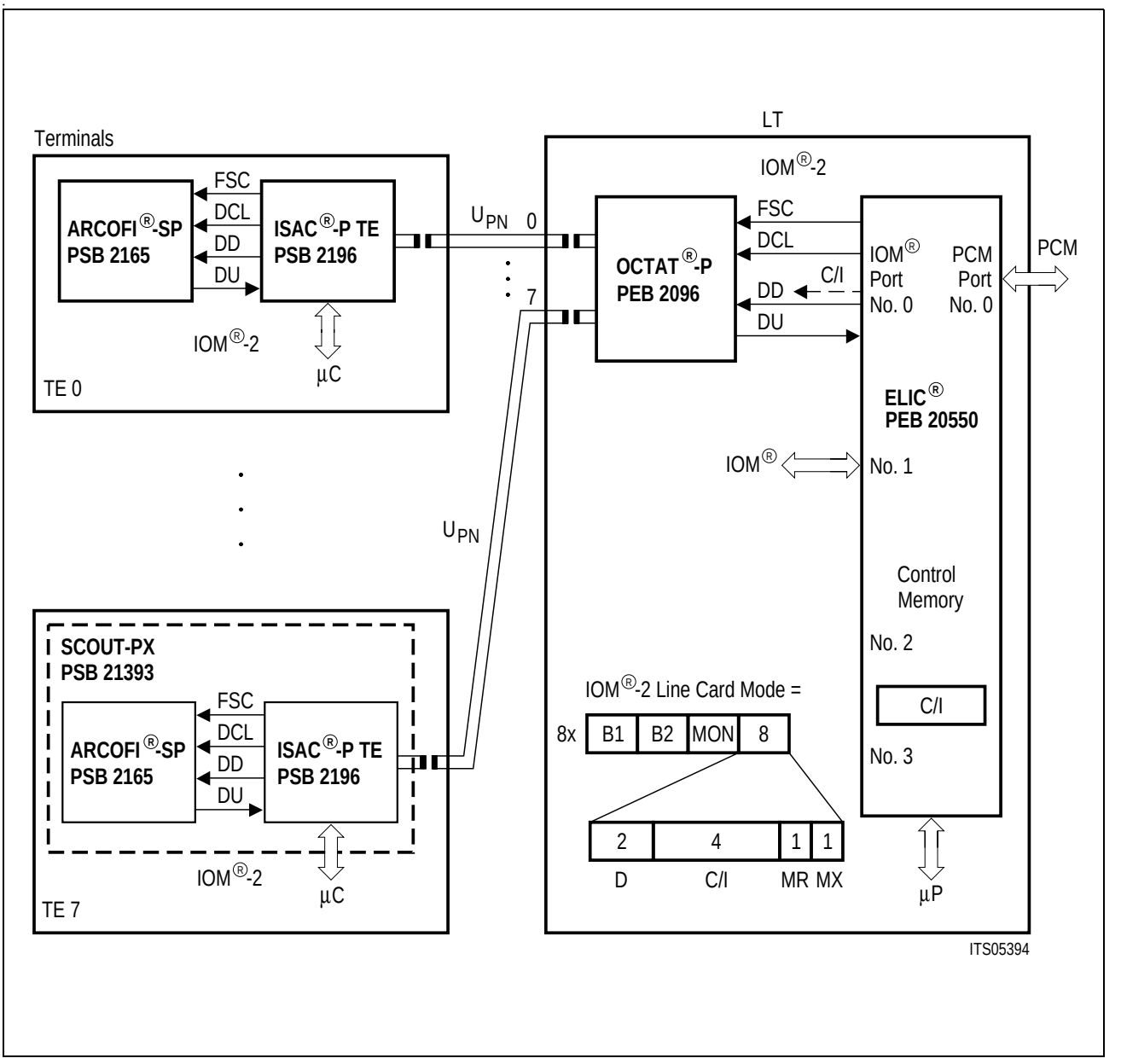


Figure 2-3 System Integration, IOM® Interface

The IOM interface is a four-wire serial interface with a data clock (DCL), an 8 kHz frame synchronization clock (FSC), and one data line per direction: data downstream (DD) and data upstream (DU). One IOM-2 frame consists of up to 8 IOM channels (subframes) (**Figure 2-4**).

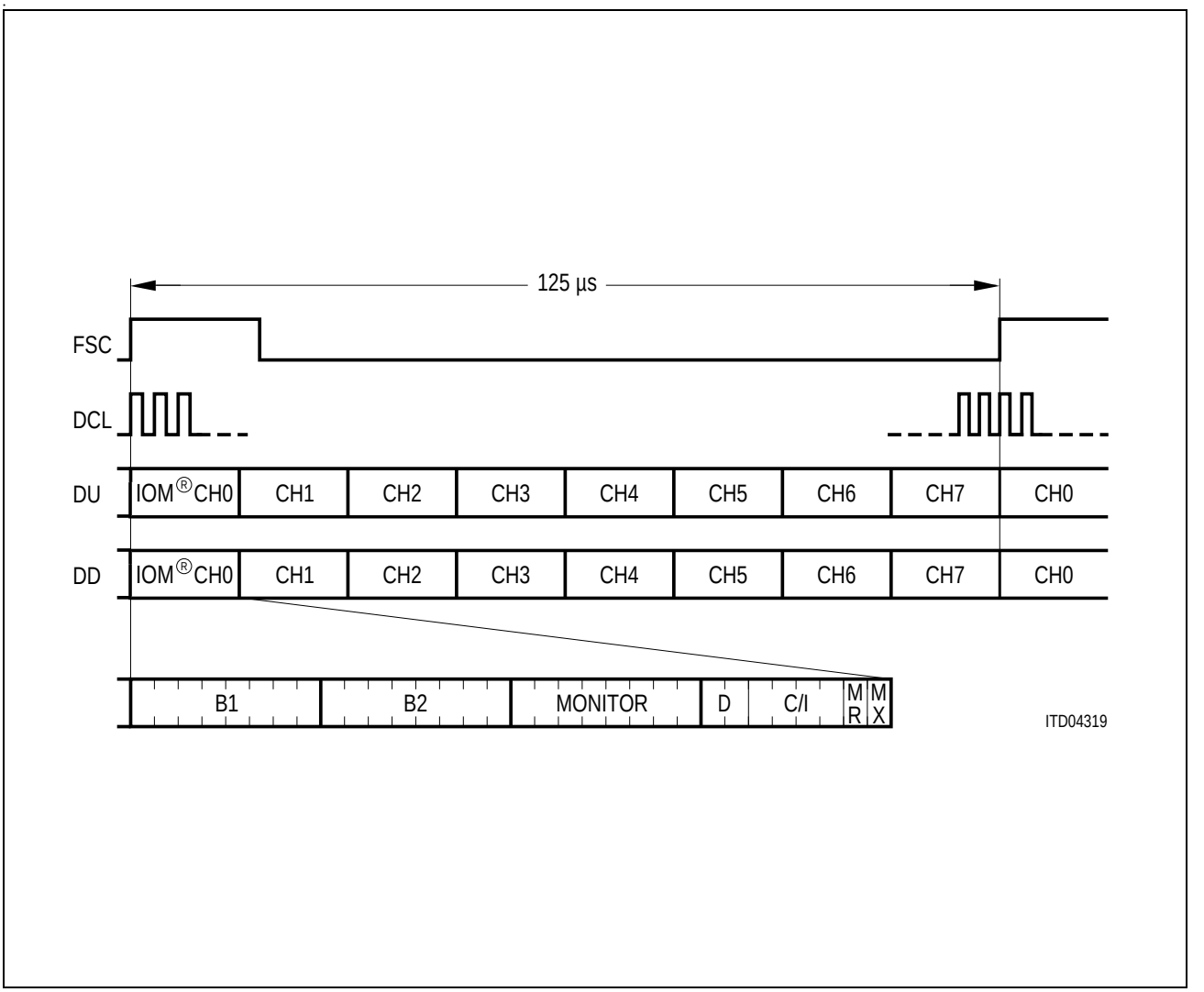


Figure 2-4 Multiplexed Frame Structure of the IOM®-2 Interface in LT-Mode with 2.048 Mbit/s Data Rate

Each IOM channel consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 overhead bits for monitor and control information (activation/deactivation of OSI layer-1 and maintenance functions).

The ISDN user data rate is 144 kbit/s (B1 + B2 + D).

The data is transmitted transparently synchronous and in phase in both directions over the IOM interface using time division multiplexing within the 125 µs IOM-2 interface frame.

Nominal bit rate of data (DD and DU):	256 kbit/s	… 4096 kbit/s
Nominal frequency of DCL:	512 kHz	… 8192 kHz
Nominal frequency of FSC:	8 kHz	

Note: The bit rate must be a multiple of 256 kbit/s.

In order to allow the use of the eight channels also with a maximum clock rate of 2,048 kHz provided by the system, the OCTAT-P can also run the IOM interface with only half the nominal DCL clock rate, i.e. 2,048 kHz for 2,048 kbit/s (Input pin IDS = 1).

The OCTAT-P requires three IOM frames to synchronize to the DCL frequency. A corrupted IOM frame caused by different amount of DCL pulses within two consecutive IOM frames (e.g. caused by spikes on DCL or FSC) resets internally all registers and the activation and deactivation state machine, **Figure 3-8**.

The allocation between U_{PN} line interfaces and the IOM-2 interface channels is according to their numbers, i.e. LI0a,b is allocated to IOM channel 0, LI1 to channel 1, and so on.

For details refer to **Figure 2-1** and **Figure 2-2** and to the **Chapter 5.8** and the IOM Interface Specification, Rev. 2.

Monitor Channel

The monitor channel is used to convey messages (e.g. when a bit error occurs on U_{PN}) or for access to internal registers: Identification Register, General Configuration Register, Bit Error Register, Configuration Register for U_{PN} and Test Registers.

The PEB 2096, OCTAT-P, has implemented the monitor channel protocol according to the IOM Interface Specification, Rev. 2, in the first of the eight IOM channels allocated to the eight U_{PN} interfaces. Refer also to the **Chapter 3.8**.

C/I-Channel

The C/I-channel is used for communication between the PEB 2096, OCTAT-P, and a processor via a layer-2 device, to control and monitor layer-1 functions. The OCTAT-P has 8 IOM-2 channels and thus 8 C/I-channels; one for each transceiver.

The codes originating from layer-2 devices are called “commands”, those from the PEB 2096, OCTAT-P, are called “indications”. For a list of the C/I (command/indication) codes and their use, refer to the **Chapter 3.9**.

Data Rates on IOM-2 Interface

The OCTAT-P supports the following types of IOM-2 interfaces:

Table 1

Mode of IOM-2 Interface	2	4	8
Nominal bit rate of data (DD and DU)	2048 kbit/s	4096 kbit/s	8192 kbit/s
Nominal frequency of DCL (2 x data rate)	4096 kHz	8192 kHz	not supported
Selectable frequency of DCL (1 x data rate)	2048 kHz	4096 kHz	8192 kHz
Nominal frequency of FSC	8 kHz	8 kHz	8 kHz
Number of IOM channels per one IOM-2 frame	8	16	32
Number of time slots per one IOM-2 frame	32	64	128
Number of OCTAT-P on one IOM-2 interface	1	2	4

Notes:

1. One OCTAT-P requires 8 complete IOM channels.
2. Additional delayed FSCs are needed in modes 4 and 8 for connecting several OCTATs to the IOM bus.

2.2.3 JTAG Boundary Scan Test Interface

The OCTAT-P provides fully IEEE Standard 1149.1 compatible boundary scan support to allow cost effective board testing. It consists of:

- Complete boundary scan test
- Test access port controller (TAP)
- Four dedicated pins (TCK, TMS, TDI, TDO)
- One 32-bit IDCODE register
- Specific functions for LIna,b

2.2.3.1 Boundary Scan Test

The following OCTAT-P pins are included in the boundary scan:
CLK2, CLK1, RST, IDS, DU, DD, DCL, FSC, MODE, $\overline{\text{SSYNC}}$, XTAL1.
Three additional user specific instruction codes control the transmission of continuous pulses at the line interface LIna,b.

Depending on the pin functionality one or two boundary scan cells are provided.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	Input
Output	2	Output, enable

When the TAP controller is in the appropriate mode data is shifted into/out of the boundary scan via the pins TDI/TDO using a 6.25 MHz clock on pin TCK.

The OCTAT-P pins are included in the following sequence in the boundary scan:

Boundary Scan

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
1	35	CLK2	O	2
2	36	CLK1	O	2
3	38	RST	I	1
4	39	IDS	I	1
5	40	DU	O	2
6	41	DD	I	1
7	42	DCL	I	1
8	43	FSC	I	1
9	17	MODE	I	1
10	18	$\overline{\text{SSYNC}}$	I	1
11	20	XTAL1	I	1

2.2.3.2 TAP Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE St. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

The TAP controller supports 8 instructions:

- 5 instructions following the standard definition and
- 3 user specific instructions.

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code register
11xx	BYPASS	Bypass operation
1001	User specific	Continuous pulses on LIna and LInb
1010	User specific	Continuous pulses on LIna
1011	User specific	Continuous pulses on LInb

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state “update DR”, all output pins are updated with the falling edge of TCK. When it has entered state “capture DR” the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state “update DR”, all inputs are updated internally with the falling edge of TCK. When it has entered state “capture DR” the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 0011 (IDCODE) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

Note: The input pin XTAL1 should not be evaluated.
The input frequency (15.36 MHz) is not synchronous to TCK (6.25 MHz) which causes unpredictable snap-shots on the pin XTAL1.

IDCODE

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacture code (11 bits). The LSB is fixed to “1”.

Code for the Version 2.1 is “0011”.

Version	Device Code	Manufacture Code		Output
00XX	0000 0000 0001 0100	0000 1000 001	1	--> TDO

Version No. 0000 = V1.1
0001 = V1.2
0010 = V1.3
0011 = V2.1

Note: In the state “test logic reset” the code “0011” is loaded into the instruction code register.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

User Specific Instructions

Three different user specific pulse types are selectable, **Figure 2-5**.

An oscillator with a 15.36 MHz clock or an external clock is necessary for 192 kHz test pulse generation; according to the instruction code 9_H.

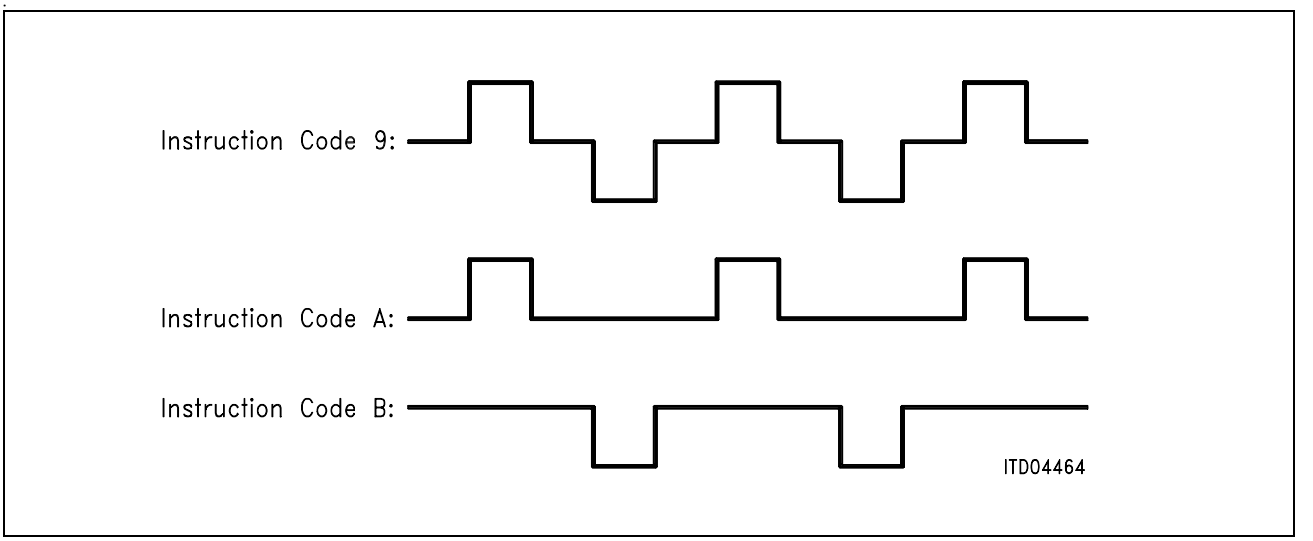


Figure 2-5 Test Pulse Wave Forms

2.3 Individual Functions

2.3.1 Transceiver, Analog Connections

The receiver input stages consist of an amplifier/equalizer, followed by a peak detector adaptive controlling the thresholds of the comparators and a digital oversampling unit.

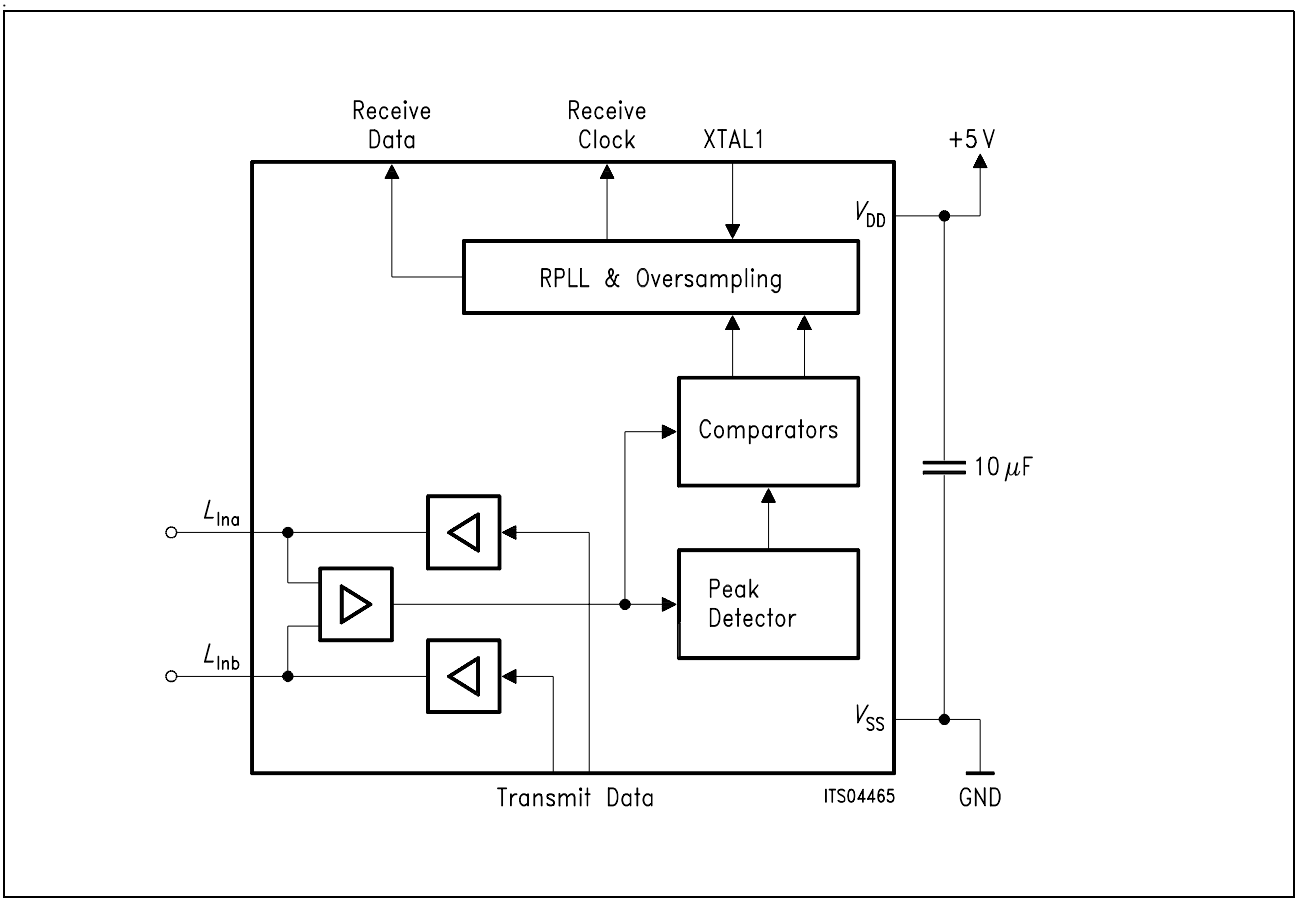


Figure 2-6 Transceiver Functional Blocks

External to the line interface pins LIna,b are connected: a transformer, external resistors and two capacitors (100 nF and 0.33 µF). Voltage overload protection is achieved by adding clamping diodes.

Depending on the transformer ratio employed (2:1 or 1.25:1), the resistor values have to be chosen and the resistors have to be connected accordingly:

Figure 2-7 depicts the analog connections for a transformer with the ratio 2:1 and **Figure 2-8** depicts the analog connections for a transformer with the ratio 1.25:1.

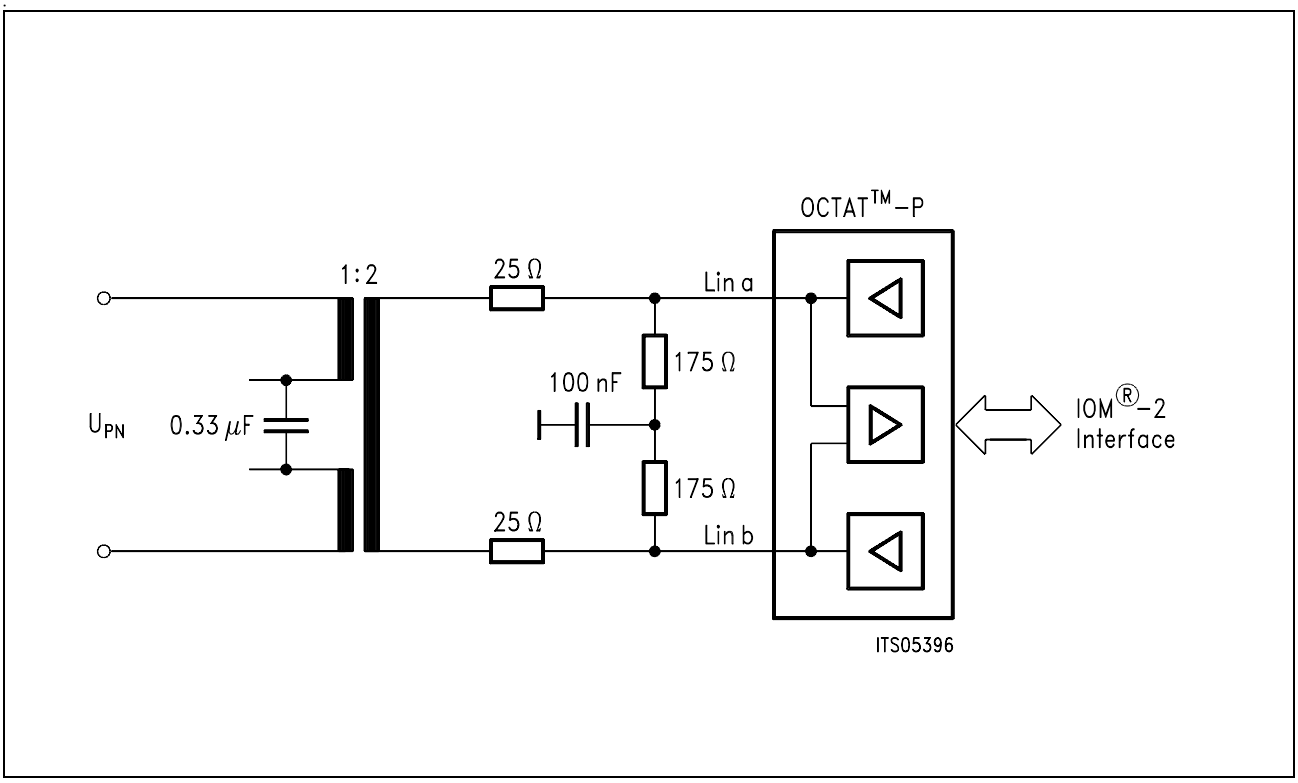


Figure 2-7 Transceiver with a 2:1 Transformer

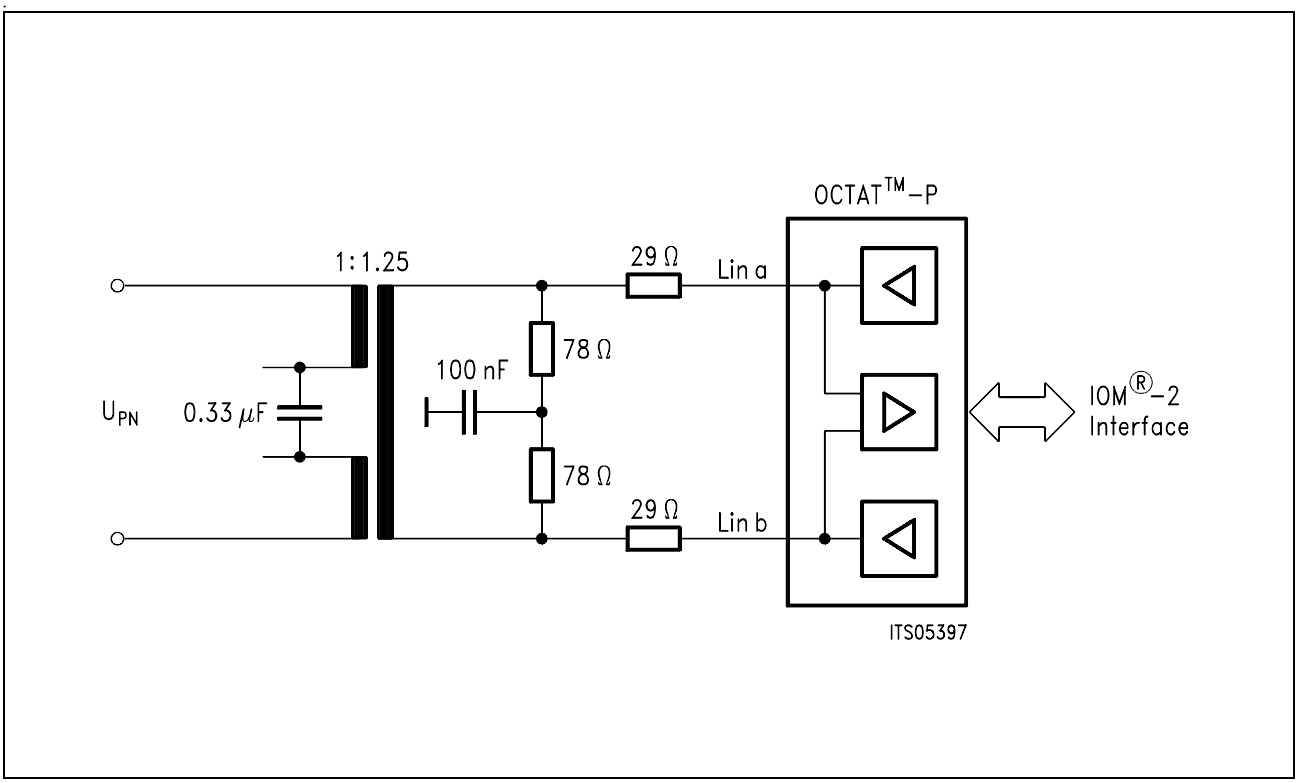


Figure 2-8 Transceiver with a 1.25:1 Transformer

The PEB 2096, OCTAT-P, covers the electrical requirements of the U_{PN} interface for loop lengths depending on the used transformer and the cable quality:

a) If the equalizer is enabled

(EQUDIS in Configuration Register for U_{PN} Line Interface is set to low)

Transformer	Cable	Loop Length
2:1	J-Y (ST) Y $2 \times 2 \times 0.6$	up to 1 km
	AWG 26	up to 1.3 km

b) If the equalizer is disabled

(EQUDIS in Configuration Register for U_{PN} Line Interface is set to high)

Transformer	Cable	Loop Length
2:1	J-Y (ST) Y $2 \times 2 \times 0.6$	up to 0.8 km
	AWG 26	up to 1.3 km

Concerning the 1.25:1 transformer, the maximum line attenuation is decreased by 3 dB.

*Note: The actual values of the external resistors depend on the selected transformer. The resistor values in **Figure 2-7** and **Figure 2-8** are optimal for an ideal transformer (R_{Cu} = 0).*

2.3.2 Transmit PLL

The transmit PLL (XPLL) synchronizes a 768 kHz transmit clock derived from the oscillator clock to FSC (8 kHz). When the oscillator clock is synchronous to FSC (fixed divider ratio of 1920 from 15.36 MHz clock) the XPLL will not perform any tracking after having locked the phase, i.e. the input jitter on clocks XTAL and FSC will not be increased.

Alternatively, when a free running oscillator is used, XPLL tracking increases FSC jitter by 32.5 ns (half oscillator period).

2.3.3 Receive PLL

The receive PLL (RPLL) recovers bit timing from a comparator output signal. The comparator has a threshold of 90 % with respect to the signal stored by the peak detector. The RPLL performs PLL tracking after detecting phase shifts of the same polarity in four pulses. A phase adjustment is done by adding or substracting 65 ns (one oscillator period) to or from the 384 kHz receive clock.

2.3.4 Receive Signal Oversampling

In order to additionally reduce the bit error rate in severe conditions, the OCTAT-P performs oversampling of the received signal and uses majority decision logic. As illustrated in **Figure 2-9**, each received bit is sampled 6 times at 15.36 MHz clock intervals inside the estimated bit window. The samples obtained are compared against a threshold of 50 % with respect to the signal stored by the peak detector. If at least 4 samples have an amplitude exceeding the 50 % threshold, a logical “1” is considered to be detected; otherwise a logical “0” (no signal) is considered to be detected

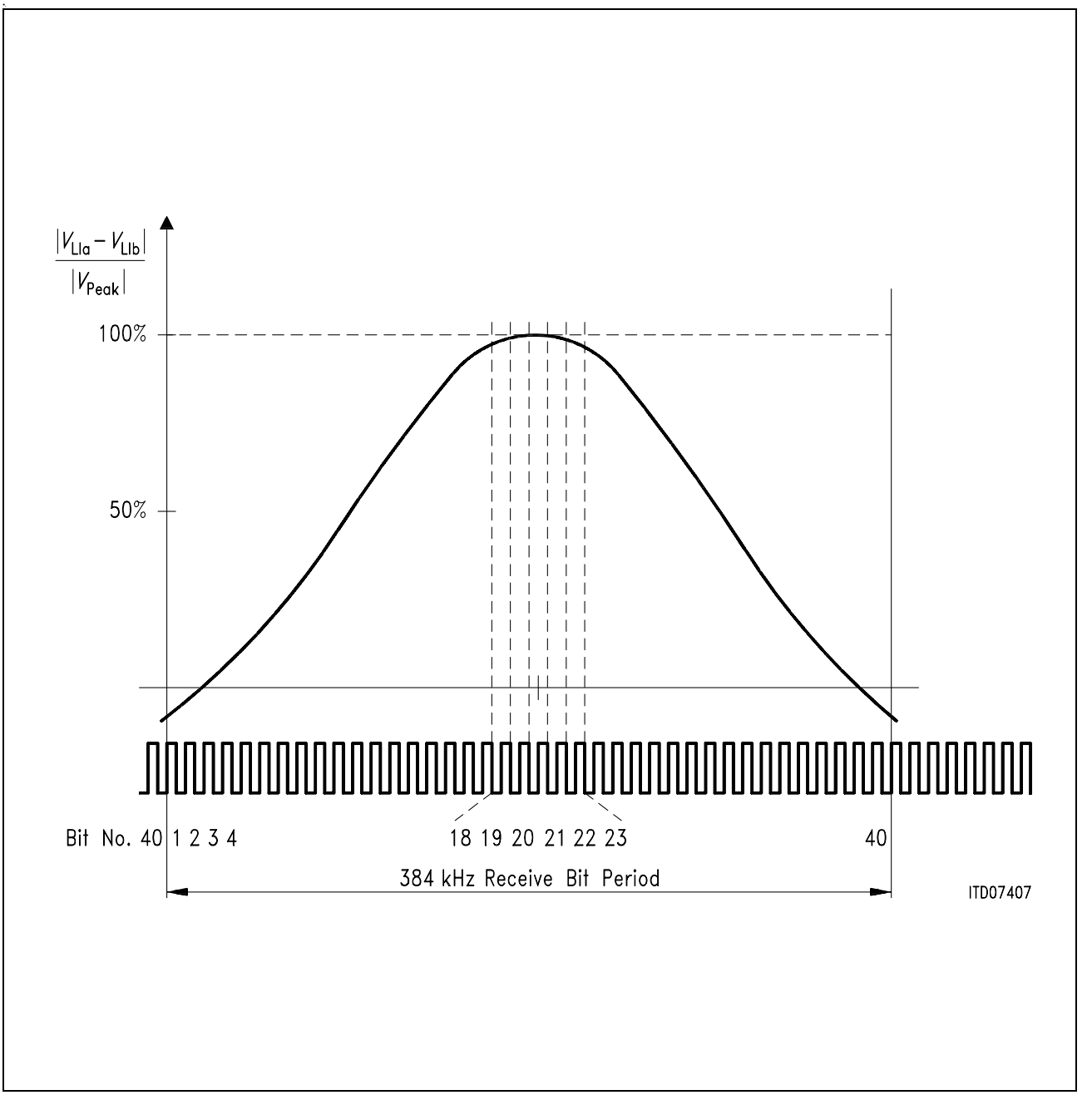


Figure 2-9 U_{PN} Receive Signal Oversampling

2.3.5 Activation / Deactivation

An incorporated finite state machine controls the activation and deactivation procedures and communicates with the layer-2 unit via the IOM-2 C/I channel. Each of the eight C/I channels is allocated to its corresponding line interface.

2.3.6 Diagnostic Functions

Loop 2 is activated over the IOM interface with Activate Request Loop 2 (AR2). The loop will be closed in the TE after detection of the associated bit in the U_{PN} maintenance bit (S-bit).

Loop 1 is activated over the IOM interface with Activate Request Loop 1 (ARL). No U_{PN} line is required. INFO 4 is looped back to the receiver and also sent to the U_{PN} interface. When the receiver is synchronized, the message “AI” is sent in the C/I channel.

3 Operational Description

3.1 General

All procedures required for data transmission over the U_{PN} interface are implemented. These comprise the U_{PN} interface frame and multiframe synchronization, activation/ deactivation procedure, and timing requirements such as bit rate and jitter.

The internal finite state machine of the PEB 2096, OCTAT-P, controls the activation/ deactivation procedures, switching of loops and transmission of special pulse patterns. Such actions can be initiated by signals on the U_{PN} transmission line (INFO's) or by control (C/I) codes sent over the IOM interface. Refer to **Figure 3-8.**

The exchange of control information in the C/I channel is state oriented. This means that a code in the C/I channel is repeated in every IOM frame until a change is necessary. A new code must be found in two consecutive IOM frames to be considered valid (double last look criterion).

The monitor channel is used to convey message oriented information. This means that an information in the monitor channel is transferred once, and the receiver stores that message. In order to ensure safe data transfer, a handshake procedure between monitor channel transmitter and receiver is necessary. An example show **Figure 3-6** and **Figure 3-7**.

For details refer to the IOM-2 Interface Specification, Rev. 2.

3.2 Clocking, Reset and Initialization

At power up, a reset pulse (RST) should be applied to force the line interfaces of the PEB 2096, OCTAT-P, to the state "reset". No clocks are required during that procedure.

The pin $\overline{\text{SSYNC}}$ must be set to V_{DD} if not used.

After that the line interfaces of the PEB 2096, OCTAT-P, may be operated according to the state diagram (**Figure 3-8**), each controlled via the corresponding C/I channel.

3.3 Tristate Capability on IOM-2 Interface

Push-pull configuration is possible also in the modes > 2.048 Mbit/s (> 8 IOM channels). In IOM channels, which are not used by the OCTAT-P, the data upstream direction (DU) line is in high impedance state (tristate)

3.4 Push – Pull Sensing on Pin DU

The OCTAT-P supports configurations where multiple ICs are connected to the IOM-2 interface. If the MODE pin is connected to V_{DD} the OCTAT-P senses after reset whether an external pull-up resistor is connected to pin DU or not. If no resistor is detected the pin DU is changed to push-pull. If a resistor is detected the pin DU is changed to open

drain. The sensing is done within 2 consecutive IOM frames at bit position 15 (last bit of B2 channel).

The pin DU is always push-pull if the MODE pin is connected to V_{SS}.

3.5 Transmit Delay on U_{PN} Interface in respect to IOM®-2 Interface

The OCTAT-P causes delays of B- and on D-channels with respect to the IOM channel number. **Figure 3-1** shows this delay at a data rate of 2.048 Mbit/s.

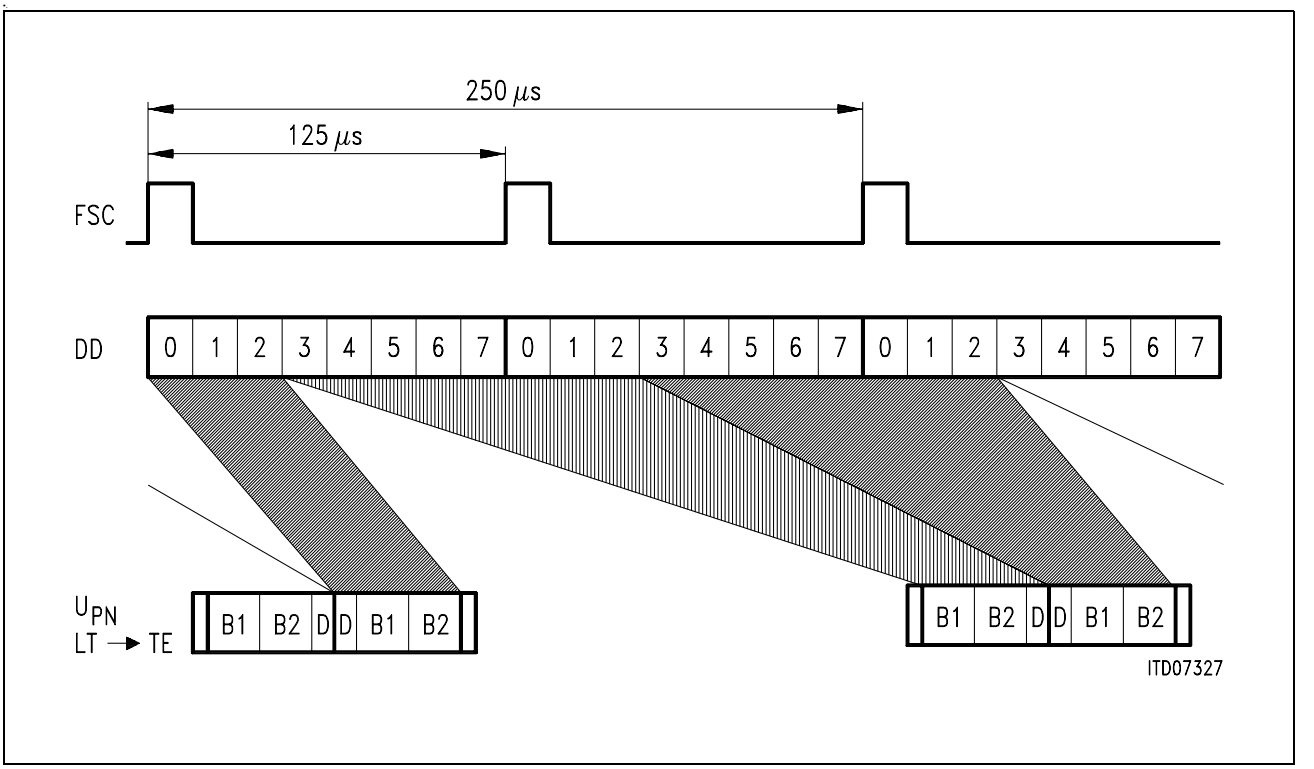


Figure 3-1 Transmit Delay of B- and D-Channels

3.6 U_{PN} Multiframe Synchronization

There are two possibilities how to synchronize the U_{PN} multiframe: With a short FSC or with $\overline{SSYNC}$.

3.6.1 Synchronization with a Short FSC

The short FSC pulse has a width of one DCL clock (in normal use the FSC is at least 2 DCL wide). The $\overline{SSYNC}$ input must be set to 1. The period of the short FSC pulses must be a multiple of 1 ms. The U_{PN} frame with a code violation in the M bit starts in the IOM channel 0 which follows the short FSC pulse. Refer to **Figure 3-2**.

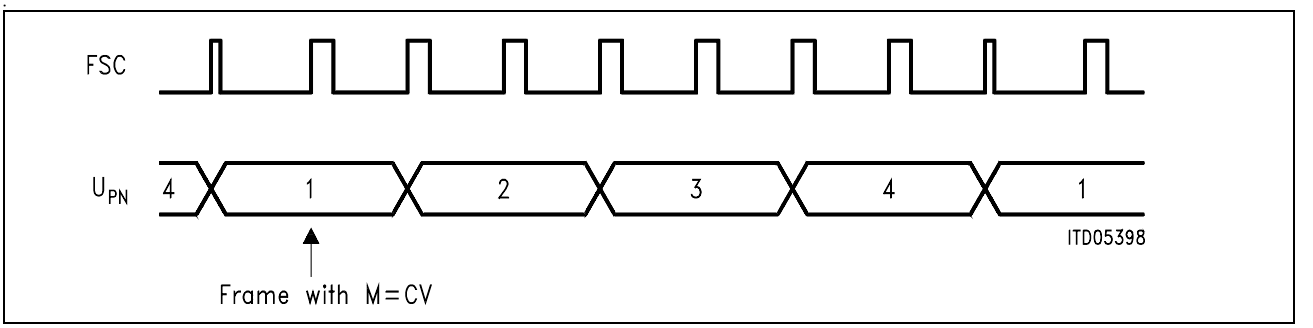


Figure 3-2 Synchronization with a short FSC

3.6.2 Synchronization using $\overline{\text{SSYNC}}$ (for DECT)

A zero pulse on the $\overline{\text{SSYNC}}$ input forces the OCTAT-P to start a multiframe with a code violation in the next M-bit. Refer to **Figure 3-3**.

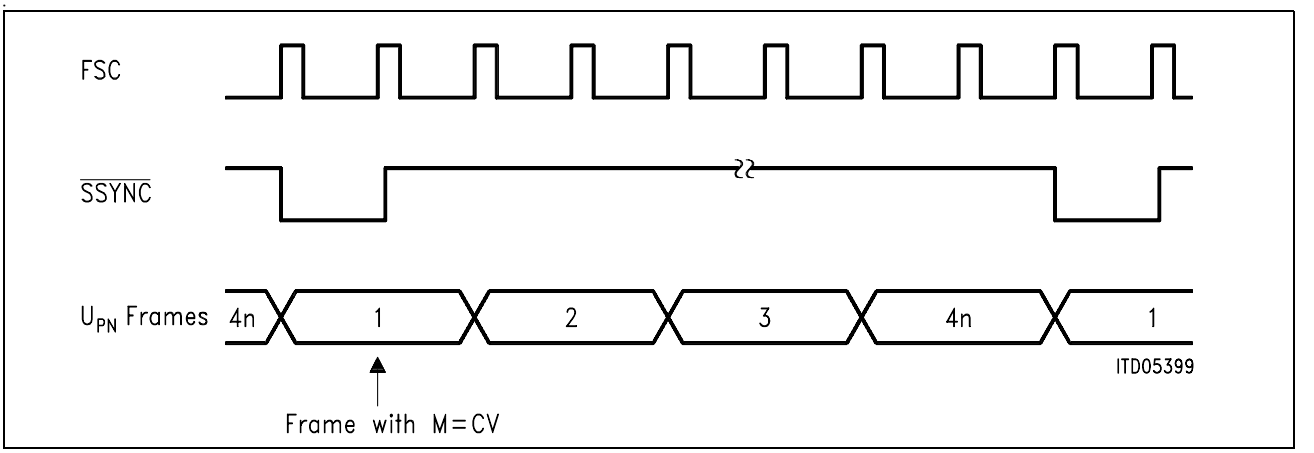


Figure 3-3 Synchronization with $\overline{\text{SSYNC}}$

While using $\overline{\text{SSYNC}}$ for U_{PN} multiframe synchronization the short FSC signal is not allowed. If the bit SYNEN is set (Configuration Register, bit 7) the zero pulse on $\overline{\text{SSYNC}}$ forces the OCTAT-P also to set the T bit to '1' in the next U_{PN} frame. If not used the $\overline{\text{SSYNC}}$ input must be connected to V_{DD}.

Note: Before using $\overline{\text{SSYNC}}$ if the bit SYNEN is set, the T-bit must be set to '0' by the C/I command AI.
n = number of U_{pn} frames.

3.7 D-Channel Handling

Decentralized D-Channel processing can be realized by the use of only one multiplexed HDLC-Controller, which is integrated with a D-channel Arbiter in the ELIC, PEB 20550.

Typically the D-channel load has a very bursty characteristic. Taking this into account, the ELIC provides the capability to multiplex one HDLC-controller among several subscribers. This feature results in a drastical reduction of hardware requirements while maintaining all benefits of HDLC based signaling (**Figure 3-4**).

A D-channel arbiter is used to assign the receive and transmit HDLC-channels independently to the subscriber terminals.

In downstream direction the arbiter links the transmit channel to one or more (broadcast) programmable IOM-2 D-channels (ports).

In upstream direction the arbiter assigns the HDLC-receive channel to a requesting subscriber and indicates to all other subscribers that their D-channels are blocked, using a control channel.

This configuration supports full duplex layer-2 protocols with bus capability e.g. LAPD or proprietary implementations. Consequently no polling overhead is necessary providing the full 16-kbit/s bandwidth of the D-channel for data exchange.

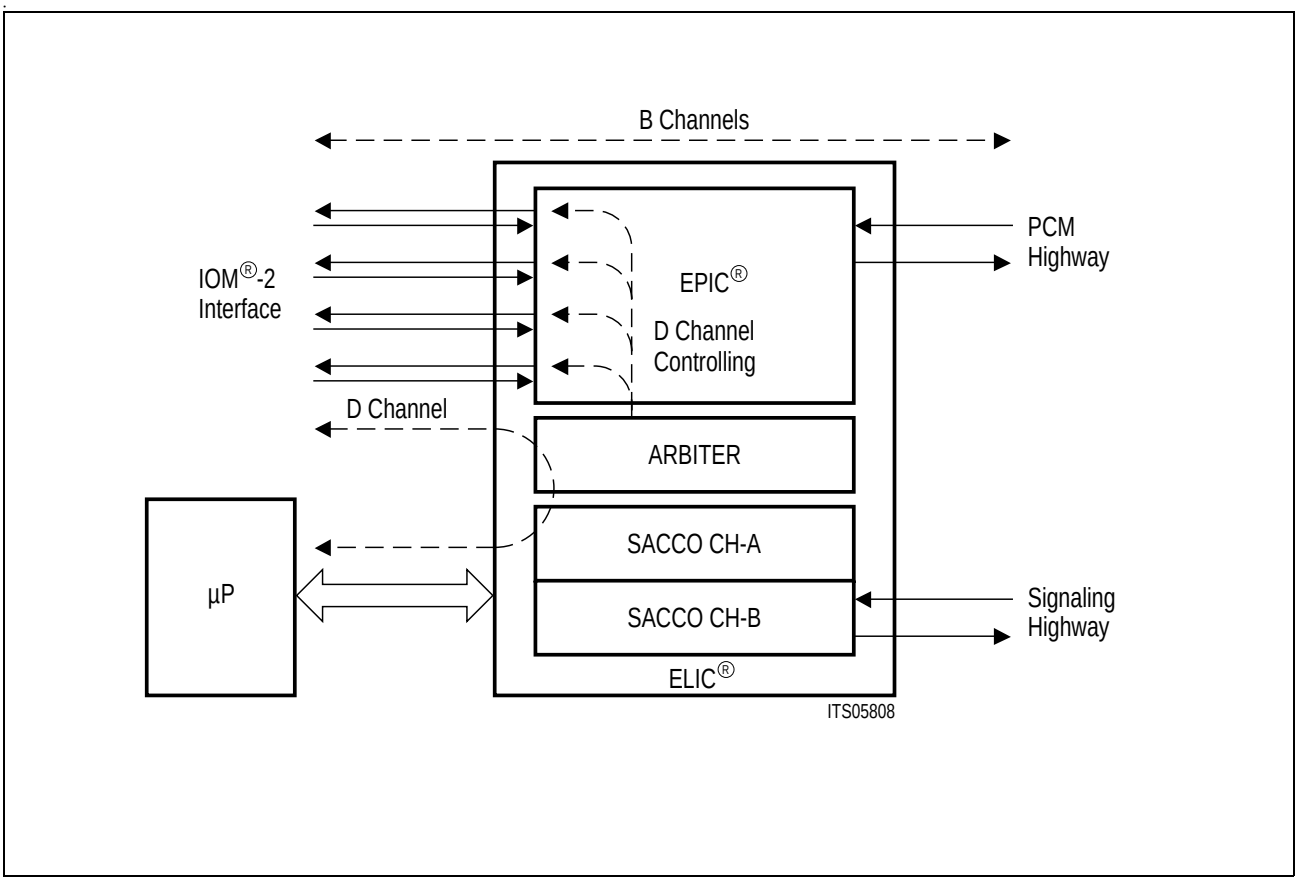


Figure 3-4 D-Channel Handling with only one Multiplexed HDLC-Controller (SACCO-A)

The control channel is unidirectional and forwards the status information of the corresponding D-channel (blocked or available) towards the subscriber terminal.

Different existing channel structures are used to implement the control channel between the HDLC-controllers on the line card and in the subscriber terminal.

Control Channel Implementation on the U_{PN}-Interface

On U_{PN}-line card, the control channel is integrated in the C/I-channel.

The OCTAT-P uses the T-channel to transmit the control channel information to the terminal. The T-channel is a subchannel of the U_{PN}-interface with a bandwidth of 2 kbit/s.

In the subscriber terminal the control channel is included again in the IOM-2 interface.

Depending on the terminal configuration two alternatives can be selected in the terminal transceiver device.

The blocked/available information is translated directly into the S/G-bit (Stop/Go) when no subsequent transceiver circuit is present in the terminal. The S/G-bit is evaluated by the terminal HDLC-controller ICC. It stops data transmission immediately when the S/G-bit is set to 1 (T-Bit=0).

When an additional transceiver device is integrated in the terminal (e.g. an S-adapter, PEB 2081 (SBCX)) the control channel is translated into the A/B-bit. The A/B-bit is monitored by the SBCX. A/B = 1 indicates that the corresponding D-channel is available (A/B = 0 blocked). Depending on this information, the SBCX controls the E-bit on the S-bus and the S/G-bit on the IOM-2 interface. When A/B = 0 the E-bit is forced in the inverted D-bit state, the S/G-bit is set to high. As a result all active transmitters in the terminal and on the S-bus are forced to abandon their messages.

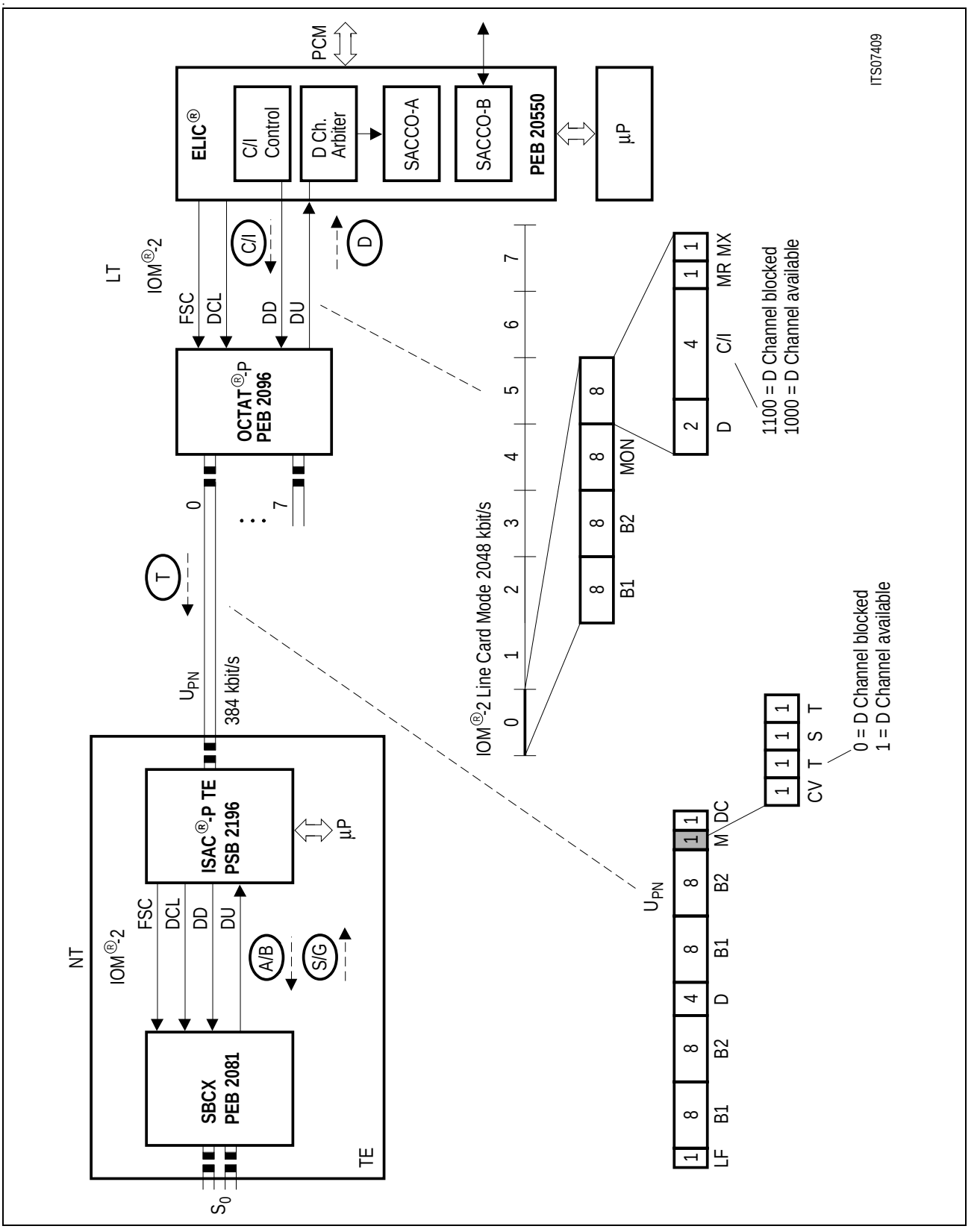


Figure 3-5 Control Channel Implementation with OCTAT®-P (PEB 2096) as Line Card Transceiver and S-Adapter.

3.8 IOM®-2 Interface Monitor Channel

The monitor channel is used to convey message oriented information. This means that an information in the monitor channel is transferred once, and the receiver stores that message. There is a defined handshake procedure between the monitor channel transmitter and the receiver in order to ensure a safe data transfer over the IOM-2 interface.

The OCTAT-P uses the monitor channel of IOM channel 0 for local programming and reading (register access).

The monitor channel operates on an asynchronous basis. While data transfer on the bus takes place synchronized to frame sync, the data flow is controlled by a handshake procedure using the monitor channel receive bit (MR) and the monitor channel transmit bit (MX). For example: data is placed onto the monitor channel and the MX bit is activated (active low). This data will be transmitted repeatedly once per 8 kHz frame until the transfer is acknowledged via the MR bit.

The monitor channel is in an idle condition when the MX bit is inactive in two or more consecutive frames (indication of End Of Message EOM).

Before starting a transmission to the OCTAT-P, the microprocessor should verify that the transmitter of the OCTAT-P is inactive, i.e. that a previous transmission has been terminated.

The OCTAT-P has a monitor transmitter time-out function of minimum 4 ms implemented. This prevents the monitor message to be transmitted continuously if the monitor data won't be acknowledged by the receiver.

An example for a µP, ELIC and OCTAT-P communication is shown in **Figure 3-6** and **Figure 3-7.**

First the Identification Register of the OCTAT-P may be read. Two bytes are transmitted to the OCTAT-P and as a result of the read operation two bytes are returned to the controller. In case of a write operation the data are only acknowledged and no data are returned from the OCTAT-P to the controller.

The first byte of the data transmitted to the OCTAT-P always indicates the type of the desired monitor operation (i.e. read or write to the internal registers).

The example shows the typical register access of the ELIC and gives a feeling about the important bits.

The ELIC uses a 16-byte FIFO for transmission and reception of the monitor data. Therefore the user doesn't need to provide routines for the handshake protocol.

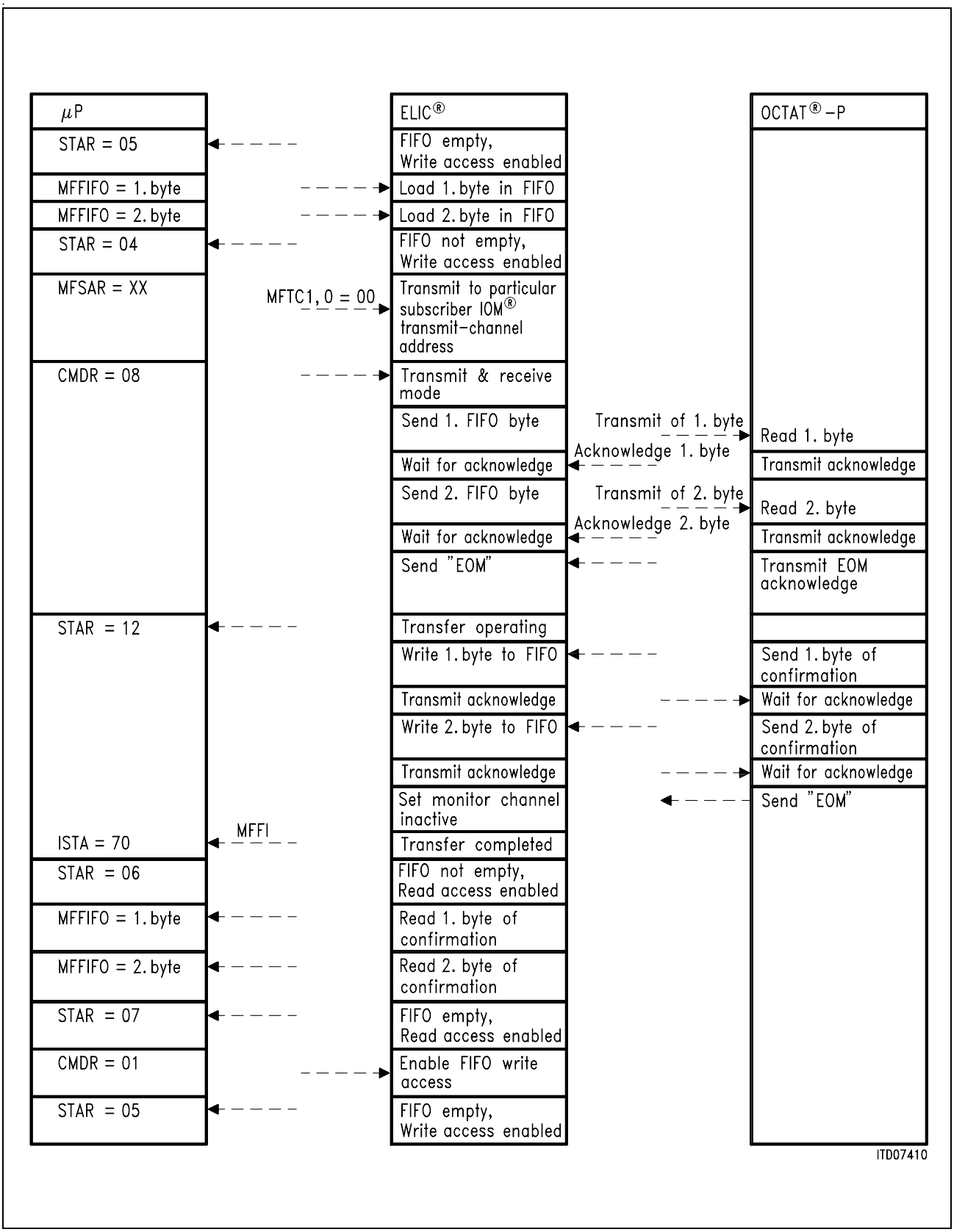


Figure 3-6 Monitor Channel Handling: µP ↔ ELIC ↔ OCTAT-P

A detailed description of the hand-shake procedure using MX and MR bits is shown on **Figure 3-7.**

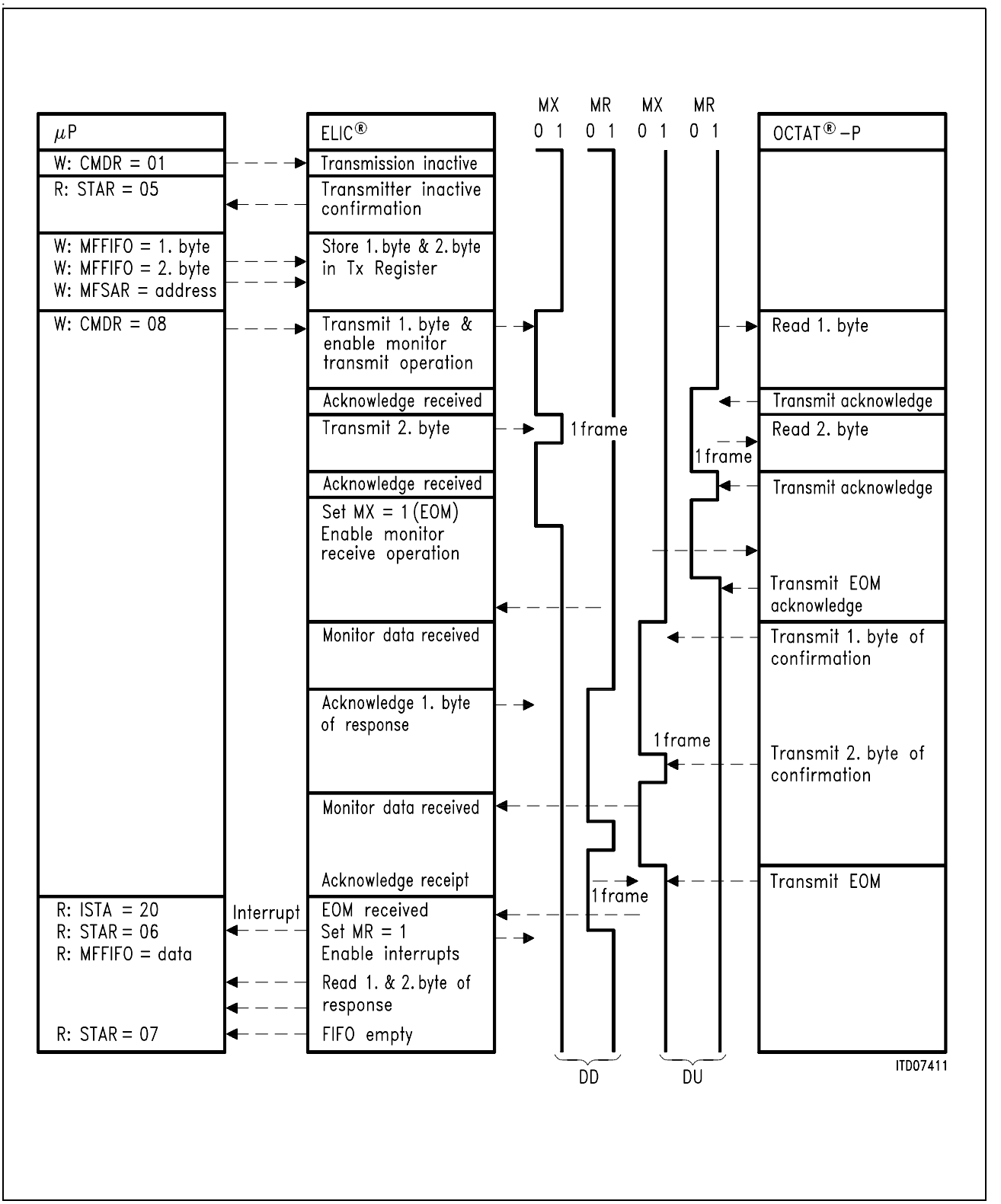


Figure 3-7 Monitor Channel Handling: Hand-shake by the Use of MX and MR Bits

3.9 Command / Indicate Channel

The C/I channel is used for communication between the OCTAT-P and a layer-2 device (or ELIC), to control and monitor layer-1 functions. The layer-2 device monitors the layer-1 indication continuously and indicates a change if a new code is found to be valid in two consecutive IOM frames (double last look criterion).

Table 2
Commands

Command (downstream)	Abbr.	Code	Remarks
Deactivate request	DR	0000	
Reset	RES	0001	
Test mode 2	TM2	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency
Test mode 1	TM1	0011	Transmission of pseudo-ternary pulses at 192 kHz frequency
Activate request = “available“	AR	1000	Transmission of INFO 2 or INFO 4, T bit set to one
Activate request test loop 2	AR2	1010	Transmission of INFO 2, switching of loop 2 (at TE), T bit set to one
Activate request local test loop	ARL	1001	Transmission of INFO 2, switching of loop 1 (on U interface), T bit set to one
Activate indication = “blocked“	AI	1100	Transmission of INFO 4, T bit set to zero
Deactivate confirmation	DC	1111	Deactivation acknowledgment, quiescent state

Table 3
Indications

Indication (upstream)	Abbr.	Code	Remarks
Timing required (to activate IOM-2)	TIM	0000	Deactivated state, activation from the line not possible
Resynchronization (loss of framing)	RSY	0100	Receiver is not synchronous
Activate request	AR	1000	INFO 1w received
U only activation indication	UAI	0111	INFO 1 received synchronous receiver
Activate indication	AI	1100	Layer-1 fully activated
Deactivate indication	DI	1111	INFO 0 or DC received after deactivation request

In PBX applications with decentral D-channel handling, all D-channels can be handled by a D-channel arbiter of the ELIC, PEB 20550; one signalling controller in multiplexer mode (SACCO-A) can be used for up to 32 ISDN subscribers. A terminal is allowed to send data only when the signalling controller is available and the subscriber was selected by the arbiter. The command

C/I = 1000_B indicates to the OCTAT-P that the selected D-channel can be used (is “available“),

C/I = 1100_B indicates that the D-channel currently can not be used as the signalling controller is allocated to an other terminal. The addressed D-channel is “blocked“.

The OCTAT-P controls the terminal transmitter (e.g. ISAC-P TE) accordingly. It translates the information whether the D-channel is “available” or “blocked” by setting the T-bit on the U_{PN} interface.

T = 1 indicates to the terminal (via the U_{PN} transmitter) that its HDLC controller can send data.

T = 0 indicates that the HDLC controller can not send data or has to abort sending data.

Note: The two codes (C/I = 1000_B and 1100_B) can only be used when the OCTAT-P is in a state INFO 4 transmission.

3.10 Activation and Deactivation, State Machine

The activation and deactivation implemented in the PEB 2096, OCTAT-P, agree with the U_{P0} interface as implemented in the PEB 2095, IBC.

3.10.1 States Description

OCTAT-P state machine enters two different kind of states:

Unconditional and conditional states, **Figure 3-8.**

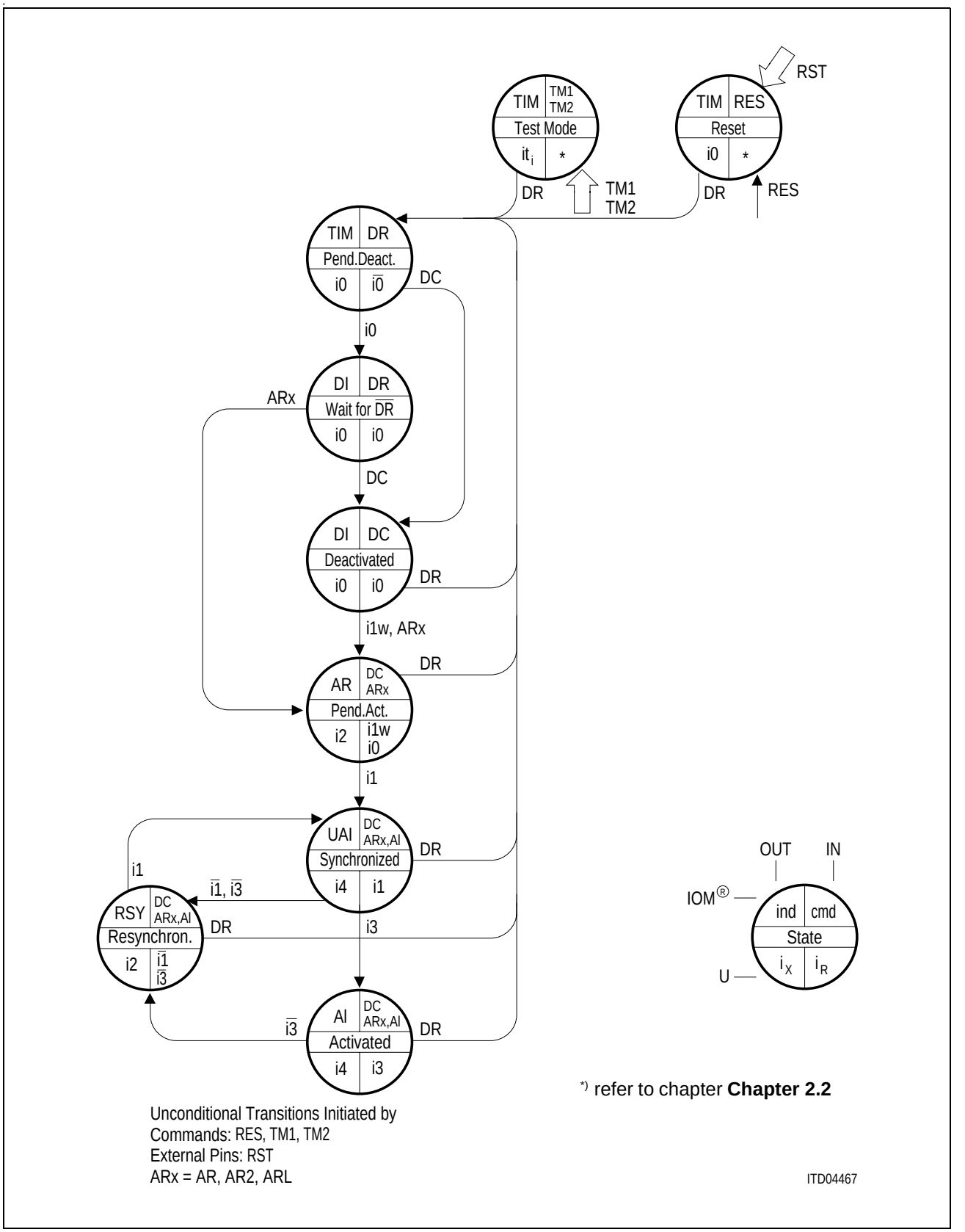


Figure 3-8 OCTAT-P State Diagram

Unconditional States

Reset

This state is entered unconditionally after a high appears on the RST pin or after the receipt of command RES (software reset). The analog section is disabled (transmission of INFO 0) and the U_{PN} interface awake detector is inactive. Hence, activation from PT or TE is not possible.

Test Mode

The test signal (it_i), sent to the U_{PN} interface in this state is dependant on the command which originally invoked the state. TM2 causes single alternating pulses to be transmitted (it_2); TM1 causes continuous alternating pulses to be transmitted (it_1). The burst mode technique normally employed on the U interface is suspended in this state and the test signals are transmitted continuously.

Pending Deactivation

To access any of the conditional states from any of the above unconditional states the pending deactivation state must be entered. This occurs after the receipt of a DR command. In this state the awake detector is activated and the state is exited only when the line has settled (i.e. INFO 0 has been detected for 2 ms) or by the command DC.

Note: Although DR is shown as a normal command it can in fact be seen as an unconditional command. No matter which state the LT is in, the reception of a DR command will always result in the pending deactivation state being entered.

Conditional States

Wait for $\overline{\text{DR}}$

This state is entered from the pending deactivation state once INFO 0 or DC has been identified. From here the line may be either activated, deactivated or a test loop may be entered.

Deactivated

This is the power down state of the physical protocol. The awake detection is active and the device will respond to an INFO 1w (wake signal) by initiating activation.

Pending Activation

This state results from a request for activation of the line, either from the terminal (INFO 1w) or from the layer-2 device (AR, AR2 or ARL). INFO 2 is then transmitted and the OCTAT-P waits for the responding INFO 1 from the remote device.

Synchronized

Upon receipt of INFO 1 the OCTAT-P must synchronize itself to the signal. This process takes at most 10 ms.

Activated

INFO 1 has a code violation in the framing bit (F bit) with respect to the last received bit whereas INFO 3 has none. Upon the receipt of 2 frames without a code violation in the F bit, the OCTAT-P enters the activated state and outputs INFO 4. The line is now activated; the OCTAT-P sends INFO 4 to the remote, the remote sends INFO 3 to the OCTAT-P.

Resynchronization

If the OCTAT-P fails to recognize INFO 3, for whatever reason, it will attempt to resynchronize. Entering this state it will output INFO 2. This is similar to the original synchronization procedure in the pending activation state (the indication given to layer 2 is different). However as before, recognition of INFO 1 leads to the synchronized state.

OCTAT-P state diagram is shown in **Figure 3-8**.

3.10.2 Info Structure on the U_{PN} Interface

Signals controlling and indicating the internal state of all U_{PN} transceiver state machines are called INFOs. Four different INFOs (INFO 0, 1W, 1/2 and 3/4) can be sent over the U_{PN} interface depending on the actual state (Synchronized, Activated, Pending Activation, Test Mode, Deactivated, Reset,...) of the connected transceivers (e.g. OCTAT-P and ISAC-P TE). When the line is deactivated INFO 0 is exchanged by the U_{PN} transceivers at either end of the line. Info 0 indicates that there is no signal on the line; in either direction.

When the line is activated INFO 3 (in upstream direction) and INFO 4 (in downstream direction) are continually sent. INFO 3 and 4 contain the transmitted data (B1, B2, D, M).

INFO 1w and 1/2 are used for initialization and tests. The form of all INFO is shown in the following table:

Name	Direction	Description
INFO 0	Upstream Downstream	No signal on the line
INFO 1W	Upstream	Asynchronous wake signal 2 kHz burst rate F0001000100010001000101010100010111111 Code violation in the framing bit (F)
INFO 1	Upstream	4 kHz burst rate F0001000100010001000101010100010111111M[1]DC[2] Code violation in the framing bit with respect to the last received ’1’
INFO 2	Downstream	4 kHz burst rate F0001000100010001000101010100010111111M[1] Code violation in the framing bit with respect to the last transmitted ’1’
INFO 3	Upstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC bit[2] optional
INFO 4	Downstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC bit[2]) optional

Note: [1] The M channel superframe contains:
CV code violation [1 kbit/s (once in every fourth frame)]
S bits transparent [1 kbit/s channel]
T bits set to one [2 kbit/s channel]
[2] DC balancing bit
F = Framing bit

3.10.3 Example of Activation and Deactivation

An activation and deactivation procedure between an OCTAT-P and an IBC or ISAC-P TE in TE mode over the U_{PN} interface line is shown in **Figure 3-3**. It illustrates how the state machines of the respective modes interwork to facilitate activation and deactivation. In this case activation was initiated by an AR request at the terminal side and deactivation by a DR command at the LT side. Activation could also be initialized at the LT side using an AR request.

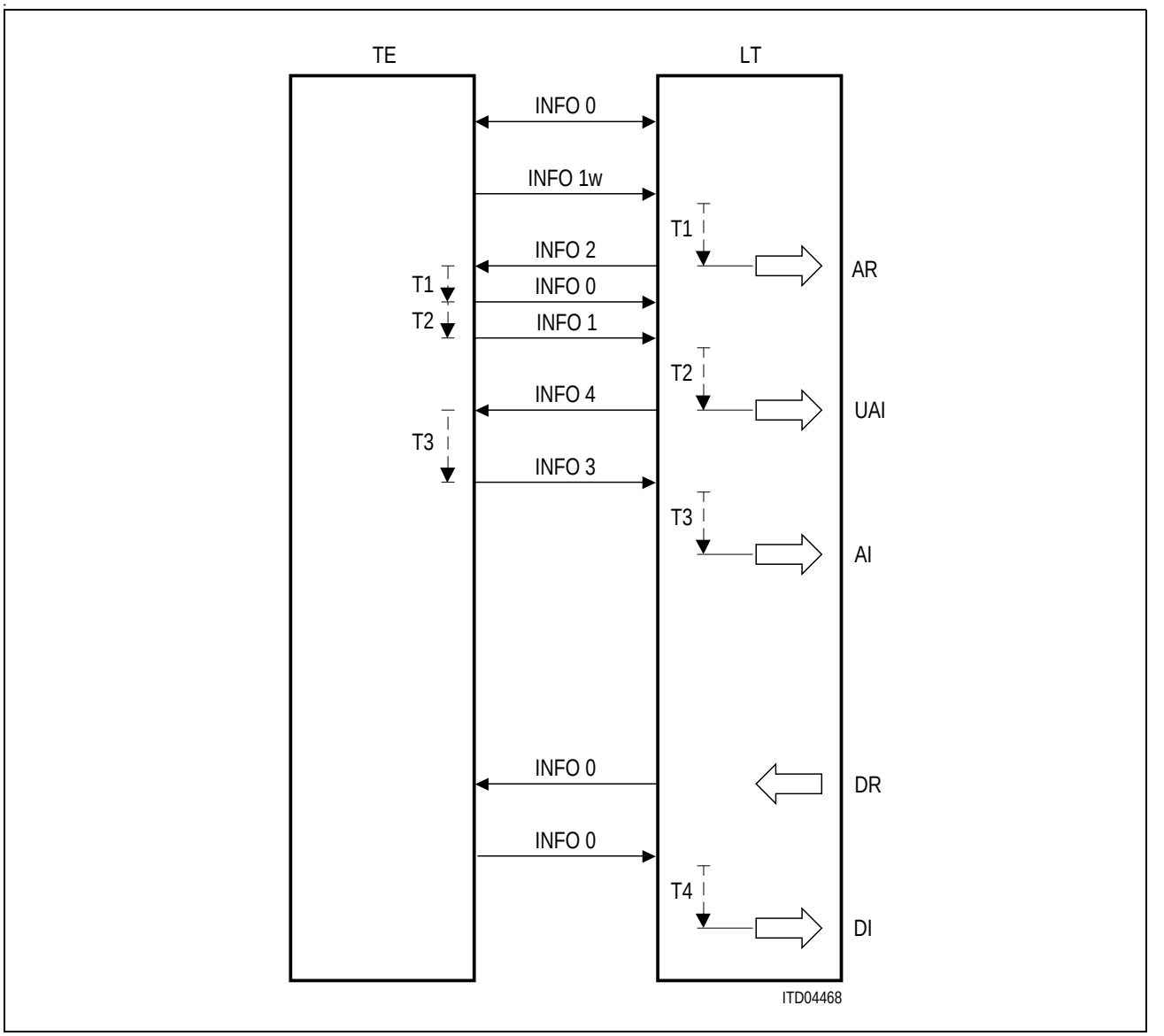


Figure 3-9 Example for an ISAC®-P TE <---> OCTAT-P Activation and Deactivation

Note: T1: < 250 µs time for error free level detection
T2: < 10 ms time for synchronization
T3: ≤ 1 ms four subsequent bursts with no CV in F bit
T4: ≤ 2 ms time for error free detection of INFO 0

4 Registers Description

The monitor channel is used for programming local functions.
It is implemented in OCTAT-P IOM channel 0 only.

Accesses to the registers are treated as local functions and therefore are marked with the code “1000” in the first four bits of the message:

Monitor message:

Code = 1 0 0 0	Internal address	D7 D6 D5 D4	D3 D2 D1 D0

Register Read

An internal register is read by setting the internal address to zero (0_H) and indicating the address of the specific register in the bits D(3:0). The bits D(7:4) are set to zero.

E.g. “80_H 01_H” is the read command for the register 1_H, the General Configuration Register.

Code = 1 0 0 0	0 0 0 0	0 0 0 0	register addr.= 01H

The response message from OCTAT-P comprises two bytes, the first showing the address after the local-function-code, the second showing the register data.

E.g. “81_H (D7:0)” is the response to a read command on address 1_H, where D(7:0) is the content of the Configuration Register.

Code = 1 0 0 0	register addr. = 01H	D7 D6 D5 D4	D3 D2 D1 D0

Register Write

An internal register is written by setting the internal address to the address of the specific register. The register will then be loaded with the value of D(7:0),
e.g. “81_H $5D_H$” programs the Configuration Register (addr. 1_H) with the value $5D_H$.

Code = 1 0 0 0	register addr.	0 1 0 1	1 1 0 1

*Note: Hardware Reset or a corrupt IOM frame (refer to **Chapter 2.2.2**) leads to the initial value of all writable registers.*

4.1 Identification Register – (Read)

Address: 0_H

Value: 0 0 0 0 0 1 0 0 = 04_H

Description: The value of this register is specific for the PEB 2096, OCTAT-P.

4.2 General Configuration Register – (Write)

Address: 1_H

Format:

bit 7							bit 0
IC7D	IC6D	IC5D	IC4D	IC3D	IC2D	IC1D	BEM

Initial Value: FF_H if the MODE pin is connected to V_{DD} or
01_H if the MODE pin is connected to V_{SS}

Description:

ICnD: IOM interface channel n disable (channel 1-7)
0...IOM channel n is enabled
1...IOM channel n is tristated

BEM: Bit error mask
0...whenever the Bit Error Register value is unequal to zero, the register value is transmitted via the monitor channel
1...the Bit Error Register may be read, but there are no unsolicited monitor messages

4.3 Bit Error Register – (Read)

Address: 1_H

Format:

bit 7							bit 0
BEO7	BEO6	BEO5	BEO4	BEO3	BEO2	BEO1	BEO0

Initial Value: 00_H

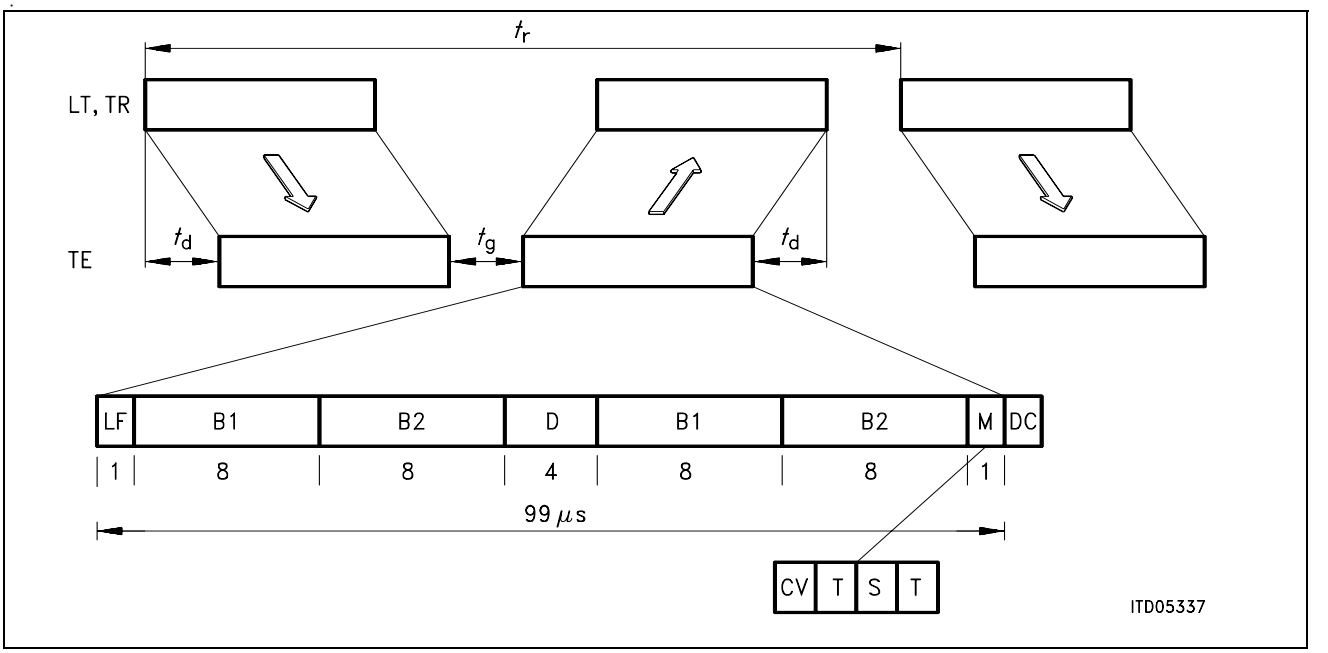
Description: **BEOn** = 1: Bit error occurred on U_{PN} line n.
The Bit Error Register is reset after reading the register

4.4 Test Registers – (Read/Write)

Test registers are implemented in the address range of 8_H to B_H; they are not for customer use.

4.5 Line Delay Measurement of the U_{PN} Interface

The delay of each U_{PN} interface cable can be measured by one 8-bit counter with a programmable resolution of 65 ns or 130 ns. The line delay time t_d can be measured in the range up to 16.57 µsec with the resolution of 65 ns and
33.15 µsec with the resolution of 130 ns.



The access to the delay measurement control logic is done via the IOM-2 monitor channel of IOM-Channel 0.

Configuration Register for U_{PN} Line Interfaces - (Write)

Address: 2_H
Format:

bit7							bit0
SYNEN	BALEN	EQUDIS	TOD	**DSEL2**	**DSEL1**	**DSEL0**	**RESOL**

Initial Value: 00_H if the MODE pin is connected to V_{DD} or
20_H if the MODE pin is connected to V_{SS}

Description: **DSEL(2:0):** Selects the U_{PN} Line Interface of which the delay measurement is executed
0_H: U_{PN} Transceiver No. 0 is selected
1_H: U_{PN} Transceiver No. 1 is selected
2_H: U_{PN} Transceiver No. 2 is selected
3_H: U_{PN} Transceiver No. 3 is selected

4_H: U_{PN} Transceiver No. 4 is selected
5_H: U_{PN} Transceiver No. 5 is selected
6_H: U_{PN} Transceiver No. 6 is selected
7_H: U_{PN} Transceiver No. 7 is selected

RESOL: Resolution of the delay counter for the U_{PN} Interface
0: Resolution of 65 ns
1: Resolution of 130 ns

TOD: Time Out Disable
0: Enable (after reset)
1: Disable

Delay Register for U_{PN} Line Interfaces - (Read)

Address: 2_H
Format:

bit7							bit0
DELAY7	DELAY6	DELAY5	DELAY4	DELAY3	DELAY2	DELAY1	DELAY0

Initial Value: 00_H

DELAY(7:0): Measured delay between U_{PN} transmit and receive frame with a programmed resolution of 65 ns or 130 ns.
The measured value indicates the delay between the transmitted M bit and the received LF bit minus two bits (the guard time).
In order to evaluate the delay in one direction the measured delay is divided by two.
After hardware reset, the line delay of transceiver No. 0 is measured with a resolution of 1 oscillator period. The delay is measured only if the selected channel is in the state "Activated". The measured delay is valid if at least 2 U_{PN} frames have been received in the state "Activated". If the selcted transceiver No. was changed by programming the Configuration Register for U_{PN} Line Interfaces with a new value the new delay is also valid after the receiption of at least 2 U_{PN} frames.
The transmitter and receiver delays of OCTAT-P analog path are included in the delay measurement.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under voltage conditions) is given as a function of the width of a rectangular input current pulse.

For the destruction current limits refer to **Figure 5-1**.

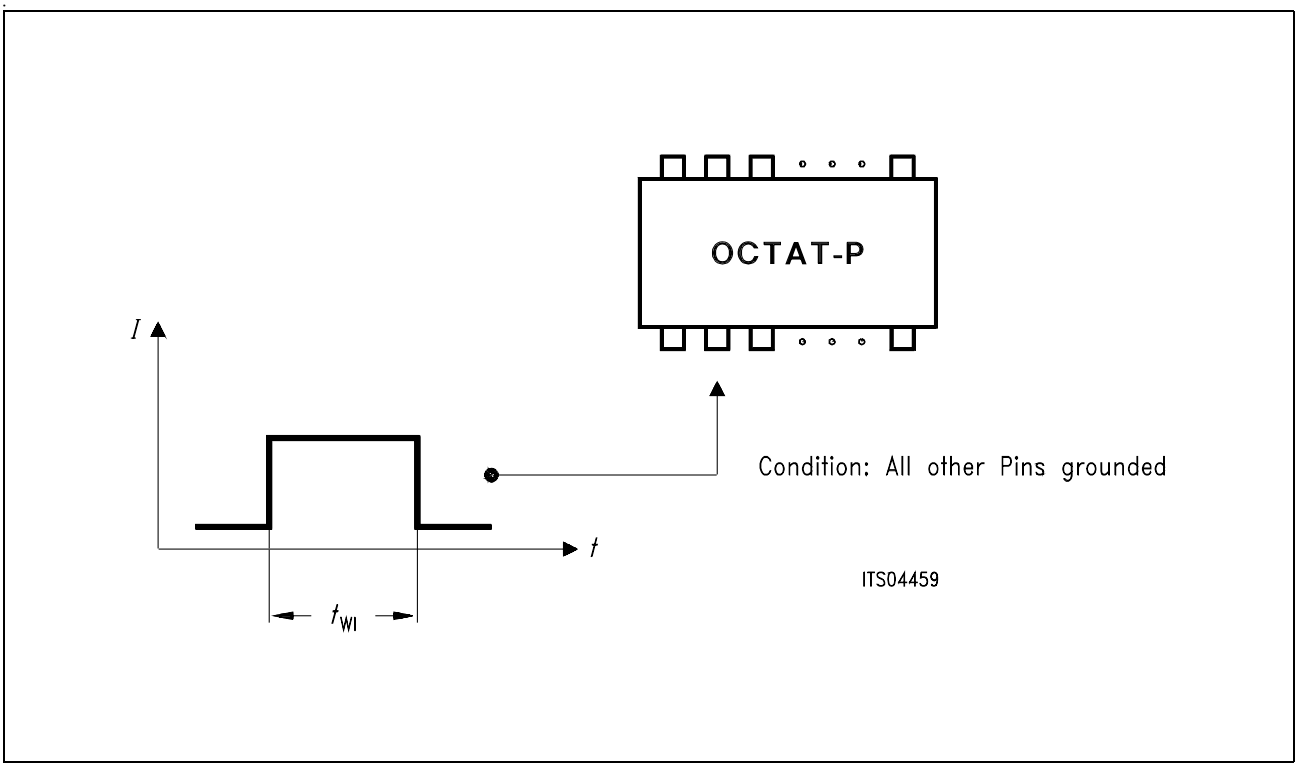


Figure 5-1

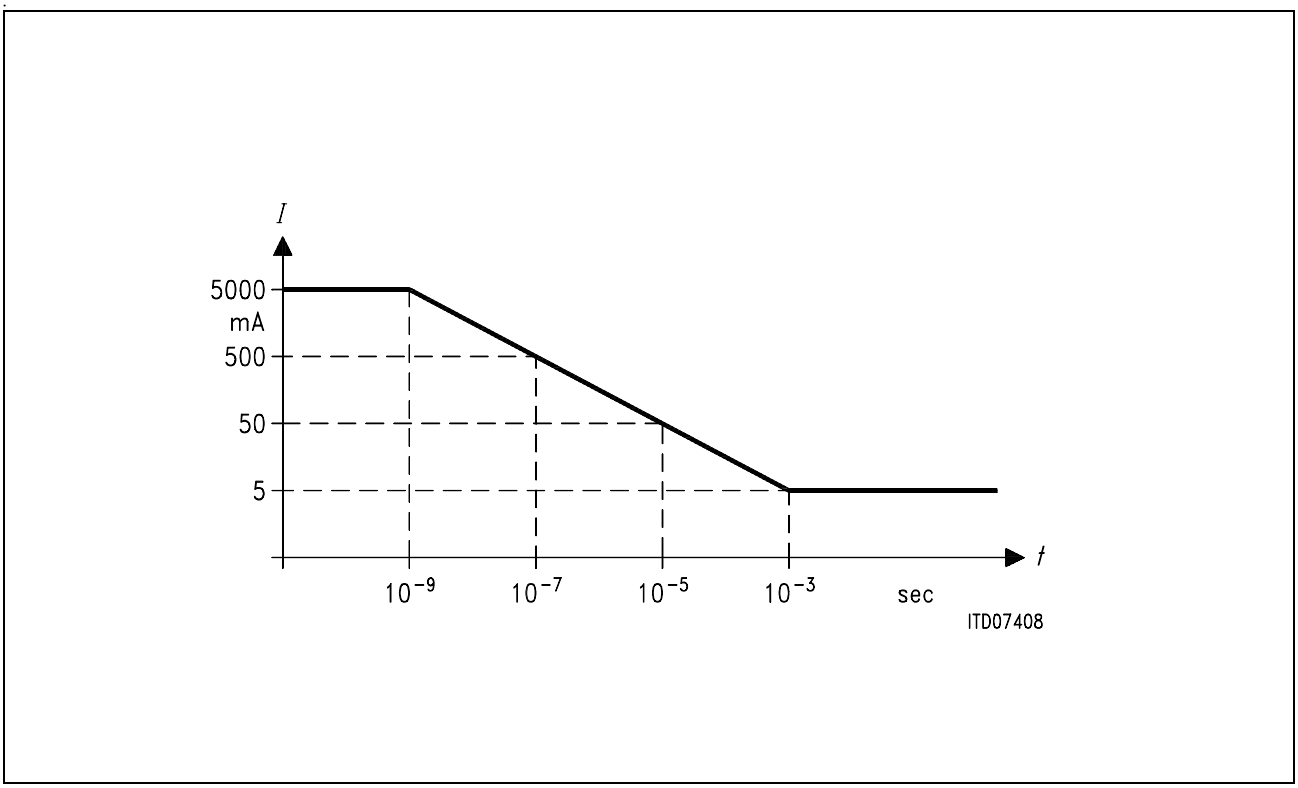


Figure 5-2 Maximum Line Input Current

5.2 DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V
All pins except LIna,b; XTAL1, 2

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.4	+ 1.5	V	
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage	V_{OL} V_{OL1}		0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA (DU only)
H-output voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA
H-output voltage	V_{OH}	V_{DD} – 0.5		V	I_{OH} = – 100 µA
Input leakage current	I_{LI} I_{LO}		± 1	µA	0 V ≤ V_{IN} ≤ V_{DD} 0 V ≤ V_{OUT} ≤ V_{DD} All pins except: LIna, b; XTAL1,2; TDI; TMS
TDI; TMS					

5.2 DC Characteristics (cont'd)

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V
All pins except LIna,b; XTAL1, 2

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input leakage current high	I_{LIH}		1	µA	$V_{IN} = V_{DD}$
Input leakage current low	I_{LIL}	50	400	µA	V_{IN} = 0 V; internal pull-up resistor
LIna, b					
Operational supply current	I_{CC}		50 + n × 2.8	mA	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, transformer ratio 2:1 n = number of line interfaces activated, no output load at CLK, DU
Transmitter output impedance		7	30	Ω	I_{OUT} = 20 mA V_{DD} = 5 V
Receiver input impedance	Z_R	10		kΩ	V_{DD} = 5 V; transmitter stage inactive
XTAL1					
H-input voltage	V_{IH}	3.5	V_{DD} + 0.4	V	
L-input voltage	V_{IL}	– 0.4	1.5	V	
XTAL2					
H-output voltage	V_{OH}	V_{DD} – 0.5		V	I_{OH} = 100 µA, $C_{LD} \leq$ 60 pF
L-output voltage	V_{OL}		0.45	V	I_{OL} = 100 µA, $C_{LD} \leq$ 60 pF

5.3 Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V
All pins except LIna, b

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pin capacitance	$C_{I/O}$		7	pF	

LIna,b

Output capacitance against V_{SS}	C_{OUT}		10	pF	

XTAL1, 2 Recommended typical crystal parameters. Refer to **Figure 3-5.**

Motional capacitance	C_1	20		fF	
Shunt	C_0	7		pF	
Load	C_L	≤ 30		pF	
Resonance resistor	R_r	≤ 65		Ω	

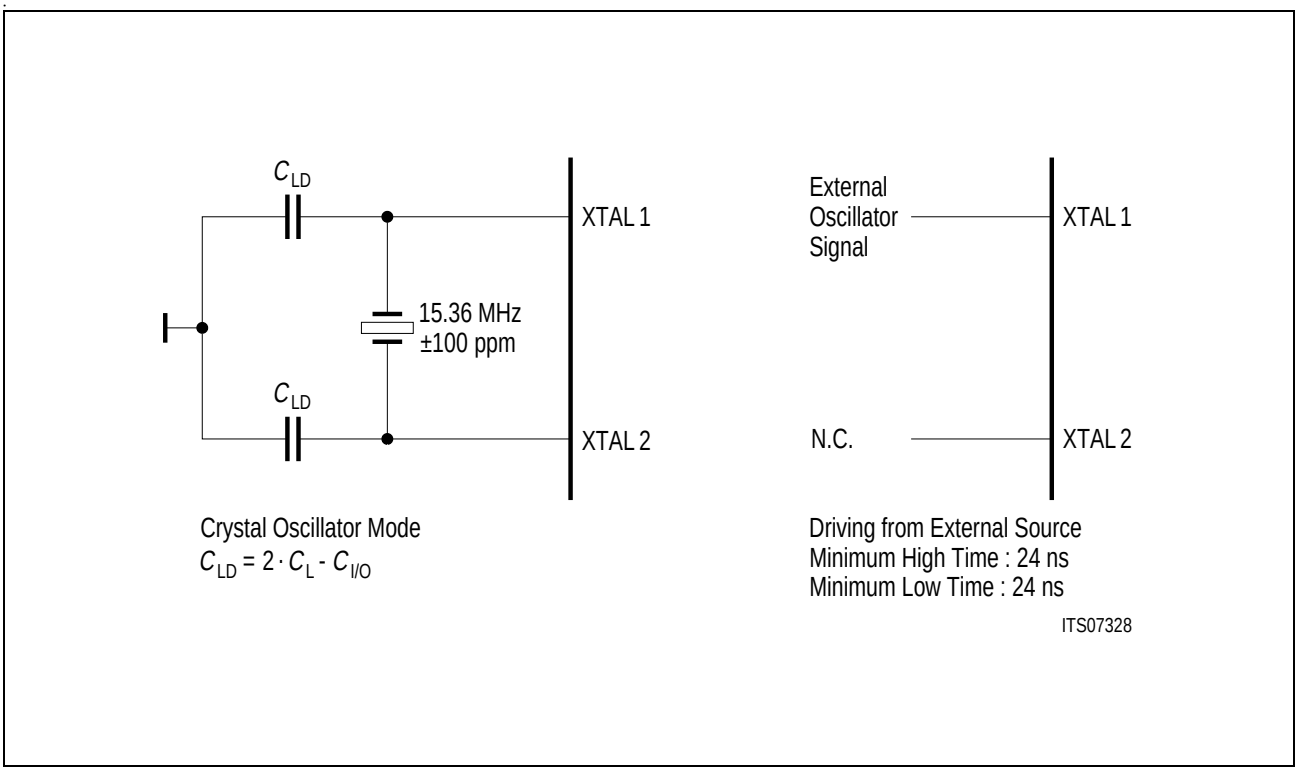


Figure 5-3 Recommended Oscillator Circuits

5.4 AC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %

AC testing: Inputs except XTAL1 are driven at 2.4 V for a logic “1” and at 0.4 V for a logic “0”.

XTAL1 is driven at V_{DD} – 0.5 V for a logic “1” and 0.5 V for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and at 0.8 V for a logic “0”.

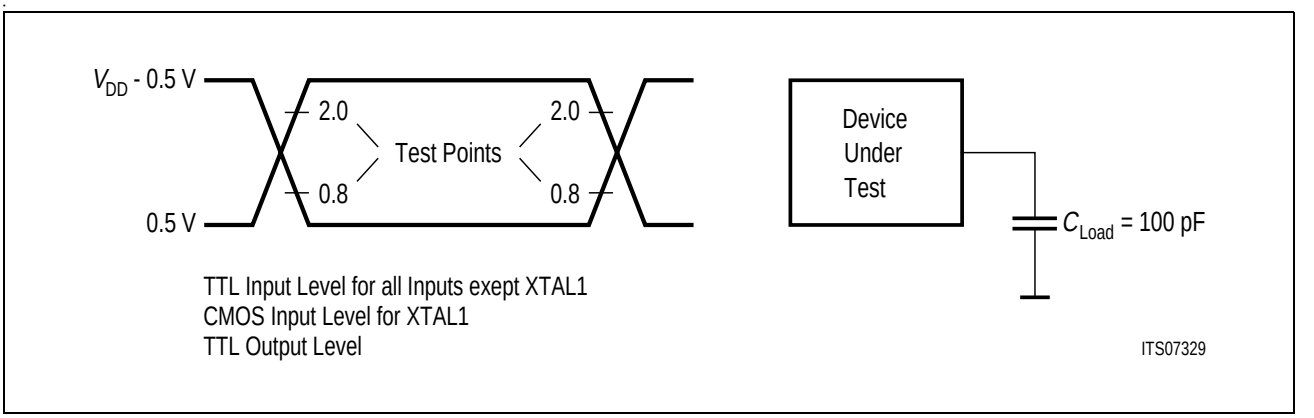


Figure 5-4

Jitter

The clock input FSC is used as reference clock to provide the 768 kHz clock for the U_{PN} interface. In the case of a plesiochronous 15.36 MHz clock generated by an oscillator with a maximum frequency deviation of ± 100 ppm, the clock FSC should have a jitter of less than 20 ns peak-to-peak, as the PLL manages max. 0.5 oscillator period (32.5 ns) in one IOM frame (in 125 µs).

5.5 Clocks

CLK1

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High phase of crystal/clock	t_{WH}	25		ns	50 pF load capacitance at CLK
Low phase of crystal/clock	t_{WL}	25		ns	50 pF load capacitance at CLK
Clock period	T_P	65.08	65.12	ns	

CLK2

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High phase of crystal/clock	t_{WH}	57		ns	50 pF load capacitance at CLK
Low phase of crystal/clock	t_{WL}	57		ns	50 pF load capacitance at CLK
Clock period	T_P	130.16	130.24	ns	

CLK2 is directly derived from the oscillator clock and can drive up to 6 oscillator inputs of the ISAC-S, PEB 2085.

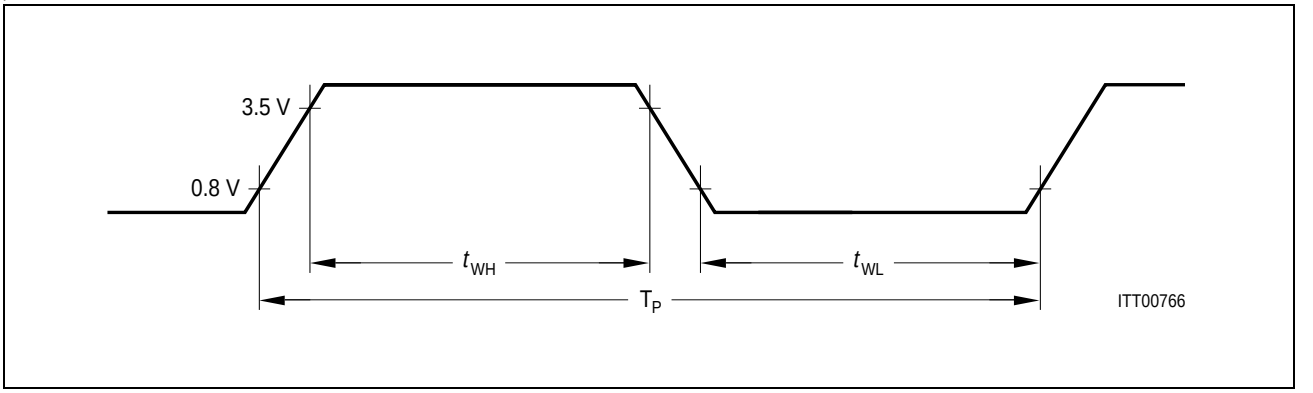


Figure 5-5 Definition of Clock Period and Width

5.6 Timing of the IOM® Interface

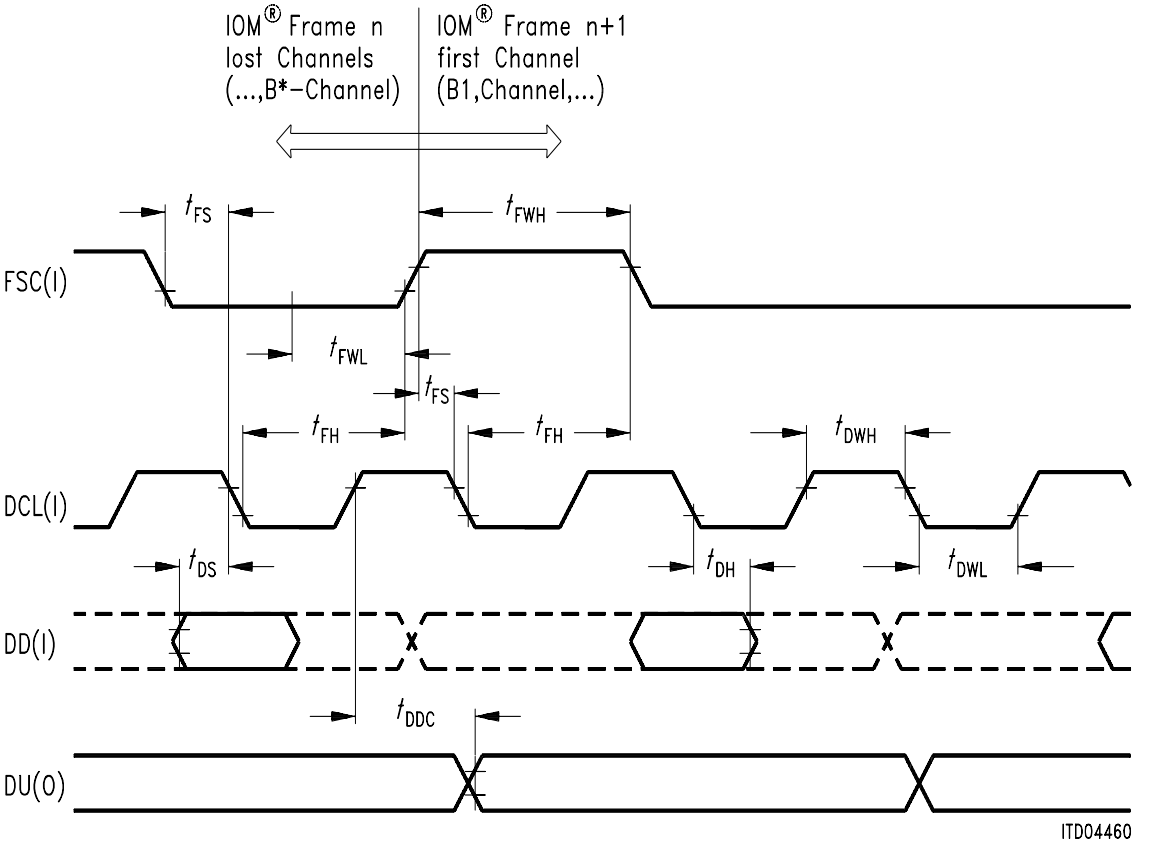


Figure 5-6 IOM® Interface Timing with Double Data Rate DCL

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync. hold	t_{FH}	30		ns
Frame sync. setup	t_{FS}	70		ns
Frame sync. high	t_{FWH}	130		ns
Frame sync. low	t_{FWL}	T_{DCL}		
Data delay to clock	t_{DDC}		100	ns
Data setup	t_{DS}	20		ns
Data hold	t_{DH}	50		ns
Superframe sync. setup	t_{SSYS}	200		ns
Superframe sync. hold	t_{SSYH}	200		ns
Data clock high	t_{DWH}	50		ns
Data clock low	t_{DWL}	50		ns

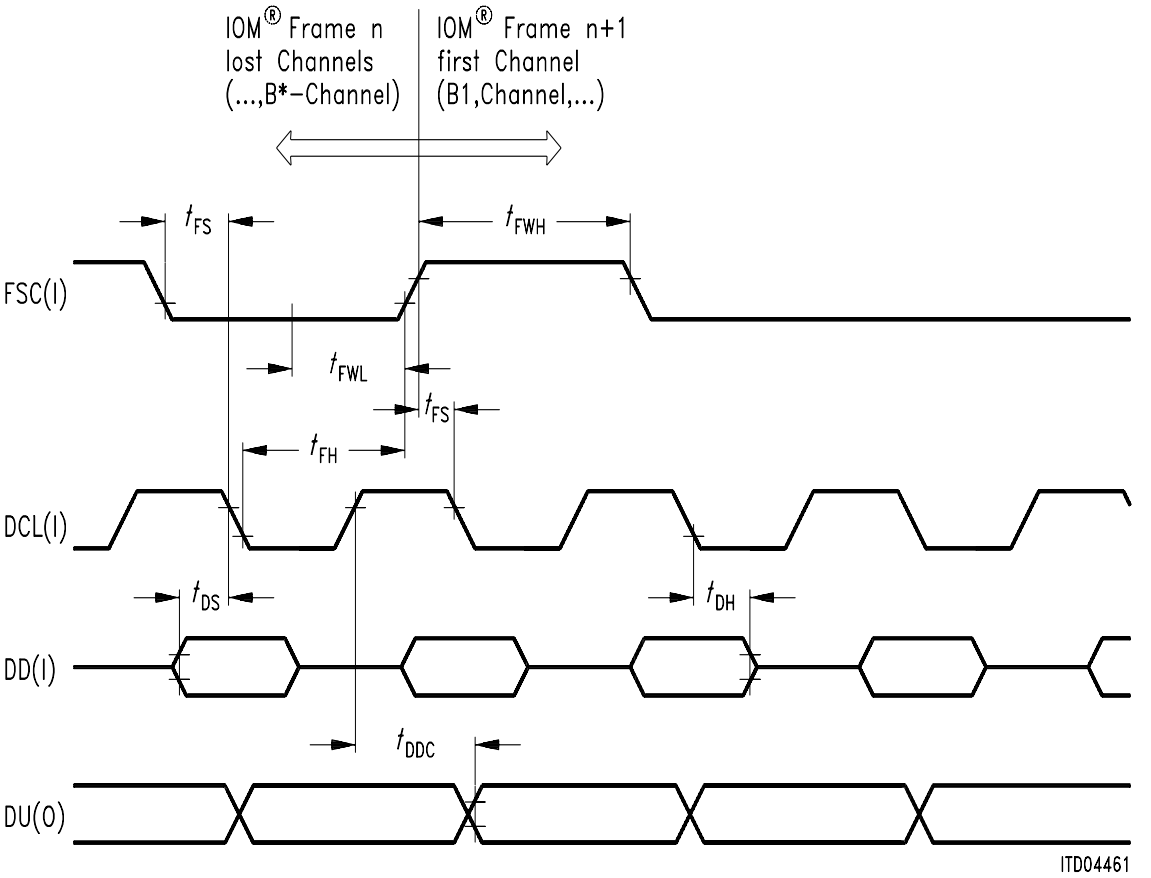


Figure 5-7 IOM®-2 Interface Timing with Single Data Rate DCL

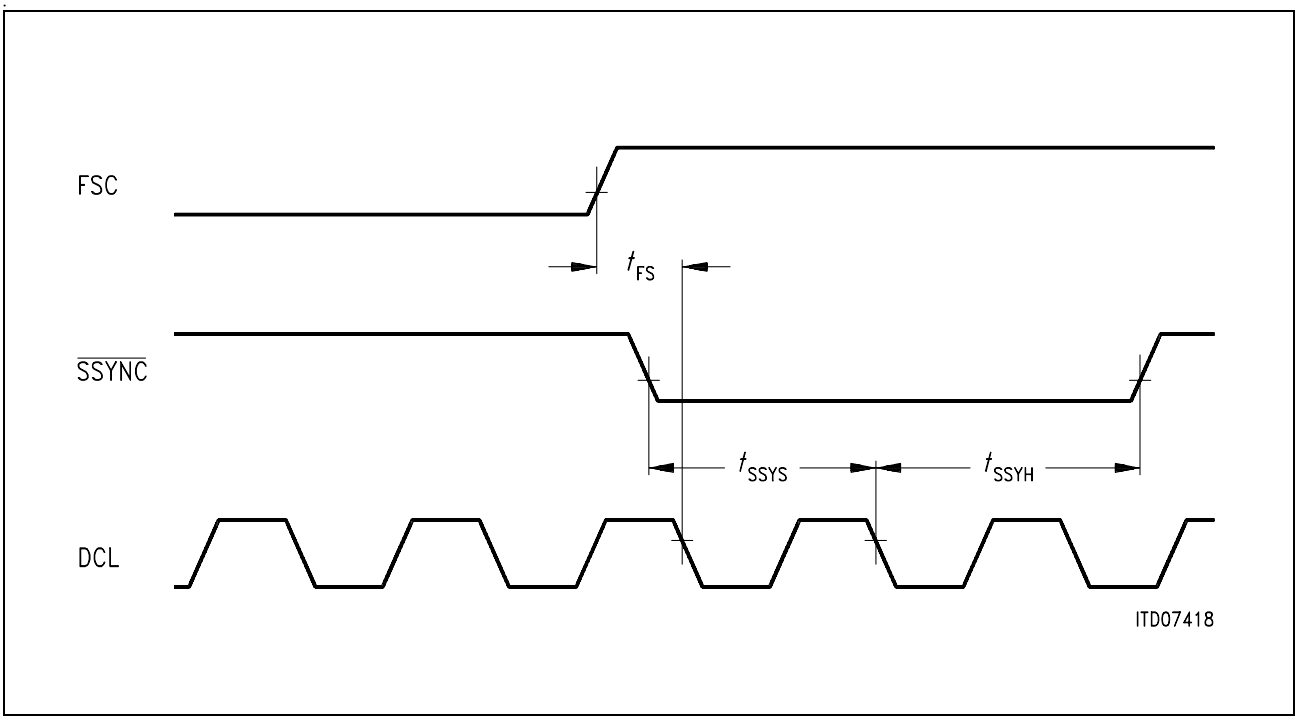


Figure 5-8 $\overline{\text{SSYNC}}$ Timing

Note: A low at $\overline{SSYNC}$ input sets the U_{PN} superframe and forces the next transmitted T-bit to high if SYNEN is programmed to high.

5.7 Boundary Scan Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Test clock period	t_{TCP}	160		ns
Test clock period low	t_{TCPL}	80		ns
Test clock period high	t_{TCPH}	80		ns
TMS setup time to TCK	t_{MSS}	30		ns
TMS hold time from TCK	t_{MSH}	30		ns
TDI setup time to TCK	t_{DIS}	10		ns
TDI hold time from TCK	t_{DIH}	30		ns
TDO valid delay from TCK	t_{DOD}		70	ns

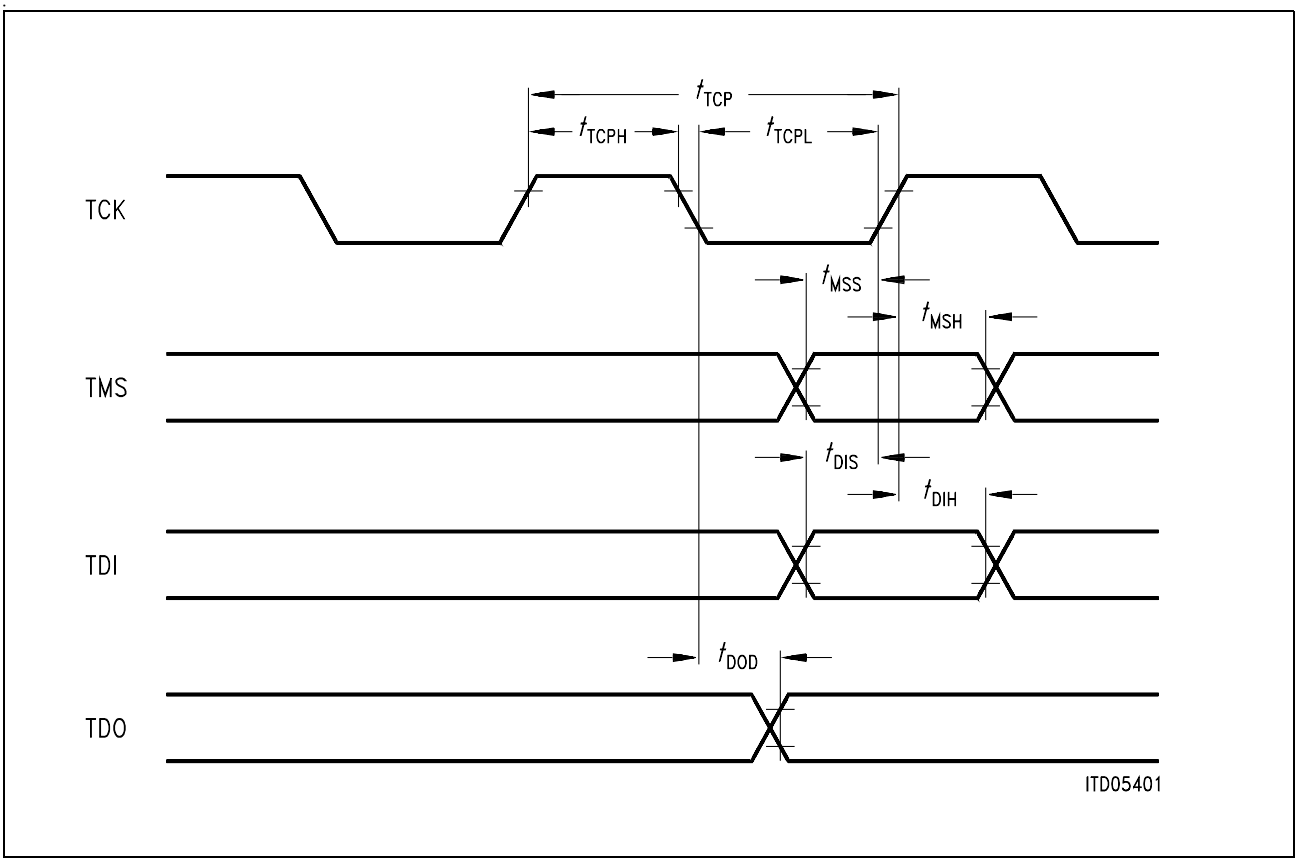


Figure 5-9 Boundary Scan Timing

5.8 U_{PN} Frame Relation to FSC in Transmit Direction

The LF-bit on the U_{PN} interface appears T0 after the last but two (3rd last falling edge) falling edge of DCL before FSC rising edge (**Figure 5-10**).

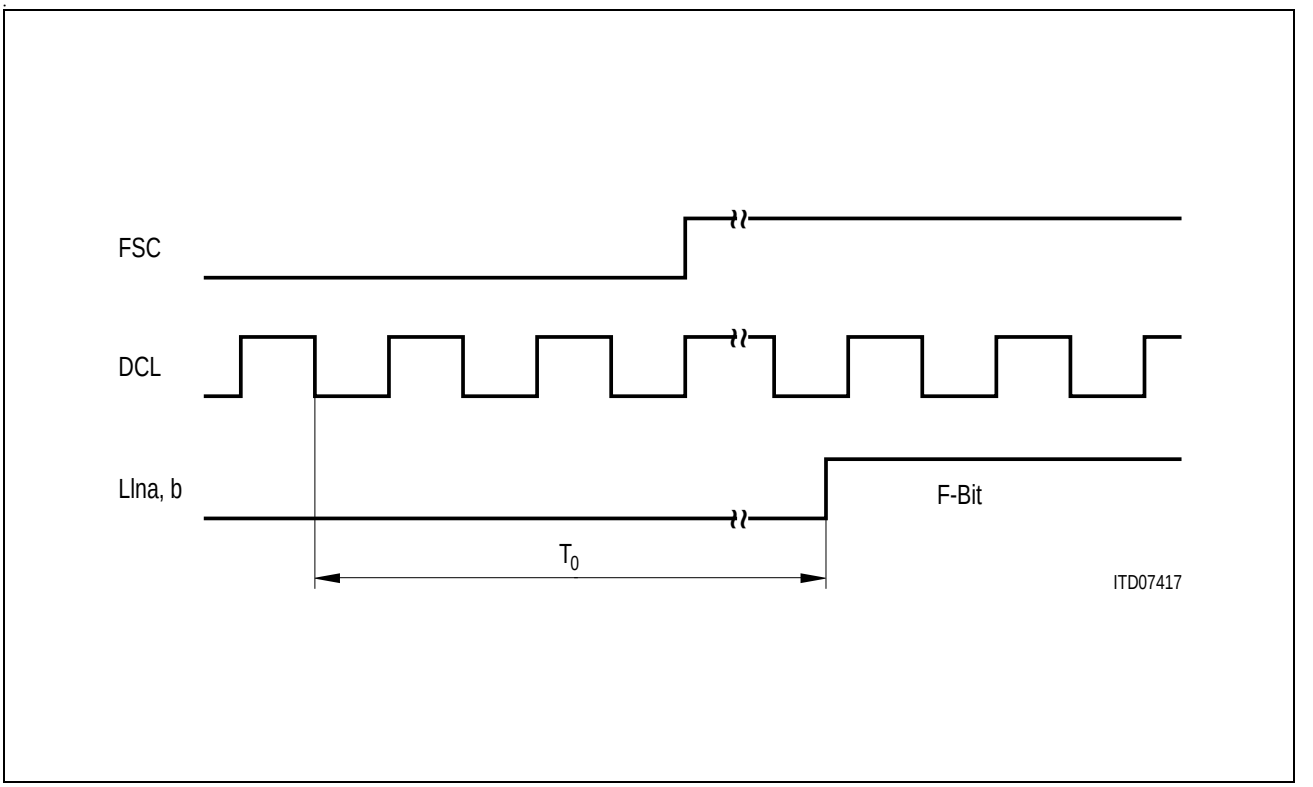


Figure 5-10 F-Bit Delay to FSC in Double Clock Mode

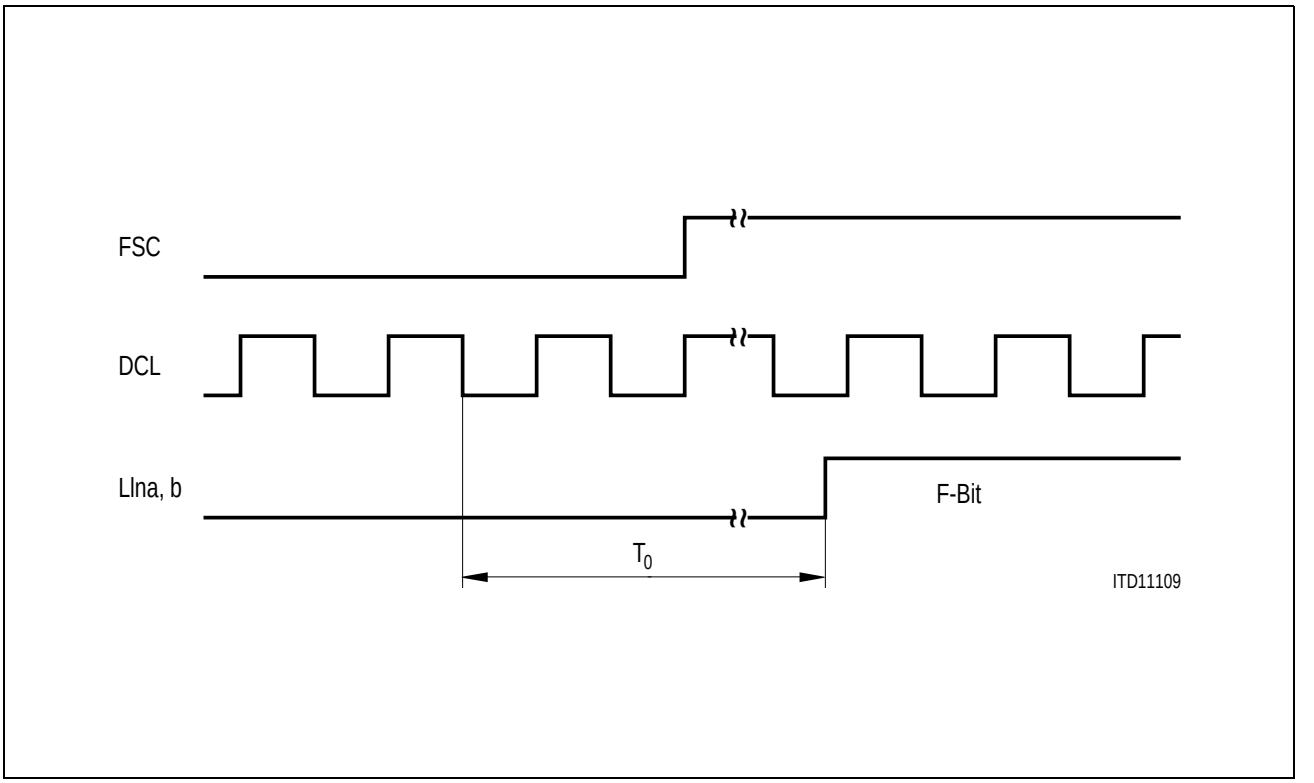


Figure 5-11 F-Bit Delay to FSC in Single Clock Mode

T0 = 85 oscillator periods + analog delay ± 0.5 oscillator periods

Analog delay < 1 oscillator period (15.36 MHz)

5.9 Transceiver Characteristics

A detailed transceiver architecture is shown in **Figure 5-12**. It comprises the transmitter output stages, the differential-to-single ended receiver input stage, the loop switch, the peak detector, and the threshold comparators.

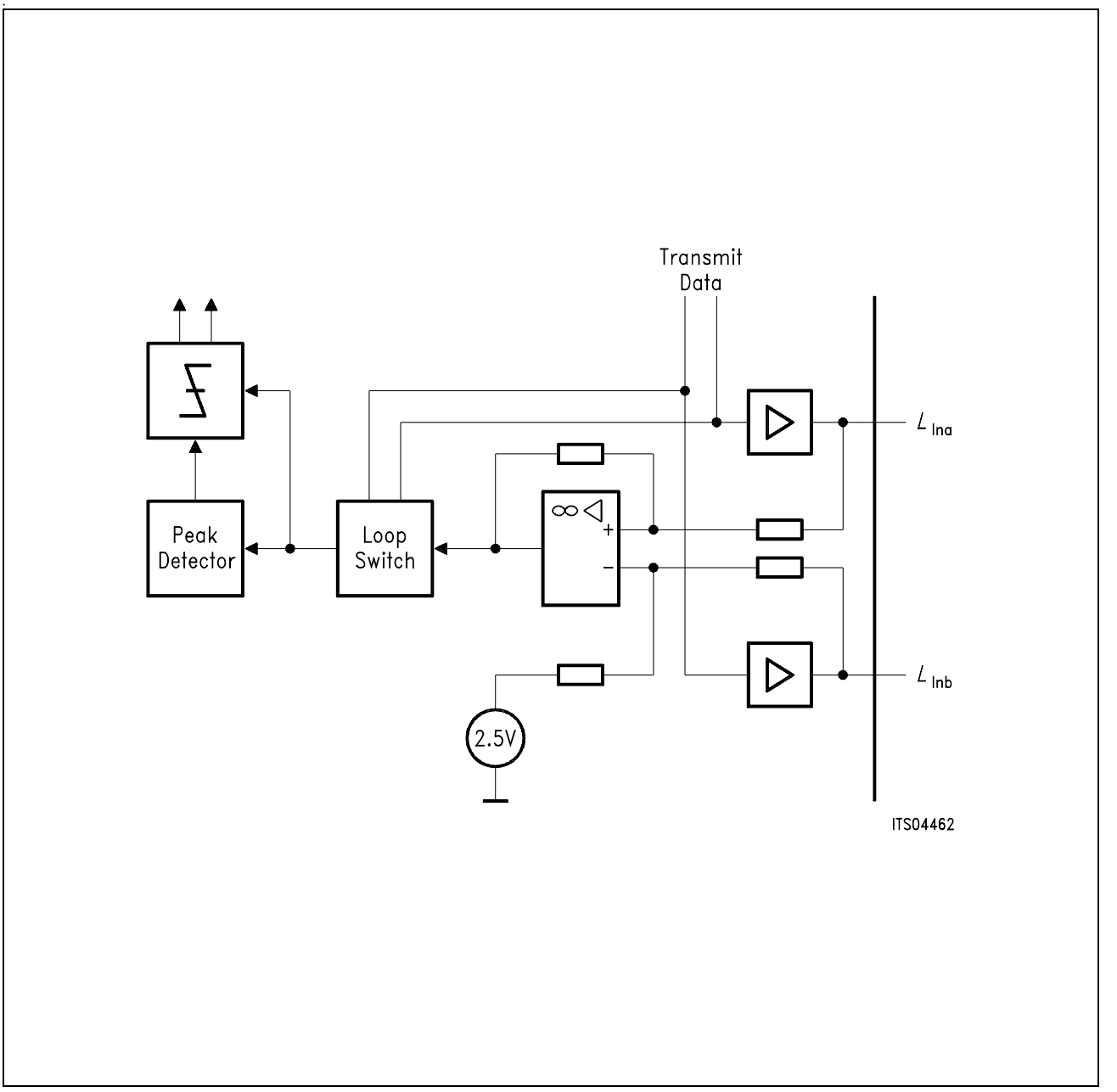


Figure 5-12 Detailed Transceiver Architecture

When transmitting a binary ONE, the transmitter output is ± 5 V (difference between LIna and LInb), when transmitting a binary ZERO, the transmitter output is in tristate.
The receiver input range is from ± 5 V to ± 150 mV.

The 150 mV level is a fixed minimum peak level.

Power Supply Rejection Ratio (PSRR)

The PSRR of the receiver is better than – 40 dB at frequencies below 100 kHz, decreasing by 20 dB per decade above 100 kHz.

Noise Immunity

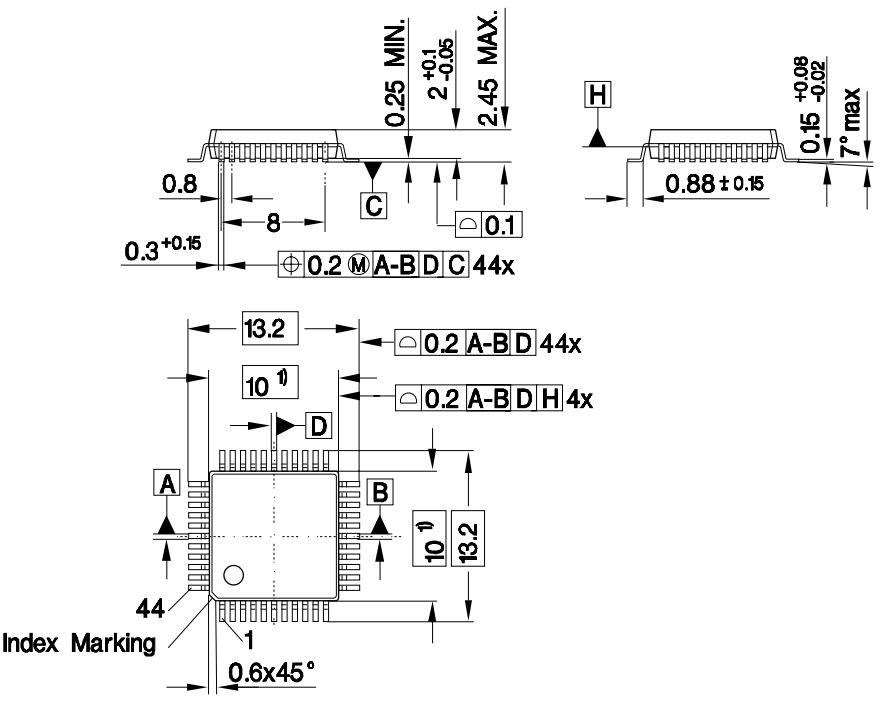
The noise immunity target of the receiver is better than 10 $\mu V/\sqrt{Hz}$ in the range up to 1 MHz, which should be achieved by both adaptive thresholds and digital oversampling techniques.

Crosstalk Immunity

The receiver immunity against crosstalk between neighbor receive channels, measured with minimum and maximum input levels at two neighbor inputs should not effect the overall transceiver performance according to the U_{P0} specification.

6 Package Outlines

P-MQFP-44
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05622

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm