



Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate leakage current	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	60	-	-	V	I <sub>D</sub> =10μA, V <sub>GS</sub> =0V
Drain cutoff current	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	1	-	2.5	V	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Drain-source on-state resistance	R <sub>DS(on)</sub> *1	-	0.7	1.0	Ω	I <sub>D</sub> =300mA, V <sub>GS</sub> =10V
		-	1.1	1.5		I <sub>D</sub> =300mA, V <sub>GS</sub> =4V
Forward transfer admittance	Y <sub>fs</sub>  *1	200	-	-	mS	V <sub>DS</sub> =10V, I <sub>D</sub> =300mA
Input capacitance	C <sub>iss</sub>	-	33	-	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	-	14	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	-	9	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *2	-	6	-	ns	I <sub>D</sub> =150mA, V <sub>DD</sub> =30V
Rise time	t <sub>r</sub> *2	-	5	-	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *2	-	13	-	ns	R <sub>L</sub> =200Ω
Fall time	t <sub>f</sub> *2	-	80	-	ns	R <sub>GS</sub> =10Ω
Total gate charge	Q <sub>g</sub> *2	-	3	6	nC	V <sub>DD</sub> =30V
Gate-source charge	Q <sub>gs</sub> *2	-	0.6	-	nC	V <sub>GS</sub> =10V
Gate-drain charge	Q <sub>gd</sub> *2	-	0.5	-	nC	I <sub>D</sub> =200mA

\*1 P<sub>W</sub>≤300μs, Duty cycle≤1%  
 \*2 Pulsed

●Packaging specifications

Type	Package	Taping
	Code	T116
	Basic ordering unit (pieces)	3000
RK7002A		○

●Electrical characteristic curves

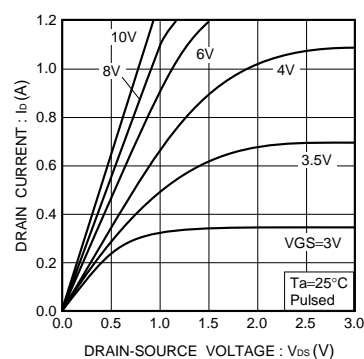


Fig.1 Typical output characteristics

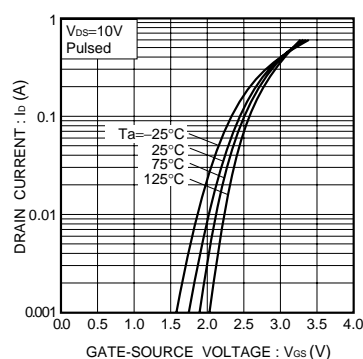


Fig.2 Typical transfer characteristics

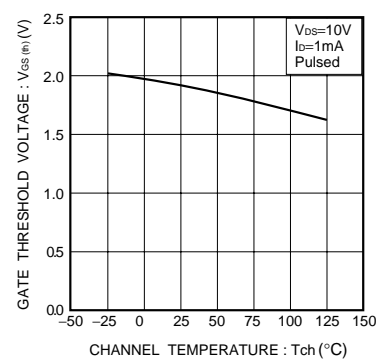


Fig.3 Gate threshold voltage vs. channel temperature

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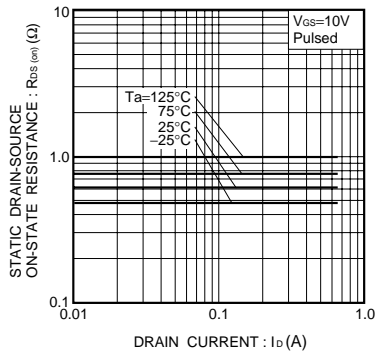


Fig.4 Static drain-source on-state resistance vs. drain current ( I )

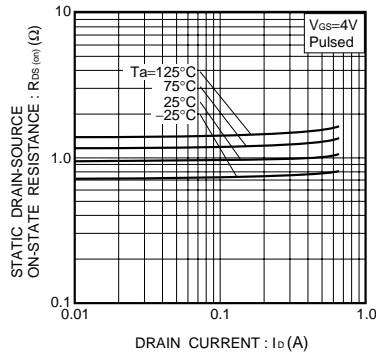


Fig.5 Static drain-source on-state resistance vs. drain current ( II )

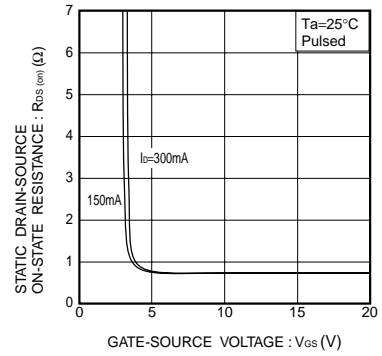


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

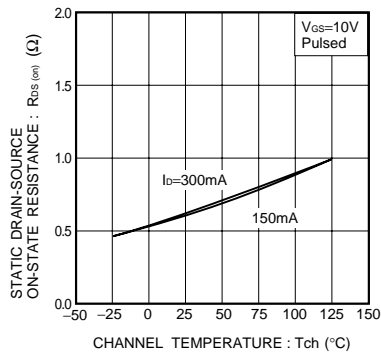


Fig.7 Static drain-source on-state resistance vs. channel temperature

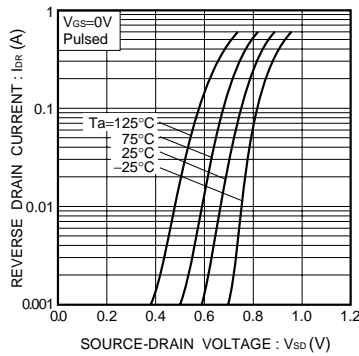


Fig.8 Reverse drain current vs. source-drain voltage ( I )

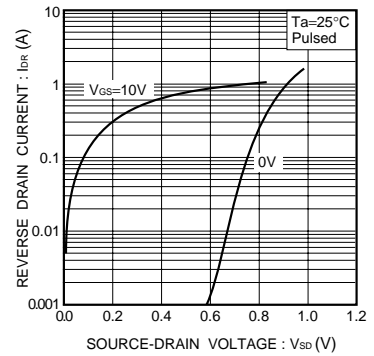


Fig.9 Reverse drain current vs. source-drain voltage ( II )

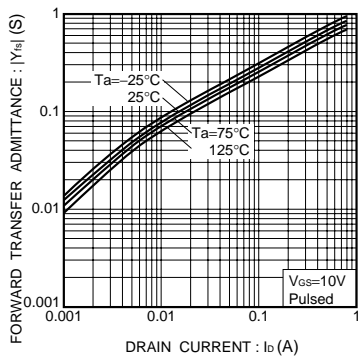


Fig.10 Forward transfer admittance vs. drain current

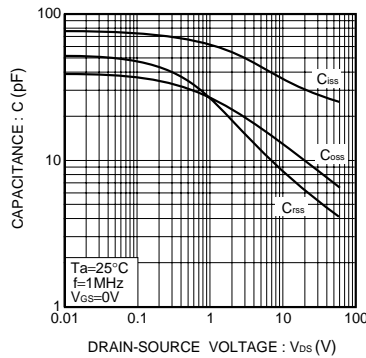


Fig.11 Typical capacitance vs. drain-source voltage

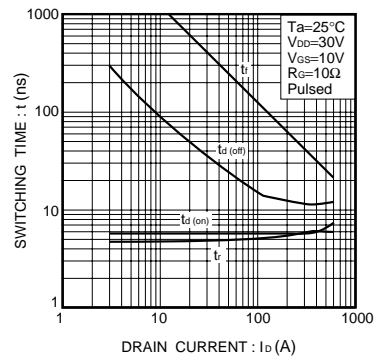


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)

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● Switching characteristics measurement circuit

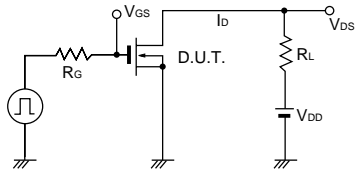


Fig.13 Switching time measurement circuit

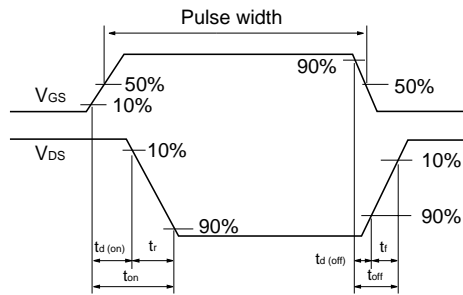


Fig.14 Switching time waveforms