GENERAL DESCRIPTION

The XRT7302 Dual Channel E3/DS3/STS-1 Transceiver IC consists of two fully integrated transmitter and receiver line transceivers designed for E3, DS3 or SONET STS-1 applications.

Each channel within the XRT7302 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channel.

In the transmit direction, each channel within the XRT7302 will encode input data to either B3ZS or HDB3 format and convert the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT7302 can perform Equalization on incoming signals, perform Clock Recovery, decode data from either B3ZS or HDB3 format, convert the receive data into TTL/CMOS format, check for LOS or LOL conditions and detect and declare the occurrence of Line code Violations.
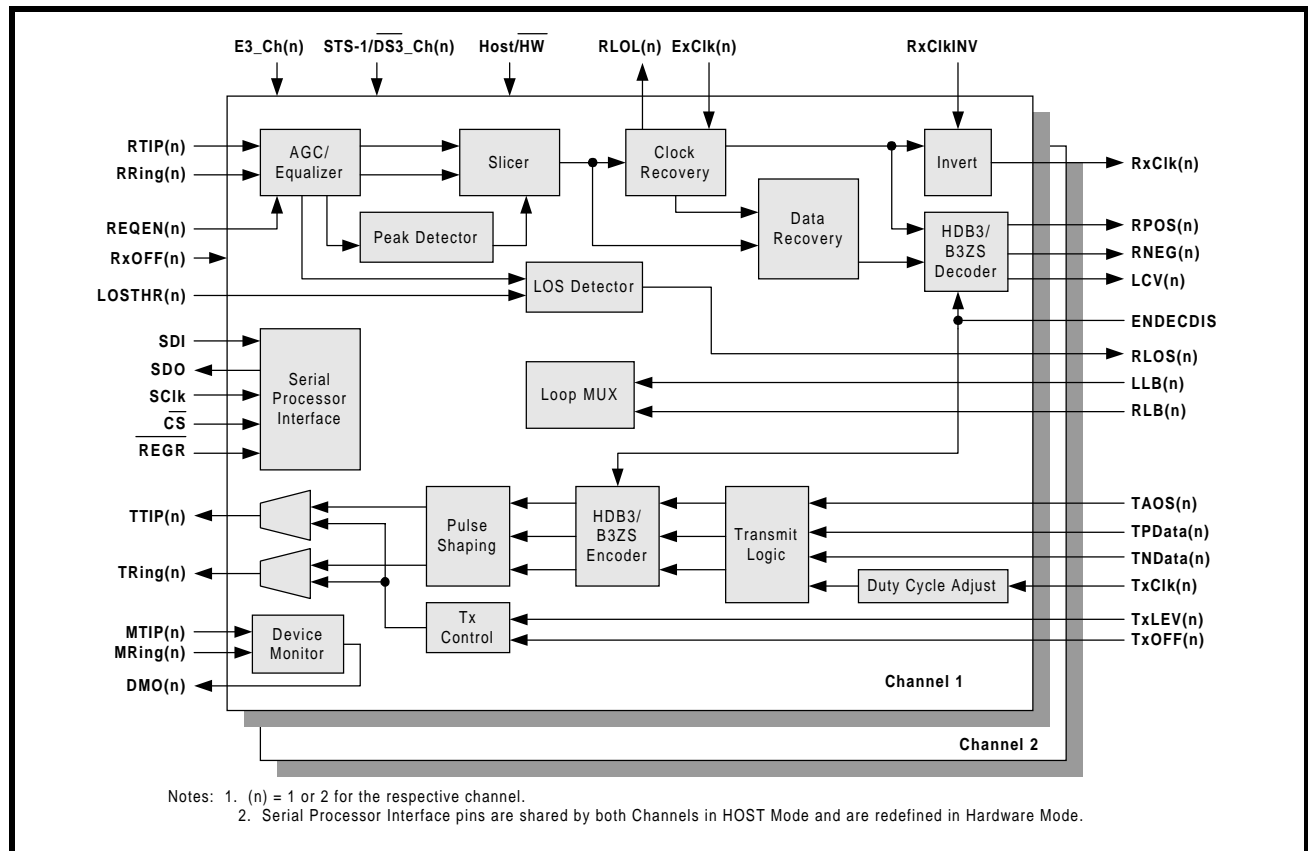
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Single +5V Power Supply
- Uses Minimum External components
- Operates over -40°C to +85°C Temperature Range
- Available in an 80 pin TQFP Thermal Enhanced package with integral Heat Sink

XRT7302 BLOCK DIAGRAM

Notes: 1. (n) = 1 or 2 for the respective channel.
        2. Serial Processor Interface pins are shared by both Channels in HOST Mode and are redefined in Hardware Mode.

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single Rail or Dual Rail data from Terminal Equipment, and generates a bipolar signal

- Integrated Pulse Shaping Circuit

- Built-in B3ZS/HDB3 Encoder (which can be disabled)

- Contains "Transmit Clock Duty Cycle Correction" Circuit on-chip

- Generates pulses that comply with the ITU-T G.703 pulse template (E3 applications)

- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993

- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE

- Transmitter can be turned off in order to support "redundancy designs"

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (Optional) and Timing Recovery

- Declares and Clears the LOS alarm per ITU-T G.775 requirements (E3 and DS3 applications)

- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 (for E3 Applications)

- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE (for DS3 Applications)

- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms

- Built-in B3ZS/HDB3 Decoder (which can be disabled)

- Recovered Data can be automatically muted while the LOS Condition is declared

- Outputs either Single Rail or Dual Rail data to the Terminal Equipment

- Receiver can be powered down in order to conserve power in "redundancy designs"
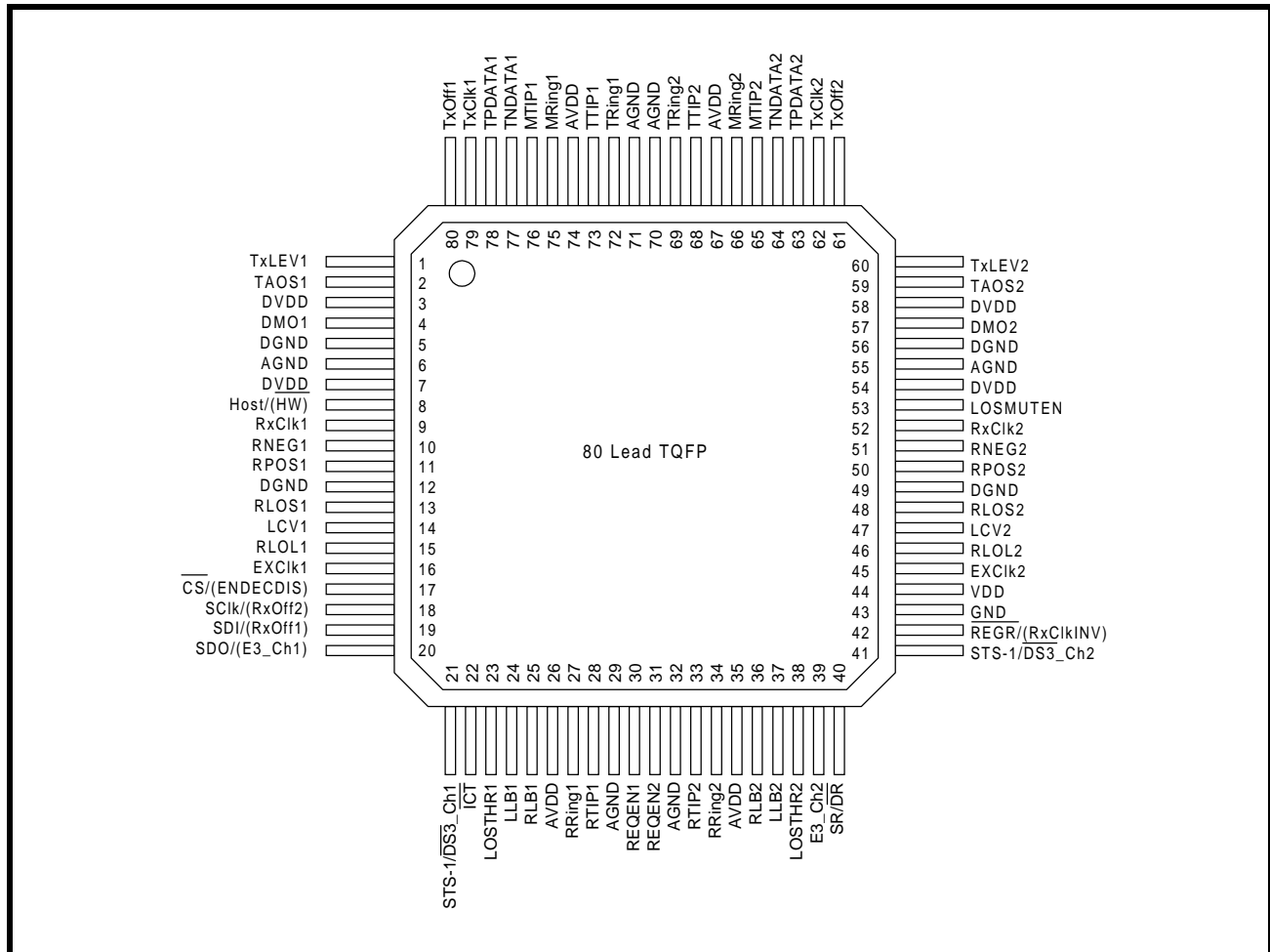
PIN OUT OF THE XRT7302

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
1	TxLEV1	I	**Transmit Line Build-Out Enable/Disable Select - Channel 1:**
			This input pin permits the user to enable or disable the Transmit Line Build-Out circuit, within Channel 1 of the XRT7302.
			Setting this pin to "HIGH" disables the Line Build-Out circuit within Channel 1. In this mode, Channel 1 will output unshaped (e.g., square-wave) pulses onto the line via the TTIP1 and TRing1 output pins.
			Setting this pin to "LOW" enables the Line Build-Out circuit within Channel 1. In this mode, Channel 1 will output shaped pulses onto the line via the TTIP1 and TRing1 output pins.
			In order to comply with the "Isolated DSX-3/STSX-1 Pulse Template Requirements (per Bellcore GR-499-CORE or Bellcore GR-253-CORE), the user should:
			1. Set this input pin to "1", if the cable length (between the Cross-Connect and the transmit output of Channel 1) is greater than 225 feet.
			2. Set this input pin to "0", if the cable length (between the Cross-Connect and the transmit output of Channel 1) is less than 225 feet.
			This pin is active only if the following two conditions are true:
			a. The XRT7302 is configured to operate in either the DS3 or SONET STS-1 Modes.
			b. The XRT7302 is configured to operate in the "Hardware" Mode.
			NOTE: *Note: The user should tie this pin to GND if the XRT7302 is going to be operating in the "Host" Mode*
2	TAOS1	I	**Transmit All Ones Select - Channel 1:**
			A "high" on this pin causes the Transmit Section, within Channel 1 to generate and transmit a continuous AMI "All 1s" pattern onto the line. The frequency of this "1s" pattern is determined by TxClk.
			NOTES:
			1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.*
			2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
3	DVDD	****	**Transmit Digital VDD (for Transmitter 1)**
4	DMO1	O	**Drive Monitor Output - Channel 1:**
			If no transmitted AMI signal is present on MTIP1 and MRing1 input pins for 128±32 TxClk periods, then DMO1 will toggle and remain "high" until the next AMI signal is detected.
5	DGND	****	**Transmit Digital GND (for Transmitter 1)**
6	AGND		**Analog GND (Substrate Connection) - Channel 1**
7	DVDD	****	**Receive Digital VDD (for Receiver 1)**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
8	Host/($\overline{\text{HW}}$)	I	**Host/$\overline{\text{HW}}$ Mode Select:** This input pin permits the user to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SClk, and CSB pins). Setting this input pin "high" enables the Microprocessor Serial Interface (or configures the XRT7302 to operate in the "Host" Mode). In this mode, the user is expected to configure the XRT7302 via the Microprocessor Serial Interface. As a consequence, when the XRT7302 is operating in the "Host" Mode, then it will ignore the states of many of the discrete input pins. Setting this input pin "low" disables the Microprocessor Serial Interface (e.g., configures the XRT7302 to operate in the "Hardware" Mode). In this mode, many of the external input control pins will be functional and therefore the unsued input pins should not be left floating.
9	RxClk1	O	**Receive Clock Output pin - Channel 1:** This output pin is the Recovered Clock signal from the incoming line signal, which is being received by Channel 1. The receive section of Channel 1 will output data via the RPOS1 and RNEG1 output pins, on the rising edge of this clock signal. ***NOTE:*** *The user can configure the Receive Section of Channel 1 to update the data on the RPOS1 and RNEG1 output pins, on the falling edge of RxClk1, by doing one of the following:* **1. If the XRT7302 is operating in the Hardware Mode** Pulling the "RClkINV" pin (pin 42) to "high". **2. If the XRT7302 is operating in the Host Mode** Writing a "1" into the "RClk(n)INV" bit-field within the Command Register.
10	RNEG1	O	**Receive Negative Pulse Output - Channel 1:** This output pin will pulse "high" whenever Channel 1, within the XRT7302 has received a "Negative Polarity" pulse, in the incoming line signal, at the RTIP1/RRing1 inputs. ***NOTE:*** *Note: If the B3ZS/HDB3 Decoder (within Channel 1) is "enabled" then the "zero suppression" patterns, in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") will not be reflected at this output.*
11	RPOS1	O	**Receive Positive Pulse Output - Channel 1:** This output pin will pulse "high" whenever Channel 1, within the XRT7302 has received a "Positive Polarity" pulse, in the incoming line signal, at the RTIP1/RRing1 inputs. ***NOTE:*** *If the B3ZS/HDB3 Decoder (within Channel 1) is "enabled" then the "zero suppression" patterns, in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") will not be reflected at this output.*
12	DGND	****	**Receive Digital GND - Channel 1**
13	RLOS1	O	**Receive Loss of Signal Output Indicator - Channel 1:** This output pin toggles "high" if Channel 1, within the XRT7302 has detected a "Loss of Signal" Condition in the incoming line signal. The exact criteria that the XRT7302 uses to declare an "LOS Condition" depends upon whether the device is operating in the E3 or DS3/STS-1 Mode and the state of the LOSTHR1 pin.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
14	LCV1	O	**Line Code Violation Indicator - Channel 1:** Whenever the Receive Section of Channel 1 detects a Line Code Violation, then it will pulse this output pin "high". This output pin will remain "low" at all other times. *The XRT7302 will output an NRZ pulse via this output pin. Hence, the user is advised to sample this output pin via the RxClk2 clock output signal.*
15	RLOL1	O	**Receive Loss of Lock Output Indicator - Channel 1:** This output pin toggles "high" if Channel 1, within the XRT7302 has detected a "Loss of Lock" Condition. Channel 1 will declare an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the ExClk input pin) by more than 0.5%.
16	EXClk1	I	**External Reference Clock Input - Channel 1:** The user is expected to apply a 34.368 MHz clock signal (for E3 applications), a 44.736 MHz clock signal (for DS3 applications), or a 51.84 MHz clock signal (for SONET STS-1 applications). ***NOTES:*** 1. *It is permissible for one to use the same clock, which is also driving the "TxClk" input pin.* 2. *It is permissible to operate Channel 1 at a different data rate than from Channel 2.*
17	$\overline{CS}$/(ENDECDIS)	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** The exact functionality of this pin depends upon whether the XRT7302 is operating in the Host or Hardware Mode. **Host Mode Operation - Chip Select Input (for the Microprocessor Serial Interface):** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT7302, via the Microprocessor Serial Interface. (Note: This pin is internally pulled "high".) **Hardware Mode - B3ZS/HDB3 Encoder & Decoder Disable:** Setting this input pin "high" disables the "B3ZS/HDB3 Encoder & Decoder" blocks (within the XRT7302) and configures the XRT7302 to transmit and receive the line signal in an AMI format. Conversely, setting this input pin "low" enables the "B3ZS/HDB3 Encoder & Decoder" blocks and configures the XRT7302 to transmit and receive the line signal in the B3ZS format, (for DS3/STS-1 operation) or in the HDB3 format, (for E3 operation). ***NOTE:*** *If the XRT7302 is operating in the "Hardware" Mode, then this pin setting configures the "B3ZS/HDB3" Encoder and Decoder Blocks for both Channels 1 and 2.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
18	SClk/(RxOFF2)	I	**Microprocessor Serial Interface Clock Signal/"Channel 2 Receiver Shut OFF" Input:** The exact role that this particular pin plays depends upon whether the XRT7302 is operating in the "Host" Mode or in the "Hardware" Mode. **Host Mode - Microprocessor Serial Interface Clock Signal:** This signal will be used to sample the data, on the SDI pin, on the rising edge. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal. **Hardware Mode - Channel 2 Receiver Shut OFF input pin:** Setting this input pin "high" shuts off the Receive Section within Channel 2. Conversely, setting this input pin "low" enables the Receive Section for full operation.
19	SDI/(RxOFF1)	I	**Serial Data Input for the Microprocessor Serial Interface/Channel 1 - Receiver Shut OFF Input pin:** The exact function of this input depends upon whether the XRT7302 is operating in the "Host" Mode or in the "Hardware" Mode. **Host Mode - Serial Data Input for the Microprocessor Serial Interface:** Whenever the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface; the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SClk pin (pin 18). **Hardware Mode - Channel 1 Receiver Shut OFF Input pin:** Setting this input pin "high" shuts off the Receive Section within Channel 1. Conversely, setting this input pin "low" enables the Receive Section for full operation.
20	SDO/(E3_Ch1)	I/O	**Serial Data Output from the Microprocessor Serial Interface/E3_Mode Select - Channel 1:** The exact functionality of this pin depends upon whether the XRT7302 is operating in the "Host" Mode or in the "Hardware" Mode. **Host Mode Operation - Serial Data Output for the Microprocessor Serial Interface:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SClk input signal. This pin will be tri-stated upon completion of data transfer. **Hardware Mode Operation - E3 Mode Select - Channel 1:** This input pin permits the user to configure Channel 1 (within the XRT7302) to operate in the E3 or STS/DS3 Modes. Setting this input pin to "HIGH" configures Channel 1 to operate in the "E3" Mode. Setting this input pin to "LOW" configures Channel 1 to operate in either the DS3 or STS-1 Modes (depending upon the state of the "STS-1/$\overline{DS3}$_Ch1 input pin (pin 21).

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
21	STS-1/$\overline{\text{DS3}}$_Ch1	I	**STS-1/$\overline{\text{DS3}}$ Select Input - Channel 1:** A "high" on this pin configures the Clock Recovery Phase Locked Loop (within Channel 1) to set its VCO Center frequency to around 51.84 MHz (optimal for SONET STS-1 operations). A "low" on this pin configures the Clock Recovery Phase Locked Loop to set the VCO Center frequency to 44.736 MHz (optimal for DS3 operations). *NOTES:* 1. *The XRT7302 will ignore this pin if the "E3_Ch1" pin (pin 20) is set to "1".* 2. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 3. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
22	$\overline{\text{ICT}}$	I	**In-Circuit Test Input** Setting this pin "low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. Hence, the user should set this pin "high" for normal operation. *NOTE: This pin is internally pulled "high".*
23	LOSTHR1	I	**Loss of Signal Threshold Control - Channel 1** The voltage forced on this pin controls the input loss of signal threshold for Channel 1. Forcing the LOSTHR1 pin to GND or VDD provides two settings. This pin must be set to the desired level upon power up and should not be changed during operation. *NOTE: This pin is only applicable during DS3 or STS-1 operations.*
24	LLB1	I	**Local Loop-back - Channel 1** This input pin, along with "RLB1" dictates which loop-back mode Channel 1 (within the XRT7302) will be operating in. A "high" on this pin (with "RLB1" being set to "low") configures Channel 1, within the XRT7302 to operate in the "Analog Local Loop-back" Mode. A "high" on this pin (with "RLB1" also being set to "high") configures Channel 1, within the XRT7302, to operate in the "Digital Local Loop-back" Mode and tristates the channel 1 transmitter output. *NOTES:* 1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
25	RLB1	I	**Remote Loop-back - Channel 1:** This input pin, along with "LLB1" dictates which loop-back mode "Channel 1 (within the XRT7302) will be operating in. A "high" on this pin (with "LLB1" being set to "low") configures Channel 1, within the XRT7302 to operate in the Remote Loop-back Mode. A "high" on this pin (with "LLB1" also being set to "high") configures Channel 1, within the XRT7302, to operate in the "Digital Local Loop-back" Mode and tristates the channel 1 transmitter output. **NOTES:** 1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
26	AVDD	****	**Receive Analog VDD - Channel 1:**
27	RRing1	I	**Receive Ring Input - Channel 1:** This input pin, along with RTIP1 is used to receive the bipolar line signal from the "Remote DS3/E3 Terminal".
28	RTIP1	I	**Receive TIP Input - Channel 1:** This input pin, along with RRing1 is used to receive the bipolar line signal from the "Remote DS3/E3/STS-1 Terminal".
29	AGND	****	**Receive Analog GND - Channel 1**
30	REQEN1	I	**Receive Equalization Enable Input - Channel 1:** Setting this input pin "low" disables the Internal Receive Equalizer, within Channel 1. Setting this pin "high" enables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2 **NOTES:** 1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
31	REQEN2	I	**Receive Equalization Enable Input - Channel 2:** Setting this input pin "high" enables the Internal Receive Equalizer, within Channel 2. Setting this pin "low" disables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. **NOTES:** 1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
32	AGND	****	**Receive Analog GND - Channel 2**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
33	RTIP2	I	**Receive TIP Input - Channel 2:** This input pin, along with RRing2 is used to receive the bipolar line signal from the "Remote DS3/E3/STS-1 Terminal".
34	RRing2	I	**Receive Ring Input - Channel 2:** This input pin, along with RTIP2 is used to receive the bipolar line signal from the "Remote DS3/E3 Terminal".
35	AVDD	****	**Receive Analog VDD - Channel 2**
36	RLB2	I	**Remote Loop-back - Channel 2:** This input pin, along with "LLB2" dictates which loop-back mode "Channel 2" (within the XRT7302) will be operating in. A "high" on this pin (with "LLB2" being set to "low") configures Channel 2, within the XRT7302 to operate in the "Remote Loop-back" Mode. A "high" on this pin (with "LLB1" also being set to "high") configures Channel 2, within the XRT7302, to operate in the "Analog Local Loop-back" Mode and tristates the channel 2 transmitter output. *NOTES:* 　1.　*This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 　2.　*The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
37	LLB2	I	**Local Loop-back - Channel 2:** This input pin, along with "RLB2" dictates which loop-back mode Channel 2 (within the XRT7302) will be operating in. A "high" on this pin (with "RLB2" being set to "low") configures Channel 2 within the XRT7302 to operate in the "Analog Local Loop-back" Mode. A "high" on this pin (with "RLB2" also being set to "high") configures Channel 2, within the XRT7302, to operate in the "Digital Local Loop-back" Mode and tristates the channel 2 transmitter output. *NOTES:* 　1.　*This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 　2.　*The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
38	LOSTHR2	I	**Loss of Signal Threshold Control - Channel 2** The voltage forced on this pin controls the input loss of signal threshold for Channel 2. Two settings are provided by forcing the LOSTHR2 pin to GND or VDD. This pin must be set to the desired level upon power up and should not be changed during operation. *NOTE: This pin is only applicable during DS3 or STS-1 operations.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
39	E3_Ch2	I	**E3 Select Input - Channel 2:** A "high" on this pin configures Channel 2 of the XRT7302 to operate in the E3 Mode. A "low" on this pin configures Channel 2 of the XRT7302 to check the state of the STS-1/($\overline{DS3}$_Ch2) input pin ***NOTES:*** *1. This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* *2. The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*
40	SR/$\overline{DR}$	I	**Receive Output Single-Rail/Dual-Rail Select:** Setting this pin "HIGH" configures the Receive Sections of both Channels, to output data (in a Single-Rail Manner) to the Terminal Equipment. Setting this pin "LOW" configures the Receive Section of both Channels, to output data (in a Dual-Rail Manner) to the Terminal Equipment.
41	STS-1/$\overline{DS3}$_Ch2	I	**STS-1/$\overline{DS3}$ Select Input - Channel 2:** A "high" on this pin configures the Clock Recovery Phase Locked Loop (in Channel2) to set its VCO Center frequency to around 51.84 MHz (optimal for SONET STS-1 operations). A "low" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 44.736 MHz (optimal for DS3 operations). ***NOTES:*** *1. The XRT7302 will ignore this pin if the E3_Ch2 pin (pin 39) is set to "1".* *2. This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* *3. The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
42	$\overline{\text{REGR}}$/ (RCIkNV)	I	**Register Reset Input pin (Invert RxClk(n) Output - Select):**
			The exact function of this particular pin depends upon whether the XRT7302 is operating in the "Host" Mode or in the "Hardware" Mode.
			Host-Mode - Register Reset Input pin:
			Setting this input pin "low" causes the XRT7302 to reset the contents of the Command Registers to their default settings. Additionally, it resets the XRT7302 to its "default" operating configuration.
			NOTE: *This pin is internally pulled "high".*
			Hardware Mode - Invert RxClk Output Select:
			Setting this input pin "high" configures the Receive Section of both Channels (within the XRT7302) to invert their "RxClk1 and RxClk2" clock output signals.
			Specifically, setting this pin "low" configures Channel 1 to output the recovered data (via the RPOS1 and RNEG1 output pins) on the "rising" edge of the RxClk1 output signal. This setting also configures Channel 2 to output the recovered data (via the RPOS2 and RNEG2 output pins) on the "rising" edge of the RxClk2 output signal.
			Conversely, setting this input pin "high" configures Channel 1 to output the recovered data (via the RPOS1 and RNEG1 output pins) on the "falling" edge of the RxClk1 output signal. This setting also configures Channel 2 to output the recovered data (via the RPOS2 and RNEG2 output pins on the "falling" edge of the RxClk2 output signal
43	GND	****	**ExClk Reference GND**
44	VDD	****	**ExClk Reference VDD**
45	EXClk2	I	**External Reference Clock Input:**
			The user is expected to apply a 34.368 MHz clock signal (for E3 applications), a 44.736 MHz clock signal (for DS3 applications), or a 51.84 MHz clock signal (for SONET STS-1 applications).
			NOTES:
			1. *It is permissible for one to use the same clock, which is also driving the "TxClk" input pin.*
			2. *It is permissible to operate Channel 2 at a different data rate than from Channel 1.*
46	RLOL2	O	**Receive Loss of Lock Output Indicator - Channel 2**
			This output pin toggles "high" if the Receive Section of Channel 2 has detected a "Loss of Lock" Condition. Channel 2 will declare an LOL (Loss of Lock) Condition if the recovered clock frequency (at Channel 2) deviates from the Reference Clock frequency (available at the ExClk input pin) by more than 0.5%.
47	LCV2	O	**Line Code Violation Indicator - Channel 2**
			Whenever the Receive Section of Channel 2 detects a Line Code Violation, then it will pulse this output pin "high". This output pin will remain "low" at all other times.
			NOTE: *The XRT7302 will output an NRZ pulse via this output pin. Hence, the user is advised to sample this output pin via the RxClk2 clock output signal.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
48	RLOS2	O	**Receive Loss of Signal Output Indicator - Channel 2** This output pin toggles "high" if Receive Section of Channel 2 has detected a "Loss of Signal" Condition in the incoming line signal. The exact criteria that the XRT7302 uses to declare an "LOS Condition" depends upon whether the device is operating in the E3 or DS3/STS-1 Mode.
49	DGND	****	**Receive Digital Ground - Channel 2**
50	RPOS2	O	**Receive Positive Pulse Output - Channel 2:** This output pin will pulse "high" whenever the Receive Section of Channel 2 has received a "Positive Polarity" pulse, in the incoming line signal, at the RTIP/RRing inputs. ***NOTE:*** *Note: If the B3ZS/HDB3 Decoder (within Channel 2) is "enabled" then the "zero suppression" patterns, in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") will not be reflected at this output.*
51	RNEG2	O	**Receive Negative Pulse Output - Channel 2:** This output pin will pulse "high" whenever the Receive Section of Channel 2 has received a "Negative Polarity" pulse, in the incoming line signal, at the RTIP/RRing inputs. ***NOTE:*** *Note: If the B3ZS/HDB3 Decoder (within Channel 2) is "enabled" then the "zero suppression" patterns, in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") will not be reflected at this output.*
52	RxClk2	O	**Receive Clock Output pin - Channel 2:** This output pin is the Recovered Clock signal from the incoming line signal, which is being received via Channel 2. The receive section of Channel 2 will output data via the RPOS2 and RNEG2 output pins, on the rising edge of this clock signal. ***NOTE:*** *The user can configure the Receive Section of Channel 2 to update the data on the RPOS2 and RNEG2 output pins, on the falling edge of RxClk2, by doing one of the following:* **1. If the XRT7302 is operating in the Hardware Mode** Pulling the "RClkINV" pin (pin 42) to "high". **2. If the XRT7302 is operating in the Host Mode** Writing a "1" into the "RClk(n)INV" bit-field within the Command Register.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
53	LOSMUTEN	I	**MUTE-upon-LOS Enable Input (Hardware Mode):** This input pin permits the user to configure the XRT7302 (while it is operating in the "Hardware Mode") to MUTE the recovered data (via the RPOS1, RNEG1, RPOS2 and RNEG2 output pins), whenever the corresponding Channel declares an LOS conditions. Setting this input pin "high" will configure Channel 1 to automatically pull the RPOS1 and RNEG1 output pins to "GND", whenever it is declaring an LOS condition (thereby MUTing the data being output to the Terminal Equipment). Similarly, Channel 2 will automatically pull the RPOS 2 and RNEG2 output pins to "GND" whenever it is declaring an LOS condition. Setting this input pin "low" configures Channels 1 and 2 to NOT automatically MUTE the recovered data, whenever an LOS condition is declared. *NOTES:* 1. *This pin will be ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is to be operated in the "Host" Mode.* 3. *This pin is internally pulled "High".*
54	DVDD	****	**Receive Digital VDD - Channel 2**
55	AGND	****	**Analog Ground (Substrate Connection) - Channel 2**
56	DGND	****	**Transmit Digital GND - Channel 2**
57	DMO2	O	**Drive Monitor Output - Channel 2:** If no transmitted AMI signal is present on the MTIP2 and MRing2 input pins for 128±32 TxClk periods, then DMO2 will toggle and remain "high" until the next AMI signal is detected.
58	DVDD	****	**Transmit Digital VDD - Channel 2**
59	TAOS2	I	**Transmit All Ones Select - Channel 2:** A "high" on this pin causes the Transmit Section, within Channel 2 to generate and transmit a continuous AMI "All 1s" pattern to be transmitted onto the line. The frequency of this "1s" pattern is determined by TxClk2. *NOTES:* 1. *This input pin is ignored if the XRT7302 is operating in the "Host" Mode.* 2. *The user should tie this pin to GND, if the XRT7302 is going to be operating in the "Host" Mode.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION

60	TxLEV2	I	**Transmit Line Build-Out Enable/Disable Select - Channel 2:**
			
			This input pin permits the user to enable or disable the Transmit Line Build-Out circuit, within Channel 2 of the XRT7302.
			
			Setting this pin to "HIGH" disables the Line Build-Out circuit within Channel 2. In this mode, Channel 2 will output unshaped (e.g., square-wave) pulses onto the line via the TTIP2 and TRing2 output pins.
			
			Setting this pin to "LOW" enables the Line Build-Out circuit within Channel 2. In this mode, Channel 2 will output shaped pulses onto the line via the TTIP2 and TRing2 output pins.
			
			In order to comply with the "Isolated DSX-3/STSX-1 Pulse Template Requirements (per Bellcore GR-499-CORE or Bellcore GR-253-CORE), the user should:
			  a. Set this input pin to "1", if the cable length (between the Cross-Connect and the transmit output of Channel 2) is greater than 225 feet.
			  b. Set this input pin to "0", if the cable length (between the Cross-Connect and the transmit output of Channel 2) is less than 225 feet.
			
			This pin is active only if the following two conditions are true:
			  a. The XRT7302 is configured to operate in either the DS3 or SONET STS-1 Modes.
			  b. The XRT7302 is configured to operate in the "Hardware" Mode.
			NOTE: *The user should tie this pin to GND if the XRT7302 is going to be operating in the "Host" Mode.*

61	TxOFF2	I	**Transmitter OFF Input - Channel 2:**
			
			Setting this input pin "high" configures the XRT7302 to turn off the Transmit Section within Channel 2. In this mode, the TTIP2 and TRing2 outputs will be tri-stated.
			NOTES:
			  1. This input pin controls the TTIP2 and TRING2 outputs, even when the XRT7302 is operating in the "Host" Mode.
			  2. For Host Mode Operation, the user should tie this pin to GND, to turn-ON/turn-OFF the Transmitter via the Microprocessor Serial Interface.

62	TxClk2	I	**Transmit Clock Input for TPData2 and TNData2 - Channel 2:** This input pin must be driven at 34.368 MHz (for E3 applications), 44.736 MHz (for DS3 applications), or 51.84 MHz (for SONET STS-1 applications). The Transmit Section of Channel 2 will use this signal to sample the TPData2 and TNData2 input pins. By default, Channel 2 will be configured to sample these two pins on the falling edge of this signal. If the XRT7302 is operating in the "Host" Mode, then Channel 2 can be configured to sample the TPData2 and TNData2 input pins on either the rising or falling edge of TxClk2.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
63	TPData2	I	**Transmit Positive Data Input - Channel 2:** The Transmit Section of Channel 2 will sample this pin, on the falling edge of TxClk2. If the Channel samples a "1" at this input pin, then it will generate and transmit a "positive" polarity pulse to the line. **NOTES:** 　1. *The data should be applied to this input pin if the "Transmit Section" is configured to accept Single-Rail data from the Terminal Equipment.* 　2. *If the XRT7302 is operating in the "Host" Mode, then the user can (if desired) configure Channel 2 to sample the TPData2 pin on either the rising or falling edge of TxClk2.*
64	TNData2	I	**Transmit Negative Data Input - Channel 2:** The Transmit Section of Channel 2 will sample this pin, on the falling edge of TxClk2. If the device samples a "1" at this input pin, then it will generate and transmit a "negative" polarity pulse to the line. **NOTES:** 　1. *This input pin will be ignored and should be tied to GND, if the Transmit Section is configured to accept "Single-Rail" data from the Terminal Equipment.* 　2. *If the XRT7302 is operating in the "Host" Mode, then the user can (if desired) configure Channel 2 to sample the TNData2 pin on either the rising or falling edge of TxClk2.*
65	MTIP2	I	**Monitor Tip Input - Channel 2:** The bipolar line output signal, from TTIP2 can be connected to this pin, via a 270-ohm resistor, in order to check for line driver failure. This pin is internally pulled "high".
66	MRing2	I	**Monitor Ring Input - Channel 2:** The bipolar line output signal, from TRing2 can be connected to this pin, via a 270-ohm resistor, in order to check for line driver failure. This pin is internally pulled "high".
67	AVDD	****	**Transmit Analog VDD - Channel 2:**
68	TTIP2	O	**Transmit TTIP Output - Channel 2:** The XRT7302 will use this pin, along with TRing2, to transmit a bipolar line signal, via a 1:1 transformer.
69	TRing2	O	**Transmit Ring Output - Channel 2:** The XRT7302 will use this pin, along with TTIP2, to transmit a bipolar line signal, via a 1:1 transformer.
70	AGND	****	**Transmit Analog GND - Channel 2**
71	AGND	****	**Transmit Analog GND - Channel 1**
72	TRing1	O	**Transmit Ring Output - Channel 1:** The XRT7302 will use this pin, along with TTIP1, to transmit a bipolar line signal, via a 1:1 transformer.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
73	TTIP1	O	**Transmit TTIP Output - Channel 1:** The XRT7302 will use this pin, along with TRing1, to transmit a bipolar line signal, via a 1:1 transformer.
74	AVDD	****	**Transmit Analog VDD - Channel 1**
75	MRing1	I	**Monitor Ring Input - Channel 1:** The bipolar line output signal, from TRing1 can be connected to this pin, via a 270-ohm resistor, in order to check for line driver failure. This pin is internally pulled "high".
76	MTIP1	I	**Monitor Tip Input - Channel 1:** The bipolar line output signal, from TTIP1 can be connected to this pin, via a 270-ohm resistor, in order to check for line driver failure. This pin is internally pulled "high".
77	TNData1	I	**Transmit Negative Data Input - Channel 1:** The XRT7302 will sample this pin, on the falling edge of TxClk1. If the device samples a "1" at this input pin, then it will generate and transmit a "negative" polarity pulse to the line. *NOTES:* 1. *This input pin will be ignored and should be tied to GND, if the Transmit Section is configured to accept "Single-Rail" data from the Terminal Equipment.* 2. *If the XRT7302 is operating in the "Host" Mode, then the user can (if desired) configure the XRT7302 to sample the TNData pin on either the rising or falling edge of TxClk.*
78	TPData1	I	**Transmit Positive Data Input - Channel 1** The XRT7302 will sample this pin, on the falling edge of TxClk. If the device samples a "1" at this input pin, then it will generate and transmit a "positive" polarity pulse to the line. *NOTES:* 1. *The data should be applied to this input pin if the "Transmit Section" is configured to accept Single-Rail data from the Terminal Equipment.* 2. *If the XRT7302 is operating in the "Host" Mode, then the user can (if desired) configure the XRT7302 to sample the TPData pin on either the rising or falling edge of TxClk.*
79	TxClk1	I	**Transmit Clock Input for TPData and TNData - Channel 1:** This input pin must be driven at 34.368 MHz (for E3 applications), 44.736 MHz (for DS3 applications), or 51.84 MHz (for SONET STS-1 applications). The XRT7302 will use this signal to sample the TPData and TNData input pins. By default, the XRT7302 will be configured to sample these two pins on the falling edge of this signal. If the XRT7302 is operating in the "Host" Mode, then the device can be configured to sample the TPData and TNData input pins on either the rising or falling edge of TxClk.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
80	TxOFF1	I	**Transmitter OFF Input - Channel 1:** Setting this input pin "high" configures the XRT7302 to turn off the Transmit Section within Channel 1. In this mode, the TTIP1 and TRing1 outputs will be tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP1 and TRING2 outputs, even when the XRT7302 is operating in the "Host" Mode.* 2. *For Host Mode Operation, the user should tie this pin to GND, to turn-ON/turn-OFF the Transmitter via the Microprocessor Serial Interface.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65^{0}C to + 150^{0}C
Operating Temperature	- 40^{0}C to + 85^{0}C
Supply Voltage Range	-0.5V to +6.0V
Theta-JA	23° C/W
Theta-JC	5.32° C/W

NOTE: *The XRT7302 is assembled in a thermally enhanced package with an intergral Copper Heat Slug. The heat Slug is solder plated on the bottom of the package and is electrically connected to the Ground connections of the device. This Heat Slug can be soldered to the mounting board if desired, but must be isolated from any V_{DD} connections.*

ELECTRICAL CHARACTERISTICS (T$_A$ = 25^{0}C, V$_{DD}$ = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
V_{DDD}	DC Supply Voltage (Digital)	4.75	5	5.25	V
V_{DDA}	DC Supply Voltage (Analog)	4.75	5	5.25	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all "1s" DS3 Mode STS-1 Mode		335 360	400 440	mA mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA	0		0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA	2.8		V_{DD}	V
I_L	Input Leakage Current*			±10	µA

NOTE: ** Not applicable to pins with pull-down resistors.*

ELECTRICAL CHARACTERISTICS (CONTINUED) (TA = 25⁰C, VDD = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

	AC ELECTRICAL CHARACTERISTICS (SEE ƒIGURE 1)				
	TERMINAL SIDE TIMING PARAMETERS (SEE ƒIGURE 2 AND ƒIGURE 3)				
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
	TxClk1, TxClk2 Clock Duty Cycle (DS3/STS-1)	30	50	70	%
	TxClk1, TxClk2 Clock Duty Cycle (E3)	30	50	70	%
	TxClk1, TxClk2 Frequency (SONET STS-1)		51.84		MHz
	TxClk1, TxClk2 Frequency (DS3)		44.736		MHz
	TxClk1, TxClk2 Frequency (E3)		34.368		MHz
t_{RTX}	TxClk1, TxClk2 Clock Rise Time (10% to 90%)			4.0	ns
t_{FTX}	TxClk1, TxClk2 Clock Fall Time (90% to 10%)			4.0	ns
t_{TSU}	TPData/TNData to TxClk1, 2 Falling Set up time	3.0			ns
t_{THO}	TPData/TNData to TxClk1, 2 Falling Hold time	3.0			ns
t_{LCVO}	RxClk1, 2 to rising edge of LCV1, 2 output delay		2.5		ns
t_{TDY}	TTIP1, 2/TRing1, 2 to TxClk1, 2 Rising Propagation Delay time	0.6		14.0	ns
	RxClk1, RxClk2 Clock Duty Cycle	45	50	55	%
	RxClk1, RxClk2 Frequency (SONET STS-1)		51.84		MHz
	RxClk1, RxClk2 Frequency (DS3)		44.736		MHz
	RxClk1, RxClk2 Frequency (E3)		34.368		MHz
t_{CO}	RxClk1, 2 to RPOS1, 2/RNEG1, 2 Delay Time			4.0	ns
t_{RRX}	RxClk1, RxClk2 Clock Rise Time (10% to 90%)		2.0	4.0	ns
t_{FRX}	RxClk1, RxClk2 Clock Fall Time (10% to 90%)		1.5	3.0	ns
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

FIGURE 1. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES (TYPICAL CHANNEL SHOWN)
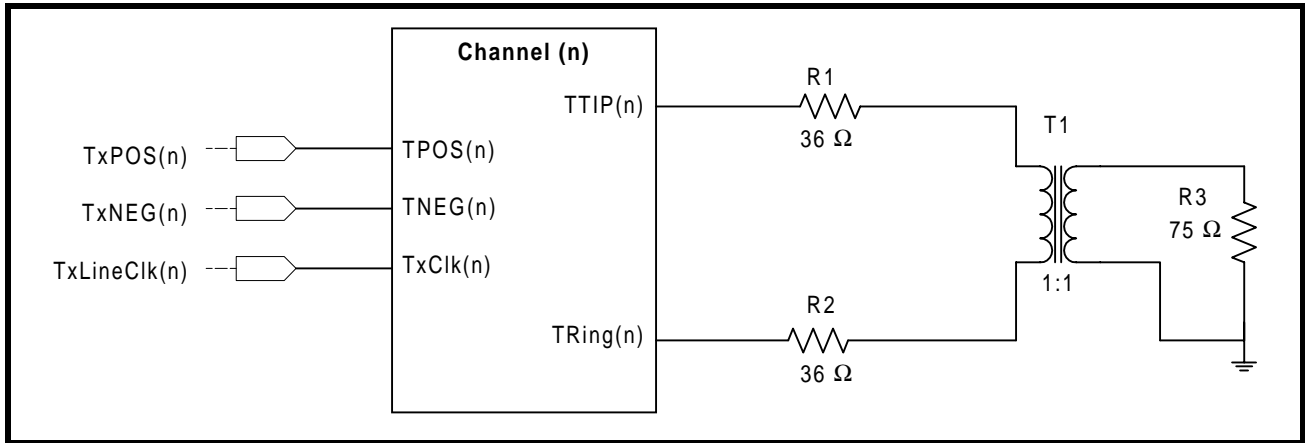
FIGURE 2. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE
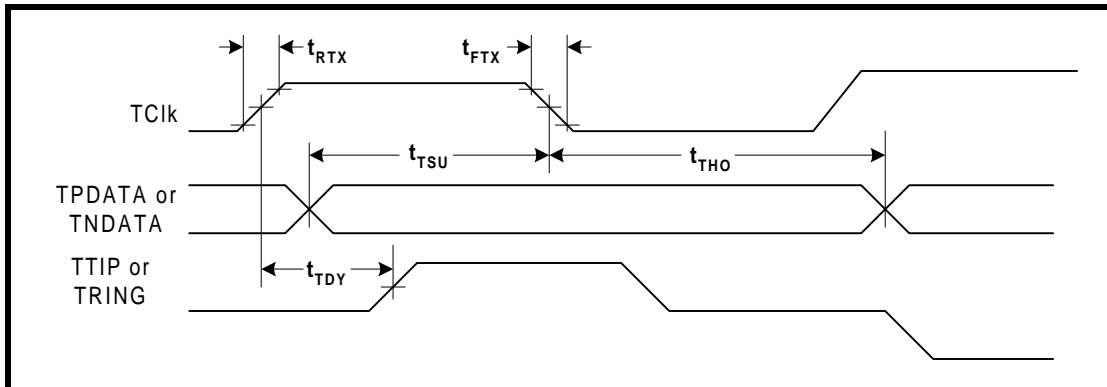
FIGURE 3. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE
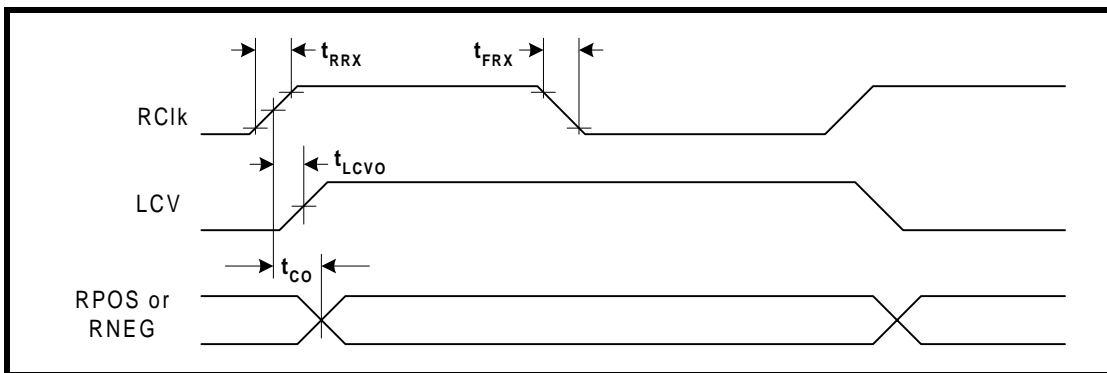
ELECTRICAL CHARACTERISTICS (CONTINUED), (TA = 25⁰C, VDD = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
LINE SIDE PARAMETERS E3 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE ƒIGURE 2)					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer, see Figure 1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UIpp
Receive Line Characteristics (See ƒigure 3)					
	Receive Sensitivity (Length of cable)	1100			feet
	Interference Margin	-20	-17		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10	100	255	UI
	Termination of LOS to LOS Clearance Time	10	100	255	UI
	Intrinsic Jitter (all "Ones" Pattern)[1]		0.01		UI
	Intrinsic Jitter (all "100" Pattern)		0.03		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	30			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	4			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.15			UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (TA = 25⁰C, VDD = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
LINE SIDE PARAMETERS SONET STS-1 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 2)					
	Transmit Output Pulse Amplitude (Measured with TxLEV=0, see Figure 1)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured with TxLEV=1, see Figure 1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UI
Receive Line Characteristics (See Figure 3)					

ELECTRICAL **C**HARACTERISTICS (**C**ONTINUED), (**T**A = 25⁰C, V**DD** = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS SONET STS-1 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 2)					
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
	Receive Sensitivity (Length of Table)	900			feet
	Signal Level to Declare Loss of Signal (LOSTHR = 0, REQ_IN = 1)			75	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0, REQ_IN = 1)	270			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1, REQ_IN = 1)			25	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1, REQ_IN = 1)	110			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 0, REQ_IN = 0)			55	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0, REQ_IN = 0)	210			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1, REQ_IN = 0)			90	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1, REQ_IN = 0)	90			mV
	Intrinsic Jitter (all "Ones" Pattern)[2]		0.03		UI
	Intrinsic Jitter (all "Ones" Pattern)		0.03		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.4			UI

(1) Measured with Equalizer enabled, 12db Cable attenuation, V$_{DD}$ = 5V and T$_A$ = 25°C

(2) Measured at nominal STSX-1 level with equalizer enabled, V$_{DD}$ = 5V and T$_A$ = 25°C

ELECTRICAL **C**HARACTERISTICS (**C**ONTINUED), (**T**A = 25⁰C, V**DD** = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS DS3 APPLICATION					
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
TRANSMIT CHARACTERISTICS (SEE ƒIGURE 2)					
	Transmit Output Pulse Amplitude (Measured a 0 feet, TxLEV=0, see Figure 1)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured a 0 feet, TxLEV=1, see Figure 1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UI
Receive Line Characteristics (See ƒigure 3)					

ELECTRICAL CHARACTERISTICS (CONTINUED), (TA = 25^{0}C, VDD = 5V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS DS3 APPLICATION					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Receive Sensitivity (Length of Cable)	900			feet
	Receive Intrinsic Jitter (All One's Pattern)		0.01		UI
	Receive Intrinsic Jitter (Using PRBS 2^{23-1} Pattern)		0.02		UI
	Signal Level to Declare Loss of Signal (LOSTHR = 0, REQ_IN = 1)			55	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0, REQ_IN = 1)	220			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1, REQ_IN = 1)			22	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1, REQ_IN = 1)	90			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 0, REQ_IN = 0)			35	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0, REQ_IN = 0)	155			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1, REQ_IN = 0)			17	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1, REQ_IN = 0)	70			mV
	Intrinsic Jitter (all "Ones" Pattern)		0.01		UI
	Intrinsic Jitter (all "100" Pattern)[1]				UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.4			UI

(1) Measured at nominal DSX3 level, Equalizer enabled, V_{DD} = 5V, T$_A$ = 25°C

ELECTRICAL CHARACTERISTICS (CONTINUED), (TA = 25⁰C, VDD = 5 ± 5%, UNLESS OTHERWISE SPECIFIED)

	MICROPROCESSOR SERIAL INTERFACE TIMING (SEE ƒIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	50			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SClk Hold Time	20			ns
t_{23}	SDI to Rising Edge of SClk Setup Time	50			ns
t_{24}	SDI to Rising Edge of SClk Hold Time	50			ns
t_{25}	SClk "Low" Time	240			ns
t_{26}	SClk "High" Time	240			ns
t_{27}	SClk Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SClk Hold Time	50			ns
t_{29}	$\overline{CS}$ "Inactive" Time	250			ns
t_{30}	Falling Edge of SClk to SDO Valid Time			200	ns
t_{31}	Falling Edge of SClk to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SClk, or rising edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

FIGURE 4. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE
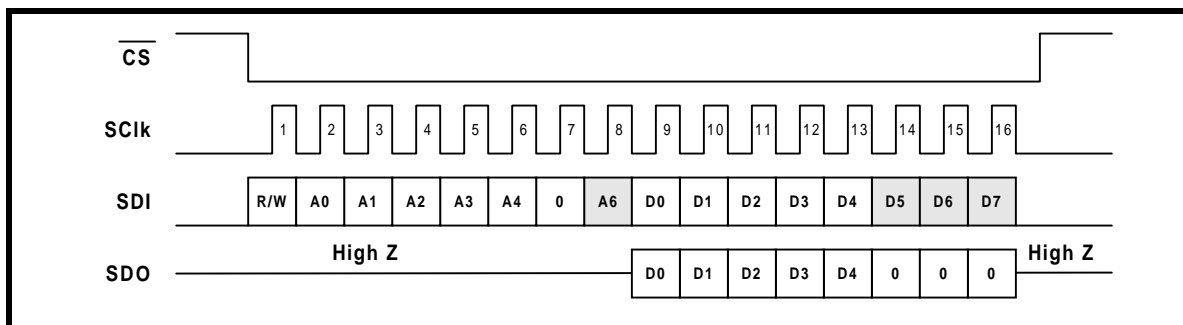
NOTES:

1. A4 and A5 are always "0".

2. R/W = "1" for "Read" Operations

3. R/W = "0" for "Write" Operations

4. A shaded pulse, denotes a "don't care" value.

FIGURE 5. **TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE**
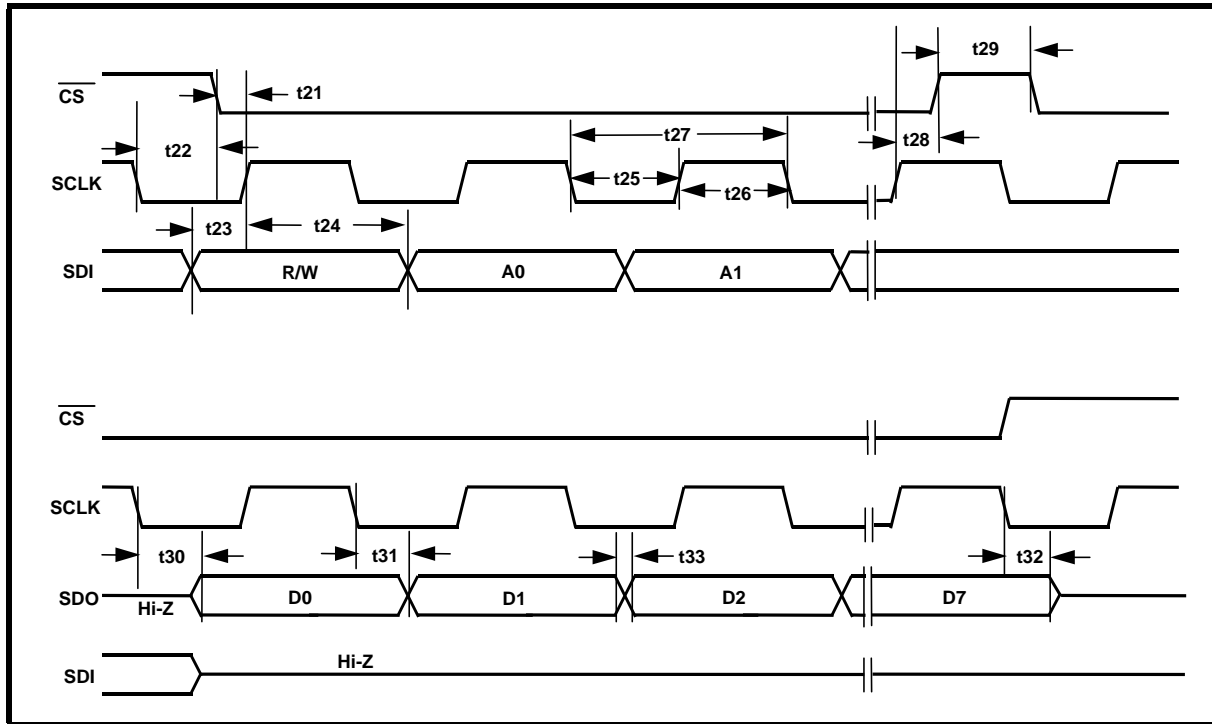
SYSTEM DESCRIPTION

A functional block diagram of the XRT7302 E3/DS3/STS-1 Transceiver IC is presented in Figure 6. In general, the XRT7302 contains three distinct sections:

- The Transmit Section - Channels 1 and 2
- The Receive Section - Channels 1 and 2
- The Microprocessor Serial Interface

Each of these sections are briefly discussed below.

THE TRANSMIT SECTION (CHANNELS 1 AND 2)

The Transmit Section, within each Channel, accepts TTL/CMOS level signals from the "Terminal Equipment" in either a "Single-Rail" or "Dual Rail" format. The Transmit Section will then take this data and do the following.

- Encode this data into the B3ZS format (if the DS3 or SONET STS-1 Modes have been selected) or into the HDB3 format (if the E3 Mode has been selected).
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drive these pulses onto the line via the TTIP and TRing output pins, across a 1:1 Transformer.

NOTE: *Note: The Transmit Section will drive a "1" (or a "Mark") onto the line by driving either a positive or negative polarity pulse across the 1:1 Transformer, within a given bit period. The Transmit Section will drive a "0" (or a "Space") onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION (CHANNELS 1 AND 2)

The Receive Section, within each Channel, receives a bipolar signal from the line, through the RTIP and RRing pins via a "1:1 Transformer" or via a "0.01µF Capacitor". The Receive Section will do the following.

- Adjust the signal level through an AGC circuit.
- Optionally equalize this signal for cable loss.
- The "sliced" data will be routed to the "HDB3/B3ZS" Decoder; during which the data content (as transmitted by the Remote Terminal Equipment) is restored to its original content.
- The recovered clock and data will be output to the "Local Terminal Equipment", in the form of CMOS level signals, via the RPOS, RNEG, RxClk1 and RxClk2 output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT7302 can be configured to operate in either the "Hardware" Mode or the "Host" Mode. Each of these modes will be discussed below.

THE HARDWARE MODE

When the XRT7302 is operating in the "Hardware Mode", then the following is true.

1. The Microprocessor Serial Interface block is disabled.
2. The XRT7302 is configured via input pin settings.

The XRT7302 can be configured to operate in the "Hardware Mode" by tying the "Host/$\overline{\text{HW}}$" input pin (pin 8) to GND.

Each of the pins associated with the Microprocessor Serial Interface will take on their alternative role, as defined in Table 1.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT7302 IS OPERATING IN THE "HARDWARE" MODE

PIN #	PIN NAME	FUNCTION, WHILE IN HARDWARE MODE
17	$\overline{\text{CS}}$/(ENDECDIS)	ENDECDIS
18	SClk/(RxOFF2)	RxOFF2
19	SDI/(RxOFF1)	RxOFF1
20	SDO/(E3_CH1)	E3_CH1
42	$\overline{\text{REGR}}$/(RClkINV)	RCKLKINV

Additionally, when the XRT7302 is operating in the "Hardware" Mode, all of the remaining input pins become active.

THE HOST MODE

The XRT7302 can be configured to operate in the "Host" Mode by tying the "Host/$\overline{\text{HW}}$" input pin (pin 8) to VDD.

When the XRT7302 is operating in the "Host Mode", then the following is true.

1. The Microprocessor Serial Interface block is enabled. Writing the appropriate data into the on-chip Command Registers makes many configuration selections.

2. All of the following input pins are disabled.

- Pin 1 - TxLEV1
- Pin 2 - TAOS1
- Pin 21 - STS-1/$\overline{\text{DS3}}$_Ch1
- Pin 24 - LLB1

- Pin 25 - RLB1
- Pin 30 - REQEN1
- Pin 31 - REQEN2
- Pin 36 - RLB2
- Pin 37 - LLB2
- Pin 39 - E3_Ch2
- Pin 41 - STS-1/$\overline{\text{DS3}}$_Ch2
- Pin 59 - TAOS2
- Pin 60 - TxLEV2

The user is advised to tie each of these pins to GND to operate the XRT7302 IC in the "Host" Mode.

In Host Mode Operation, the "TxOFF1" and "TxOFF2" input pins can still be used to turn on or turn off the "Transmit Output Drivers" within Channels 1 and 2, respectively. The intent behind this feature is to permit a system (designed for redundancy) to quickly switch out a defective line card, and switch-in the back-up line card.

The remainder of this document presents a detailed description of the features associated with the XRT7302.

FIGURE 6. FUNCTIONAL BLOCK DIAGRAM OF THE XRT7302

Notes: 1. (n) = 1 or 2 for the respective channel.
2. Serial Processor Interface pins are shared by both Channels in Host Mode and are redefined in Hardware Mode.
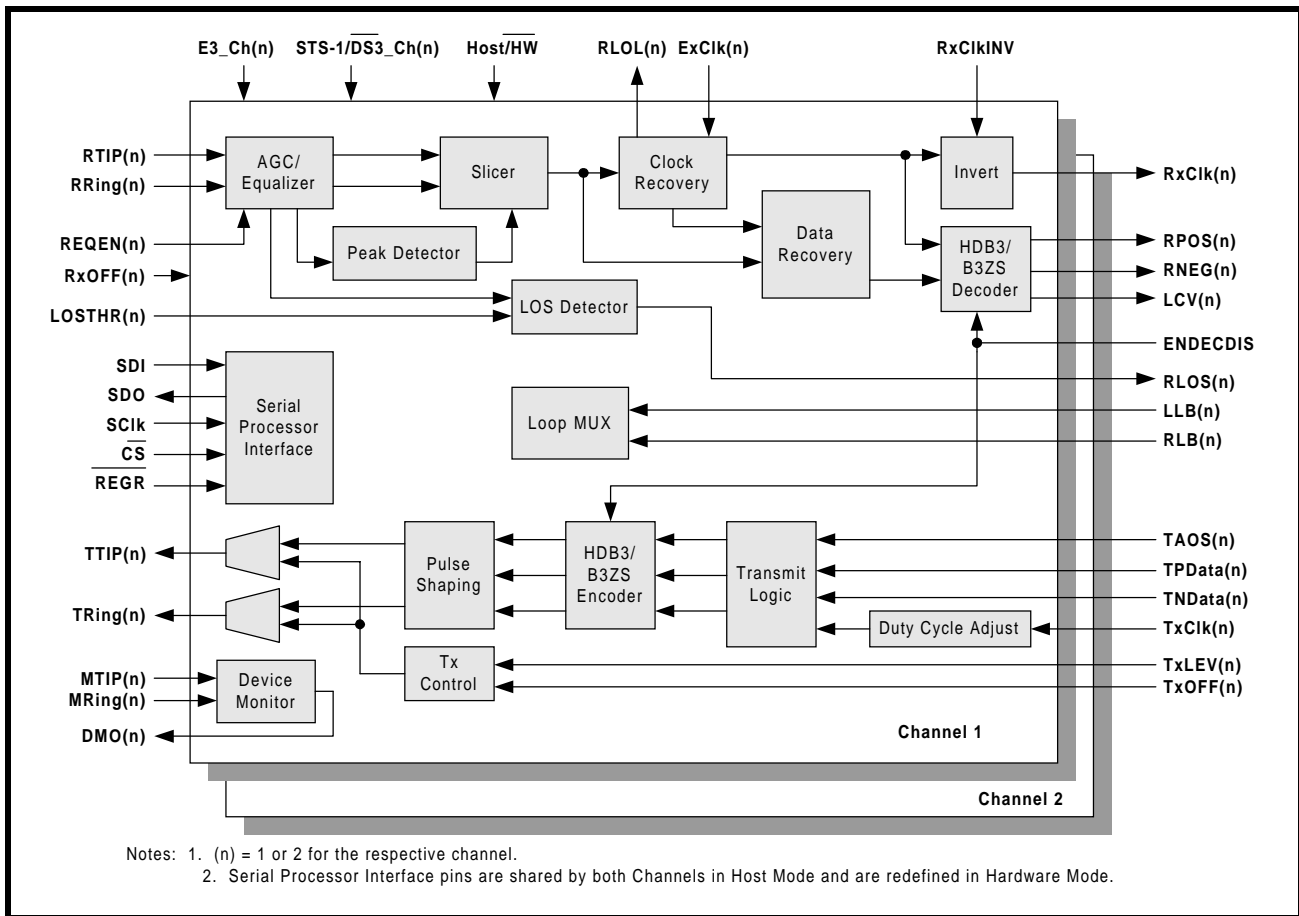
1.0   SELECTING THE DATA RATE

Each channel within the XRT7302 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Further, each channel can be configured to operate in a mode/data rate that is independent of the other channel.

The XRT7302 permits the user to select the data rate (for each Channel) via one of two ways.

1.1   CONFIGURING CHANNEL 1

a. When operating in the "Hardware" Mode.

In order to configure Channel 1 into the appropriate mode, the user must set the "E3_Ch1", and the "STS-1/$\overline{\text{DS3}}$_Ch1 input pins to the appropriate logic states, as presented below in Table 2.

TABLE 2: SELECTING THE DATA RATE FOR CHANNEL 1, (WITHIN THE XRT7302), VIA THE "E3_CH1" AND "STS-1/$\overline{DS3}$_CH1" INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3_CH1 PIN (PIN 20)	STATE OF STS-1/($\overline{DS3}$_CH1) PIN (PIN 21)	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

b. When operating in the "Host" Mode.

In order to configure Channel 1 into the appropriate mode, the user must write the appropriate values into the "STS-1/$\overline{DS3}$_Ch1" and "E3_Ch1" bit-fields, within Command Register CR4, as illustrated below.

COMMAND REGISTER, CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/($\overline{DS3}$_Ch1)	E3_Ch1	LLB1	RLB1
x	x	x	x	x

Table 3 relates the values of these two bit-fields to the selected data rates.

TABLE 3: SELECTING THE DATA RATE FOR CHANNEL 1 (WITHIN THE XRT7302); VIA THE "STS-1/$\overline{DS3}$_CH1" AND THE "E3_CH1" BIT-FIELDS, WITHIN COMMAND REGISTER CR4 (HOST MODE)

SELECTED DATA RATE	STS-1/($\overline{DS3}$_CH1) (D3)	"E3_CH1" (D2)
E3	X (Don't Care)	1
DS3	0	0
STS-1	1	0

By making these selections, the user is doing the following:

• Configuring the VCO Center Frequency of the Clock Recovery Phase-Locked-Loop (within Channel 1) to match the selected data rate.

• Configuring the "B3ZS/(HDB3)" Encoder and Decoder blocks to support B3ZS Encoding/Decoding, if the DS3 or STS-1 data rates were selected; or

• Configuring the "B3ZS/(HDB3)" Encoder and Decoder blocks to support HDB3 Encoding/Decoding, if the E3 data rate was selected.

• Configuring the on-chip "Pulse-Shaping" circuitry to generate Transmit Output pulses, of the appropriate shape and width to meet the applicable pulse template requirement.

• Establishes the LOS Declaration/Clearance Criteria (for Channel 1). (See section 3.6)

1.2 CONFIGURING CHANNEL 2

a. When operating in the "Hardware" Mode

In order to configure Channel 2 into the appropriate mode, the user must set the "E3_Ch2" and the "STS-1/($\overline{DS3}$_Ch2)" input pins to the appropriate logic states as presented below in Table 4.

TABLE 4: SELECTING THE DATA RATE FOR CHANNEL 2 (WITHIN THE XRT7302) VIA THE "E3_CH2" AND "STS-1/$\overline{DS3}$_CH2" INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3_CH2 PIN (PIN 39)	STATE OF STS-1/ ($\overline{DS3}$_CH2) PIN (PIN 41	MODE OF B3ZS/(HDB3) ENCODER/DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

b. When operating in the "Host" Mode.

In order to configure Channel 2 into the appropriate mode, the user must write the appropriate values into

the "STS-1/($\overline{DS3}$_Ch2)" and "E3_Ch2" bit-fields, within Command Register CR12, as illustrated below.

Table 5 relates the values of these two bit-fields to the selected data rates.

COMMAND REGISTER, CR12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
X	STS-1(/$\overline{DS3}$_Ch2)	E3_Ch2	LLB2	RLB2
x	x	x	x	x

TABLE 5: SELECTING THE DATA RATE FOR CHANNEL 2 (WITHIN THE XRT7302) VIA THE "E3_CH2" AND "STS-1/$\overline{DS3}$_CH2" BIT FIELDS, WITHIN COMMAND REGISTER CR4 (HOST MODE)

DATA RATE	STATE OF E3_CH2 PIN (PIN 39)	STATE OF STS-1/($\overline{DS3}$_CH2) PIN (PIN 41	MODE OF B3ZS/(HDB3) ENCODER/DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

By making these selections, the user is doing the following:

• Configuring the VCO Center Frequency of the Clock Recovery Phase-Locked-Loop (within Channel 2) to match the selected data rate.

• Configuring the "B3ZS/(HDB3)" Encoder and Decoder blocks to support B3ZS Encoding/Decoding, if the DS3 or STS-1 data rates were selected; or

• Configuring the "B3ZS/(HDB3)" Encoder and Decoder blocks to support HDB3 Encoding/Decoding, if the E3 data rate was selected.

• Configuring the on-chip "Pulse-Shaping" circuitry to generate Transmit Output pulses, of the appropriate shape and width to meet the applicable pulse template requirement.

• Establishes the LOS Declaration/Clearance Criteria (for Channel 2). (See section 3.6)

NOTE: *The user is required to apply the appropriate clock signals to both the EXClk1 and EXClk2 input pins, in order for the "Receive Sections" (of Channels 1 and 2) to function properly.*

2.0   THE TRANSMIT SECTION

Figure 6 indicates that the Transmit Section, within each Channel of the XRT7302 consists of the following blocks:

• Transmit Logic Block

• The TxClk Duty Cycle Adjust Block

• HDB3/(B3ZS) Encoder

• Pulse Shaping Block

Each of these blocks will be discussed in some detail below

In general, the purpose of the "Transmit Section", within each Channel of the XRT7302, is to take TTL/CMOS level data, from the terminal equipment, and encode it into a format such that it can:

1. Be efficiently transmitted over coaxial cable; at E3, DS3, or STS-1 data rates; and

2. Be reliably received by the Remote Terminal Equipment at the other end of the E3, DS3, or STS-1 data link.

3. Comply with the applicable pulse template requirements.

The circuitry that the Transmit Section, (within each Channel of the XRT7302) takes to accomplish this goal is discussed below.

NOTE: *The following discussion applies equally to both Channels 1 and 2. Hence, the Transmit Section signals will be referred to via their generic rates (e.g., TxClk) as opposed to "TxClk1" and "TxClk2".*

2.1   THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single Rail (e.g., a binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

2.1.1   Accepting "Dual-Rail" Data from the Terminal Equipment

Whenever the XRT7302 accepts dual-rail data from the Terminal Equipment, it does so via the following input signals.

- **TPData**

- **TNData**

- **TxClk**

Figure 7 presents an illustration of the typical interface for the transmission of data in a "Dual-Rail" Format between the Terminal Equipment and the Transmit Section of the XRT7302.

FIGURE 7. ILLUSTRATION OF THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL RAIL FORMAT, FROM THE "TRANSMITTING" TERMINAL EQUIPMENT TO THE "TRANSMIT SECTION" OF A CHANNEL WITHIN THE XRT7302
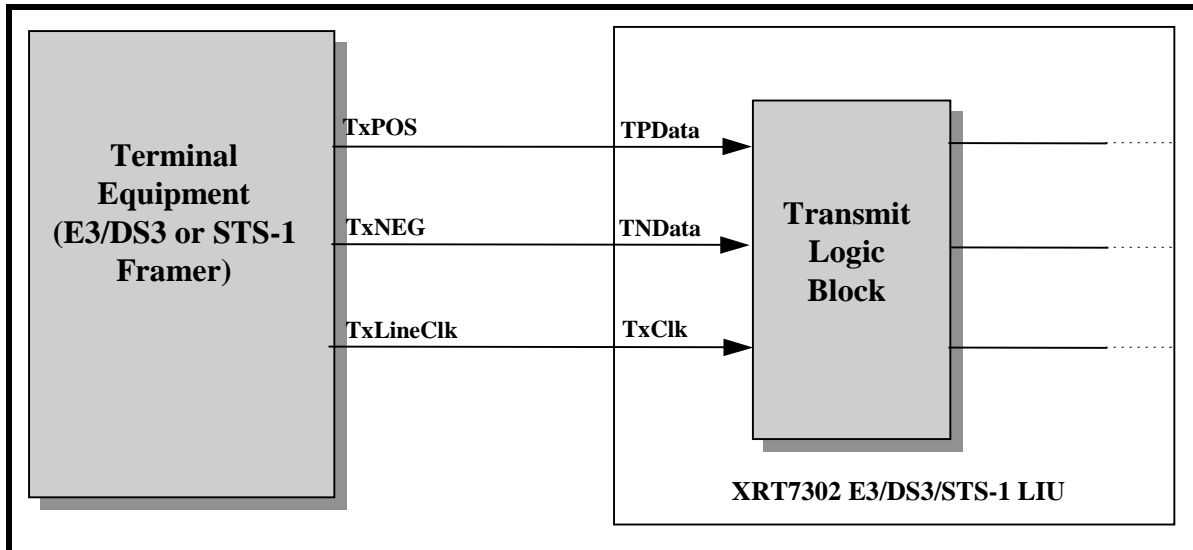
The manner that the LIU handles "Dual-Rail" data is described below and is illustrated in Figure 8. The Transmit Section (of a Channel) will typically sample the data on the TPData and TNData input pins on the falling edge of TxClk.

FIGURE 8. ILLUSTRATION ON HOW THE XRT7302 SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS
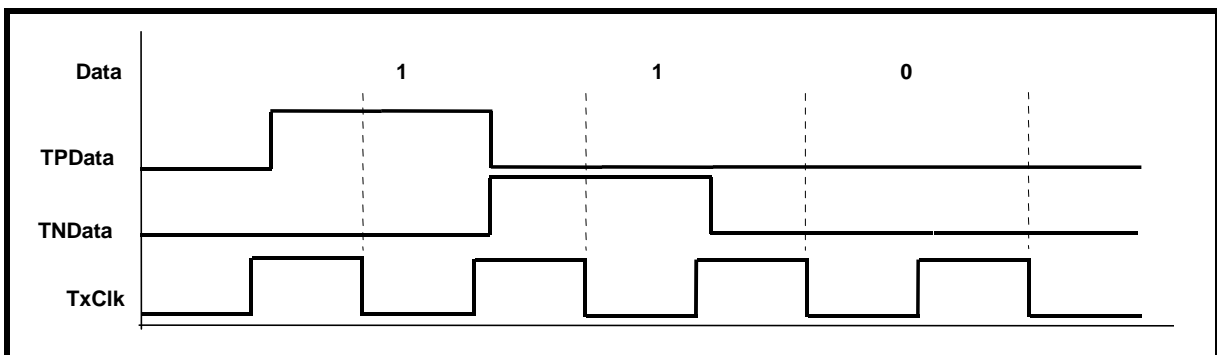
TxClk is typically a clock signal that is of the selected data rate frequency. For the E3 data rate, TxClk is 34.368 MHz. For the DS3 data rate, TxClk is 44.736 MHz, and for the SONET STS-1 rate, TxClk is 51.84 MHz. If the Transmit Section samples a "1" on the TPData input pin, then the "Transmit Section" of the device will ultimately generate a positive polarity pulse via the TTIP and TRing output pins (across a

1:1 transformer). Conversely, if the Transmit Section samples a "1" on the TNData input pin, then the "Transmit Section" of the device will ultimately generate a negative polarity pulse via the TTIP and TRing output pins (across a 1:1 transformer).

2.1.2   Accepting "Single-Rail" Data from the Terminal Equipment

If the user wishes to transmit data from the "Terminal Equipment" to the Transmit Section within a given channel in a "single-rail" format (e.g., a binary data stream), without having to convert it into a "dual-rail" format; the user can do the following.

a. Configure the XRT7302 to operate in the "Host" Mode.

b. Access the Microprocessor Serial Interface, and execute the following steps, for each Channel.

To Configure Channel 1 to accept Single-Rail Data from the Terminal Equipment:

Write a "1" into the "TxBIN1" (TRANSMIT BINary) bit-field, within Command Register 1 (for Channel 1), as depicted below.

COMMAND REGISTER 1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
x	x	x	x	1

NOTE: *Executing this write operating to Command Register 1 will not configure the Transmit Section (within Channel 2) to accept "Single-Rail" data from the Terminal Equipment.*

To Configure Channel 2 to accept Single-Rail Data from the Terminal Equipment:

Write a "1" into the "TxBIN2" bit-field, within Command Register 9 (for Channel 2), as depicted below.

COMMAND REGISTER 9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
x	x	x	x	1

NOTE: *Executing this write operating to Command Register CR9 will not configure the Transmit Section (within Channel 2) to accept Single-Rail data from the Terminal Equipment.*

The Transmit Section (of each channel) will sample this input pin on the "falling" edge of the TxClk clock signal, and will encode this data into the appropriate bipolar line signal across the TTIP and TRing output pins.

NOTES:

1. *In this mode, the Transmit Logic Block will ignore the TNData input pin.*

2. *If the user configures the Transmit Section (within a given channel) to accept "Single-Rail" data from the Terminal Equipment, then the user must enable the "B3ZS/HDB3" Encoder.*

Figure 9 Illustrates the behavior of the TPData and TxClk signals, when the Transmit Logic Block has been configured to accept "single-rail" data from the Terminal Equipment

FIGURE 9. ILLUSTRATION OF THE BEHAVIOR OF THE TPDATA AND TXCLK INPUT SGNALS, WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT
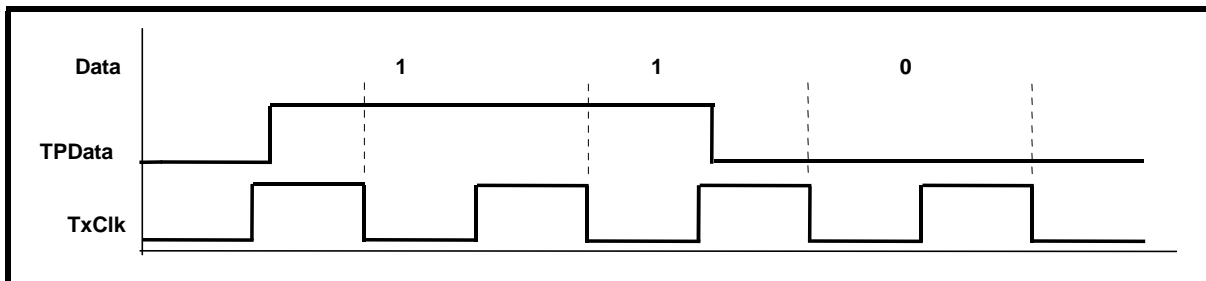
2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip "Pulse-Shaping" circuitry (within the Transmit Section of each Channel in the XRT7302) generates pulses of the appropriate shapes and width, in order to meet the applicable pulse template requirement. The widths of these "output" pulses are defined by the width of the "half-period" pulses within the TxClk signal.

However, if the widths of the pulses, within the TxClk clock signal are allowed to vary significantly, this could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, and thereby failing the applicable "Pulse Template" requirement specification.   As consequence, the chip's ability to generate compliant pulses could depend upon the duty cycle of the clock signal, applied to the TxClk input pin.

The Transmit Clock Duty Cycle Adjust Circuitry accepts clock pulses from the TxClk input pin with duty cycles ranging from 30% to 70%, and to regenerate these signals at a 50% duty cycle.

2.3 THE HDB3/B3ZS ENCODER BLOCK

The purpose of the "HDB3/B3ZS" Encoder Block is to aid in the "Clock Recovery" process (at the Remote Terminal Equipment) by ensuring an upper limit on the number of consecutive zeros that can exist within the line signal.

2.3.1 B3ZS Encoding

If the user has configured the XRT7302 to operate in the DS3 or SONET STS-1 Modes, then the "HDB3/B3ZS" Encoder blocks will operate in the "B3ZS" Mode. When the Encoder is operating in this mode, it will parse through and search the "Transmit Binary Data Stream" (from the Transmit Logic Block) for the occurrence of three (3) consecutive zeros (e.g., "000"). If the "B3ZS Encoder" finds an occurrence of three consecutive zeros, then it will substitute these three "0s", with either a "00V" or a "B0V" pattern.

Where:

"B" represents a "Bipolar" pulse that is compliant with the "Alternating Polarity" requirements of the AMI (Alternate Mark Inversion) line code; and

"V" represents a "bipolar Violation" (e.g., a "bipolar" pulse that violates the "Alternating Polarity" requirements of the AMI line code).

The B3ZS Encoder will decide whether to substitute with either the "00V" or the "B0V" pattern in order to insure that an odd number of "bipolar" pulses exist between any two consecutive "violation" pulses.

Figure 10 illustrates the "B3ZS Encoder" operation, with two separate strings of three (or more) consecutive zeros.

FIGURE 10. AN EXAMPLE OF B3ZS ENCODING
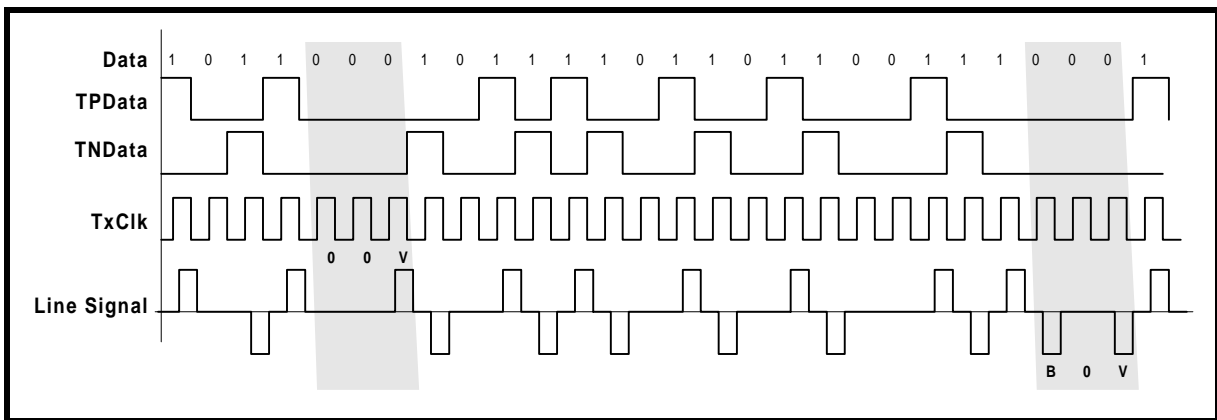
2.3.2 HDB3 Encoding

If the user has configured the XRT7302 to operate in the "E3 Mode", then the "HDB3/B3ZS" Encoder blocks will operate in the "HDB3" Mode. When the Encoder is operating in this mode, it will parse through and search the "Transmit Data Stream" (from the Transmit Logic Block) for the occurrence of four (4) consecutive zeros (e.g., "0000"). If the "HDB3 Encoder" finds an occurrence of four consecutive zeros,

then it will substitute these four "0s", with either a "000V" or a "B00V" pattern. The HDB3 Encoder will decide whether to substitute with either the "000V" or the "B00V" pattern in order to insure that an odd number of "bipolar" pulses exist between any two consecutive "violation" pulses.

Figure 11 illustrates the "HDB3 Encoder" operation, with two separate strings of four (or more) consecutive zeros.

FIGURE 11. AN EXAMPLE OF HDB3 ENCODING
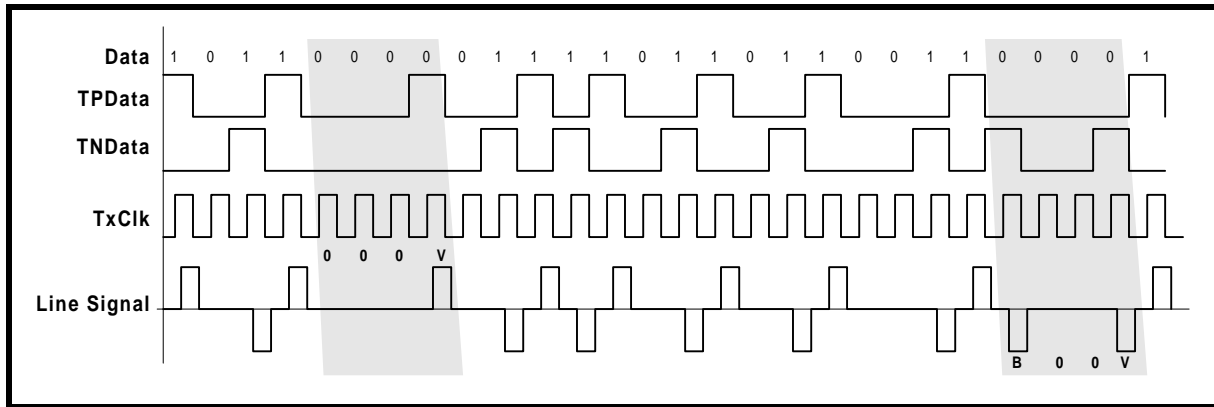
2.3.3 Disabling the "HDB3/B3ZS" Encoder

The XRT7302 permits the user to disable the "HDB3/B3ZS" Encoder by two means.

When the XRT7302 is operating in the "Hardware" Mode.

The "HBD3/B3ZS Encoder" blocks (within both channels) are disabled by setting the "ENDECDIS (Encoder/Decoder Disable)" input pin (pin 17) to "0".

NOTE: *By executing this step, the user will globally disable the "HDB3/B3ZS" Encoder and Decoder blocks within each channel of the XRT7302.*

When the XRT7302 is operating in the "Host" Mode.

Configuring Channel 1

When the XRT7302 is operating in the "Host" Mode, then the "HDB3/B3ZS" Encoders (within each channel) can be individually enabled or disabled. The user can disable the "HDB3/B3ZS Encoder" block within Channel 1 by setting the "ENDECDIS1" bit-field, within Command Register (CR2), to "1" as illustrated below.

COMMAND REGISTER, CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
X	1	X	X	X

Configuring Channel 2

Likewise, the user can disable the "HDB3/B3ZS Encoder" block within Channel 2 by writing a "1" into the "ENDECDIS2" bit-field within Command Register CR10, as illustrated below.

COMMAND REGISTER, CR10 (ADDRESS = 0X0A)

D4	D3	D2	D1	D0
Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
X	1	X	X	X

NOTE: *Note: This method can only be used if the XRT7302 is operating in the "Host" Mode.*

If the user employs either of these two methods to disable the "HDB3/B3ZS" Encoder, then the LIU will be transmitting the data, onto the line, as it is received via the TPData and TNData input pins.

2.4 THE TRANSMIT PULSE SHAPING CIRCUITRY

The Transmit Pulse Shaper Circuitry consists of a Transmit Line Build-Out circuit which can be enabled or disabled, by setting the TxLEV input pin (or "TxLEV" bit-field) to "HIGH" or "LOW". The purpose of the "Transmit Line Build-Out" circuit is to permit the user to configure each channel within the XRT7302 to transmit an output pulse which is compliant to either of the following pulse template requirements (when measured at the Digital Cross Connect System). Each of these Bellcore specifications further state that the cable length (between the Transmit Output

and the Digital Cross Connect system) can range anywhere from 0 to 450 feet.

The Isolated DSX-3 Pulse Template Requirement (per Bellcore GR-499-CORE) is illustrated in Figure 12.

FIGURE 12. THE "BELLCORE GR-499-CORE" TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS
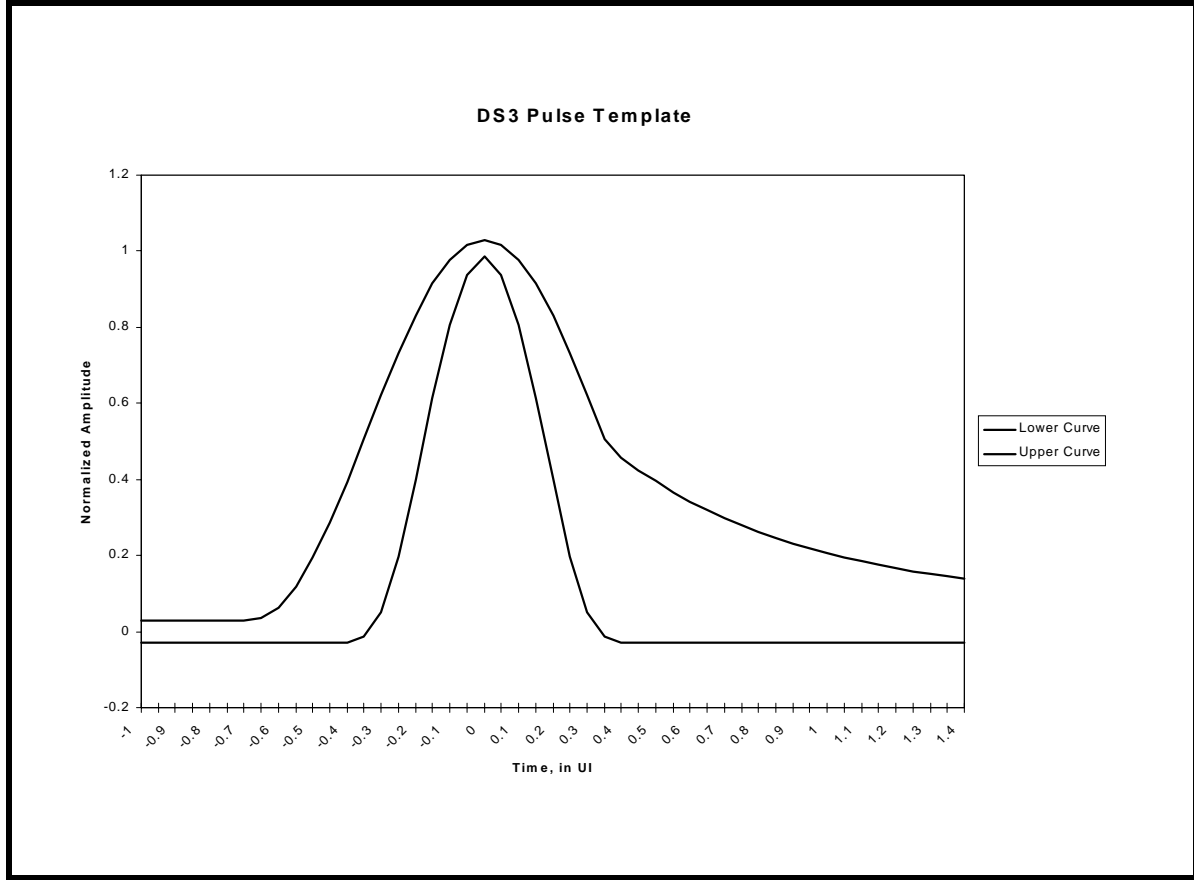
DS3 Pulse Template

The Isolated STSX-1 Pulse Template Requirement (per Bellcore GR-253-CORE), is illustrated in Figure 13.

FIGURE 13. THE "BELLCORE GR-253-CORE" TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS
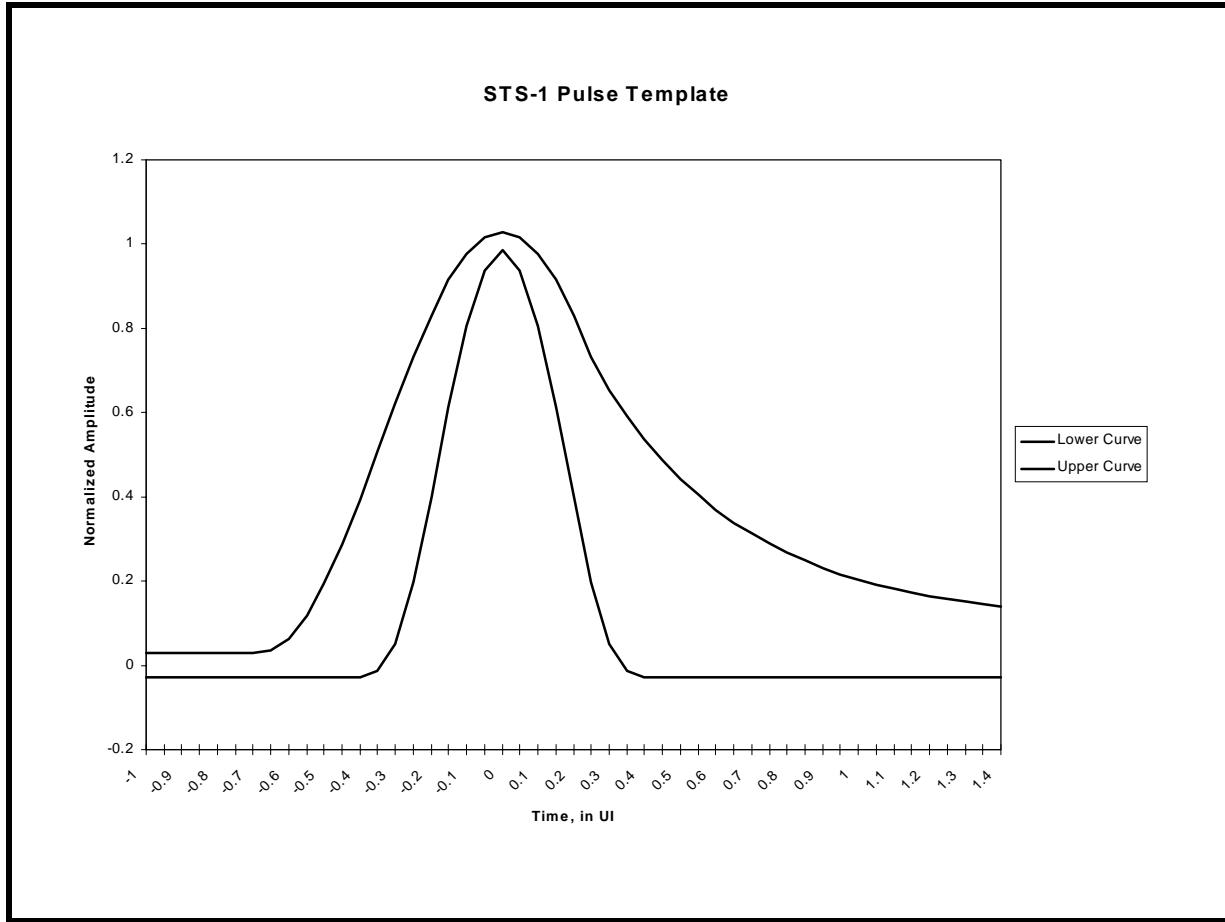
2.4.1   Enabling the Transmit Line Build-Out Circuit

If the user enables the "Transmit Line Build-Out" Circuit, then the "Transmit Section" of the Channel (within the XRT7302) will output shaped pulses onto the line via the TTIP and TRing output pins.

The user enables the Transmit Line Build-Out circuit (for each channel within the XRT7302) by doing the following:

Channel 1

In the "Hardware" Mode

• Set the "TxLEV1" input pin (pin 1) to "LOW"

And;

In the "Host" Mode

• Set the "TxLEV1" bit-field to "0", as illustrated below.

COMMAND REGISTER, CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0	X	X	0	X

Channel 2

In the "Hardware" Mode

• Set the "TxLEV2" input pin (pin 60) to "LOW".

In the "Host" Mode

And;

• Set the "TxLEV2" bit-field to "0", as illustrated below.

35

COMMAND REGISTER, CR9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0	X	X	0	X

2.4.2   Disabling the Transmit Line Build-Out Circuit

If the user disables the "Transmit Line Build-Out" circuit, then the XRT7302 will output un-shaped (e.g., square-wave) pulses onto the line via the TTIP and TRing output pins.

The user disables the Transmit Line Build-Out circuit (within the XRT7302) by doing the following:

Channel 1

In the "Hardware" Mode.

• Set the "TxLEV1" input pin (pin 1) to "HIGH".

And;

In the "Host" Mode.

• Set the "TxLEV1" bit-field to "1" as illustrated below.

COMMAND REGISTER, CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0	X	X	1	X

Configuring Channel 2

If the XRT7302 is operating in the "Hardware" Mode.

• Set the "TxLEV2" input pin (pin 60) to "HIGH".

And;

In the "Host" Mode.

• Set the "TxLEV2" bit-field to "1", as illustrated below.

COMMAND REGISTER, CR9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0	X	X	1	X

2.4.3   Design Guideline for Setting the Transmit Line Build-Out Circuit

The "TxLEV" input pins or bit-fields should be set based upon the overall cable length between the Transmitting Terminal and the Digital Cross Connect system (where the pulse template measurements are made).

If the cable length (between the Transmitting Terminal and the DSX-3 or STSX-1) is less than 225 feet

The user is advised to enable the "Transmit Line Build-Out circuit" by setting the "TxLEV" input pin or bit-field to "0".

NOTE: In this case, the configured channel (within the XRT7302) will output shaped (e.g., not square-wave) pulses onto the line via its TTIP and TRing output pins. The shape of this output pulse is such that it will comply with the pulse template requirements even when subjected to cable loss ranging from 0 to 225 feet.

If the cable length (between the Transmitting Terminal and the DSX-3 or STSX-1) is greater than 225 feet.

The user is advised to disable the "Transmit Line Build-Out circuit" by setting the "TxLEV" input pin or bit-field to "1".

NOTE: In this case, the configured channel (within the XRT7302) will output un-shaped (e.g., square-wave) pulses onto the line via the TTIP and TRing output pins. The cable loss, that these pulses will experience over long cable lengths (e.g., greater than 225 feet) will cause these pulses to be "properly shaped" and comply with the appropriate pulse template requirement.

2.4.4   The Transmit Line Build-Out Circuit and E3 Applications

The "ITU-T G.703 Pulse Template Requirements for E3" states that the E3 transmit output pulse should be measured at the Secondary Side of the Transmit Output Transformer, for "Pulse Template" compliance. In other words, there is no "Digital Cross Connect System" pulse template requirement for E3. As a consequence, the "Transmit Line Build-Out" circuit, within a given Channel (within the XRT7302), is disabled whenever that channel has been configured to operate in the E3 Mode.

2.5   INTERFACING THE TRANSMIT SECTIONS OF THE XRT7302 TO THE LINE

The E3, DS3, and SONET STS-1 specification documents all state that line signals transmitted over coaxial cable are to be terminated with 75 Ohm resistor. As a consequence, the user is encouraged to interface the "Transmit Section" of the XRT7302, in the manner as illustrated in Figure 14. Figure 14 indicates that the user should connect two 36 Ohm resistors in series with the primary side of the transformer. These two 36 Ohm resistors will closely match the 75 Ohm load termination resistor; thereby maximizing "Transmit Return Loss".

FIGURE 14. RECOMMENDED SCHEMATIC FOR INTERFACING THE TRANSMIT SECTION OF THE XRT7302 TO THE LINE
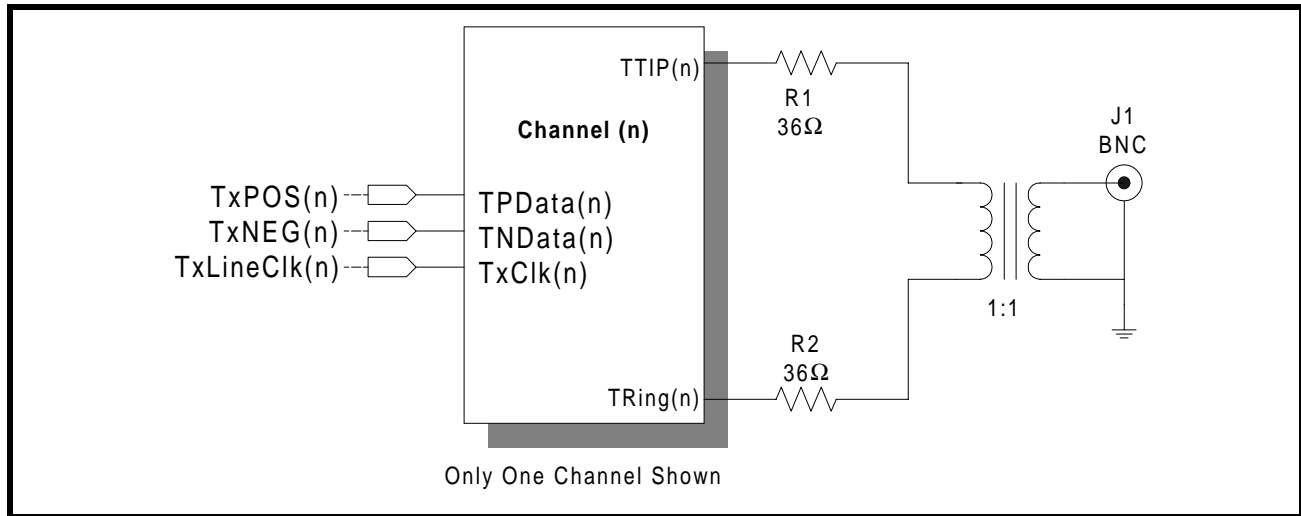
Transmit Transformer Recommendations

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	4µH
Isolation Voltage	1500Vrms
Leakage Inductance	0.06µH

PART #	INSULATION	PACKAGE TYPE
PE-68629	3000V	Large Thru-Hole
PE-65966	1500V	Small Thru-Hole
PE-65967	1500V	Small, SMT

PART #	INSULATION	PACKAGE TYPE
T3001	1500V	Small, SMT

TRANSFORMER VENDOR INFORMATION

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Singapore 368324

Tel: 65-287-8998

FAX: 65-280-0080

3.0   THE RECEIVE SECTION

Figure 6 indicates that the Receive Section, within the XRT7302 consists of the following blocks:

• Attenuator/Equalizer

• Peak Detector

• Slicer

• Clock Recovery PLL

• Data Recovery

• HDB3/B3ZS Decoder

Each of these blocks will be discussed in some detail below.

In general, the purpose of the "Receive Section" within the XRT7302 is to take an incoming attenuated/distorted bipolar signal, from the line, and to encode it back into the TTL/CMOS format where it can be received and processed by the Terminal Equipment.

3.1   INTERFACING THE RECEIVE SECTIONS OF THE XRT7302 TO THE LINE

The design of the Receive Circuitry within the XRT7302 permits the user to transformer-couple or capacitive-couple the Receive Section to the line. As mentioned earlier, the specification documents for E3, DS3, and STS-1 all specify 75 Ohm termination loads, when transmitting over coaxial cable. As a result, it is recommended to interface the "Receive Section" of the XRT7302 to the line in a manner as shown in Figure 15 and Figure 16.

FIGURE 15. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTION OF THE XRT7302 TO THE LINE (TRANSFORMER-COUPLING)
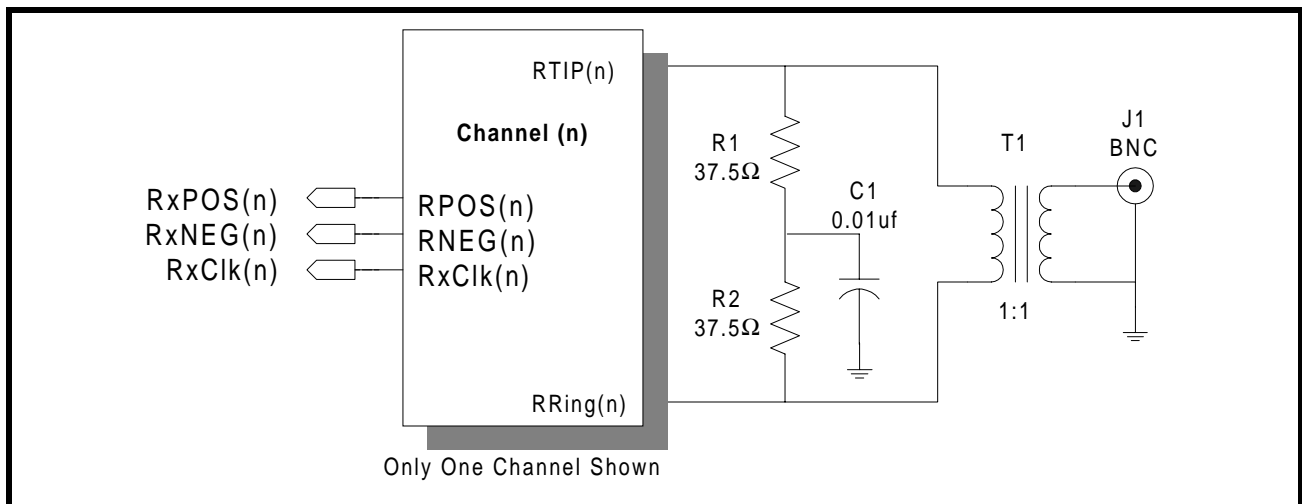
Receive Transformer Recommendations

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40μH
Isolation Voltage	1500Vrms
Leakage Inductance	0.6μH

PART #	INSULATION	PACKAGE TYPE
PE-68629	3000V	Large Thru-Hole
PE-65966	1500V	Small Thru-Hole
PE-65967	1500V	Small, SMT
T3001	1500V	Small, SMT

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Figure 16 presents the recommended schematic for capacitive-coupling each Receive Section of the XRT7302 to the line.

FIGURE 16. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTION OF THE XRT7302 TO THE LINE (CAPACITIVE-COUPLING) - (TYPICAL CHANNEL SHOWN)

.
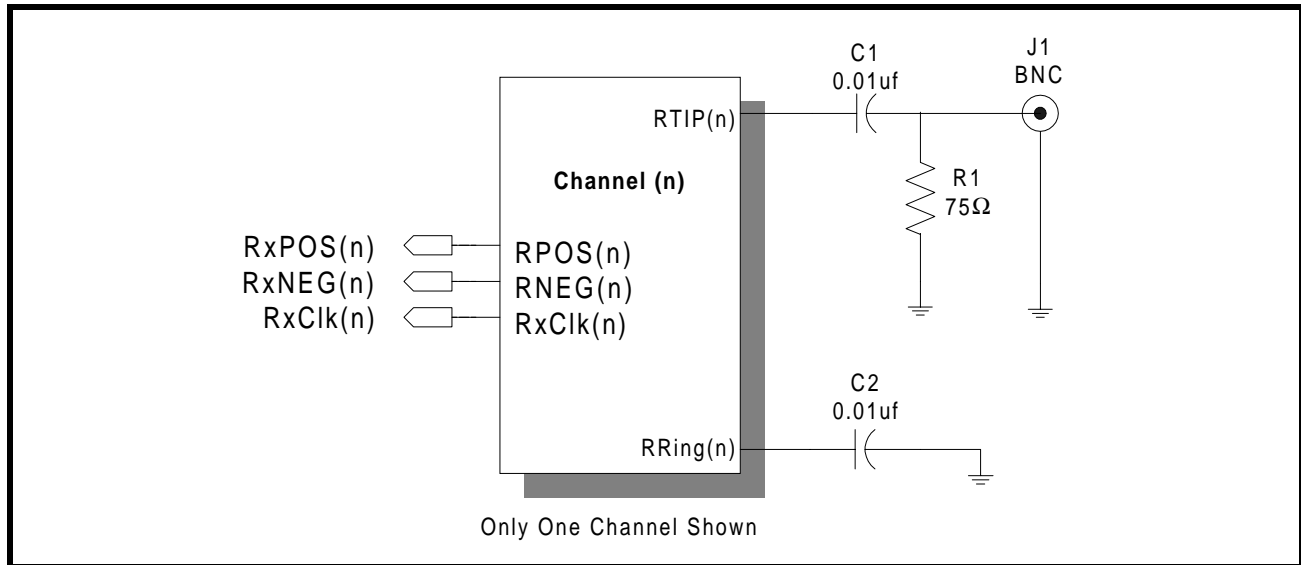
FIGURE 17. ILLUSTRATION OF THE TYPICAL APPLICATION FOR THE SYSTEM INSTALLER
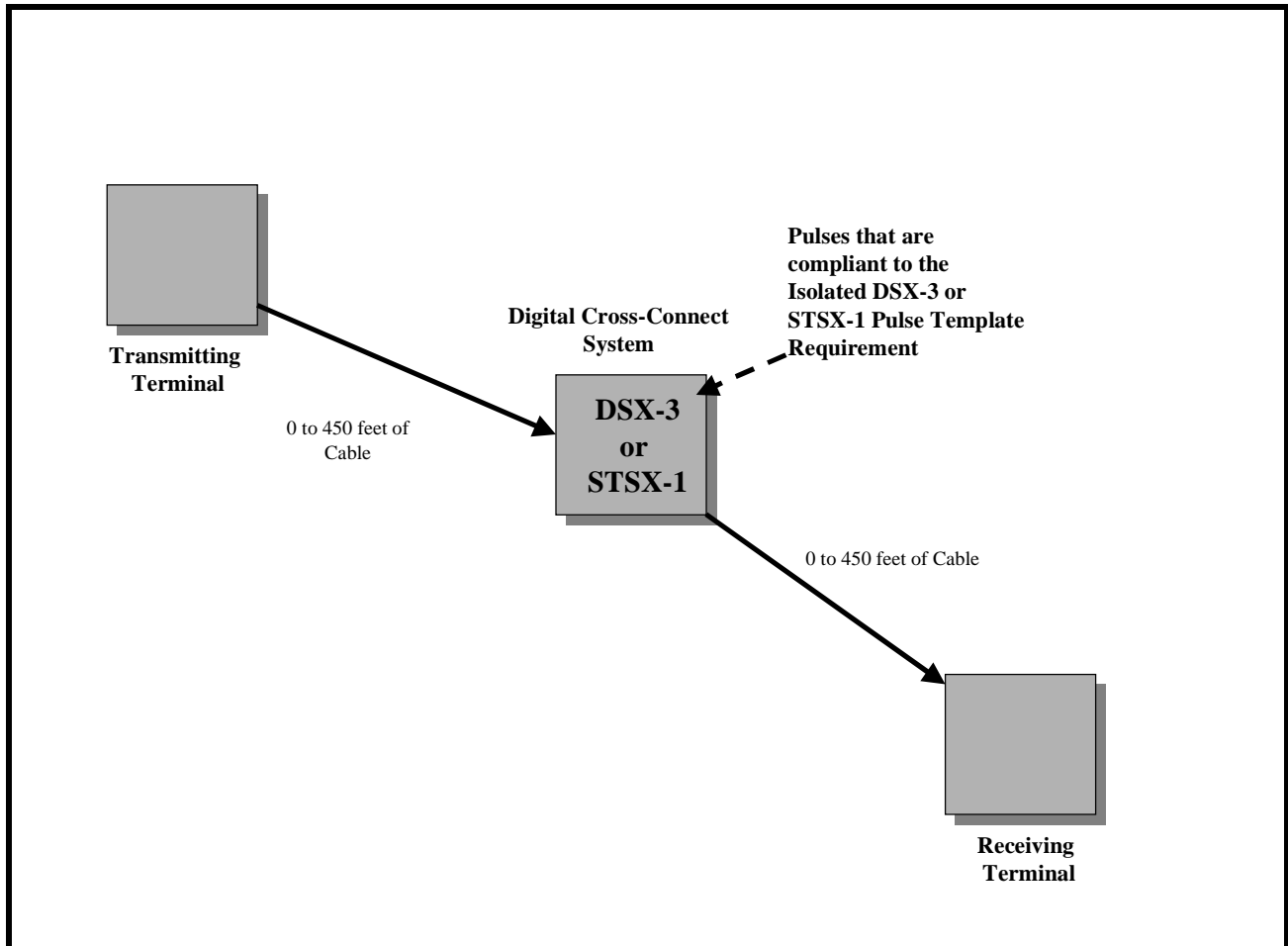
3.2   THE RECEIVE EQUALIZER BLOCK

Design Considerations (for DS3 and STS-1 Applications)

When installing equipment into environments as depicted in Figure 17, we recommend that the user enable the Receive Equalizer, by setting the "REQEN1" input pin (for Channel 1) or the "REQEN2" input pin (for Channel 2) "high", or the respective bit-fields to "1". In fact, the only time that the user should disable the Receive Equalizer is when an off-chip equalizer is in the Receive path between the Digital Cross-Connect system and the RTIP/RRing input pins, or in applications where the Receiver is monitoring the transmit output signal directly.

Design Considerations (for E3 Applications or if the Overall Cable Length is known)

Figure 17 indicates the following.

a. That the length of cable between the Transmitting Terminal and the Digital Cross-Connect system can range between 0 and 450 feet.

b. That the length of cable between the Digital Cross-Connect system and the Receive Terminal can range between 0 and 450 feet.

As a consequence, the overall cable length (between the Transmitting Terminal and the Receiving Terminal) can range between very short cable length (e.g., near 0 feet) up to 900 feet.

If, during System Installation, the overall cable length is known, then (in order to optimize the performance of the XRT7302, in terms of receive jitter performance, etc.) the user should enable or disable the Receive Equalizer, based upon the following recommendations.

As a guideline, the Receive Equalizer should be "turned ON", if the Receive Section (of a given channel) is going to receive a line signal with an overall cable length of 300 feet or greater. Conversely, the Re-

ceive Equalizer should be "turned OFF" if the Receive Section (of a given channel) is going to receive a line signal over a cable length of less than 300 feet.

NOTES:

1. *If the user turns "ON" the Receive Equalizer block (within a given Receive Section that is receiving a line signal over short cable length), he/she runs the risks of "over-equalizing" the received line signal which could degrade performance by increasing the amount of jitter that exists within the recovered data and clock signals, or by creating bit-errors.*

2. *The Receive Equalizer has been designed to counter the "frequency-dependent" (e.g., cable loss) that a line signal experiences as it travels from the transmitting terminal to the receiving terminal.*

However, Receive Equalizer was not designed to counter "flat loss" (e.g., where all of the Fourier frequency components within the line signal are subject to the same amount of attenuation). Flat loss is handled by the AGC block.

The user can disable the Receive Equalizer block by doing either of the following.

Configuring Channel 1

1. Setting the "REQEN1" input pin "low" (when operating in the "Hardware" Mode); or

2. Writing a "0" to the "REQEN1" bit-field within Command Register, CR2 (when operating the XRT7302 in the "Host" Mode), as illustrated below.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
RESERVED	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
X	X	X	X	0

Configuring Channel 2

1. Setting the "REQEN2" input pin "low" (when operating in the "Hardware" Mode); or

2. Writing a "0" to the "REQEN2" bit-field within Command Register, CR9 (when operating the XRT7302 in the "Host" Mode), as illustrated below.

COMMAND REGISTER CR10 (ADDRESS = 0X0A)

D4	D3	D2	D1	D0
RESERVED	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
X	X	X	X	0

3.3 PEAK DETECTOR AND SLICER

After the incoming line signal has passed through the Receive Equalizer block, it will next be routed to the "Slicer" block. The purpose of the "Slicer" block is to quantify a given bit-period (or symbol) within the incoming line signal as either a "1" or a "0".

3.4 CLOCK RECOVERY PLL

The output of the "Slicer" block (which is now dual-rail digital pulses) is routed to the Clock Recovery PLL. The purpose of the Clock Recovery PLL is to track the incoming "dual-rail" data stream and to derive and generate a "recovered clock signal".

It is important to note that the "Clock Recovery PLL" requires a "line rate" clock signal at the "EXClk" input pin.

The "Clock Recovery PLL" operates in one of two modes:

- The "Training" Mode.

- The "Data/Clock Recovery" Mode

Each of these modes will be briefly discussed below.

1. The Training Mode

If a given channel (within the XRT7302) is not receiving a line signal (via the "RTIP" and "RRing" input pins), or if the frequency difference between the line signal and that applied via the EXClk input pin exceeds 0.5%, then the channel will be operating in the "Training Mode". When the channel is operating in the "Training Mode", it will do the following:

a. Declare a "Loss of Lock" indication, by toggling its respective "RLOL" output pin "high".

b. Output a clock signal (via the RxClk1 and RxClk2 output pins) which is derived from the signal applied to the "EXClk" input pin.

2. The "Data/Clock Recovery" Mode

If the frequency difference between the line signal and that applied via the EXClk input pin is less than 0.5%, then the channel will be operating in the "Data/Clock Recovery" mode. In this mode, the "Clock Re-

covery" PLL will be "locked" onto the line signal (via the RTIP and RRing input pins).

3.5 THE HDB3/B3ZS DECODER

The Remote Transmitting Terminal, typically encodes the line signal into some sort of "Zero Suppression" Line Code (e.g., HDB3 for E3, and B3ZS for DS3 and STS-1). The purpose of this encoding activity was to aid in the Clock Recovery process, of this data, within the "Near-End" Receiving Terminal. However, once the data has made it across the E3, DS3 or STS-1 Transport Medium, and has been "recovered" by the Clock Recovery PLL, it is now necessary to restore the original content of the data. Hence, the purpose of the "HDB3/B3ZS Decoding" block is to restore the data (transmitted over the E3, DS3 or STS-1 line) to its original content prior to "Zero Suppression" Coding.

3.5.1 B3ZS Decoding (DS3/STS-1 Applications)

FIGURE 18. AN EXAMPLE OF B3ZS DECODING

If the XRT7302 is configured to operate in the DS3 or STS-1 Modes, then the "HDB3/B3ZS" Decoding Blocks will perform "B3ZS" Decoding. When the Decoders are operating in this mode, each of the Decoders will parse through its respective incoming "Dual Rail" data and check for the occurrence of either a "00V" or a "B0V" pattern. If the B3ZS Decoder detects this particular pattern, then it will substitute these bits with a "000" pattern.

NOTE: *If the B3ZS Decoder detects any bipolar violations that is not in accordance with the"B3ZS Line Code" format; or if the "B3ZS Decoder" detects a string of 3 (or more) consecutive "0s", in the incoming line signal, then the "B3ZS Decoder" will flag this event as a "Line Code Violation" by pulsing the "LCV" output pin "high".*

Figure 18 presents an illustration of the "B3ZS Decoder" at work, with two separate "Zero Suppression" patterns, in the incoming "Dual Rail Data Stream".

3.5.2 HDB3 Decoding (E3 Applications)

If the XRT7302 is configured to operate in the "E3 Mode" then each of the "HDB3/B3ZS" Decoding Blocks will perform "HDB3" Decoding. When the Decoders are operating in this mode, they will each parse through the incoming "Dual Rail" data and check for the occurrence of either a "000V" or a "B00V" pattern. If the HDB3 Decoder detects this particular pattern, then it will substitute these bits with a "0000" pattern.

Figure 19 presents an illustration of the "HDB3 Decoder" at work, with two separate "Zero Suppression" patterns, in the incoming "Dual Rail Data Stream".

FIGURE 19. AN EXAMPLE OF HDB3 DECODING
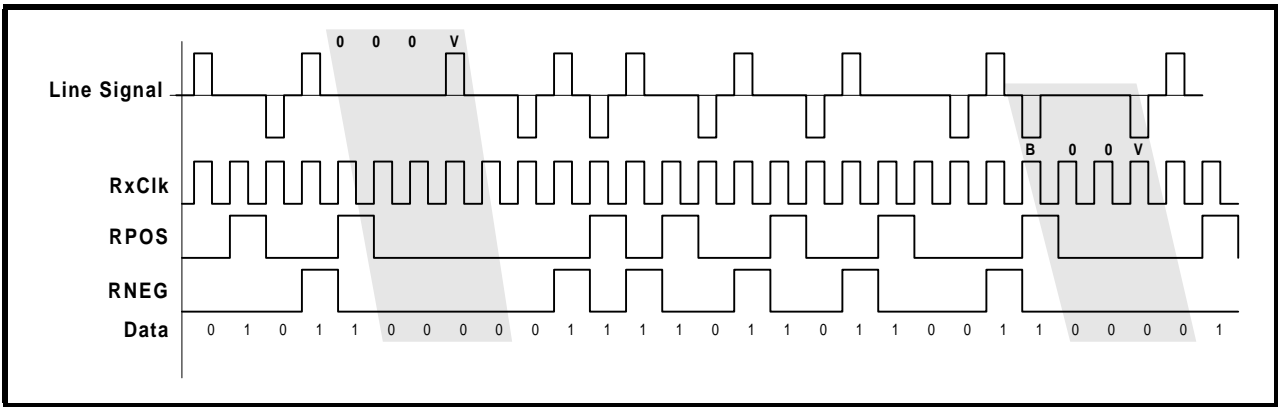
NOTE: If the HDB3 Decoder detects any bipolar violation (e.g., "V") pulses that is not in accordance with the "HDB3 Line Code" format, or if the "HDB3 Decoder" detects a string of 4 (or more) "0's" in the incoming line signal, then the "HDB3 Decoder" will flag this event as a "Line Code Violation" by pulsing the "LCV" output pin "high".

3.5.3   Configuring the HDB3/B3ZS Decoder

The "HDB3/B3ZS Decoder" blocks (within each Channel of the XRT7302) can be enable or disable by either of the following means.

If the XRT7302 is configured to operate in the "Host" Mode

Configuring Channel 1

The user can enable the "HDB3/B3ZS Decoder" block within Channel 1 by writing a "0" into the "ENDECDIS1" bit-field within Command Register CR2, as illustrated below.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Rserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
X	0	X	X	1

Likewise, the user can to disable the "HDB3/B3ZS Decoder" block within Channel 1, by writing a "1" into this bit-field.

Configuring Channel 2

The user can enable the "HDB3/B3ZS Decoder" block within Channel 2 by writing a "0" into the "ENDECDIS2" bit-field within Command Register CR10, as illustrated below.

COMMAND REGISTER CR10 (ADDRESS = 0X0A)

D4	D3	D2	D1	D0
Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
X	0	X	X	1

Likewise, the user can to disable the "HDB3/B3ZS Decoder" block within Channel 2 by writing a "1" into this bit-field.

If the XRT7302 is configured to operate in the "Hardware" Mode

The user can globally enable both "HDB3/B3ZS Decoder" blocks (within the XRT7302) by pulling the "ENDECDIS" input pin "low". Conversely, the user can globally disable both "HDB3/B3ZS Decoder" blocks (within the XRT7302) by pulling the "ENDEC-DIS" input pin "high".

3.6   LOS DECLARATION/CLEARANCE

Each channel (within the XRT7302) contains circuitry that will monitor the following two parameters associated with the incoming line signals.

1. The amplitude of the incoming line signal via the RTIP and RRing inputs; and

2. The number of pulses, detected (in the incoming line signal) within a certain amount of time.

If a given channel (within the XRT7302) determines that the incoming line signal is missing (either due to insufficient amplitude or a lack of pulses in the incoming line signal), then it will declare a "Loss of Signal" (LOS) condition. The channel (within the XRT7302) declares the LOS condition by toggling its respective RLOS output pin "high", and by setting its corresponding "RLOS" bit field, within Command Register 0 (or Command Register 8) to "1".

Conversely, if the channel (within the XRT7302) determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal); then it will clear the LOS condition by toggling its respective RLOS output pin

"low" and setting its corresponding "RLOS" bit-field to "0".

In general, the LOS Declaration/Clearance scheme that is employed within the XRT7302 is based upon ITU-T Recommendation G.775 for both E3 and DS3 applications.

3.6.1   The LOS Declaration/Clearance Criteria for E3 Applications

When the XRT7302 is operating in the "E3 Mode", a given channel will declare an LOS Condition if its "receive line" signal amplitude drops to -35dB or below. Further, the channel will clear the LOS Condition if its "receive line" signal amplitude rises back up to -15dB or above. Figure 20 presents an illustration of the signal levels at which each channel (within the XRT7302) will declare and clear LOS.

FIGURE 20. ILLUSTRATION OF THE SIGNAL LEVELS THAT THE XRT7302 WILL DECLARE AND CLEAR LOS
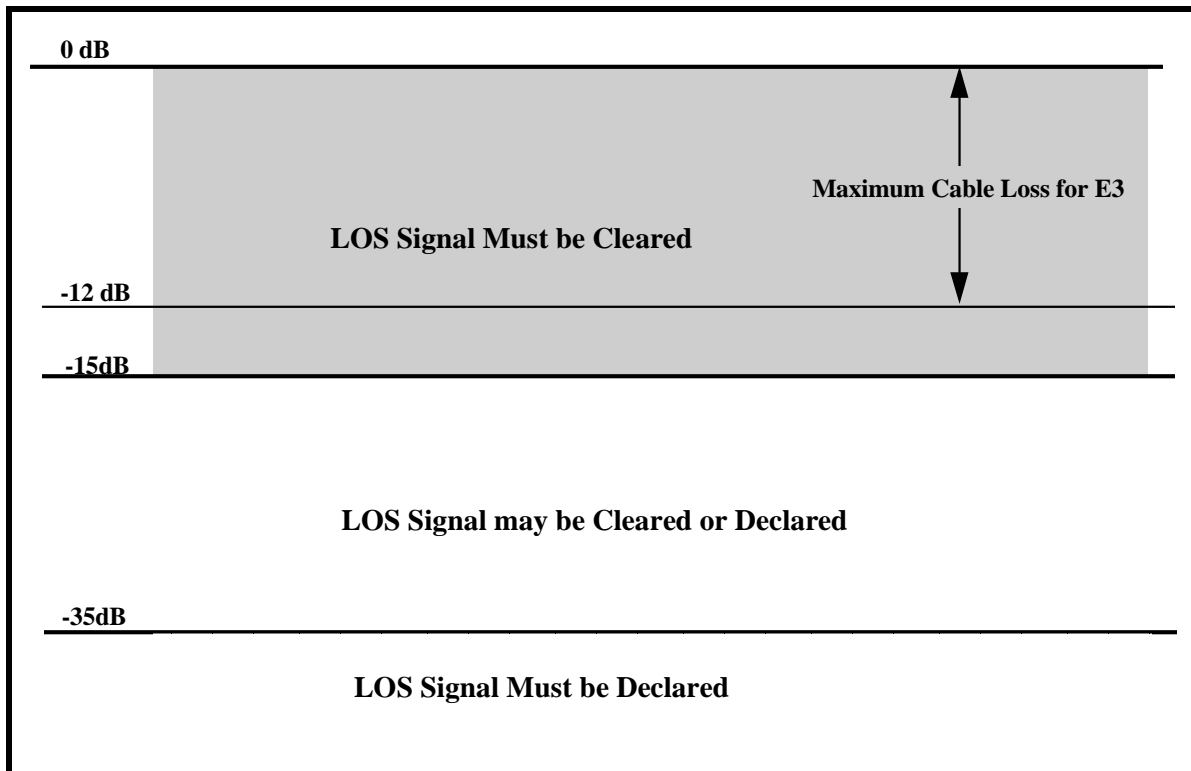
Timing Requirements associated with Declaring and Clearing the LOS Indicator

The XRT7302 was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, a channel (within the XRT7302) will declare an LOS, between 10 and 255 UI (or E3 bit-periods) after the actual time

the LOS condition occurred. Further, the channel will clear the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 21, illustrates the LOS Declaration and Clearance behavior, in response to first, the "Loss of Signal" event and then afterwards, the restoration of the signal.

FIGURE 21. THE BEHAVIOR THE LOS OUTPUT INDICATOR, IN RESPONSE TO THE LOSS OF SIGNAL, AND THE RESTORATION OF SIGNAL
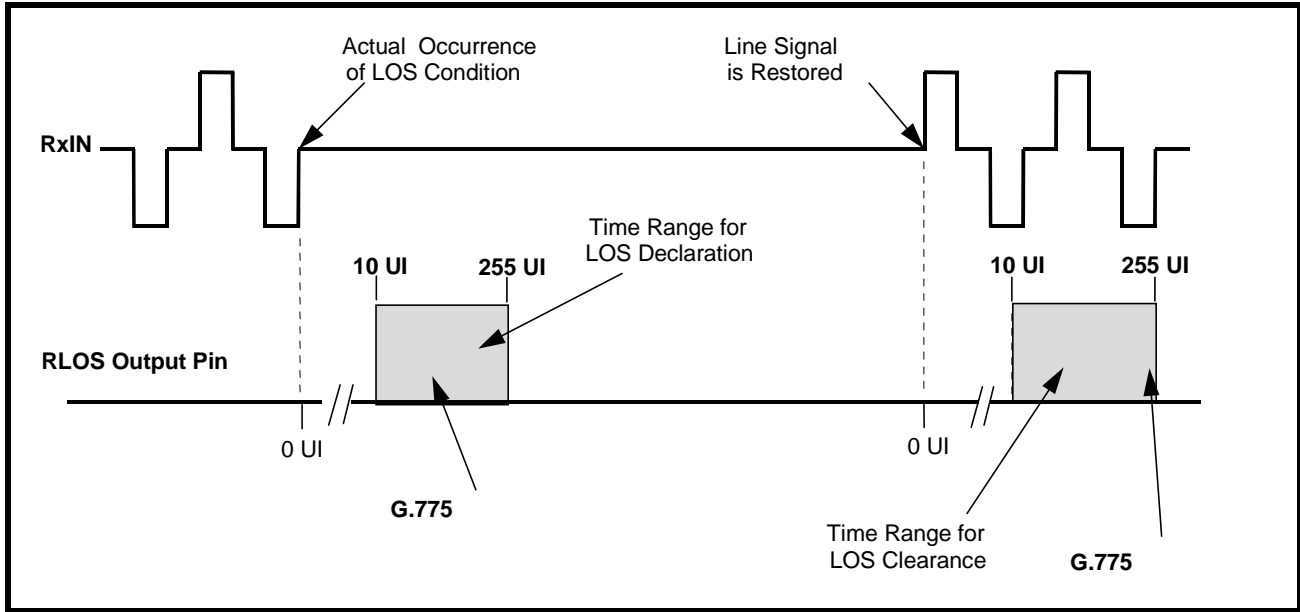
3.6.2 The LOS Declaration/Clearance Criteria for DS3 and STS-1 Applications

When the XRT7302 is operating in the DS3 or STS-1 Mode, then each channel (within the XRT7302) will declare and clear LOS based upon the following two criteria.

Analog LOS (ALOS) Declaration/Clearance Criteria

Digital LOS (DLOS) Declaration/Clearance Criteria

In the DS3 Mode, the LOS output (RLOS) is simply the logical "OR" of the ALOS and DLOS states. The Declaration/Clearance criteria for ALOS and DLOS are discussed below.

1. The Analog LOS (ALOS) Declaration/Clearance Criteria

A channel (within the XRT7302) will declare an "Analog LOS (ALOS) Condition if the amplitude of the incoming line signal drops below a specific amplitude as defined by the voltage at the LOSTHR input pin, and by whether the Receive Equalizer is enabled or not.

Table 6 presents the various voltage levels at the LOSTHR input pin, the state of the Receive Equalizer, and the corresponding ALOS (Analog LOS) threshold amplitudes.

TABLE 6: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS	SGNAL LEVEL TO CLEAR ALOS
DS3	1	0	$\leq$55mV	$\geq$220mV
	1	1	$\leq$22mV	$\geq$90mV
	0	0	$\leq$35mV	$\geq$155mV
	0	1	$\leq$17mV	$\geq$70mV
STS-1	1	0	$\leq$75mV	$\geq$270mV
	1	1	$\leq$25mV	$\geq$115mV
	0	0	$\leq$55mV	$\geq$210mV
	0	1	$\leq$20mV	$\geq$90mV

Declaring ALOS

A channel (within the XRT7302) will declare ALOS whenever the amplitude of the receive line signal falls below the "Signal Level to Declare ALOS" levels specified in Table 6.

Clearing ALOS

A channel (within the XRT7302) will clear ALOS whenever the amplitude of the receive line signal increases above the "Signal Level to Clear ALOS" levels specified in Table 6.

NOTE: There is approximately a 2dB hysteresis in the received signal level that exists between declaring and clearing ALOS, in order to prevent "chattering" in the RLOS output signal.

Monitoring the State of ALOS

If the XRT7302 is operating in the "Host" Mode, then the user can poll or monitor the state of ALOS, within Channel 1 by reading in the contents of Command Register 0. The bit-field of Command Register 0 is presented below.

COMMAND REGISTER 0, (ADDRESS = 0X00)

D4	D3	D2	D1	D0
RLOL1	RLOS1	ALOS1	DLOS1	DMO1
Read Only	Read Only	Read Only	Read Only	Read Only

Likewise, the user can also poll or monitor the state of ALOS, within Channel 2, by reading in the contents of Command Register 8. The bit-field of Command Register 8 is presented below.

COMMAND REGISTER 8, (ADDRESS = 0X08)

D4	D3	D2	D1	D0
RLOL2	RLOS2	ALOS2	DLOS2	DMO2
Read Only	Read Only	Read Only	Read Only	Read Only

If the "ALOS" bit-field contains a "1", then the corresponding channel is currently declaring an ALOS condition. Conversely, if the ALOS bit-field contains a "0", then the channel is not currently declaring an ALOS condition.

Disabling the ALOS Detector

For debugging purposes, it may be useful to be able to disable the ALOS Detector, within the XRT7302. If the XRT7302 is operating in the "Host" Mode, then the user can disable the ALOS Detector, (within Channel 1) by writing a "1" into the "ALOSDIS1" bit-field, within Command Register 2; as shown below.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
X	X	1	X	X

Likewise, the user can disable the ALOS Detector (within Channel 2) by writing a "1" into the "ALOSDIS2" bit-field, within Command Register 10; as depicted below.

COMMAND REGISTER CR10 (ADDRESS = 0X0A)

D4	D3	D2	D1	D0
Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
X	X	1	X	X

2. The Digital LOS (DLOS) Declaration/Clearance Criteria

A given channel (within the XRT7302) will declare a Digital LOS (DLOS) condition if the XRT7302 detects

160±32 or more consecutive "0s" in the incoming data.

The channel (within the XRT7302) will clear DLOS if it detects four consecutive sets of 32 bit-periods, each

of which containing at least 10 "1s" (e.g., average pulse density of greater than 33%).

Monitoring the State of DLOS

If the XRT7302 is operating in the "Host" Mode, then the user can poll or monitor the state of DLOS, within Channel 1 by reading in the contents of Command Register 0. The bit-field of Command Register 0 is presented below.

COMMAND REGISTER CR0, (ADDRESS = 0X00)

D4	D3	D2	D1	D0
RLOL1	RLOS1	ALOS1	DLOS1	DMO1
Read Only	Read Only	Read Only	Read Only	Read Only

Likewise, the user can also poll or monitor the state of DLOS within Channel 2, by reading in the contents of

Command Register 8. The bit-field of Command Register 8 is presented below.

COMMAND REGISTER CR8, (ADDRESS = 0X08)

D4	D3	D2	D1	D0
RLOL2	RLOS2	ALOS2	DLOS2	DMO2
Read Only	Read Only	Read Only	Read Only	Read Only

If the "DLOS" bit-field contains a "1", then the corresponding channel is currently declaring a DLOS condition. Conversely, if the DLOS bit-field contains a "0", then the channel is currently declaring the DLOS condition.

Disabling the DLOS Detector

For debugging purposes, it is useful to be able to disable the DLOS detector, within the XRT7302. If the XRT7302 is operating in the "Host" Mode, the user can disable the DLOS Detector, (within Channel 1) by writing a "1" into the "DLOSDIS1" bit-field, within Command Register 2, as depicted below.

COMMAND REGISTER CR2 (ADDRESS = 0X02

D4	D3	D2	D1	D0
Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
X	X	X	1	X

NOTE: *Setting both the "ALOSDIS1" and "DLOSDIS1" bit-fields to "1" will disable LOS Declaration by Channel 1.*

Likewise, the user can disable the DLOS Detector (within Channel 2) by writing a "1" into the

"DLOSDIS2" bit-field, within Command Register 10, as depicted below.

COMMAND REGISTER CR10 (ADDRESS = 0X0A

D4	D3	D2	D1	D0
Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
X	X	X	1	X

NOTE: *Setting both the "ALOSDIS2" and "DLOSDIS2" bit-fields to "1" will disable LOS Declaration by Channel 2.*

3.6.3   Muting the Recovered Data while the LOS is being Declared

In some applications it is not desirable for a channel (within the E3/DS3/STS-1 LIU) to recover data and route it to the "Receiving Terminal", while the channel is declaring an LOS condition. Consequently, the XRT7302 includes an "LOS Muting" feature. This feature (if enabled) will cause a given channel (within the XRT7302) to halt transmission of the recovered data (to the Receiving Terminal) while the LOS condition is "true". In this case, the RPOS and RNEG output pins will be forced to "0". Once the LOS condition

has been cleared, then the channel (within the XRT7302) will resume normal transmission of the recovered data to the "Receiving Terminal.

This feature is available whenever XRT7302 is operating in the Host Mode or Hardware Mode. The approach for configuring the "MUTing upon LOS" feature for both the Hardware and Host Modes are presented below.

Enabling and Disabling the "MUTing upon LOS" feature if the XRT7302 is operating in the Hardware Mode.

To enable the "MUTing upon LOS" feature, pull the "LOSMUTEN" output pin (pin 53) "high". Then, the

"MUTEing upon LOS" feature will be enabled globally for both channels within the XRT7302.

Enabling and Disabling the "MUTing upon LOS" feature if the XRT7302 is operating in the Host Mode.

The "MUTing upon LOS" feature for Channel 1can be enabled by writing a "1" into the "LOSMUT1" bit-field, within Command Register 3, as shown below.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RClk1_INV	Reserved
X	1	x	x	x

NOTES:

1. This step only enables the "MUTing upon LOS" feature within Channel 1.

2. Each channel, within the XRT7302, automaticallly declares an "LOS" (Loss of Signal) condition anytime it has been configured to operate in either the "Analog Local Loop-Back or "Digital Local Loop-Back" Modes. Consequently, the user the user must disable the "MUTing-upon-LOS" feature, prior to configuring the chip to operate in either of these local loop-back modes.

The "MUTing upon LOS" feature for Channel 2 can be enabled by writing a "1" into the "LOSMUT2" bit-field, within Command Register 11, as shown below.

COMMAND REGISTER CR11 (ADDRESS = 0X0B)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_2	LOSMUT2	RxOFF2	RClk2_INV	Reserved
X	1	x	x	x

NOTES:

1. This step only enables the "MUTing upon LOS" feature within Channel 1.

2. Each channel, within the XRT7302, automaticallly declares an "LOS" (Loss of Signal) condition anytime it has been configured to operate in either the "Analog Local Loop-Back or "Digital Local Loop-Back" Modes. Consequently, the user the user must disable the "MUTing-upon-LOS" feature, prior to configuring the chip to operate in either of these local loop-back modes.

3.7 ROUTING THE RECOVERED TIMING AND DATA INFORMATION TO THE "RECEIVING TERMINAL EQUIPMENT"

Each channel, within the XRT7302, ultimately takes the Recovered Timing and Data information, converts it into CMOS levels and routes it to the Receiving Terminal Equipment via the RPOS, RNEG and RxClk output pins.

Each channel, within the XRT7302 can "deliver" the recovered data and clock information (to the "Receiving Terminal") in either a "Single-Rail" or "Dual-Rail" format. Each of these methods are discussed below.

3.7.1 Routing "Dual-Rail" Format Data to the Receiving Terminal Equipment

Whenever a channel (within the XRT7302) delivers dual-rail format to the Terminal Equipment, it does so via the following signals.

• RPOS(n)

• RNEG(n)

• RxClk(n)

Figure 22 presents an illustration of the typical interface for the transmission of data in a "Dual-Rail" Format from the Receive Section of a channel (within the XRT7302) to the "Receiving Terminal Equipment"

.

FIGURE 22. ILLUSTRATION OF THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT, FROM THE "RECEIVE SECTION" OF THE XRT7302" TO THE RECEIVING TERMINAL EQUIPMENT
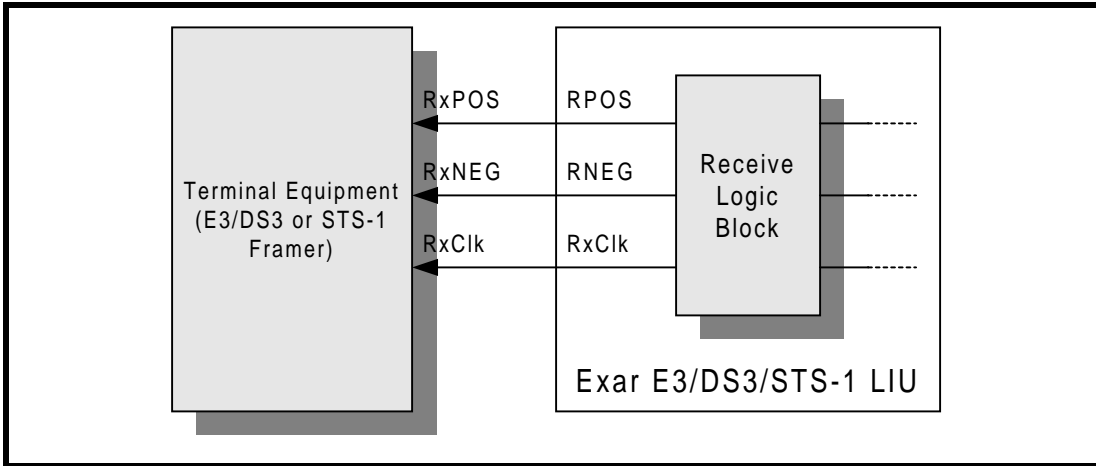
The manner that a given channel transmits "Dual-Rail" data (to the Receiving Terminal Equipment) is described below and is illustrated in Figure 23. Each channel (within the XRT7302) will typically update the data (on the RPOS and RNEG output pins) on the rising edge RxClk.

FIGURE 23. ILLUSTRATION ON HOW THE XRT7302 OUTPUTS DATA ON THE RPOS AND RNEG OUTPUT PINS
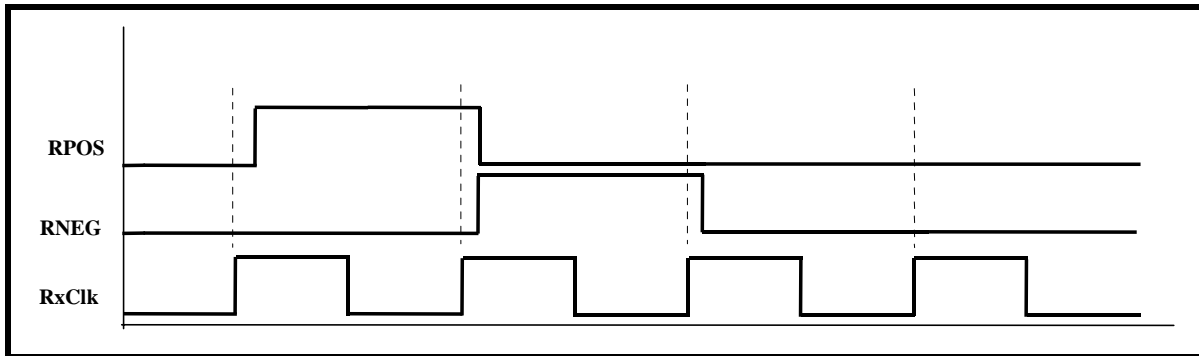
RxClk, is the Recovered Clock signal, from the incoming "Received" line signal. As a result, these clock signals are typically 34.368 MHz for E3 applications; 44.736 MHz for DS3 applications, and 51.84 MHz for SONET STS-1 applications.

In general, if a given channel (within the XRT7302) received a "positive-polarity" pulse in the incoming line signal (via the RTIP and RRing input pins), then the channel will pulse its corresponding RPOS output pin "high". Conversely, if the channel received a "negative-polarity" pulse in the incoming line signal (via the RTIP and RRing input pins), then the channel will pulse its corresponding RNEG output pin "high".

Inverting the RxClk1 and RxClk2 outputs

Both channels (within the XRT7302) can invert Rx-Clk(n) signals, with respect to the "delivery" of the "RPOS" and RNEG" output signals to the "Receiving Terminal Equipment". This feature may be useful for those customer whose "Receiving Terminal Equipment" logic design is such that the RPOS and RNEG data must be sampled on the rising edge of RxClk. Figure 24 illustrates the behavior of the RPOS,

RNEG, and RxClk signals, when the RxClk signal has been inverted.

FIGURE 24. ILLUSTRATION OF THE BEHAVIOR OF THE RPOS, RNEG, AND RXCLK(N) SIGNALS, WHEN RXCLK(N) IS INVERTED
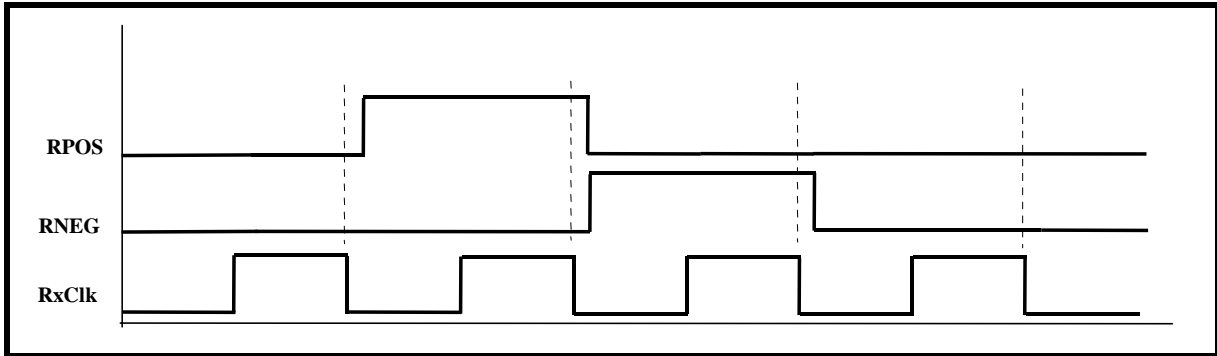
Inverting the RxClk Signals via the Host Mode

In order to configure a single channel (within the XRT7302) to invert the RxClk output signal; the user must be operating the XRT7302 in the "Host" Mode.

If the user wishes to invert RxClk1, associated with Channe1, then the user should write a "1" into the "RClk1_INV" bit-field within Command Register 3.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RClk1_INV	Reserved
X	X	X	1	X

Similarly, if the user wishes to invert RxClk2, associated with Channel 2, then the user should write a "1" into the "RClk2_INV" bit-field within Command Register 11; as illustrated below.

COMMAND REGISTER CR11 (ADDRESS = 0X0B)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_2	LOSMUT2	RxOFF2	RClk2_INV	Reserved
X	X	X	1	X

Inverting the RxClk signals via the Hardware Mode

The user also has the ability to invert both the RxClk1 and RxClk2 output signals while the XRT7302 is operating in the "Hardware" Mode. Setting the "RClk-INV" input pin (pin 42) "high" will invert both the RxClk1 and RxClk2 output signals.

3.7.2 Routing Single-Rail Format (Binary Data Stream) data to the Receive Terminal Equipment

If the user wishes to route "Single-Rail" format data (e.g., a binary data stream), from the Receive Section

of a channel (within the XRT7302), to the "Receiving Terminal Equipment", he/she can do the following.

If the XRT7302 is operating in the "Host" Mode

If the XRT7302 is operating in the "Host" Mode, then the user has the option to configure each channel (individually) to output data in a Single-Rail or Dual-Rail manner to the Terminal Equipment.

a. In order to configure Channel 1 to output "Single-Rail" data to the Terminal Equipment: Write a "1" into the "SR/$\overline{DR}$_1" bit-field, within Command Register 3; as depicted below.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RClk1_INV	Reserved
1	X	X	X	X

b. In order to configure Channel 2 to output "Single-Rail" data to the Terminal Equipment: Write a "1" into the "SR/$\overline{DR}$_2" bit-field, within Command Register 11, as depicted below.

COMMAND REGISTER 11 (ADDRESS = 0X0B)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_2	LOSMUT2	RxOFF2	RClk2_INV	Reserved
1	X	X	X	X

After the user has taken these steps, then the configured channel (within the XRT7302) will output "Single-Rail" data to the "Receiving Terminal Equipment" via its corresponding RPOS and RxClk output pins, as illustrated below in Figure 25 and Figure 26.

If the XRT7302 is operating in the Hardware Mode

The user can configure the XRT7302 to output "Single-Rail" data from the Receive Sections of both channels by pulling the "SR/$\overline{DR}$" pin (pin 40) to VDD.

NOTE: *When the XRT7302 is operating in the Hardware Mode, the setting of the "SR/$\overline{DR}$" input pin applies to globally to both channels.*

FIGURE 25. ILLUSTRATION OF THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A SINGLE-RAIL FORMAT, FROM THE RECEIVE SECTION OF THE XRT7302 TO THE RECEIVING TERMINAL EQUIPMENT
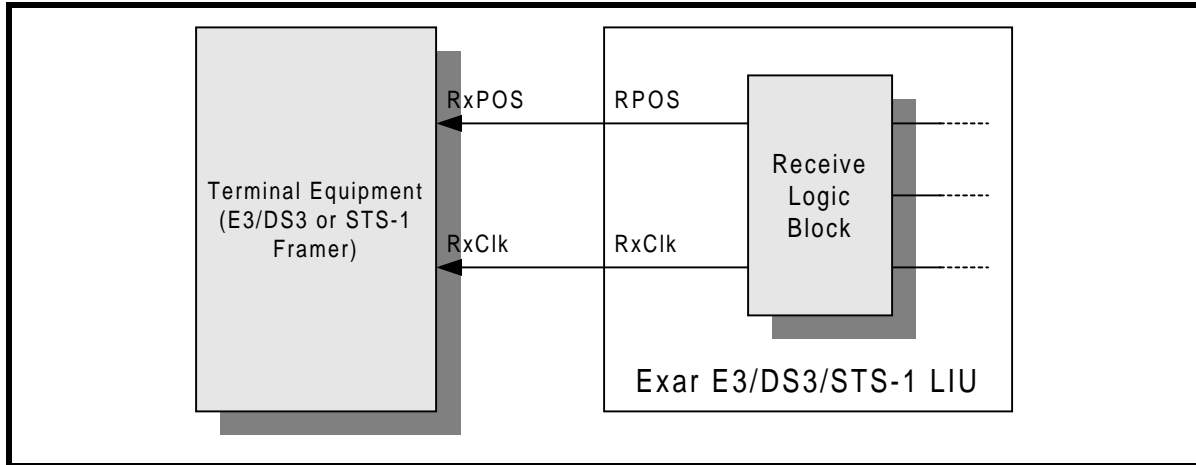
FIGURE 26. ILLUSTRATION OF THE BEHAVIOR OF THE RPOS AND RXCLK OUTPUT SIGNALS, WHILE THE XRT7302 IS TRANSMITTING "SINGLE-RAIL" DATA TO THE RECEIVING TERMINAL EQUIPMENT
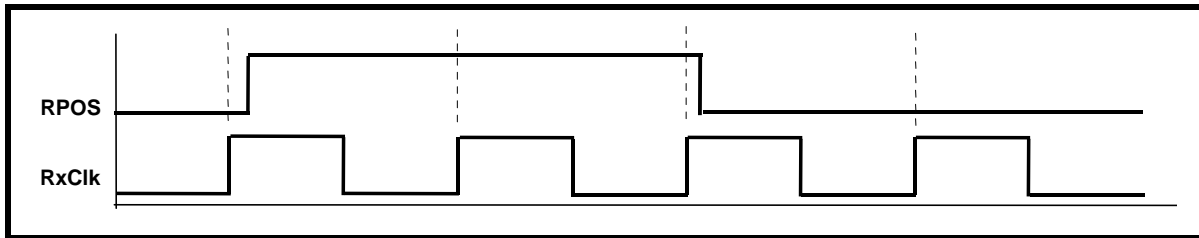
NOTE: *The RNEG output pin will be internally tied to Ground, whenever this feature is implemented.*

3.8   SHUTTING OFF THE RECEIVE SECTION

The Receive Section of each channel of the XRT7302 can be turned off. This feature may be useful in some "redundant system designs". Particularly, in those designs where the Receive Termination within the Secondary LIU Line Card, has been "switched-out" and is not receiving any traffic in parallel with the "Primary Line Card". In this case, having the LIU (on the "Secondary Line Card) consume the normal amount of current is a waste of power. Hence, this feature can permit the user to power down the "Receive Section" of the LIUs on the Secondary Line Card, which will reduce their power consumption by approximately 80%.

The user can implement the "RxOFF1" by the following means:

If the XRT7302 is operating in the "Hardware" Mode

Configuring Channel 1

The user can shut off the Receive Section of Channel 1 (within the XRT7302) by pulling the "RxOFF1" input pin (pin 19) "high". Conversely, the user can turn on the Receive Section of Channel 1 by pulling the "RxOFF1" input pin to "low".

Configuring Channel 2

The user can shut off the Receive Section of Channel 2 (within the XRT7302) by pulling the "RxOFF2" input pin (pin 18) "high". Conversely, the user can turn on the Receive Section of Channel 2 by pulling the "RxOFF2" input pin "low".

If the XRT7302 is operating in the "Host" Mode

Configuring Channel 1

The user can shut off the Receive Section of Channel 1 (within the XRT7302) by writing a "1" into the

"RxOFF1" bit-field (within Command Register CR3), as illustrated below.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
SR/$\overline{\text{DR}}$_1	LOSMUT1	RxOFF1	RClk1_INV	Reserved
X	X	1	X	X

Conversely, the user can turn on the Receive Section of Channel 1 by writing a "0" into the "RxOFF1" bit-field, within Command Register CR3.

Configuring Channel 2

The user can shut off the Receive Section of Channel 2 (within the XRT7302) by writing a "1" into the "RxOFF2" bit-field (within Command Register, CR11) as illustrated below.

COMMAND REGISTER CR11 (ADDRESS = 0X0B)

D4	D3	D2	D1	D0
SR/$\overline{\text{DR}}$_2	LOSMUT2	RxOFF2	RClk2_INV	Reserved
X	X	1	X	X

Conversely, the user can turn on the Receive Section of Channel 2 by writing a "0" into the "RxOFF2" bit-field, within Command Register CR11.

4.0 DIAGNOSTIC FEATURES OF THE XRT7302

The XRT7302 supports equipment diagnostic activities by supporting the following loop-back modes within each channel (within the XRT7302).

- Analog Local Loop-back.
- Digital Local Loop-back
- Remote Loop-back

The next two sections briefly discussed each of these Loop-back schemes.

4.1 THE ANALOG LOCAL LOOP-BACK MODE

When a given channel (within the XRT7302) is configured to operate in the "Analog Local Loop-back" Mode, the channel will ignore any signals that are input to its RTIP and RRing input pins. The "Transmitting Terminal Equipment" will transmit clock and data into this channel via the TPData, TNData, and TxClk input pins. This data will be processed through the "Transmit Clock Duty Cycle Circuit" and the "HDB3/B3ZS Encoder". Finally, this data will be output to the line via the TTIP and TRing output pins. Additionally, this data (which is being output via the TTIP and TRing output pins) will also be looped back into the "Receive Equalizer Block". As a consequence, this data will be processed through the entire "Receive Section" of the channel. After this "post-loop-back" data has been processed through the "Receive Section" it will be output, to the "Near-End Receiving Terminal Equipment" via the RPOS, RNEG and RxClk output pins.

Figure 27 illustrates the path that the data takes (within a given channel of the XRT7302), when the channel is configured to operate in the "Analog Local Loop-back" Mode.

FIGURE 27. ILLUSTRATION OF A TYPICAL CHANNEL(N) (WITHIN THE XRT7302) OPERATING IN THE ANALOG LOCAL LOOP-BACK MODE
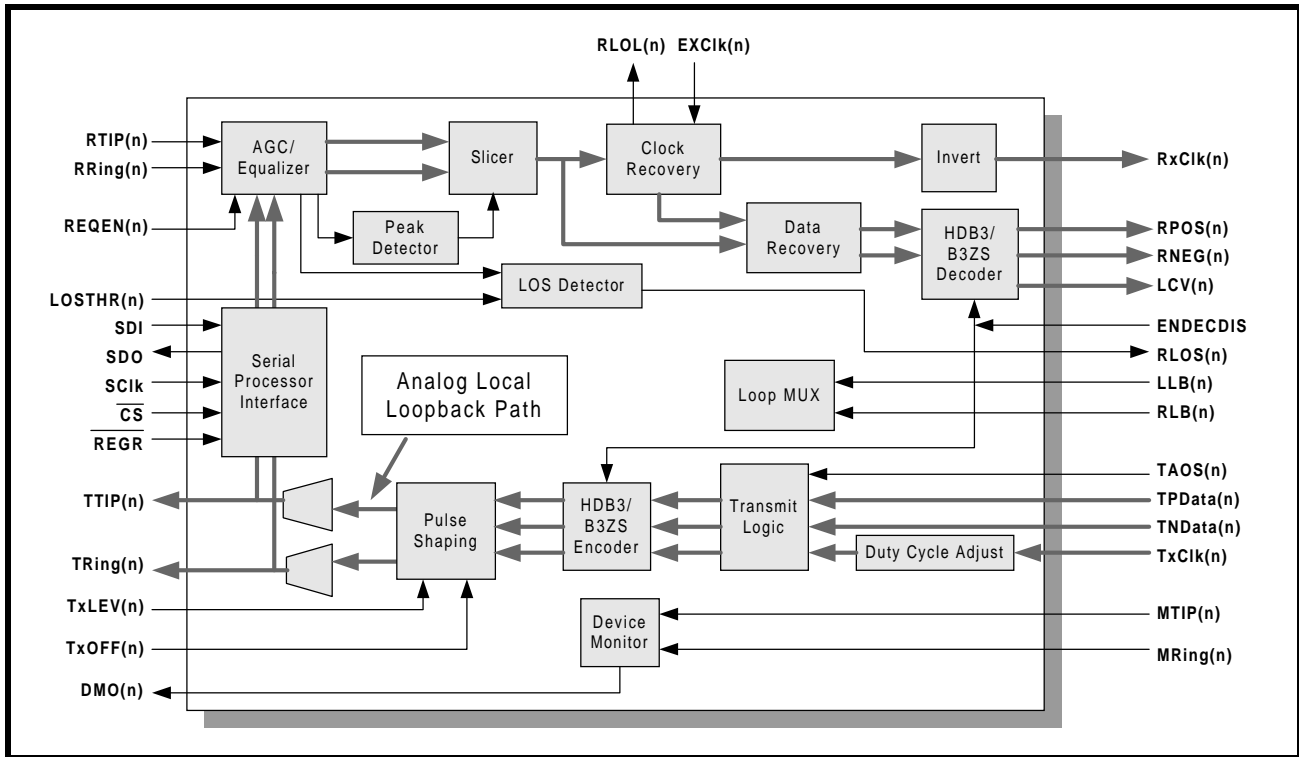
The user can configure a given channel, (within the XRT7302) to operate in the Analog Local Loop-back Mode, by employing either one of the following two steps

a. If the XRT7302 is operating in the "Host" Mode

To configure Channel 1 to operate in the "Analog Local Loop-Back" Mode, write a "1" into the "LLB1" bit-field and a "0" into the "RLB1" bit-field within Command Register 4, as illustrated below.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch1	E3_Ch1	LLB1	RLB1
X	X	X	1	0

Likewise, to configure Channel 2 to operate in the "Analog Local Loop-Back" Mode, write a "1" into the "LLB2" bit-field and a "0" into the "RLB2" bit-field within Command Register 12, as illustrated below.

COMMAND REGISTER CR12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch2	E3_Ch2	LLB2	RLB2
X	X	X	1	0

b. If the XRT7302 is operating in the "Hardware" Mode

To configure Channel 1 to operate in the "Analog Local Loop-back" Mode, set the "LLB1" input pin (pin 24) "high" and the "RLB1" input pin (pin 25) "low".

Likewise, to configure Channel 2 to operate in the "Analog Local Loop-back" Mode, set the "LLB2" input pin (pin 37) "high" and the "RLB2" input pin (pin 36) "low".

NOTE: The "Analog Local Loop-back" Mode does not work if the user has turned off the transmitter via the "TxOFF" feature.

4.2 THE DIGITAL LOCAL LOOP-BACK MODE.

When a given channel, within the XRT7302 is configured to operate in the "Digital Local Loop-back" Mode, the channel will ignore any signals that are input to the RTIP and RRing input pins. The "Transmitting Terminal Equipment" will transmit clock and data into the XRT7302 via the "TPData", "TNData" and "TxClk" input pins. This data will be processed through the "Transmit Clock Duty Cycle Circuit" and the "HDB3/B3ZS Encoder" block. At this point, this data will be looped back to the "HDB3/B3ZS Decoder" block. After this "post-loop back" data has been processed through the "HDB3/B3ZS Decoder" block, it will be output to the "Near-End" Receiving Terminal Equipment" via the RPOS, RNEG and RxClk output pins.

Figure 28 illustrates the path that the data takes (within the XRT7302), when the chip is configured to operate in the "Digital Local Loop-back" Mode.

FIGURE 28. ILLUSTRATION OF THE "DIGITAL LOCAL LOOP-BACK" PATH IN A TYPICAL CHANNEL(N) (OF THE XRT7302)

The user can configure a channel (within the XRT7302) to operate in the "Digital Local Loop-back" Mode, by employing either one of the following two-steps:

a. If the XRT7302 is operating in the "Host" Mode

To configure Channel 1 to operate in the "Digital Local Loop-Back" Mode, write a "1" into both the "LLB1" and "RLB1" bit-fields within Command Register 4, as illustrated below.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch1	E3 Ch1	LLB1	RLB1
X	X	X	1	1

Likewise, configure Channel 2 to operate in the "Digital Local Loop-back" Mode, write a "1" into both the "LLB2" and the "RLB2" bit-fields, within Command Register 12, as illustrated below.

COMMAND REGISTER CR12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch2	E3_Ch2	LLB2	RLB2
X	X	X	1	1

b. If the XRT7302 is operating in the "Hardware" Mode.

To configure Channel 1 to operate in the "Digital Local Loop-back" Mode, pull both the "LLB1" input pin (pin 24) and the "RLB1" input pin (pin 25) "high".

Likewise, to configure Channel 2 to operate in the "Digital Local Loop-back" Mode, pull both the "LLB2" input pin (pin 37) and the "RLB2" input pin (pin 36) "high".
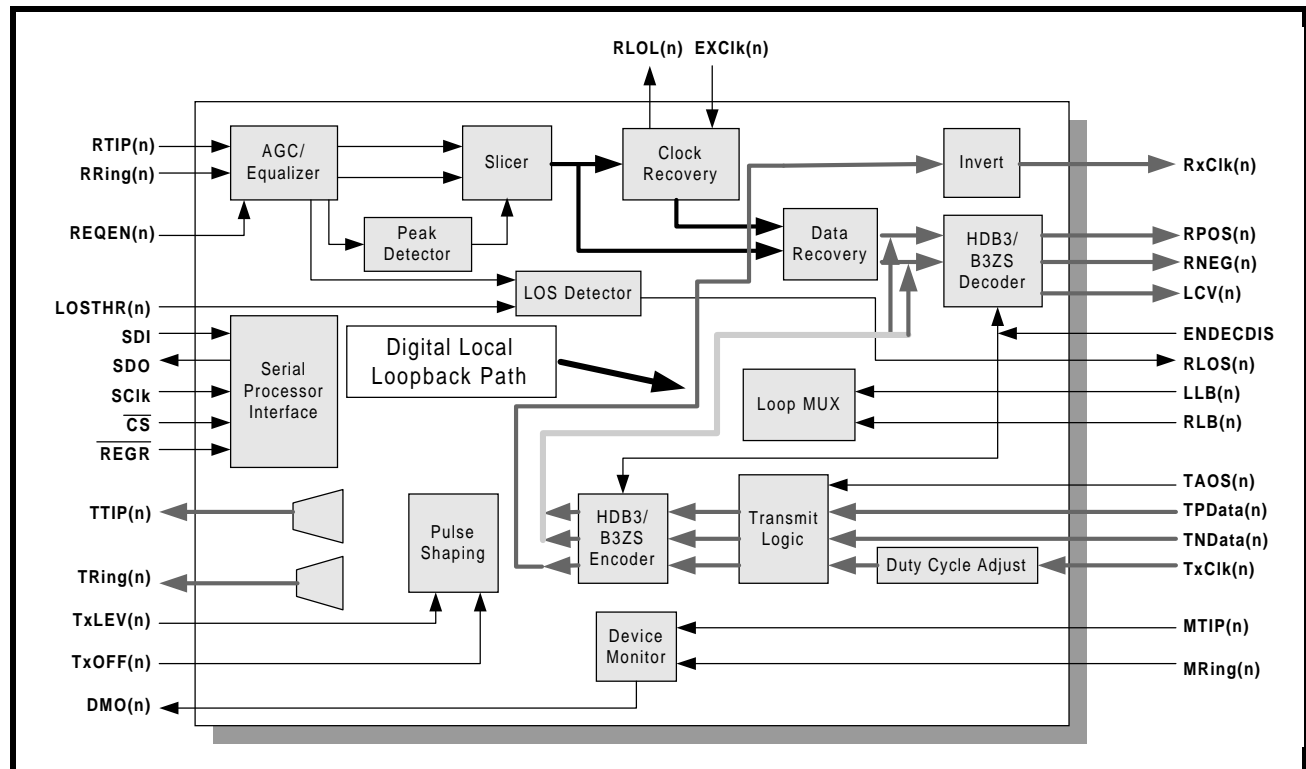
NOTE: *The ""Digital Local Loop-back" Mode will work even if the user has turned off the transmitter via the "TxOFF" feature.*

4.3   THE REMOTE LOOP-BACK MODE

When a given channel (within the XRT7302) is configured to operate in the Remote Loop-back Mode, the channel will ignore any signals that are input to the TPData and TNData input pins. The channel will receive the incoming line signal, via the RTIP and RRing input pins. This data will be processed through the entire Receive Section (within the channel) and will be output to the "Receive Terminal Equipment" via the RPOS, RNEG and RxClk output pins. Additionally, this data will also be internally looped back into the "Pulse-Shaping" block within the "Transmit Section". At this point, this data will be routed through the remainder of the "Transmit Section" of the channel and will be transmitted out onto the line via the TTIP and TRing output pins.

Figure 29 illustrates the path that the data takes (within the configured channel of the XRT7302), when the chip is configured to operate in the "Remote Loop-back" Mode.

FIGURE 29. ILLUSTRATION OF THE "REMOTE LOOP-BACK" PATH, WITHIN A TYPICAL CHANNEL(N) (OF THE XRT7302)
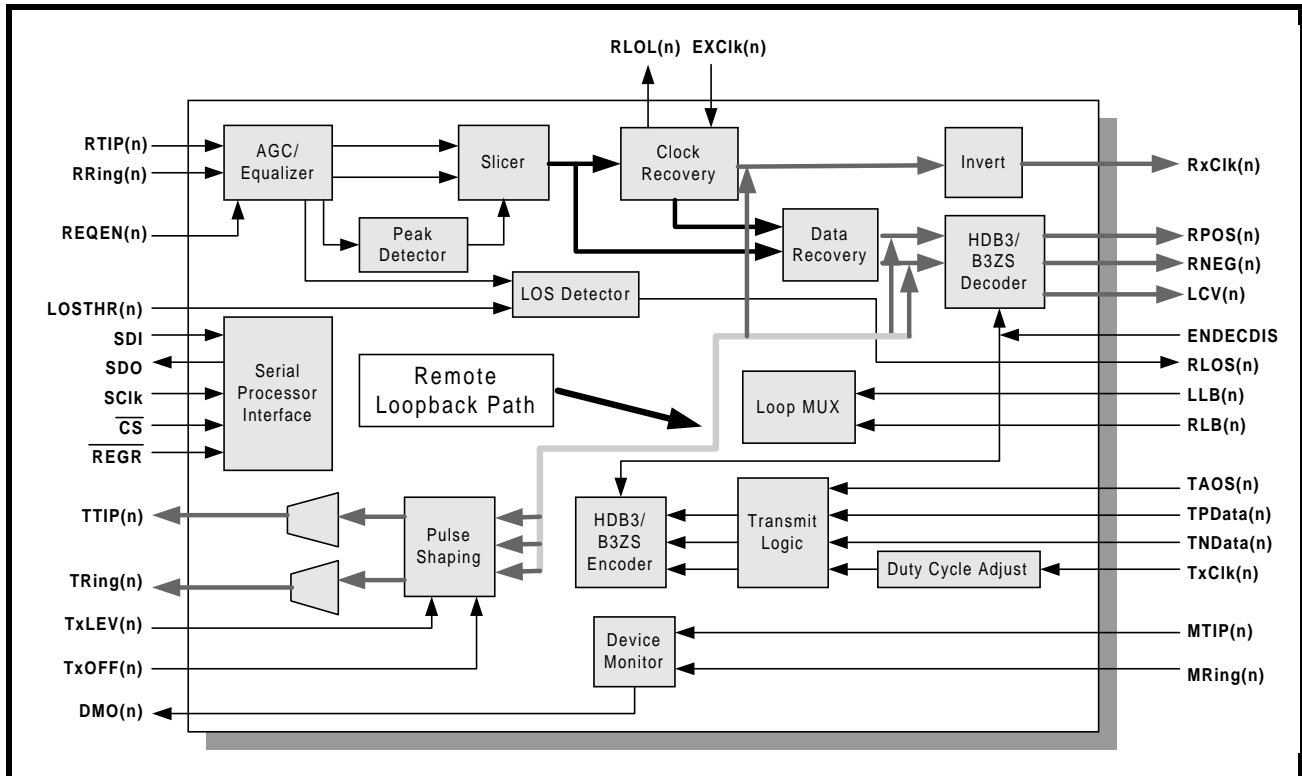
The user can configure a channel (within the XRT7302) to operate in the "Remote Loop-back" Mode, by employing either one of the following two steps

a. If the XRT7302 is operating in the "Host" Mode

To configure Channel 1 to operate in the "Remote Loop-back" Mode, write a "1" into the "RLB1" bit-field, and a "0" into the "LLB1" bit-field, within Command Register 4, as illustrated below.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch1	E3_Ch1	LLB1	RLB1
X	X	X	0	1

Likewise, to configure Channel 2 to operate in the "Remote Loop-back" Mode, write a "1" into the "RLB2" bit-field, and a "0" into the "LLB2" bit-field, within Command Register 12, as illustrated below.

COMMAND REGISTER CR12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch2	E3_Ch2	LLB2	RLB2

COMMAND REGISTER CR12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
X	X	X	0	1

b. If the XRT7302 is operating in the "Hardware" Mode

To configure Channel 1 to operate in the "Remote Loop-back" Mode, pull both the "RLB1" input pin (pin 25) to "high", and the "LLB1" input pin (pin 24) to "low".

Likewise, to configure Channel 2 to operate in the "Remote Loop-back" Mode, pull both the "RLB2" in-put pin (pin 36) to "high", and the "LLB2" input pin (pin 37) to "low".

4.4 TxOFF FEATURES

The XRT7302 permits the user to shut off the "Trans-mit Section of each Channel (within the XRT7302). When this feature is invoked the Transmit Section (of the configured channel) will be shut-off, and the Transmit Output signals (e.g., TTIP and TRing) will be tri-stated. This feature can come in handy for system redundancy conditions or during diagnostic testing.

The user can activate this feature by either of the following ways.

When the XRT7302 is operating in the "Hardware" Mode

Shutting off the Transmitter of Channel 1

The user can shut off the Transmit Driver (within Channel 1) by toggling the "TxOFF1" input pin (pin 80) "high". Conversely, the user can turn on the "Transmit Driver" by toggling the "TxOFF1" input pin "low".

Shutting off the Transmitter of Channel 2

The user can shut off the Transmit Driver (within Channel 2) by toggling the "TxOFF2" input pin (pin 61) "high". Conversely, the user can turn on the "Transmit Driver" by toggling the "TxOFF2" input pin "low".

When the XRT7302 is operating in the "Host" Mode

Shutting off the Transmitter of Channel 1

The user can turn off the Transmit Driver (within Channel 1) by setting the "TxOFF1" bit-field (within Command Register CR1) to "1", as illustrated below.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
1	X	X	X	X

Conversely, writing a "0" into this bit-field enables the "Transmit Driver within Channel 1.

Shutting off the Transmitter of Channel 2

The user can turn off the Transmit Driver (within Channel 2) by setting the "TxOFF2" bit-field (within Command Register CR9) to "1", as illustrated below.

COMMAND REGISTER CR9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
1	X	X	X	X

Conversely, writing a "0" into this bit-field enables the "Transmit Driver within Channel 2.

NOTE: *In order to permit a system (designed for redundancy) to quickly shut-off a defective line card and turn-on the "back-up" line card, the XRT7302 was designed such that either Transmitter can quickly be turned-on or turned-off by toggling the "TxOFF1" or "TxOFF2" input pins. This approach is much quicker then setting the "TxOFF1" and "TxOFF2" bit-fields via the Microprocessor Serial Interface.*

Table 7 presents a "Truth Table" which relates the setting of the "TxOFF" external pin and bit-field (for a channel) to the state of the Transmitter. Please note that this table applies to both Channels 1 and 2.

TABLE 7: THE RELATIONSHIP BETWEEN THE "TxOFF" INPUT PIN, THE "TxOFF" BIT FIELD AND THE STATE OF THE TRANSMITTER

STATE OF THE "TxOFF" INPUT PIN	STATE OF THE "TxOFF" BIT FIELD	STATE OF THE TRANSMITTER
LOW	0	ON (Transmitter is Active)
LOW	1	OFF (Transmitter is Tri-Stated)
HIGH	0	OFF (Transmitter is Tri-Stated)
HIGH	1	OFF (Transmitter is Tri-Stated)

As a consequence, if the user wishes to control the state of each transmitter, via the Microprocessor Serial interface, then he/she must connect the "TxOFF1" and "TxOFF2" input pins to GND.

4.5 THE TRANSMIT DRIVE MONITOR FEATURES

The Transmit Drive Monitor permits the user to monitor the line, in the Transmit Direction, for the occurrence of fault conditions such as a short circuit (on

the line), or a defective Transmit Drive in the XRT7302 or even another LIU device.

The user activates the Transmit Drive Monitor, within Channel 1 by connecting the MTIP1 pin (pin 76) to the TTIP1 line (through a 270 Ohm resistor connected in series); and by connecting the MRing1 pin (pin 75) to the TRing1 line (through a 270 Ohm resistor connected in series). Likewise, the user also activates the Transmit Drive Monitor, within Channel 2 by connecting the MTIP2 pin (pin 65) to the TTIP2 line

(through a 270 Ohm resistor connected in series); and by connecting the MRing2 pin (pin 66) to the

TRing2 line (through a 270 Ohm resistor connected in series). Such an approach is illustrated in Figure 30.

FIGURE 30. ILLUSTRATION OF A TYPICAL CHANNEL OF THE XRT7302 EMPLOYING THE TRANSMIT DRIVE MONITOR FEATURES
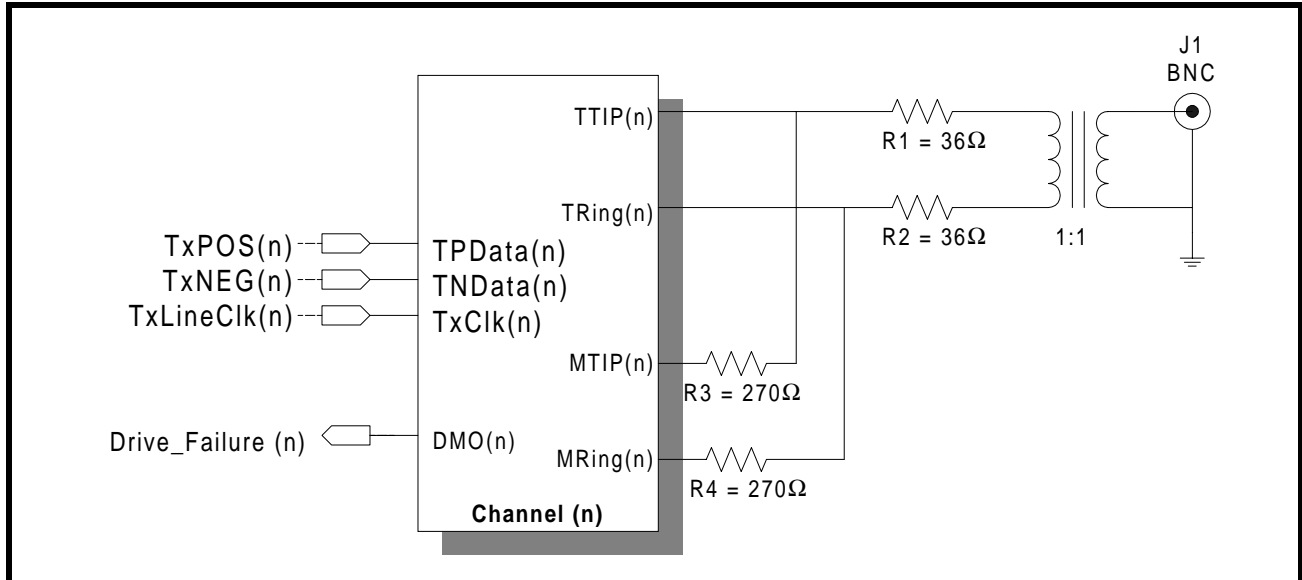
When the Transmit Drive Monitor circuitry (within a given line) is connected to the line, as illustrated in Figure 30, then it will monitor the line for transitions. As long as the Transmit Drive Monitor circuitry detects transitions on the line (via the MTIP and MRing pins), then it will keep the DMO (Drive Monitor Output) signal "low". However, if the Transmit Drive Monitor circuit detects no transitions on the line for 128(32 TxClk periods, then the DMO (Drive Monitor Output) signal will toggle "high".

NOTE: *The user does not have to use the Transmit Drive Monitor circuit in order to operate the Transmit Section of the XRT7302. This is purely a diagnostic feature.*

4.6 THE TAOS (TRANSMIT ALL ONES) FEATURE

The XRT7302 permits the user to command either channel to transmit an "All Ones" pattern onto the line by toggling a single input pin, or by setting a single bit-field (within one of the Command Registers) to "1". Please note that when this feature is activated, the Transmit Section of the configured channel (within the XRT7302) will overwrite the "Terminal Equipment" data with this "All Ones" pattern. The user can activate this feature by either of the following ways.

When the XRT7302 is operating in the "Hardware" Mode.

Configuring Channel 1

The user can configure Channel 1 (within the XRT7302) to transmit an "All Ones" pattern by toggling the "TAOS1" input pin (pin 2) "high". Converse-

ly, the user can terminate the "All Ones" pattern by toggling the "TAOS1" input pin "low".

Configuring Channel 2

The user can configure Channel 2 (within the XRT7302) to transmit an "All Ones" pattern by toggling the "TAOS2" input pin (pin 59) "high". Conversely, the user can terminate the "All Ones" pattern by toggling the "TAOS2" input pin "low".

When the XRT7302 is operating in the "Host" Mode.

Configuring Channel 1

The user can configure Channel 1 (within the XRT7302) to transmit an "All Ones" pattern by writing to Command Register CR1 and setting the "TAOS1" bit-field (bit D3) to "1", as illustrated below.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0	1	X	X	X

Conversely, the user can terminate the "All Ones" pattern by writing to Command Register, CR1 and setting the "TAOS" bit-field (D3) to "0".

Configuring Channel 2

The user can configure Channel 2 (within the XRT7302) to transmit an "All Ones" pattern by writing

to Command Register CR9 and setting the "TAOS1" bit-field (bit D3) to "1"; as illustrated below.

COMMAND REGISTER CR9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0	1	X	X	X

Conversely, the user can terminate the "All Ones" pattern by writing to Command Register, CR9 and setting the "TAOS" bit-field (D3) to "0".

5.0   THE MICROPROCESSOR SERIAL INTERFACE

The XRT7302 DS3/E3/STS-1 Line Interface Unit IC permits the user to have access to the "on-chip" Command Registers. Through these Command Registers, the user can configure the XRT7302 into a wide-variety of modes. This section discusses the following:

1. The description of the Command Registers.

2. A description on how to use the Microprocessor Serial Interface.

5.1   DESCRIPTION OF THE COMMAND REGISTERS

Table 8 lists the Command Registers, their Addresses, and their bit-formats.

TABLE 8: ADDRESSES AND BIT FORMATS OF XRT7302 COMMAND REGISTERS

ADDRESS	COMMAND REGISTER	TYPE	REGISTER BIT-FORMAT				
			D4	D3	D2	D1	D0
0x00	CR0	RO	RLOL1	RLOS1	ALOS1	DLOS1	DMO1
0x01	CR1	R/W	TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0x02	CR2	R/W	Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
0x03	CR3	R/W	SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RxClk1_INV	Reserved
0x04	CR4	R/W	Reserved	STS-1/$\overline{DS3}$_Ch1	E3_Ch1	LLB1	RLB1
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	RLOL2	RLOS2	ALOS2	DLOS2	DMO2
0x09	CR9	R/W	TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0x0A	CR10	R/W	Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
0x0B	CR11	R/W	SR/$\overline{DR}$_2	LOSMUT2	RxOFF2	RxClk2_INV	Reserved
0x0C	CR12	R/W	Reserved	STS-1/$\overline{DS3}$_Ch2	E3_Ch2	LLB2	RLB2
0x0D	CR13	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR14	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR15	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

The "role/meaning" associated with each of these bit-fields is presented below.

Address

The register addresses presented in the "hexadecimal" format.

Type:

The Command Registers are either "Read-Only" (RO) type of registers, or are "Read/Write" (R/W) type of registers.

NOTE: The default value for each of the bit-fields, within these register will be "0".

Description of Bit-Fields for each Command Register

5.1.1 Command Register - CR0

The bit-format and default values for Command Register CR0 are listed below.

COMMAND REGISTER CR0, (ADDRESS = 0X00)

D4	D3	D2	D1	D0
RLOL1	RLOS1	ALOS1	DLOS1	DMO1
1	1	1	1	1

The function of each of these bit-fields are presented below.

Bit D4 - RLOL1 (Receive Loss of Lock Status - Channel 1)

This "Read-Only" bit-field reflects the "lock" status of the "Clock Recovery Phase-Locked-Loop", within Channel 1 of the XRT7302.

This bit-field will be set to "0" if the "Clock Recovery PLL" (within Channel 1) is in "lock" with the incoming line signal. Conversely, this bit-field will be set to "1" if

the "Clock Recovery PLL" (within Channel 1) is "out of lock" with the incoming line signal.

Bit D3 - RLOS1 (Receive Loss of Signal Status - Channel 1)

This "Read-Only" bit-field indicates whether or not the Receiver, within Channel 1 is currently declaring an LOS (Loss of Signal) Condition.

This bit-field will be set to "0" if Channel 1 is not (currently) declaring the LOS Condition. Conversely, this bit-field will be set to "1" if Channel 1 is declaring an LOS Condition.

Bit D2 - ALOS1 (Analog Loss of Signal Status - Channel 1)

This "Read-Only" bit-field indicates whether or not the "Analog LOS Detector", within Channel 1, is currently declaring an LOS condition.

This bit-field will be set to "0" if the "Analog LOS Detector", within Channel 1, is NOT (currently) declaring an LOS condition. Conversely, this bit-field will be set to "1" if the "Analog LOS Detector", within Channel 1, is currently declaring an LOS condition.

NOTE: *The purpose of this feature is to isolate the Detector (e.g., either the "Analog LOS" or the "Digital LOS" detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes*

Bit D1 - DLOS1 (Digital Loss of Signal Status - Channel 1)

This "Read-Only" bit-field indicates whether or not the "Digital LOS Detector", within Channel 1, is currently declaring an LOS condition.

This bit-field will be set to "0" if the "Digital LOS Detector", within Channel 1, is NOT (currently) declaring an LOS condition. Conversely, this bit-field will be set to "1" if the "Digital LOS Detector", within Channel 1, is currently declaring an LOS condition.

NOTE: *The purpose of this feature is to isolate the Detector (e.g., either the "Analog LOS" or the "Digital LOS" detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D0 - DMO1 (Drive Monitor Output Status - Channel 1)

This "Read-Only" bit-field reflects the status of the DMO1 output pin.

5.1.2 Command Register CR1

The bit-format and default values for Command Register CR1 are listed below.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - TxOFF1 (Transmitter OFF - Channel 1)

This "Read/Write" bit-field permits the user to turn off the Transmitter (within Channel 1).

Writing a "1" to this bit field will turn off the Transmitter and tri-state the Transmit Output. Conversely, writing a "0" to this bit-field will turn-on the Transmitter.

Bit D3 - TAOS1 (Transmit All OneS - Channel 1)

This "Read/Write" bit-field permits the user to command the Transmitter (within Channel 1) to generate and transmit an "All Ones" pattern onto the line.

Writing a "1" to this bit-field commands the Transmitter to transmit an "All Ones" pattern onto the line. Writing a "0" to this bit-field commands normal operation.

Bit D2 - TxClkINV1 (Transmit Clock Invert - Channel 1)

This "Read/Write" bit-field permits the user to configure the "Transmitter" (within the XRT7302) to sample the signal (at the TPData and TNData pins) on the "rising edge" or "falling edge" of TxClk (the Transmit Line Clock signal).

Writing a "1" to this bit-field configures the Transmitter to sample the TPData and TNData input pins, on the "rising edge" of TxClk. Conversely, writing a "0" to this bit-field configures the Transmitter to sample the TPData and TNData input pins, on the "falling edge" of TxClk.

Bit D1 - TxLEV1 (Transmit Line Build-Out Enable/Disable Select - Channel 1)

This "Read/Write" bit-field permits the user to enable or disable the Transmit Line Build-Out circuit, within Channel 1 of the XRT7302.

Setting this bit-field "HIGH" disables the Line Build-Out circuit within Channel 1. In this mode, Channel 1 will output unshaped (e.g., square-wave) pulses onto the line via the TTIP1 and TRing1 output pins.

Setting this bit-field "LOW" enables the Line Build-Out circuit within Channel 1. In this mode, Channel 1 will output shaped pulses onto the line via the TTIP1 and TRing1 output pins.

In order to comply with the "Isolated DSX-3/STSX-1 Pulse Template Requiremnts (per Bellcore GR-499-CORE or GR-253-CORE), the user should:

a. Set this bit-field to "1", if the cable length (between the Cross-Connect and the transmit output of Channel 1) is greater than 225 feet.

b. Set this bit-field to "0", if the cable length (between the Cross-Connect and the transmit output of Channel 1) is less than 225 feet.

This bit-field is active only if the XRT7302 is configured to operate in the DS3 or SONET STS-1 Modes.

If the cable length is greater than 225 feet, then the user should set this bit-field to "1" (in order to increase the amplitude of the Transmit Output Signal). Conversely, if the cable length is less than 225 feet, then the user should set this bit-field to "0".

NOTE: *This option is only available when the XRT7302 is operating in the DS3 or STS-1 Mode.*

Bit D0 - TxBIN1 (Transmit Binary Data - Channel 1)

This "Read/Write" bit-field permits the user to configure the "Transmitter" (within Channel 1) to accept an (un-encoded) binary data stream (via the TPData input) and converts this data into the appropriate bipolar signal (to the line).

Writing a "1" configures the "Transmitter" to accept a binary data stream via the TPData input. (Note: The TNData input will be ignored). This form of data acceptance is sometimes referred to as "Single-rail" mode operation. The Transmitter will then encode this data into the appropriate line code (e.g., B3ZS or HDB3) prior to its transmission over the line.

Writing a "0" configures the "Transmitter" to accept data in a "dual-rail" manner (e.g., via both the TPData and TNData inputs).

5.1.3   Command Register CR2

The bit-format and default values for Command Register CR2 are listed below.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDEC_DIS1	ALOSDIS1	DLOSDIS1	REQ_EN1
X	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - Reserved

Bit D3 - ENDEC_DIS1 (B3ZS/HDB3 Encoder/Decoder-Disable - Channel 1)

This "Read/Write" bit-field permits the user to enable or disable the B3ZS/HDB3 Encoder and Decoder blocks, within Channel 1.

Writing a "1" to this bit-field disables the B3ZS/HDB3 Encoder and Decoder blocks. Writing a "0" to this bit-field enables the B3ZS/HDB3 Encoder and Decoder blocks.

NOTE: *This Encoder/Decoder will perform HDB3 Encoding/ Decoding if the XRT7302 is operating in the "E3 Mode". Otherwise, it will perform B3ZS Encoding/Decoding.*

Bit D2 - ALOSDIS1 (Analog LOS Disable - Channel 1)

This "Read/Write" bit-field permits the user to disable the Analog LOS Detector, within Channel 1.

Writing a "0" to this bit-field enables the Analog LOS Detector.   Writing a "1" to this bit-field disables the Analog LOS Detector.

Note: If the user disables the Analog LOS Detector, then the RLOS input pin will only be asserted by the DLOS (Digital LOS Detector).

Bit D1 - DLOSDIS1 (Digital LOS Disable - Channel 1)

This "Read/Write" bit-field permits the user to disable the Digital LOS Detector within Channel 1.

Writing a "0" to this bit-field enables the Digital LOS Detector.   Writing a "1" to this bit-field disables the Digital LOS Detector.

NOTE: *If the user disables the Digital LOS Detector, then the RLOS input pin will only be asserted by the ALOS (Analog LOS Detector).*

Bit D0 - REQ_EN1 (Receive Equalization Enable - Channel 1)

This "Read/Write" bit-field permits the user to either enable or disable the internal Receive Equalizer, within Channel 1 of the XRT7302.

Writing a "1" to this bit-field enables the "Internal Equalizer". Conversely, writing a "0" to this bit-field disables the "Internal Equalizer".

5.1.4   Command Register CR3

The bit-format and default values for Command Register CR3 are listed below.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RxClk1_INV	Reserved
0	1	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - SR/$\overline{DR}$_1 (Single-Rail/Dual-Rail Data Output - Channel 1)

This "Read/Write" bit-field permits the user to configure Channel 1 (within the XRT7302) to output the "received" data (from the Remote Terminal) in a binary or "dual-rail" format.

Writing a "1" to this bit-field configures Channel 1 to output data (to the Terminal Equipment) in a binary (single-rail) format via the RPOS1 output pin, RNEG1 will be grounded. Conversely, a "0" to this bit-field configures Channel 1 to output data (to the Terminal Equipment) in a "Dual Rail" format via both the RPOS1 and RNEG1 output pins.

Bit D3 - LOSMUT1 (Recovered Data MUTing, during LOS Condition - Channel 1)

This "Read/Write" bit-field permits the user to configure Channel 1 (within the XRT7302) to not output any recovered data (from the line), while it is declaring an LOS condition.

Writing a "0" to this bit-field configures the chip to output recovered data, even while the XRT7302 is declaring an "LOS" condition. Writing a "1" to this bit-field configures the chip to NOT output the recovered data, while an LOS condition is being declared. (Note: in this mode, RPOS1 and RNEG1 will be set to "0", asynchronously.)

Bit D2 - RxOFF1 (Receive Section - Shut OFF Select)

This "Read/Write" bit-field permits the user to shut-off the "Receive Section of Channel 1 (within the XRT7302). The purpose of this feature is to permit the user to conserve power consumption when this device is the back-up device in a "Redundancy System".

Writing a "1" into this bit-field shuts off the Receive Section of Channel 1. Conversely, writing a "0" into this bit-field turns on the Receive Section of Channel 1.

Bit D1 - RxClk1_INV (Invert RxClk1)

This "Read/Write" bit-field permits the user to configure the "Receiver" (within Channel 1 of the XRT7302) to output the recovered data on either the "rising edge" or the "falling edge" of the RxClk1 clock signal.

Writing a "0" to this bit-field configures the Receiver to output the recovered data on the "rising edge" of the RxClk1 output signal. Writing a "1" to this bit-field configures the Receiver to output the recovered data on the "falling edge" of the RxClk1 output signal.

Bit D0 - Reserved

This bit-field has no defined functionality

Command Register CR4

The bit-format and default values for Command Register CR4 are listed below.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
Reserved	STS-1/$\overline{DS3}$_Ch1	E3_Ch1	LLB1	RLB1
0	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - STS-1/$\overline{DS3}$ - Channel 1 - Mode Select

This "Read/Write" bit field permits the user to configure Channel 1, (within the XRT7302) to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures Channel 1 to operate in the "DS3 Mode". Writing a "1" into this bit-field configures Channel 1 to operate in the SONET STS-1 Mode.

Note: This bit-field is ignored if the "E3_Ch_1" bit-field (e.g., "D2" within this Command Register) is set to "1".

Bit D2 - E3 Mode Select - Channel 1

This "Read/Write" bit-field permits the user to configure Channel 1 (within the XRT7302) to operate in the E3 Mode.

Writing a "0" into this bit-field configures Channel 1 to operate in either the DS3 or SONET STS-1 Mode (as specified by the setting of the "DS3" bit-field within this Command Register). Writing a "1" into this bit-field configures Channel 1 to operate in the E3 Mode.

Bit D1 - LLB1 (Local Loop-back - Channel 1)

This "Read/Write" bit-field, along with "RLB1" permits the user to configure Channel 1 (within the XRT7302) to operate in any one of a variety of loop-back modes.

Table 9 relates the contents of "LLB1" and "RLB1" to the corresponding loop-back mode for Channel 1.

Bit D0 - RLB1 (Remote Loop-back - Channel 1)

This "Read/Write" bit-field, along with "LLB1" permits the user to configure Channel 1 (within the XRT7302) to operate in any one of a variety of loop-back modes.

Table 9 relates the contents of "LLB1" and "RLB1" to the corresponding loop-back mode for Channel 1.

TABLE 9: CONTENTS OF "LLB1" AND "RLB1" AND THE CORRESPONDING LOOP-BACK MODE FOR CHANNEL 1

LLB1	RLB1	LOOP-BACK MODE (FOR CHANNEL 1)
0	0	None
1	0	Analog Loop-Back Mode (See Section 4.1 for Details)
1	1	Digital Loop-Back Mode (See Section 4.2 for Details
0	1	Remote Loop-Back Mode (See Section 4.3 for Details

5.1.5   Command Register - CR8

The bit-format and default values for Command Register CR8 are listed below.

COMMAND REGISTER 8, (ADDRESS = 0X08)

D4	D3	D2	D1	D0
RLOL2	RLOS2	ALOS2	DLOS2	DMO2
1	1	1	1	1

The function of each of these bit-fields are presented below.

Bit D4 - RLOL2 (Receive Loss of Lock Status - Channel 2)

This "Read-Only" bit-field reflects the "lock" status of the "Clock Recovery Phase-Locked-Loop", within Channel 2 of the XRT7302.

This bit-field will be set to "0" if the "Clock Recovery PLL" (within Channel 2) is in "lock" with the incoming line signal. Conversely, this bit-field will be set to "1" if the "Clock Recovery PLL" (within Channel 2) is "out of lock" with the incoming line signal.

Bit D3 - RLOS2 (Receive Loss of Signal Status - Channel 2)

This "Read-Only" bit-field indicates whether or not the Receiver, within Channel 2 is currently declaring an LOS (Loss of Signal) Condition.

This bit-field will be set to "0" if Channel 2 is not (currently) declaring the LOS Condition. Conversely, this bit-field will be set to "1" if Channel 2 is declaring an LOS Condition.

Bit D2 - ALOS2 (Analog Loss of Signal Status - Channel 2)

This "Read-Only" bit-field indicates whether or not the "Analog LOS Detector", within Channel 2, is currently declaring an LOS condition.

This bit-field will be set to "0" if the "Analog LOS Detector", within Channel 2, is NOT (currently) declaring an LOS condition. Conversely, this bit-field will be set to "1" if the "Analog LOS Detector", within Channel 2, is currently declaring an LOS condition.

NOTE: The purpose of this feature is to isolate the Detector (e.g., either the "Analog LOS" or the "Digital LOS" detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.

Bit D1 - DLOS2 (Digital Loss of Signal Status - Channel 2)

This "Read-Only" bit-field indicates whether or not the "Digital LOS Detector", within Channel 2, is currently declaring an LOS condition.

This bit-field will be set to "0" if the "Digital LOS Detector", within Channel 2, is NOT (currently) declaring an LOS condition. Conversely, this bit-field will be set to "1" if the "Digital LOS Detector", within Channel 2, is currently declaring an LOS condition.

NOTE: The purpose of this feature is to isolate the Detector (e.g., either the "Analog LOS" or the "Digital LOS" detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.

Bit D0 - DMO2 (Drive Monitor Output Status - Channel 2)

This "Read-Only" bit-field reflects the status of the DMO2 output pin.

5.1.6   Command Register CR9

The bit-format and default values for Command Register CR9 are listed below.

COMMAND REGISTER CR9 (ADDRESS = 0X09)

D4	D3	D2	D1	D0
TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - TxOFF2 (Transmitter OFF - Channel 2)

This "Read/Write" bit-field permits the user to turn off the Transmitter (within Channel 2).

Writing a "1" to this bit field will turn off the Transmitter and tri-state the Transmit Output. Conversely, writing a "0" to this bit-field will turn-on the Transmitter.

Bit D3 - TAOS2 (Transmit All OneS - Channel 2)

This "Read/Write" bit-field permits the user to command the Transmitter (within Channel 2) to generate and transmit an "All Ones" pattern onto the line.

Writing a "1" to this bit-field commands the Transmitter to transmit an "All Ones" pattern onto the line. Writing a "0" to this bit-field commands normal operation.

Bit D2 - TxClkINV2 (Transmit Clock Invert - Channel 2)

This "Read/Write" bit-field permits the user to configure the "Transmitter" (within the XRT7302) to sample the signal (at the TPData2 and TNData2 pins) on the "rising edge" or "falling edge" of TxClk2 (the Transmit Line Clock signal).

Writing a "1" to this bit-field configures the Transmitter to sample the TPData2 and TNData2 input pins, on the "rising edge" of TxClk2. Conversely, writing a "0" to this bit-field configures the Transmitter to sample the TPData2 and TNData2 input pins, on the "falling edge" of TxClk2.

Bit D1 - TxLEV2 (Transmit Line Build-Out Enable/ Disable Select - Channel 2)

This "Read/Write" bit-field permits the user to enable or disable the Transmit Line Build-Out circuit, within Channel 2 of the XRT7302.

Setting this bit-field "HIGH" disables the Line Build-Out circuit within Channel 2. In this mode, Channel 2 will output unshaped (e.g., square-wave) pulses onto the line via the TTIP2 and TRing2 output pins.

Setting this bit-field "LOW" enables the Line Build-Out circuit within Channel 2. In this mode, Channel 2 will output shaped pulses onto the line via the TTIP2 and TRing2 output pins.

In order to comply with the "Isolated DSX-3/STSX-1 Pulse Template Requiremnts (per Bellcore GR-499-CORE or GR-253-CORE), the user should:

c. Set this bit-field to "1", if the cable length (between the Cross-Connect and the transmit output of Channel 2) is greater than 225 feet.

d. Set this bit-field to "0", if the cable length (between the Cross-Connect and the transmit output of Channel 2) is less than 225 feet.

This bit-field is active only if the XRT7302 is configured to operate in the DS3 or SONET STS-1 Modes.

Bit D0 - TxBIN2 (Transmit Binary Data - Channel 2)

This "Read/Write" bit-field permits the user to configure the "Transmitter" (within Channel 2) to accept an (un-encoded) binary data stream (via the TPData2 input) and converts this data into the appropriate bipolar signal (to the line).

Writing a "1" configures the "Transmitter" to accept a binary data stream via the TPData2 input. (Note: The TNData2 input will be ignored). This form of data acceptance is sometimes referred to as "Single-rail" mode operation. The Transmitter will then encode this data into the appropriate line code (e.g., B3ZS or HDB3) prior to its transmission over the line.

Writing a "0" configures the "Transmitter" to accept data in a "dual-rail" manner (e.g., via both the TPData2 and TNData2 inputs).

5.1.7   Command Register CR10

The bit-format and default values for Command Register CR10 are listed below.

COMMAND REGISTER CR10 (ADDRESS = 0X0A)

D4	D3	D2	D1	D0
Reserved	ENDEC_DIS2	ALOSDIS2	DLOSDIS2	REQ_EN2
X	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - ENDEC_DIS2 (B3ZS/HDB3 Encoder/Decoder-Disable - Channel 1)

This "Read/Write" bit-field permits the user to enable or disable the B3ZS/HDB3 Encoder and Decoder blocks, within Channel 2.

Writing a "1" to this bit-field disables the B3ZS/HDB3 Encoder and Decoder blocks. Writing a "0" to this bit-field enables the B3ZS/HDB3 Encoder and Decoder blocks.

NOTE: *This Encoder/Decoder will perform HDB3 Encoding/Decoding if the XRT7302 is operating in the "E3 Mode". Otherwise, it will perform B3ZS Encoding/Decoding.*

Bit D2 - ALOSDIS2 (Analog LOS Disable - Channel 2)

This "Read/Write" bit-field permits the user to disable the Analog LOS Detector, within Channel 2.

Writing a "0" to this bit-field enables the Analog LOS Detector. Writing a "1" to this bit-field disables the Analog LOS Detector.

NOTE: *If the user disables the Analog LOS Detector, then the RLOS input pin will only be asserted by the DLOS (Digital LOS Detector).*

Bit D1 - DLOSDIS2 (Digital LOS Disable - Channel 2)

This "Read/Write" bit-field permits the user to disable the Digital LOS Detector within Channel 2.

Writing a "0" to this bit-field enables the Digital LOS Detector. Writing a "1" to this bit-field disables the Digital LOS Detector.

NOTE: *If the user disables the Digital LOS Detector, then the RLOS input pin will only be asserted by the ALOS (Analog LOS Detector).*

Bit D0 - REQ_EN2 (Receive Equalization Disable - Channel 2)

This "Read/Write" bit-field permits the user to either enable or disable the internal Receive Equalizer (within Channel 2).

Writing a "1" to this bit-field enables the "Internal Equalizer". Conversely, writing a "0" to this bit-field disables the "Internal Equalizer".

5.2 COMMAND REGISTER CR11

The bit-format and default values for Command Register CR11 are listed below.

COMMAND REGISTER CR11 (ADDRESS = 0X0B)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_1	LOSMUT1	RxOFF1	RxClk1_INV	Reserved
0	1	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - SR/$\overline{DR}$_2 (Single-Rail/Dual-Rail Data Output - Channel 2)

This "Read/Write" bit-field permits the user to configure Channel 2 (within the XRT7302) to output the "received" data (from the Remote Terminal) in a binary or "dual-rail" format.

Writing a "1" to this bit-field configures Channel 2 to output data (to the Terminal Equipment) in a binary (single-rail) format via the RPOS2 output pin, RNEG2 will be grounded. Conversely, a "0" to this bit-field configures Channel 2 to output data (to the Terminal Equipment) in a "Dual Rail" format via both the RPOS2 and RNEG2 output pins.

Bit D3 - LOSMUT2 (Recovered Data MUTing, during LOS Condition - Channel 2)

This "Read/Write" bit-field permits the user to configure Channel 2 (within the XRT7302) to not output any recovered data (from the line), while it is declaring an LOS condition.

Writing a "0" to this bit-field configures the chip to output recovered data, even while the XRT7302 is declaring an "LOS" condition. Writing a "1" to this bit-field configures the chip to NOT output the recovered data, while an LOS condition is being declared. (Note: in this mode, RPOS2 and RNEG2 will be set to "0", asynchronously.)

Bit D2 - RxOFF2 (Receive Section - Shut OFF Select)

This "Read/Write" bit-field permits the user to shut-off the "Receive Section of Channel 2 (within the XRT7302). The purpose of this feature is to permit the user to converse power consumption when this device is the back-up device in a "Redundancy System".

Writing a "1" into this bit-field shuts off the Receive Section of Channel 2. Conversely, writing a "0" into this bit-field turns on the Receive Section of Channel 2.

Bit D1 - RxClk2_INV (Invert RxClk2)

This "Read/Write" bit-field permits the user to configure the "Receiver" (within Channel 2 of the XRT7302) to output the recovered data on either the "rising edge" or the "falling edge" of the RxClk2 clock signal.

Writing a "0" to this bit-field configures the Receiver to output the recovered data on the "rising edge" of the RxClk2 output signal. Writing a "1" to this bit-field configures the Receiver to output the recovered data on the "falling edge" of the RxClk2 output signal.

Bit D0 - Reserved

This bit-field has no defined functionality.

5.2.1   Command Register CR12

The bit-format and default values for Command Register CR12 are listed below.

COMMAND REGISTER CR 12 (ADDRESS = 0X0C)

D4	D3	D2	D1	D0
Reserved	STS-1/$\overline{\text{DS3}}$_Ch2	E3_Ch2	LLB2	RLB2
0	0	0	0	0

The function of each of these bit-fields are presented below.

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - STS-1/$\overline{\text{DS3}}$ - Channel 2 - Mode Select

This "Read/Write" bit field permits the user to configure Channel 2, (within the XRT7302) to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures Channel 2 to operate in the "DS3 Mode". Writing a "1" into this bit-field configures Channel 2 to operate in the SONET STS-1 Mode.

NOTE: This bit-field is ignored if the "E3_Ch_2" bit-field (e.g., "D2" within this Command Register) is set to "1".

Bit D2 - E3 Mode Select - Channel 2

This "Read/Write" bit-field permits the user to configure Channel 2 (within the XRT7302) to operate in the E3 Mode.

Writing a "0" into this bit-field configures Channel 2 to operate in either the DS3 or SONET STS-1 Mode (as specified by the setting of the "DS3" bit-field within this Command Register). Writing a "1" into this bit-field configures Channel 2 to operate in the E3 Mode.

Bit D1 - LLB2 (Local Loop-back - Channel 2)

This "Read/Write" bit-field, along with "RLB2" permits the user to configure Channel 2 (within the XRT7302) to operate in any one of a variety of loop-back modes.

Table 10 relates the contents of "LLB2" and "RLB2" and the corresponding loop-back mode for Channel 2.

Bit D0 - RLB2 (Remote Loop-back - Channel 2)

This "Read/Write" bit-field, along with "LLB2" permits the user to configure Channel 2 (within the XRT7302) to operate in any one of a variety of loop-back modes.

Table 10 relates the contents of "LLB2" and "RLB2" and the corresponding loop-back mode for Channel 2.

TABLE 10: CONTENTS OF "LLB2" AND "RLB2" AND THE CORRESPONDING LOOP-BACK MODE FOR CHANNEL 2

LLB2	RLB2	LOOP-BACK MODE (FOR CHANNEL 2)
0	0	None
1	0	Analog Loop-Back Mode (See Section 4.1 for Details)
1	1	Digital Loop-Back Mode (See Section 4.2 for Details
0	1	Remote Loop-Back Mode (See Section 4.3 for Details

5.3   OPERATING THE MICROPROCESSOR SERIAL INTERFACE.

The XRT7302 Serial Interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

• $\overline{\text{CS}}$ - Chip Select (Active Low)

• SClk - Serial Clock

• SDI - Serial Data Input

• SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure 31.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SClk input pin. Afterwards, the user will initiate a "Read" or "Write" operation by asserting the "active-low" Chip Select input pin ($\overline{\text{CS}}$). It is important to assert the $\overline{\text{CS}}$ pin (e.g., toggle it "low") at least 50ns prior to the very first rising edge of the clock signal.

Once the $\overline{\text{CS}}$ input pin has been asserted the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note:

each of these bits will be "clocked" into the SDI input, on the rising edge of SClk. These eight bits are identified and described below.

Bit 1 - "R/W" (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SClk (after $\overline{CS}$ has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 through 5: The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SClk signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT7302 that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin, in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:

The next two bits, A4 and A5 must be set to "0", as shown in Figure 31.

Bit 8 - A6

The value of "A6" is a "don't care".

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SClk periods. On the falling edge of SClk Cycle #8 (see Figure 31) the serial data output signal (SDO) becomes active. At

this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this five bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SClk pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SClk pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SClk periods. Prior to the rising edge of SClk Cycle # 9 (see Figure 31) the user must begin to apply the eight bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SClk. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this "combined" signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.
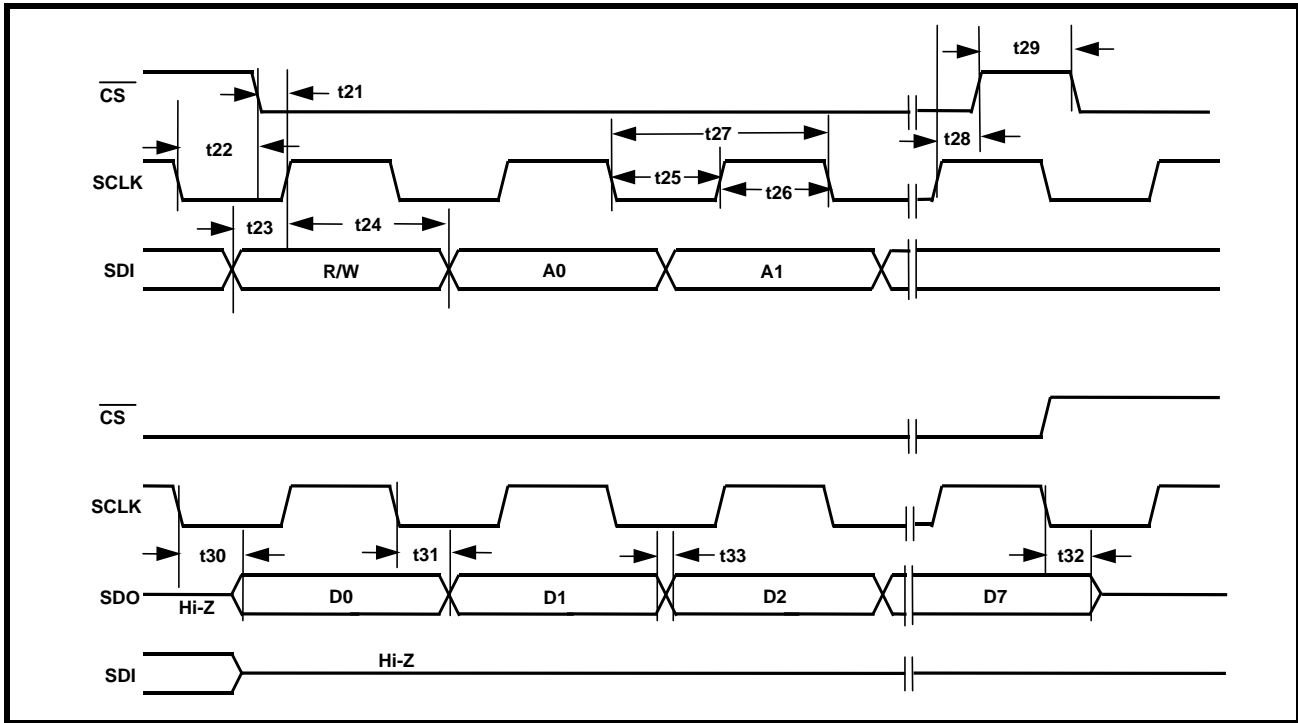
NOTES:
1. A4 and A5 are always "0"
2. R/W = "1" for "Read" Operations
3. R/W = "0" for "Write" Operations
4. - Denotes a "don't care" value

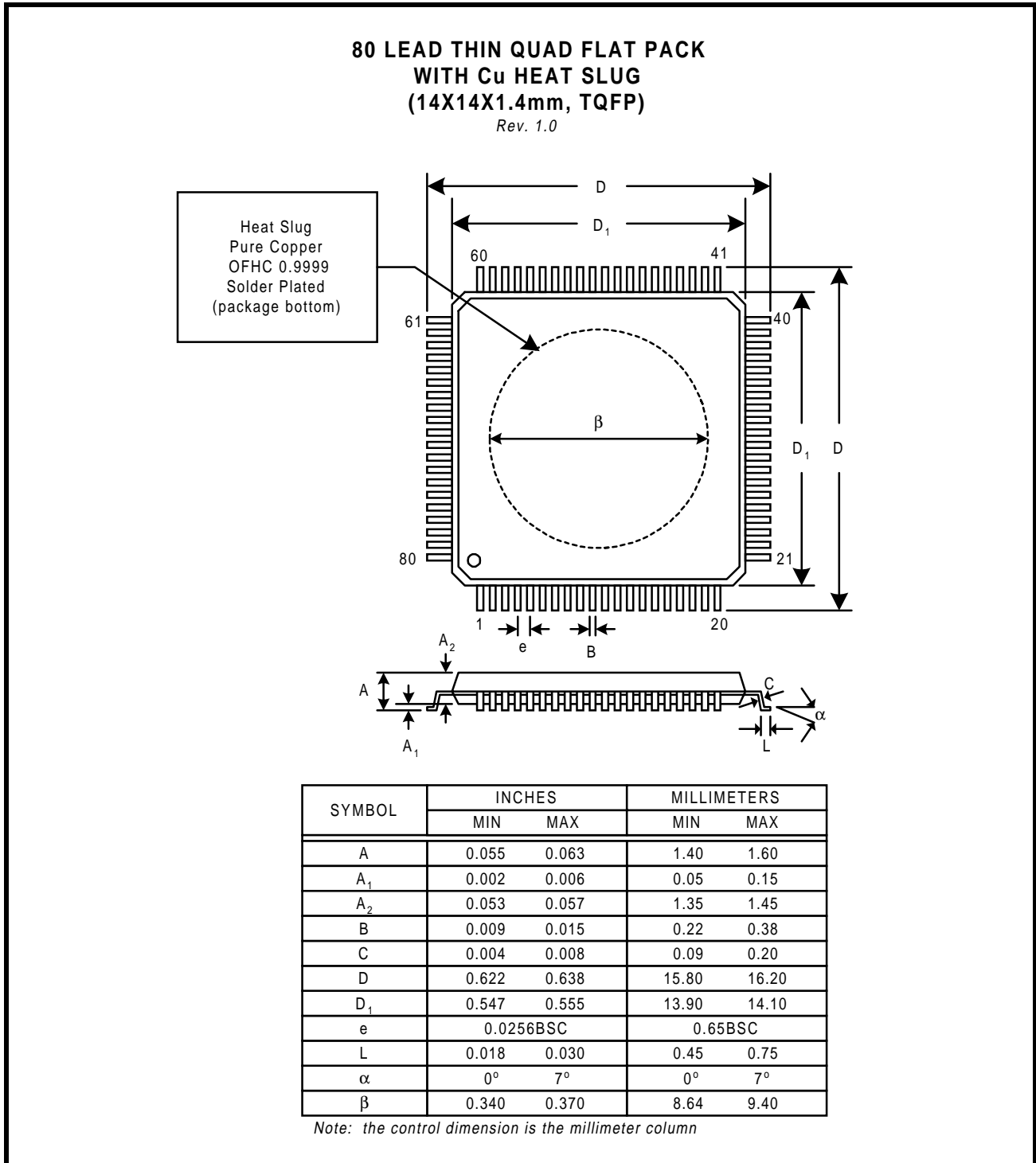**FIGURE 31. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE**
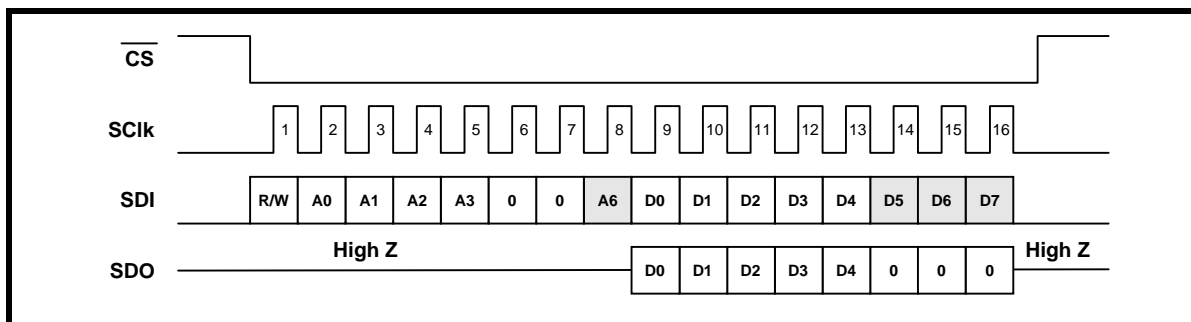
FIGURE 32. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT7302IV	80 Pin Thermally Enhanced TQFP	-40°C to +85°C
THERMAL INFORMATION	Theta - J_A = 23° C/W	Theta J_C = 5.32° C/W

PACKAGE DIMENSIONS

80 LEAD THIN QUAD FLAT PACK
WITH Cu HEAT SLUG
(14X14X1.4mm, TQFP)
Rev. 1.0

Heat Slug
Pure Copper
OFHC 0.9999
Solder Plated
(package bottom)

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D_1	0.547	0.555	13.90	14.10
e	0.0256BSC		0.65BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	0.340	0.370	8.64	9.40

Note: the control dimension is the millimeter column

REVISION HISTORY

Rev. 1.0.1: Pin naming conventions standardized with use of uppercase and lowercase letters. Modified and added title to Pin Out diagram for readability.

The pin descriptions for pins 30 ("REQ_EN1"), 31 ("REQ_EN2"), 61 ("TxOFF2"), 80 ("TxOFF1") have been revised. Added Table 7.

Rev. 1.0.2: Added Absolute Maximum Ratings and Test Conditions. Book marked PDF file.

Rev. 1.0.3: Minor formatting changes for readability

Rev. 1.1.0: Standardize pin names, updated block diagram, updated Electrical Characteristics, minor grammar edits, removed "Preliminary".

Rev. 1.1.1: Pin 7 - Receive Analog VDD to Receive Digital VDD and pin 56 - Transmit Digital GND instead of Receive. Nomenclature for GND and VDD changed to include A-for analog, and D-for Digital. Package designation from IQ to IV.

Rev. 1.1.2: Added Tx Control title in block diagram.

Rev. 1.1.3: Modified package dimensions drawing adding Heat Slug integral to package bottom.

Rev. 1.1.4: Modified figures 3 & 4

Rev. 1.1.5: Modified figure 4, LCV signal

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