AN4200
Application note

Four-layer demonstration board based on the STA333IS

Introduction

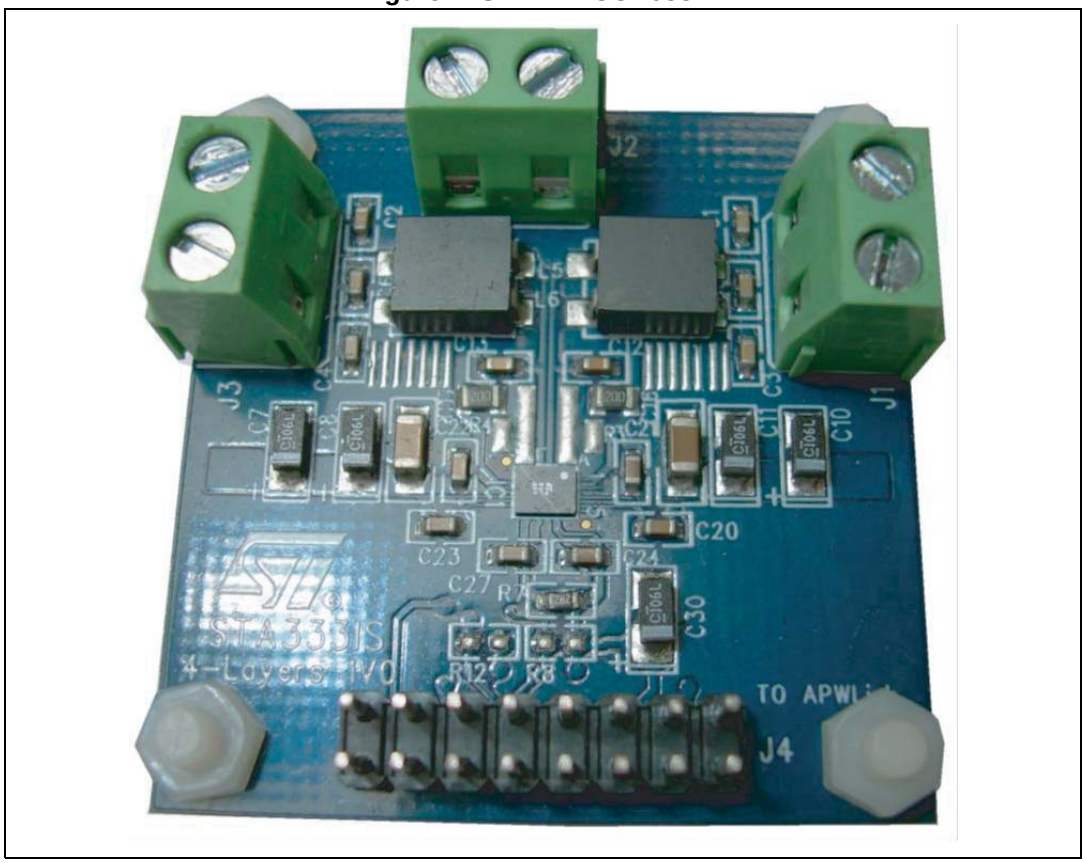
The STEVAL-CCA053V1 is a four-layer demonstration board designed for the evaluation of the STA333IS two-channel, high-efficiency Sound Terminal® device.

The purpose of this application note is to show:

- how to connect the STA333IS demonstration board
- the performance of the STA333IS device
- how to avoid critical board and layout issues

All the results and characterization data included in this application note have been measured using Audio Precision equipment. Reference documents consist of the STA333IS datasheet, schematic diagrams and PCB layout.

Figure 1. STEVAL-CCA053V1



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1 Test conditions and connections of demonstration board

1.1 Power supply signal and interface connection

1. Connect the power supply to the $+V_{CC}$ and GND terminal blocks (J2)
2. Connect the STEVAL-CCA053V1 interface board to the J4 connector
3. Connect the S/PDIF signal cable to the RCA jack on the STEVAL-CCA035V1 board. The signal source should be the Audio Precision equipment or a DVD player.
4. Adjust the voltage level of the power supply. The voltage range of the DC power supply is 4.5 V to 18 V.
5. Connect the load to the connectors J1 and J3

1.2 Output configuration

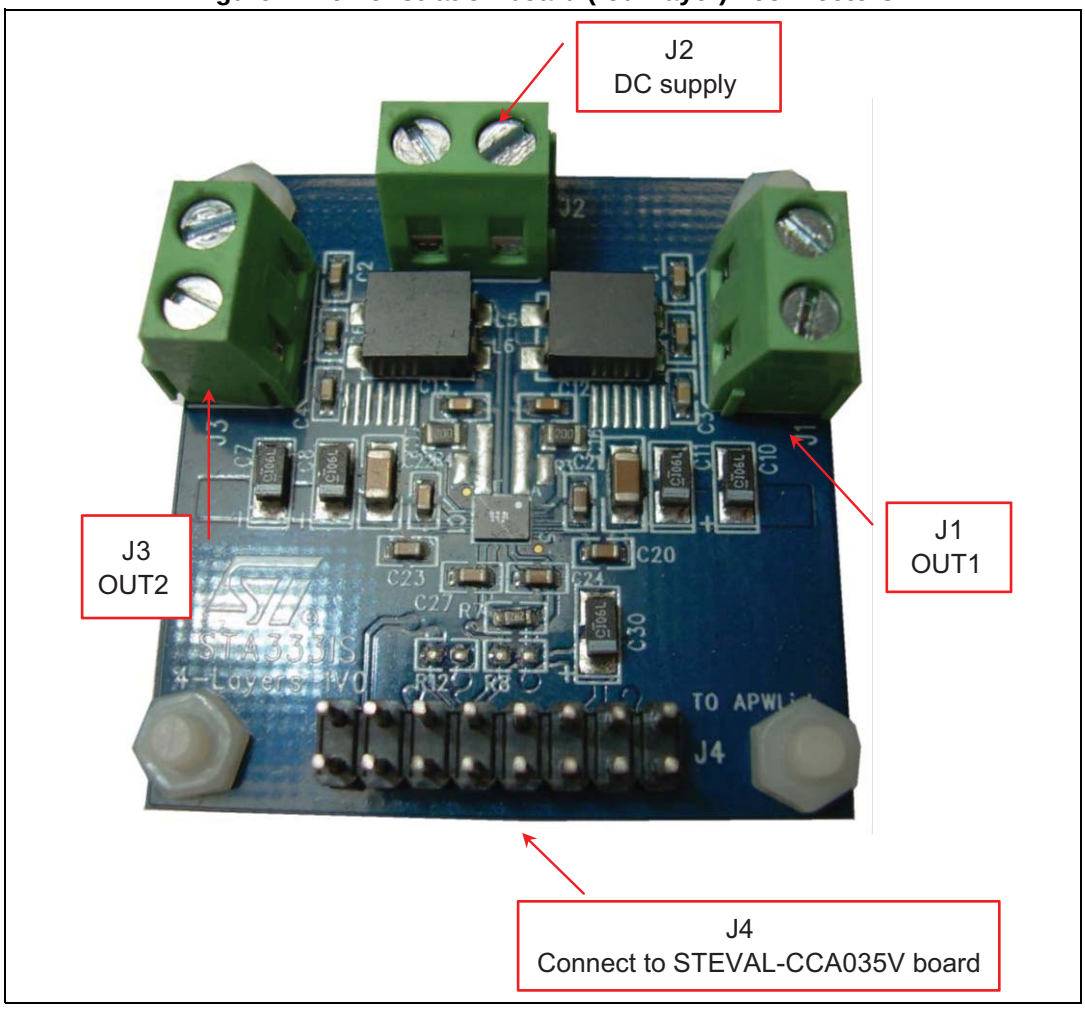
The STA333IS demonstration board can be only configured for 2.0 channels and BTL outputs.

1.3 Required equipment

- Audio Precision (System 2700)
  - Audio Analyzer: Mod. SYS2722 -192K
  - Class-D filter: AUX-0025 filter
  - Multifunction module: DCX-127
- DC power supply (4.5 V to 18 V)
  - Lambda Genesys Gen 80-19
  - HP 6038A
- Digital oscilloscope: Tektronix TDS5054B
- Digital multimeter: AGILENT Mod. 34410A
- PC with APWorkbench control software installed

1.4 Board connections

Figure 2. Demonstration board (four-layer) - connectors



2 Schematic diagram and PCB layout

2.1 Schematic

Figure 3. Schematic diagram - part 1

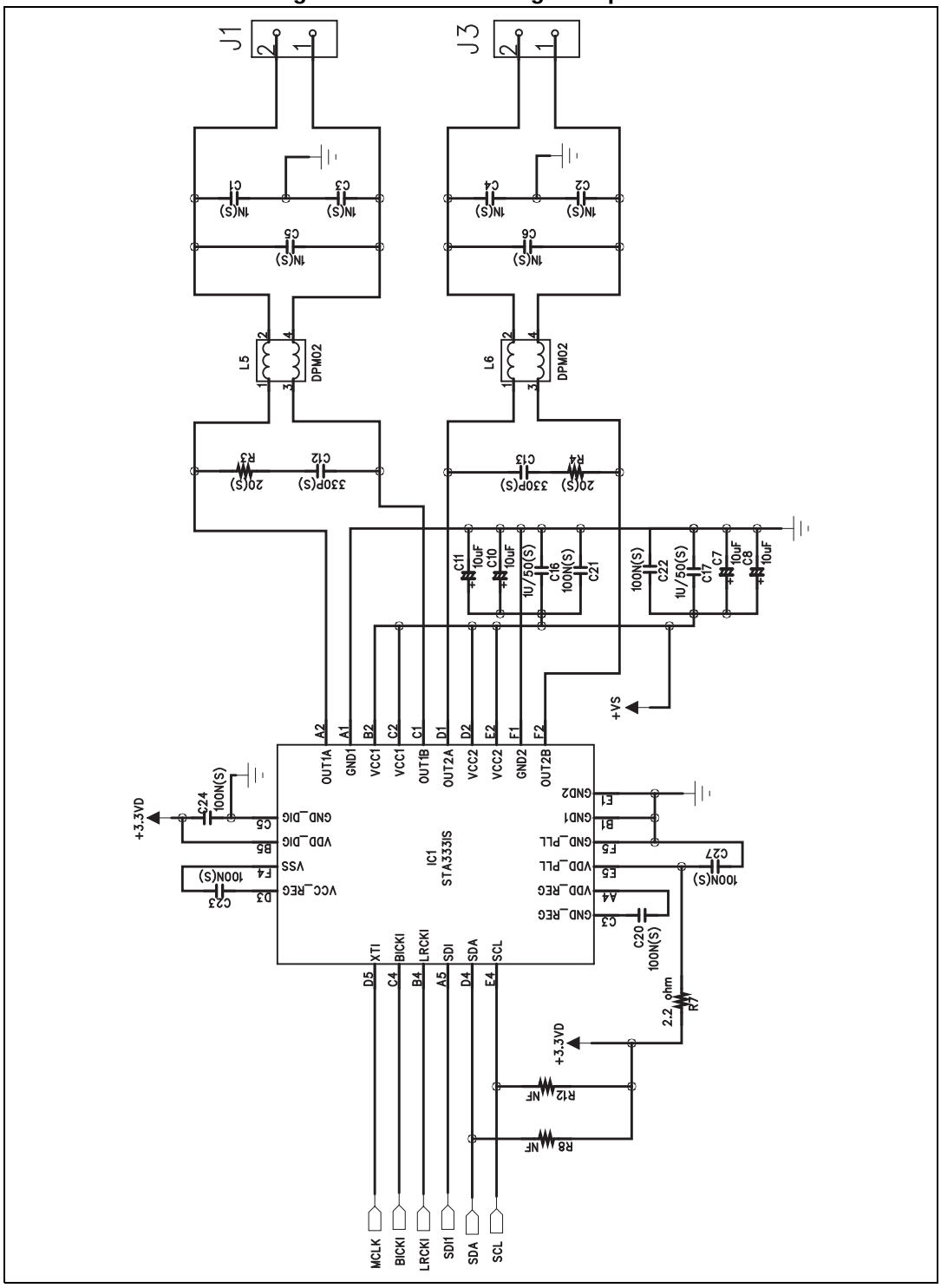
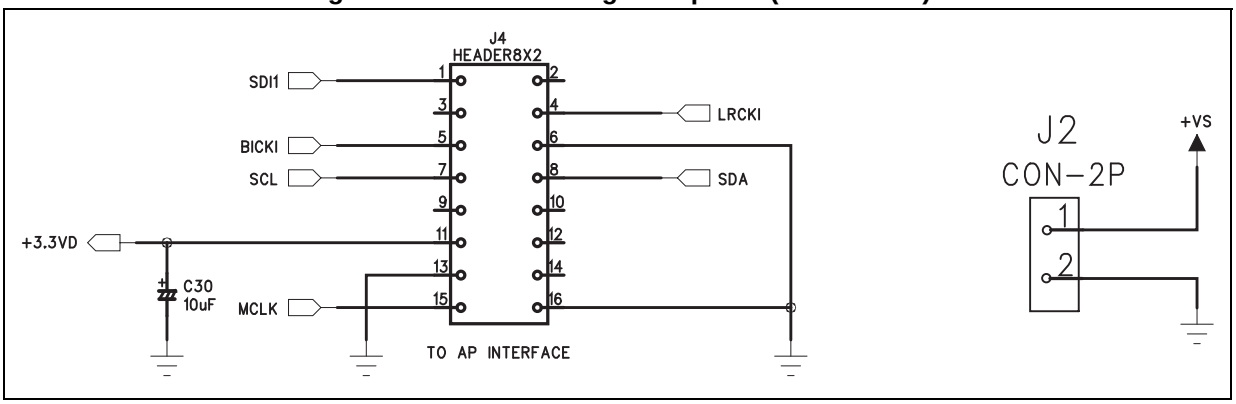
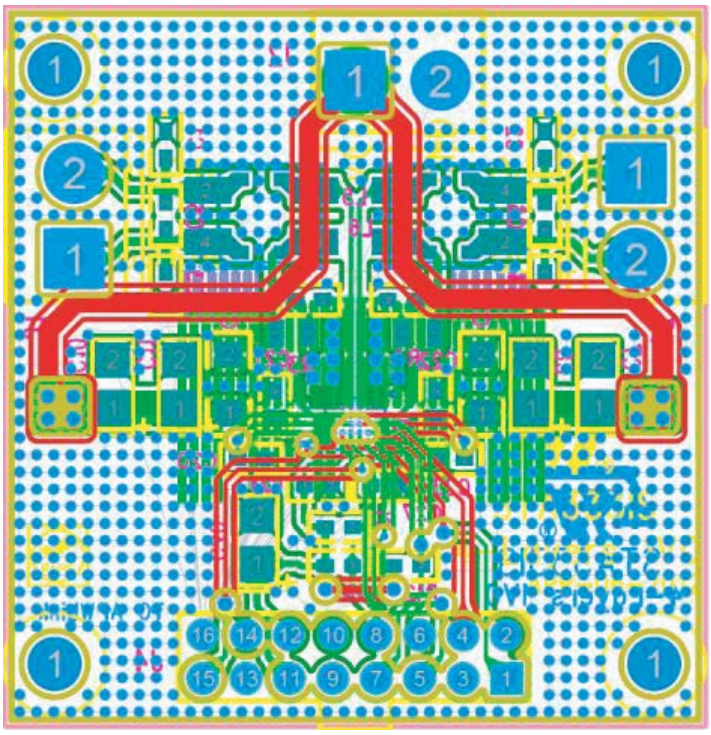


Figure 4. Schematic diagram - part 2 (connectors)



2.2 PCB layout

Figure 5. STEVAL-CCA053V1 board - four-layer PCB



Note: Please refer to Figure 18 through Figure 21 on page 17 for the top, inner layer 2, inner layer 3, and bottom views, respectively.

2.3 Bill of material

Table 1. Bill of material

No.	Type	Footprint	Description	Qty	Reference	Manufacturer
1	Connector	Through-hole	2P pitch: 5 mm connector terminal	3	J1, J2, J3	Any source
2	Header	Through-hole	16P (8 x 2 row) 2.5 mm header	1	J4	Any source
3	CCAP	CAP0603	50 Volt NPO 330 pF ±10%	2	C12, C13	Murata
4	CCAP	CAP0603	50 Volt 1nF ±10%	6	C1, C2, C3, C4, C5, C6	Murata
5	CCAP	CAP0603	50 Volt 100 nF ±10%	6	C20, C21, C22, C23, C24, C27	Murata
6	CCAP	CAP1206	50 Volt 1U ±10%	2	C16, C17	Murata
7	ECAP	CAP1206	10 µF / 16 V	5	C7, C8, C10, C11, C30	Samsung
8	RES	R1206	6R2, ±5% 1/8W	4	R1, R2, R5, R6	Murata
9	RES	R1206	20 ±5% 1/8W	2	R3, R4	Murata
10	RES	R0603	2R2 ±5% 1/16W	1	R7	Murata
11	RES	R0603	NS	2	R8, R12	
12	Plastic rod		Hexagonal rod 15 mm length, male type	4	Four corners	Any source
13	Plastic rod		Hexagonal rod 8 mm length, female type	4	Four corners	Any source
14	IC	CSP 5x6 array	STA333IS	1	IC1	STMicroelectronics
15	Coil	SMD	DPM02, MARUWA	2	L5, L6	Maruwa
16	PCB		STA333IS 4-layer 1V0	1		Fastprint

3 APWorkbench settings

Figure 6. APWorkbench - device selection

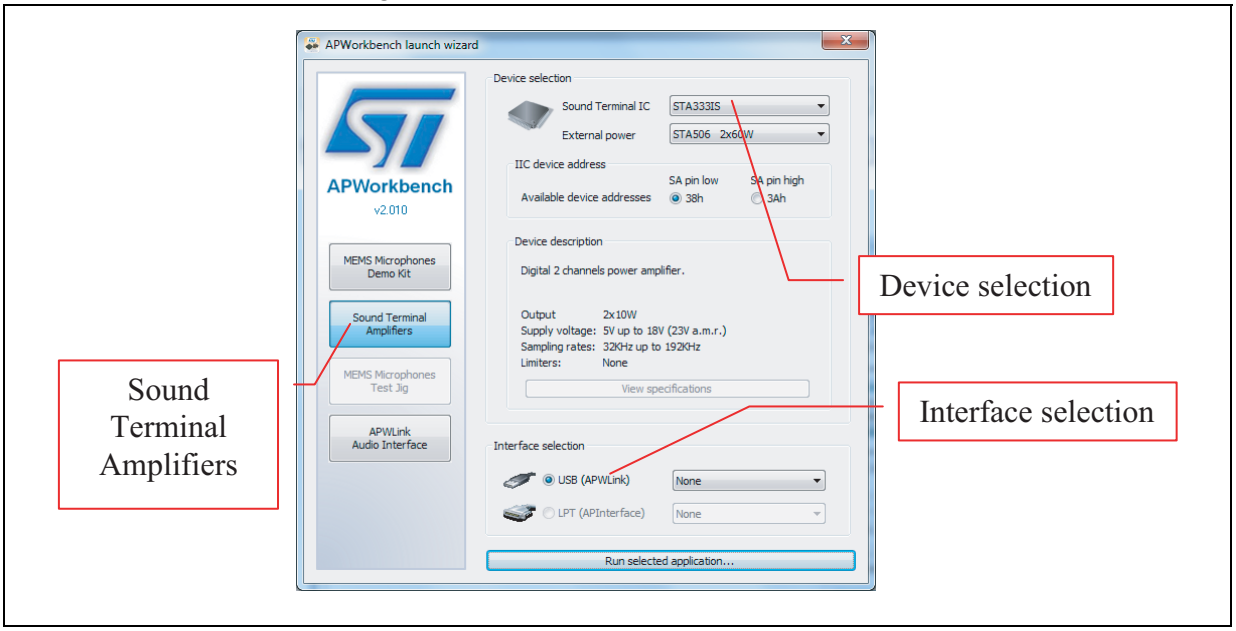
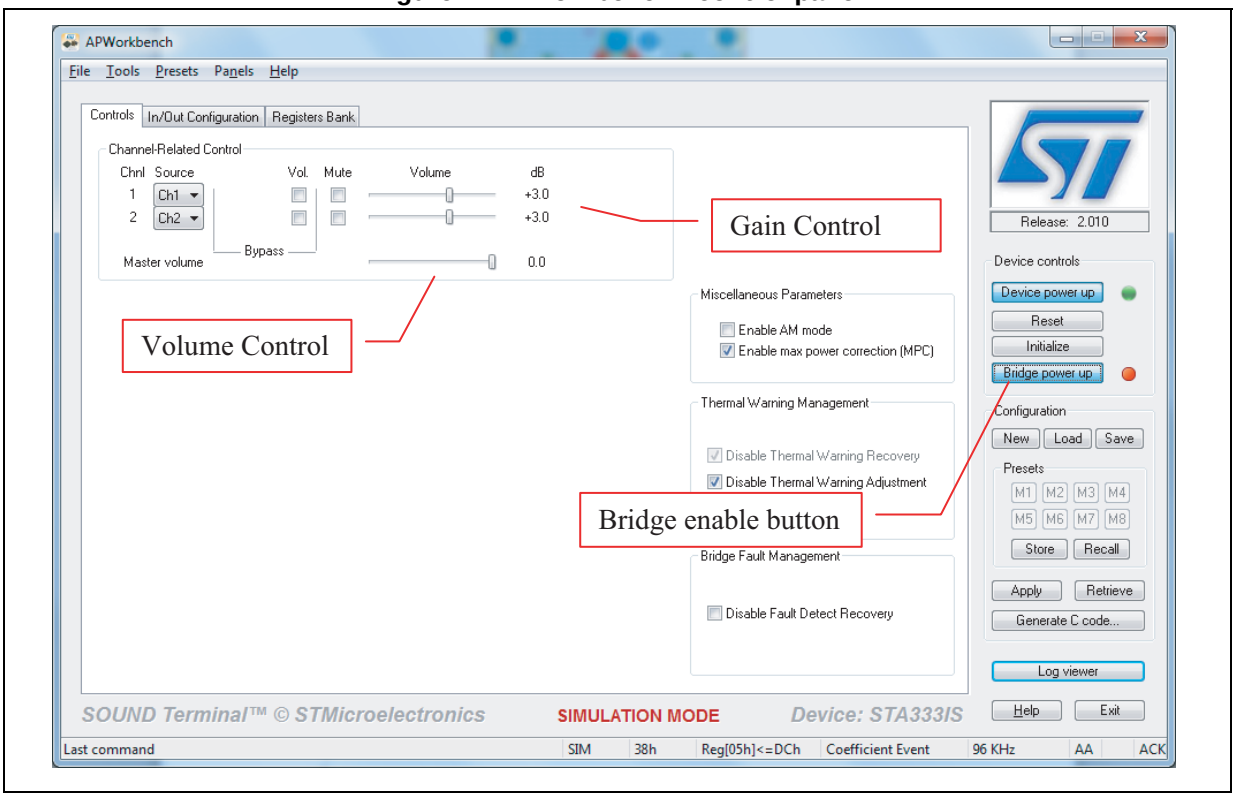
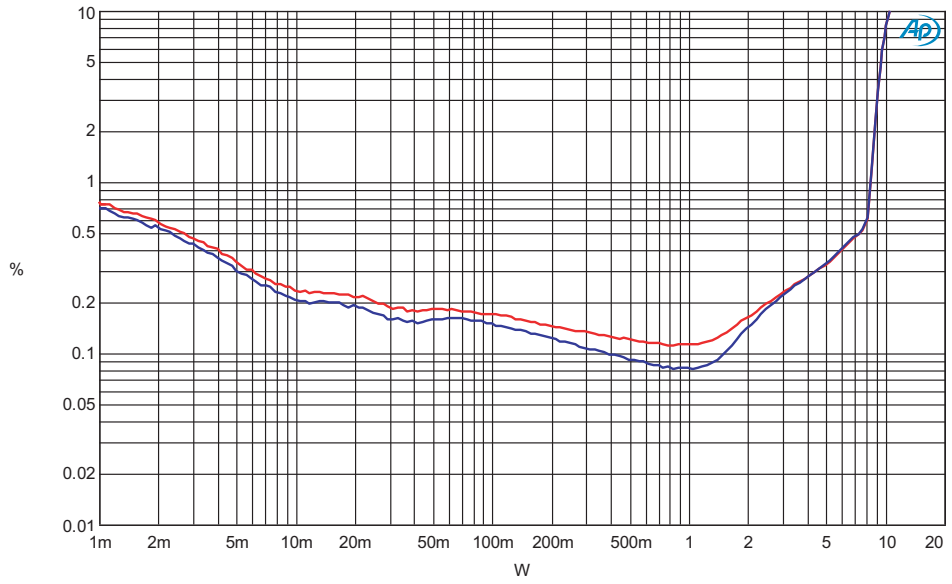


Figure 7. APWorkbench - control panel



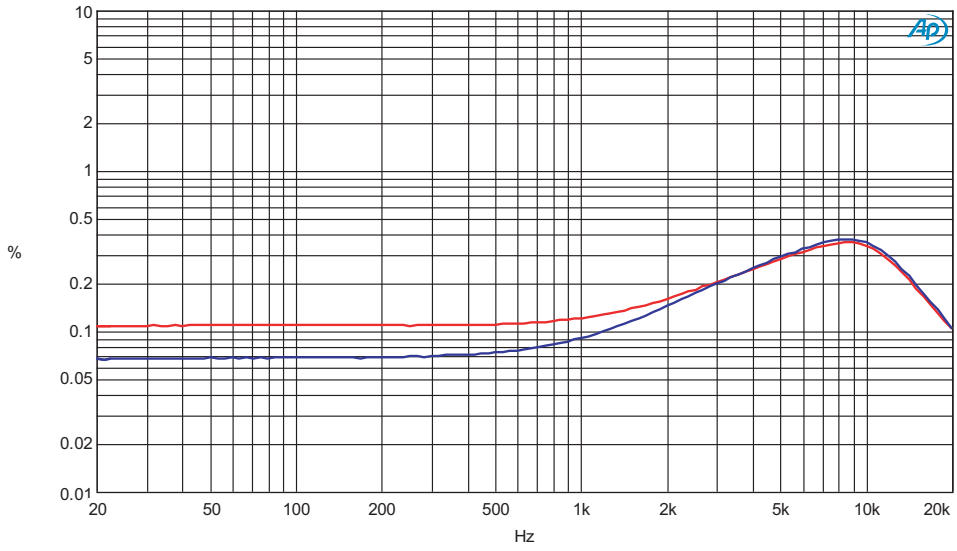
4 Test results

Figure 8. THD+N vs. power - V_{CC} = 12.5 V, load = 8 Ω, 1 kHz



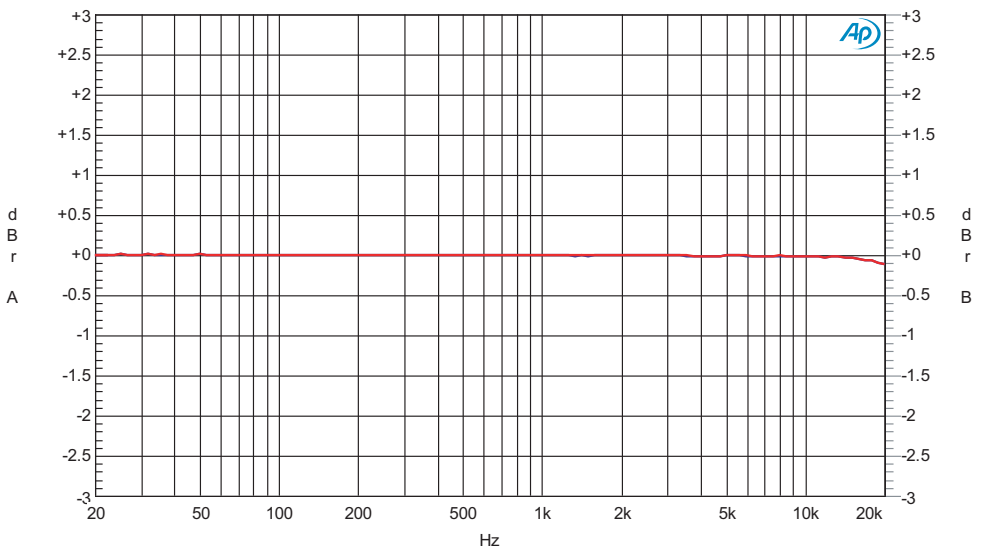
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	Ch1; Vcc= 12.5V, 1kHz, 8ohm
1	3	Blue	Solid	2	Anlr.THD+N Ratio	Left	Ch2; Vcc= 12.5V, 1kHz, 8ohm

Figure 9. THD+N vs. frequency - V_{CC} = 12.5 V, load = 8 Ω, Pout = 1 W at 1 kHz



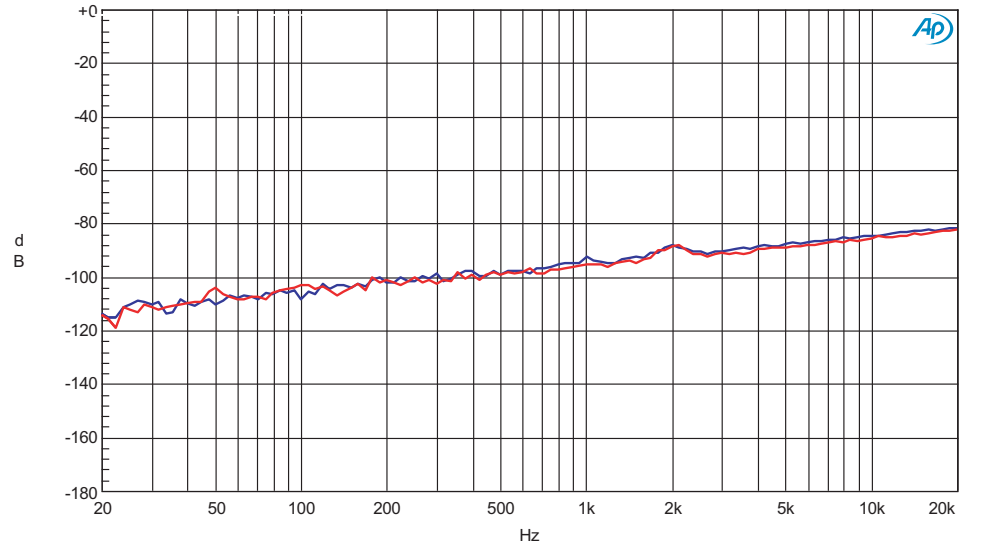
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	Ch1; Vcc= 12.5V, 1W@1kHz, 8ohm
1	2	Blue	Solid	2	Anlr.THD+N Ratio	Left	Ch2; Vcc= 12.5V, 1W@1kHz, 8ohm

Figure 10. Frequency response - V_{CC} = 12.5 V, load = 8 Ω, Pout = 1 W at 1 kHz



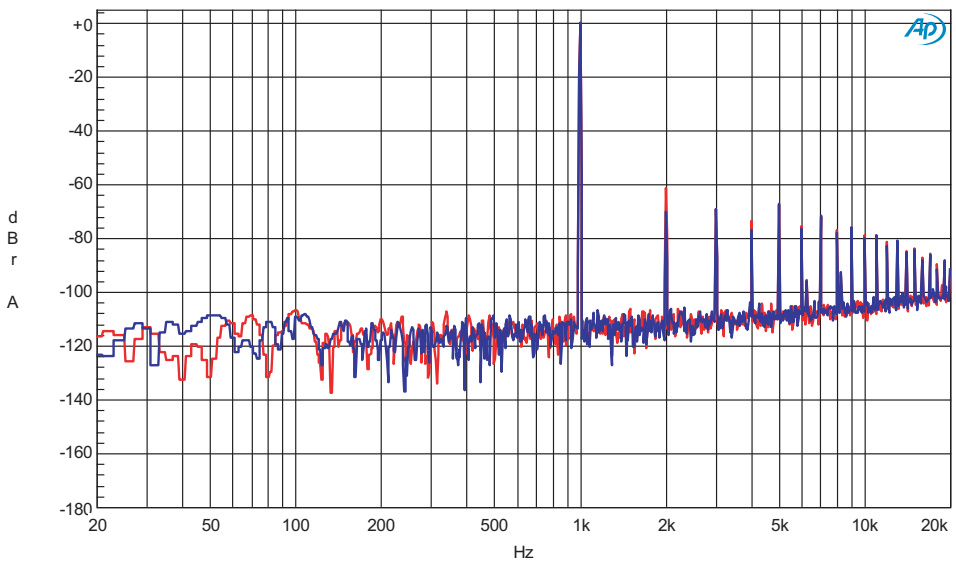
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Level A	Left	Ch1; Vcc= 12.5V, 1kHz, 8ohm
1	2	Blue	Solid	2	Anlr.Level B	Right	Ch1; Vcc= 12.5V, 1kHz, 8ohm

Figure 11. Crosstalk - V_{CC} = 12.5 V, load = 8 Ω, Pout = 1 W at 1 kHz



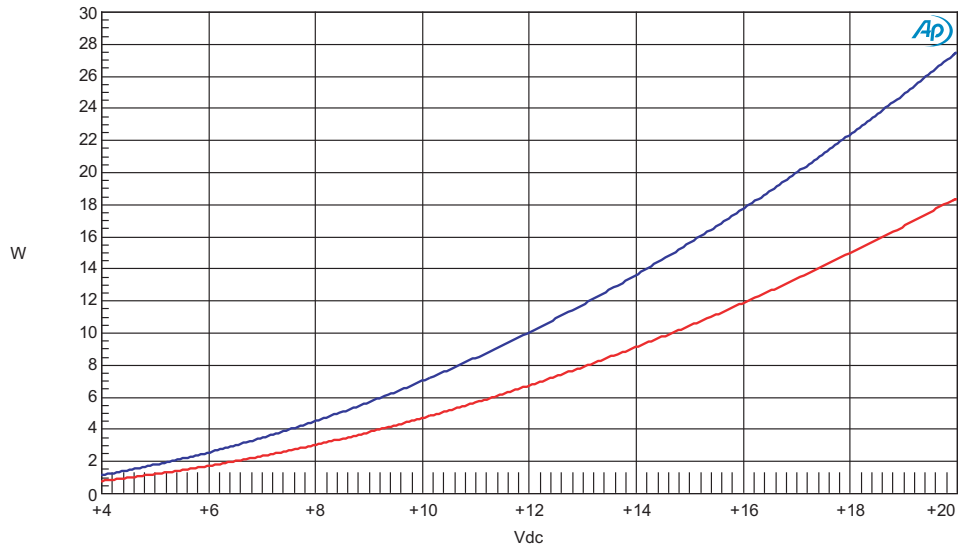
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Crosstalk	Left	Ch2 =off; Vcc=12.5V, Ref:0dB@1W@1kHz, 8ohm
1	2	Blue	Solid	2	Anlr.Crosstalk	Left	Ch1 =off; Vcc=12.5V, Ref:0dB@1W@1kHz, 8ohm

Figure 12. FFT - V_{CC} = 12.5 V, load = 8 Ω, Pout = 1 W at 1 kHz



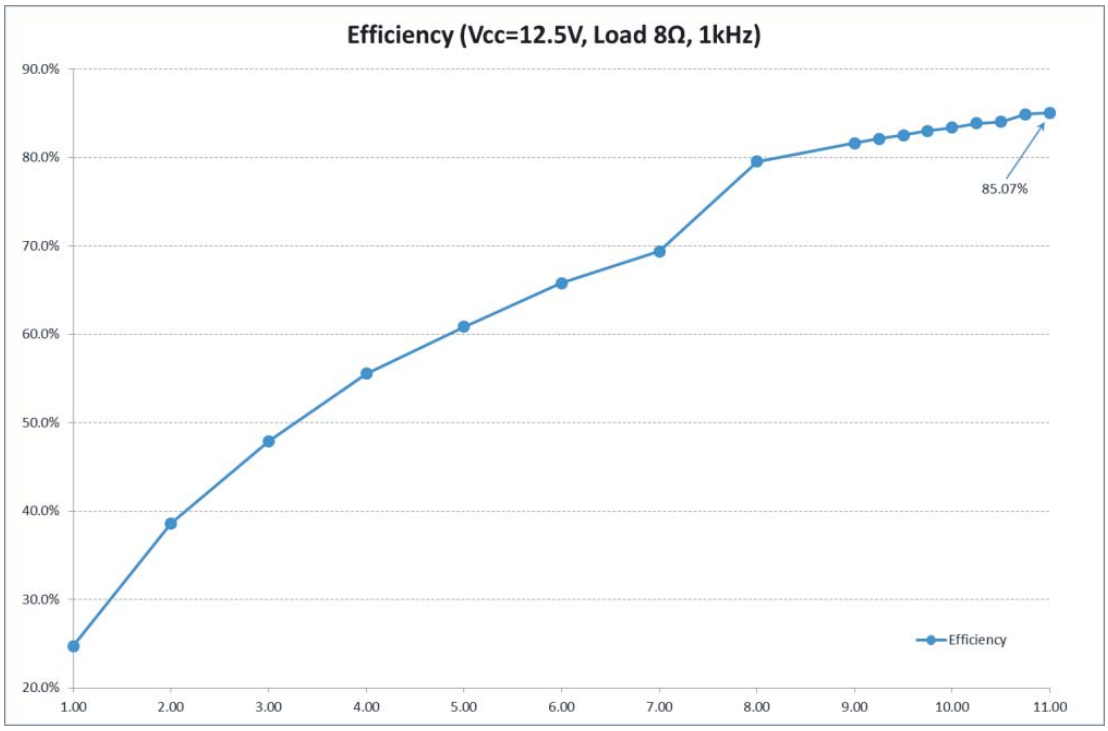
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Fft.Ch.1 Ampl	Left	Ch1; Vcc=12.5V; 1W@1kHz;
1	2	Blue	Solid	2	Fft.Ch.2 Ampl	Left	Ch2; Vcc=12.5V; 1W@1kHz;

Figure 13. Output power vs. supply voltage - load = 8 Ω, 1 kHz



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Level A	Left	Ch1; Undistorted Output; (1kHz - Gain=0dB)
1	3	Blue	Solid	2	Anlr.Level B	Left	Ch2; THD˜10%; (1kHz - Gain=+3dB)

Figure 14. Efficiency - V_{CC} = 12.5 V, 1 kHz, load = 8 Ω (stereo)



5 Thermal test - V_{CC} = 12.5 V, 1 kHz, load= 8 Ω (stereo)

5.1 Test conditions

V_{CC} =12.5 VDC

Load= 8 Ω (resistive dummy load)

Gain= +3 dB (both L&R channels)

All channels ON

AP filter= 22 Hz ÷ 22 kHz

Output power: 2 x 10 W (adj. using post-scale)

T_{amb} = 31 °C

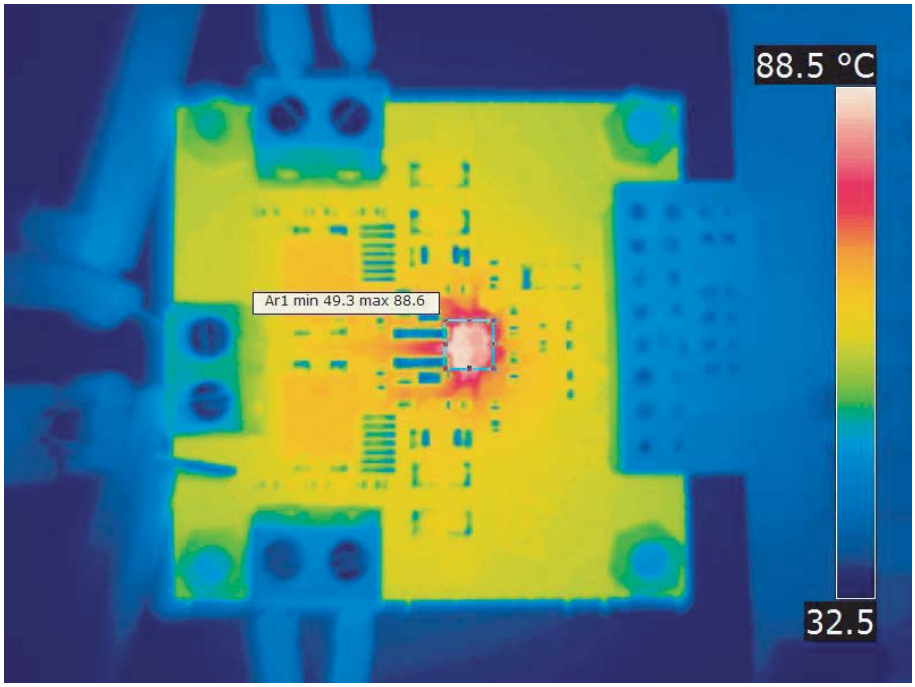
5.2 Test results

T_{max} = 88.6 °C

T_{amb} = 31 °C

ΔT = 57.6 °C

Figure 15. Thermal analysis - V_{CC} = 12.5 V - 2 x 10 W at 1 kHz



6 Design guidelines for schematic and PCB layout

6.1 General

- Absolute maximum rating: 20 V
- Bypass capacitor 100 nF in parallel to 1 µF and 10 µF for each power V_{CC} branch. Preferable dielectric is X7R.
- Vdd and ground for the digital section should be separated from the other power supply.
- Coil saturation current compatible with the peak current of the application

6.2 Decoupling capacitors

The decoupling capacitors can be shared for each V_{CC} branch. The decoupling capacitors must be placed as close as possible to the IC pins.

The capacitor and the decoupling capacitor must be on the same layer as well as the track used to connect the capacitors and the positive V_{CC} device pins.

6.3 Snubber network

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 Ω.

The power dissipation in this network can be defined by the following formula which considers the power supply, frequency and capacitor value:

$P = C \cdot Freq_{PWM} \cdot (2 \cdot V_{OUT})^2$

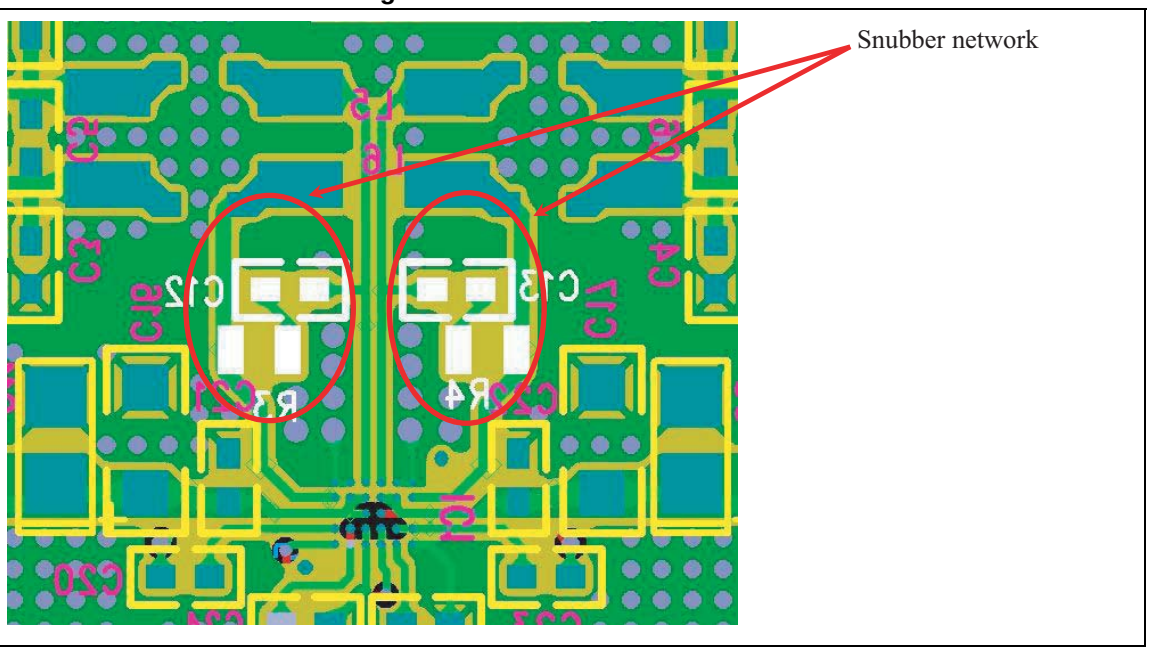
This power is dissipated on the series resistance.

6.4 PCB layout

6.4.1 Snubber layout

Solder the snubber network as close as possible to the related IC pin.

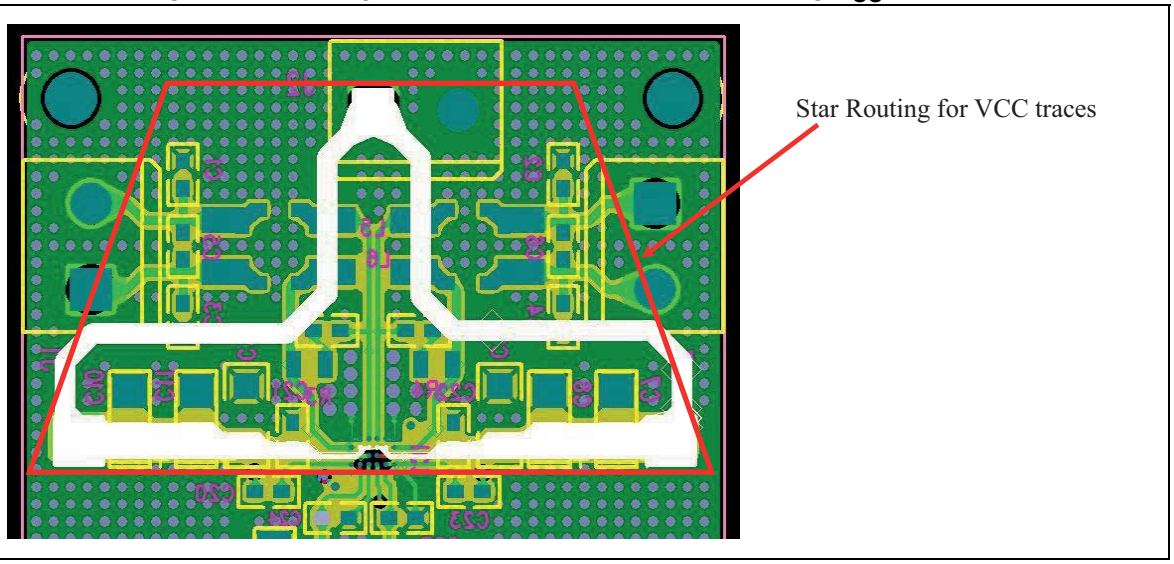
Figure 16. Snubber network



6.4.2 V_{CC} traces

Design the PCB tracks to implement a star routing for the V_{CC} traces.

Figure 17. PCB layout recommendations - star routing V_{CC} traces



6.4.3 Ground plane and heatsink

To dissipate the power not delivered to the loads, a large ground plane should be implemented. This solution allows removing the heat from the device without adding an external heatsink.

Note: It is mandatory to have a large ground plane on the top layer, inner layer 2, inner layer 3, and the bottom layer and solder the slug on the PCB.

Figure 18. PCB layout recommendation - large ground plane on the top side

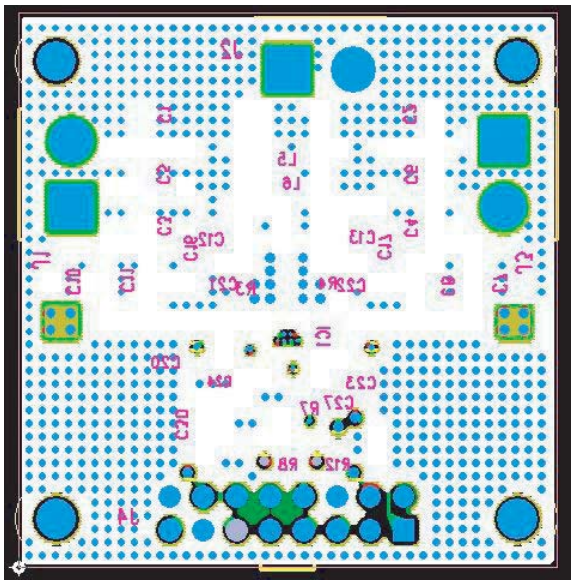


Figure 19. PCB layout recommendation - large ground plane on the inner layer 2

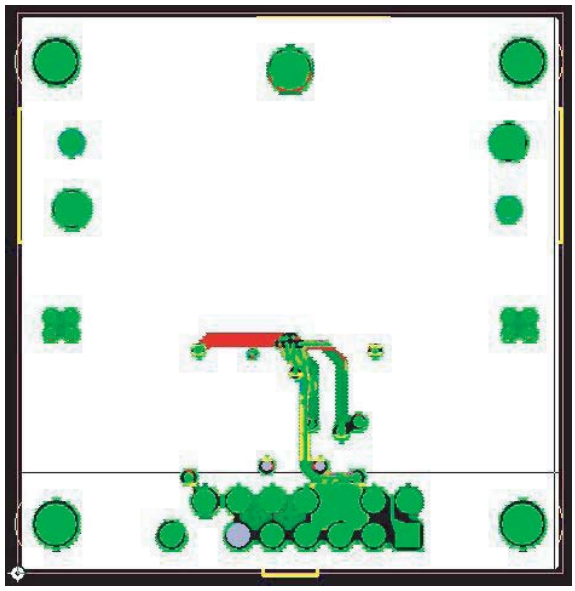


Figure 20. PCB layout recommendation - large ground plane on the inner layer 3

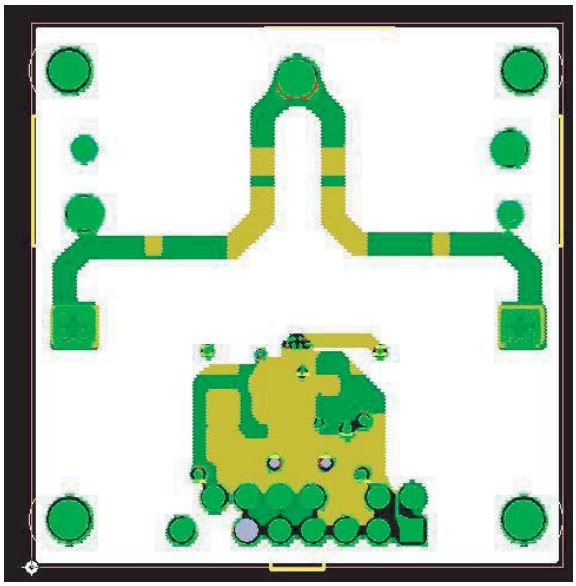
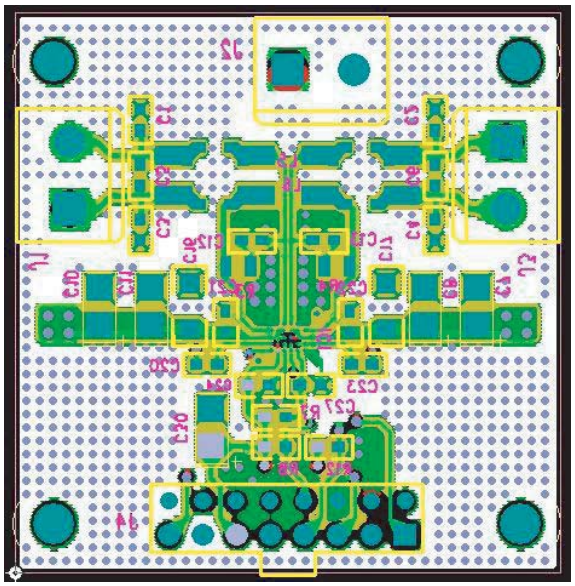


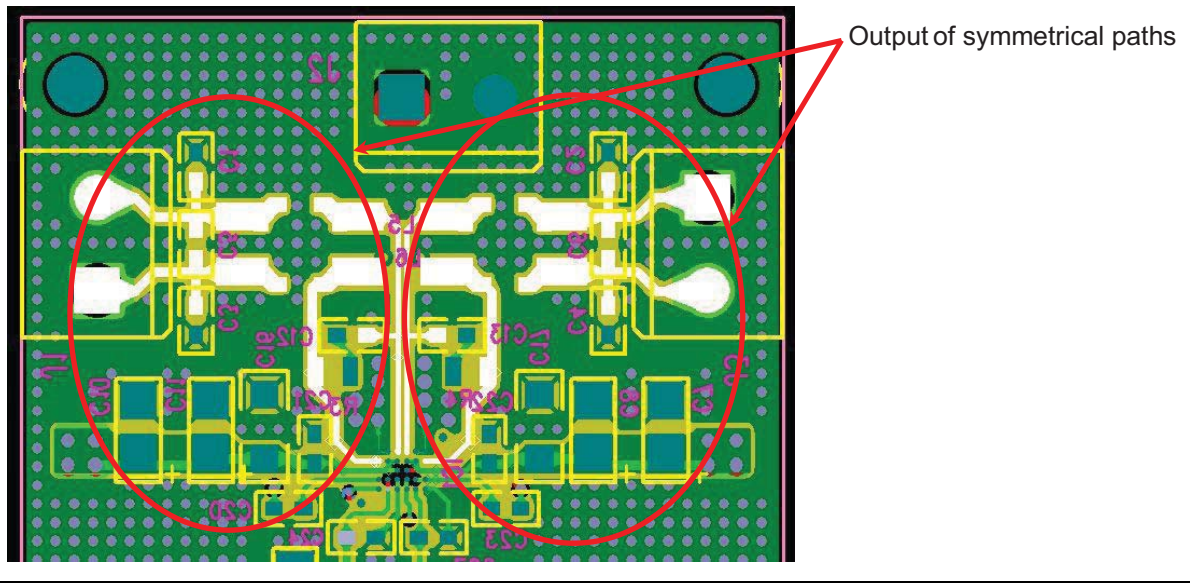
Figure 21. PCB layout recommendation - large ground plane on the bottom side



6.4.4 Output filter

It is recommended to design the PCB using symmetrical paths and tracks.

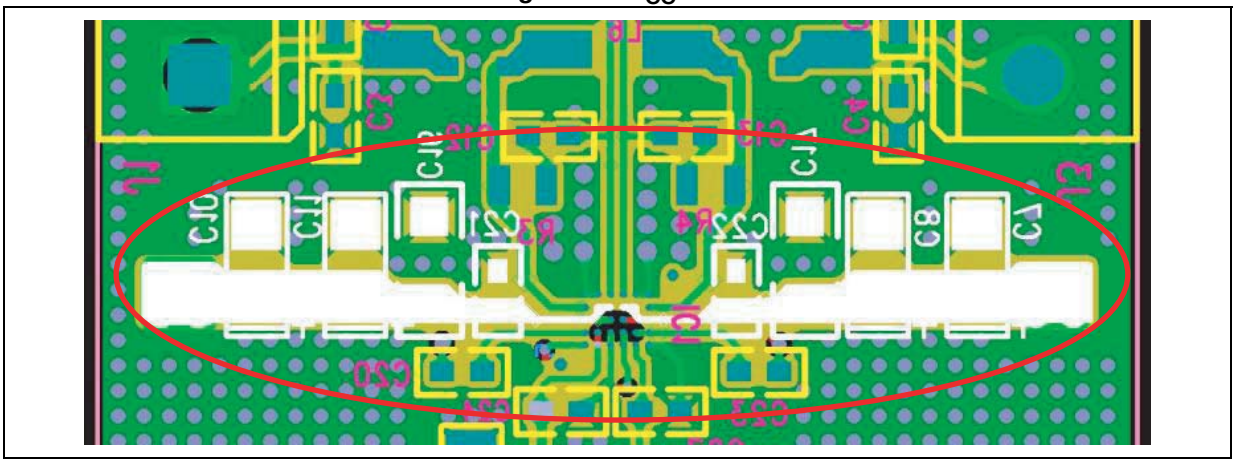
Figure 22. Output filter



6.4.5 V_{CC} filter for high frequency

The V_{CC} filter capacitors must be placed as close as possible to the supply pins. The ceramic capacitors must be positioned on the same layer of the device (in this demonstration board, on the top layer of the PCB) and the distance from the IC must be short and compatible with the minimum SMB mounting limitation.

Figure 23. V_{CC} filter



The PWM frequency is 384 kHz (with Fs = 48 kHz) with very fast transition time. In order to compensate the inductive effect of the copper track, the ceramic capacitors must be placed as close as possible to the supply pins. The recommended distance between the capacitors and the supply pins is less than 5 mm.

7 Revision history

Table 2. Document revision history

Date	Revision	Changes
01-Jul-2013	1	Initial release.

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