

# LIBERATOR CL10K50V

## Key Features



- ◆ Fully Compatible To The Altera® FLEX® 10KA Family
- ◆ Prototype Your System With Altera FPGAs
- ◆ Seamlessly Migrate Production To Clear Logic
- ◆ No ASIC Engineering, No NRE, And No Test Vector Development
- ◆ Very Fast, Dense Signal Routing Using Vertical Link Interconnect
- ◆ "Gate Array" Option Eliminates Configuration EPROMs
- ◆ Fabricated Using 0.35 Micron CMOS Process
- ◆ Very Low Power Consumption (Active And Standby)
- ◆ High Density
  - 50,000 Usable Gates
  - 2,880 Logic Elements
  - 20,480 RAM Bits
  - 274 Maximum User I/O Pins

## CL10KA Product Family Overview

Parameter	CL10K30A	CL10K50V	CL10K100A
Typical Gates (Logic and RAM)	30,000	50,000	100,000
Maximum System Gates	69,000	116,000	158,000
Logic Elements	1,728	2,880	4,992
Logic Blocks	216	360	624
Embedded Array Blocks	6	10	12
Total RAM Bits	12,288	20,480	24,576
Max User I/O Pins	189	274	406
Speed Grades	-1, -2, -3	-1, -2, -3, -4	-1, -2, -3
Packages	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin FBGA	240-pin PQFP 240-pin RQFP 356-pin SBGA	240-pin PQFP 240-pin RQFP 356-pin SBGA 484-pin FBGA 600-pin SBGA

10KA tbl 01A

**Description**

The LIBERATOR™ CL10KA family offers you all of the time-to-market benefits of designing with programmable logic. Simply use Altera FLEX 10KA FPGAs to prototype and verify the design. Then, take five minutes to submit the bitstream using Clear Logic's web site! Within eight weeks, your system can be in volume production using compatible Clear Logic devices.

LIBERATOR technology frees you to completely design, prototype, and verify your custom logic using Altera FLEX 10KA products. Clear Logic's innovative technology eliminates NRE costs, test vector development, ordering minimums, and long lead times. No re-simulation or re-layout is required, because Clear Logic offers an architecture that is exactly compatible to the functionality of the FPGA prototype. Clear Logic's NoFault® test technology ensures complete test coverage through the use of special scan test registers.

The LIBERATOR family is based upon an array of logic elements. Each logic element contains a configurable look-up table for combinatorial functions and a register for sequential operations. Eight logic elements in a group form a block. Logic functions and signal routing are defined by Clear Logic's proprietary vertical metal links.

Laser-based configuration allows quick-turn prototyping and eliminates NRE costs for photomasks. Inherent CL10KA family performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

**Configuration**

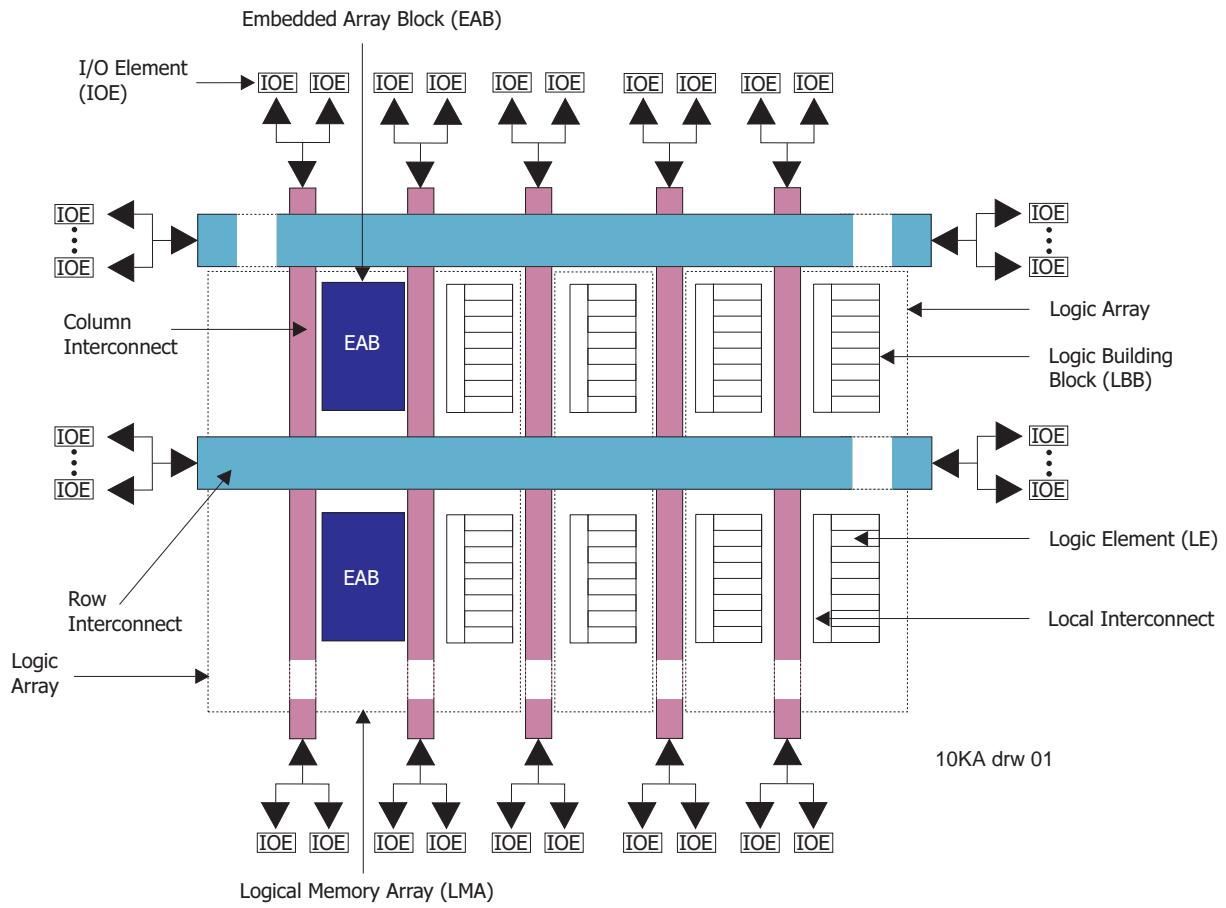
The "Gate Array" configuration mode eliminates the need for external EPROMs or software configuration. The LIBERATOR device is already factory-configured when it is shipped. When using the device in the "Gate Array" mode, it powers up fully configured. In this mode, if the customer selects INIT\_DONE option, this pin will always be high.

**Additional  
Information**

For further information on designing with the LIBERATOR family, please refer to these documents:

- ◆ AN-01: Requesting a First Article. This document provides instructions on how to request first articles by submitting a bitstream file to Clear Logic's web site.
- ◆ AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL10K family and other Clear Logic devices.
- ◆ AN-13: LIBERATOR -- A New Way To Design. This document describes the most efficient path for custom logic designs up to 200K gates using FPGA design techniques and going to production with Clear Logic.
- ◆ AN-14: CL10K Technology White Paper. This document outlines the technologies employed by the LIBERATOR family.
- ◆ AN-15: LIBERATOR System Configuration. This document contains a detailed discussion of all aspects of configuring CL10K-based systems.
- ◆ AN-16: Introduction to the Clear Logic Verilog Model Generator. Clear Logic now has Verilog models of your FPGA converted design. Learn what it is and how it can help you.
- ◆ AN-17: Clear Logic LIBERATOR Design Models. This document outlines the capabilities and freedom available in the Clear Logic Verilog and VHDL design models.
- ◆ AN-18: Debugging Designs Using Clear Logic Models. This document shows the enhanced troubleshooting capabilities that the Clear Logic LIBERATOR Verilog/VHDL design models bring to the system debugging process.

# Block Diagram



**Pin Configuration**

Pin Name	240-Pin PQFP/RQFP	356-Pin SBGA
MSEL0	124	D4
MSEL1	123	D3
nSTATUS	60	D24
nCONFIG	121	D2
DCLK	179	AC5
CONF_DONE	2	AC24
INIT_DONE	26	T24
nCE	178	AC2
nCEO	3	AC22
nWS	238	AE24
nRS	236	AE23
nCS	240	AD24
CS	239	AD23
RDYnBSY	23	U22
CLKUSR	11	AA24
DATA7	190	AF4
DATA6	188	AD8
DATA5	186	AE5
DATA4	185	AD6
DATA3	183	AF2
DATA2	182	AD5
DATA1	181	AD4
DATA0	180	AD3

10K50V tbl 01A

**Pin Configuration**

Pin Name	240-Pin PQFP/RQFP	356-Pin SBGA
TDI	177	AC3
TDO	4	AC23
TCK	1	AD25
TMS	58	D22
TRST	59	D23
Dedicated Inputs	90, 92, 210, 212	A13, B14, AF14, AE13
Dedicated Clock Pins	91, 211	A14, AF13
DEV_CLRn	209	AD13
DEV_OE	213	AE14
VCCINT	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26
VCCIO	-	A7, A23, B3, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18M AF3, AF7, AF16
GNDINT	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25
No connect	-	-
<b>Total user I/O pins</b>	<b>189</b>	<b>274</b>

10K50V tbi 01B

**DC Electrical Specifications**

**Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage		-0.5	4.6	V
V <sub>I</sub>	DC Input Voltage <sup>[1]</sup>		-2.0	5.75	V
I <sub>OUT</sub>	DC Output Current, per Pin		-25	25	mA
T <sub>STG</sub>	Storage Temperature	No Bias	-65	150	°C
T <sub>AMB</sub>	Ambient Temperature	Under Bias	-65	135	°C
T <sub>J</sub>	Junction Temperature	Under Bias		135	°C

10KA tbl 02

**Recommended Operating Conditions <sup>[2]</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply Voltage, Internal Logic and Input Buffers	Commercial Grade Devices	3.00	3.60	V
		Industrial Grade Devices	3.00	3.60	V
V <sub>CCIO</sub>	DC Input Voltage	Commercial Grade Devices	3.00	3.60	V
		Industrial Grade Devices	3.00	3.60	V
V <sub>I</sub>	Input Voltage		-0.5	5.75	V
V <sub>O</sub>	Output Voltage		0	V <sub>CCIO</sub>	V
T <sub>A</sub>	Operating Temperature	Commercial Temperature Range	0	70	°C
		Industrial Temperature Range	-40	85	°C
t <sub>R</sub>	Input Signal Rise Time			40	ns
t <sub>F</sub>	Input Signal Fall Time			40	ns

10KA tbl 03A

## DC Electrical Specifications cont.

### DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage		2.0		5.75	V
$V_{IL}$	Input LOW Voltage		-0.5		0.8	V
$V_{OH}$	3.3-V High-Level TTL Output Voltage	$I_{OH} = -8 \text{ mA DC}$	2.4			V
	3.3-V High-Level CMOS Output Voltage	$I_{OH} = -0.1 \text{ mA DC}$	$V_{CCIO} - 0.2$			V
$V_{OL}$	3.3-V High-Level TTL Output Voltage	$I_{OL} = 8 \text{ mA DC}$			0.45	V
	3.3-V High-Level CMOS Output Voltage	$I_{OL} = 0.1 \text{ mA DC}$			0.2	V
$I_{IN}$	Input Leakage Current	$V_I = 5.3\text{V to } -0.3\text{V}$	-10		10	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$V_O = 5.3\text{V to } -0.3\text{V}$	-10		10	$\mu\text{A}$
$I_{CC0}$	Standby Current	$V_I = \text{GND, no load}$		0.3	10	mA

10KA tbl 04A

### Capacitance<sup>[4]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0 \text{ V, } f = 1.0 \text{ MHz}$		10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0 \text{ V, } f = 1.0 \text{ MHz}$		10	pF

10KA tbl 05A



**AC Electrical Specifications**

**I/O Element Timing Parameters <sup>[5]</sup>**

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>IOD</sub>	IOE Register Data Delay		1.2		1.6		1.9		2.1	ns
t <sub>IOC</sub>	IOE Register Control Signal Delay		0.3		0.4		0.5		0.5	ns
t <sub>IOCO</sub>	IOE Register Clock to Output Delay		0.3		0.3		0.4		0.4	ns
t <sub>IOCOMB</sub>	IOE Combinatorial Delay		0.0		0.0		0.0		0.0	ns
t <sub>IOSU</sub>	IOE Register Setup Time Before Clock	2.8		2.8		3.4		3.9		ns
t <sub>IOH</sub>	IOE Register Hold Time After Clock	0.7		0.8		1.0		1.4		ns
t <sub>IOCLR</sub>	IOE Register Clear Delay		0.5		0.6		0.7		0.7	ns
t <sub>OD1</sub>	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = 5.0v, CL = 35 pF		2.8		3.2		3.9		4.7	ns
t <sub>OD3</sub>	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = 5.0v, CL = 35 pF		6.5		6.9		7.6		8.4	ns
t <sub>ZX</sub>	Output Buffer Disable Delay <sup>[6]</sup>		2.8		3.1		3.8		4.6	ns
t <sub>ZX1</sub>	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = 5.0v, CL = 35 pF <sup>[6]</sup>		2.8		3.1		3.8		4.6	ns
t <sub>ZX3</sub>	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = 5.0v, CL = 35 pF <sup>[6]</sup>		6.5		6.8		7.5		8.3	ns
t <sub>INREG</sub>	IOE Input Pad and Buffer to IOE Register Delay		5.0		5.7		7.0		9.0	ns
t <sub>IOFD</sub>	IOE Register Feedback Delay		1.5		1.9		2.3		2.7	ns
t <sub>INCOMB</sub>	IOE Input Pad and Buffer to Interconnect Delay		1.5		1.9		2.3		2.7	ns

10KA tbl 06A

**External Timing Parameters<sup>[4]</sup>**

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>DRR</sub>	Register to Register Delay via Four LEs, Three Row Interconnects, and Four Local Interconnects		11.2		14.0		17.2		21.1	ns
t <sub>INSU</sub>	Setup Time with Global Clock at IOE Register	5.5		4.2		5.2		6.9		ns
t <sub>INH</sub>	Hold time with Global Clock at IOE Register	0.0		0.0		0.0		0.0		ns
t <sub>OUTCO</sub>	Output Data Hold Time After Clock	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

10KA tbl 07A

## AC Electrical Specifications cont.

### Logic Element Timing Parameters<sup>[5]</sup>

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{LUT}$	Look-up Table Delay for Data-in		0.9		1.0		1.3		1.6	ns
$t_{CLUT}$	Look-up Table Delay for Carry-in		0.1		0.5		0.6		0.6	ns
$t_{RLUT}$	Look-up Table Delay for LE Register Feedback		0.5		0.8		0.9		1.0	ns
$t_{PACKED}$	Data-in to Packed Register Delay		0.4		0.4		0.5		0.7	ns
$t_{EN}$	LE Register Enable Delay		0.7		0.9		1.1		1.4	ns
$t_{CICO}$	Carry-in to Carry-out Delay		0.2		0.2		0.2		0.3	ns
$t_{CGEN}$	Data-in to Carry-out Delay		0.8		0.7		0.8		1.2	ns
$t_{CGENR}$	LE Register Feedback to Carry-out Delay		0.4		0.3		0.3		0.4	ns
$t_{CASC}$	Cascade Chain Routing Delay		0.7		0.7		0.8		0.9	ns
$t_C$	LE Register Control Signal Delay		0.3		1.0		1.3		1.5	ns
$t_{CO}$	LE Register Clock-to-output Delay		0.5		0.7		0.9		1.0	ns
$t_{COMB}$	Combinatorial Delay		0.4		0.4		0.5		0.6	ns
$t_{SU}$	LE Register Setup Time Before Clock	0.8		1.6		2.2		2.5		ns
$t_H$	LE Register Hold Time After Clock	0.5		0.8		1.0		1.4		ns
$t_{PRE}$	LE Register Preset Delay		0.8		0.4		0.5		0.5	ns
$t_{CLR}$	LE Register Clear Delay		0.8		0.4		0.5		0.5	ns
$t_{CH}$	Clock High Time	2.0		4.0		4.0		4.0		ns
$t_{CL}$	Clock Low Time	2.0		4.0		4.0		4.0		ns

10KA tbl 08A

**AC Electrical Specifications cont.**

**Interconnect Timing Parameters<sup>[5]</sup>**

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$	Delay from Dedicated Input Pin to IOE Control Input		4.7		6.0		7.1		8.2	ns
$t_{DIN2LE}$	Delay from Dedicated Input Pin to LE or EAB Control Input		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$	Delay from Dedicated Input or Clock Pin to LE or EAB Data		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$	Delay from Dedicated Clock Pin to IOE Clock		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$	Delay from Dedicated Clock Pin to LE or EAB Clock		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$	Delay from an LE to LE in Same LAB		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$	Delay for Driving a Row IOE, LE or EAB to a Row IOE, LE or EAB in the Same Row		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$	Delay from an LE to IOE in the Same Column		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$	Delay for Driving a Column IOE, LE or EAB to an LE or EAB in a Different Row		5.8		6.2		6.6		7.0	ns
$t_{TROWROWS}$	Delay for Driving a Row IOE or EAB to an LE or EAB in a Different Row		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$	Delay from an LE to IOE Control Signal via the Peripheral Control Bus		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$	Delay from an LE Carry-out Signal to an LE Carry-in Signal in a Different LAB		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$	Delay from an LE Cascade-out Signal to an LE Cascade-in Signal in a Different LAB		0.0		1.3		1.6		2.0	ns

10KA tbl 09A

## AC Electrical Specifications cont.

EAB Timing Parameters<sup>[5]</sup>

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$	Delay from Data or Address to EAB for Combinatorial Input		1.7		2.8		3.4		4.6	ns
$t_{EABDATA2}$	Delay from Data or Address to EAB for Registered Input		4.9		3.9		4.8		5.9	ns
$t_{EABWE1}$	WE Delay to EAB for Combinatorial Input		0.0		2.5		3.0		3.7	ns
$t_{EABWE2}$	WE Delay to EAB for Registered Input		4.0		4.1		5.0		6.2	ns
$t_{EABCLK}$	EAB Register Clock Delay		0.4		0.8		1.0		1.2	ns
$t_{EABCO}$	EAB Register Clock-to-output Delay		0.1		0.2		0.3		0.4	ns
$t_{EABBYPASS}$	Bypass Register Delay		0.9		1.1		1.3		1.6	ns
$t_{EABSU}$	EAB Register Setup Time	0.8		1.5		1.8		2.2		ns
$t_{EABH}$	EAB Register Hold Time	0.8		1.6		2.0		2.5		ns
$t_{AA}$	Address Access Delay		5.5		8.2		10.0		12.4	ns
$t_{WP}$	Write Pulse Width	6		4.9		6.0		7.4		ns
$t_{WDSU}$	Data Setup Time Before Falling Edge of Write Pulse	0.1		0.8		1.0		1.2		ns
$t_{WDH}$	Data Hold Time After Falling Edge of Write Pulse	0.1		0.2		0.3		0.4		ns
$t_{WASU}$	Address Setup Time Before Rising Edge of Write Pulse	0.1		0.4		0.5		0.6		ns
$t_{WAH}$	Address Hold After Falling Edge of Write Pulse	0.1		0.8		1.0		1.2		ns
$t_{WO}$	Write Enable to Date Output Delay		2.8		4.3		5.3		6.5	ns
$t_{DD}$	Data-in to Date-out Delay		2.8		4.3		5.3		6.5	ns
$t_{EABOUT}$	Data-out Delay		0.5		0.4		0.5		0.6	ns
$t_{EABCH}$	Clock High Time	2.0		4.0		4.0		4.0		ns
$t_{EABCL}$	Clock Low Time	6.0		4.9		6.0		7.4		ns

10KA tbl 10A

**AC Electrical Specifications cont.**

**EAB Timing Parameters<sup>[5]</sup>**

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>EABAA</sub>	EAB Address Access Delay		9.5		13.6		16.5		20.8	ns
t <sub>EABRCCOMB</sub>	EAB Asynchronous Read Cycle Time	9.5		13.6		16.5		20.8		ns
t <sub>EABRCREG</sub>	EAB Synchronous Read Cycle Time	6.1		8.8		10.8		13.4		ns
t <sub>EABWP</sub>	EAB Write Pulse Width	6		4.9		6.0		7.4		ns
t <sub>EABWCCOMB</sub>	EAB Asynchronous Write Cycle Time	6.2		6.1		7.5		9.2		ns
t <sub>EABWCREG</sub>	EAB Synchronous Write Cycle Time	12		11.6		14.2		17.4		ns
t <sub>EABDD</sub>	EAB Data-in to Data-out Delay		6.8		9.7		11.8		14.9	ns
t <sub>EABDATACO</sub>	EAB Clock-to-output Delay Using Output Registers		1.0		1.4		1.8		2.2	ns
t <sub>EABDATASU</sub>	EAB Data/Address Setup Time Using Input Register	5.3		4.6		5.6		6.9		ns
t <sub>EABDATAH</sub>	EAB Data/Address Hold Time Using Input Register	0		0		0.0		0.0		ns
t <sub>EABWESU</sub>	EAB WE Setup When Using Input Register	4.4		4.8		5.8		7.2		ns
t <sub>EABWESH</sub>	EAB WE Hold Time When Using Input Register	0		0		0.0		0.0		ns
t <sub>EABWDSU</sub>	EAB Data Setup Time to Falling Edge of Write Pulse When Not Using Input Registers	1.8		1.1		1.4		2.1		ns
t <sub>EABWDH</sub>	EAB Data Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0		0		0.0		0.0		ns
t <sub>EABWASU</sub>	EAB Address Setup Time to Rising Edge of Write Pulse When Not Using Input Registers	4.5		4.6		5.6		7.4		ns
t <sub>EABWAH</sub>	EAB Address Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0		0		0.0		0.0		ns
t <sub>EABWO</sub>	EAB WE to Data Output Delay		5.1		9.4		11.4		14.0	ns

10KA tbl 11A

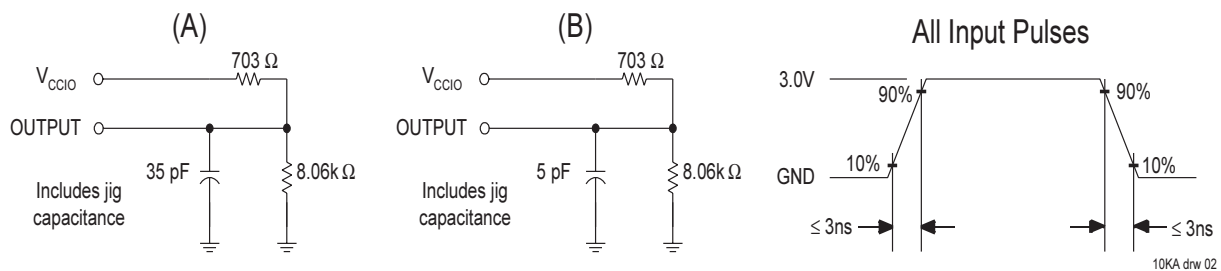
**AC Electrical Specifications cont.**

**External Bi-Directional Timing Parameters<sup>[5]</sup>**

Symbol	Parameter	Speed: -1		Speed: -2		Speed: -3		Speed: -4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	Setup for Bi-directional Pins with Global Clock at Adjacent LE Registers	2.0		2.8		3.5		4.1		ns
$t_{\text{INHIBIDIR}}$	Hold Time for Bi-directional Pins with Global Clock at Adjacent LE Registers	0.0		0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$	Clock-to-output Delay for Bi-directional Pins with Global Clock at IOE Register	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
$t_{\text{XZBIDIR}}$	Synchronous IOE Output Buffer Disable Delay		8.0		9.8		11.8		14.3	ns
$t_{\text{ZXBIDIR}}$	Synchronous IOE Output Buffer Disable Delay, Slow Slew Rate = off		8.0		9.8		11.8		14.3	ns

10KA tbl 12A

**AC Test Conditions**



A: Test fixture set-up A is for general testing.  
 B: Test fixture set-up B is for high Z testing (t<sub>ZX#</sub>).

**Notes to Tables**

1. During transitions, inputs may undershoot to -2.0V or overshoot to 5.75V for periods shorter than 20ns. Otherwise, minimum DC input voltage is -0.5V.
2. Device inputs may be driven before V<sub>CCINT</sub> and V<sub>CCIO</sub> are powered.
3. Typical values are at V<sub>CC</sub> of 3.3 volts and ambient temperature of 25 °C.
4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.
5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.
6. Use AC Test Conditions set-up B for these parameters.

**Revision History**

- 29 Feb. 2000: Created new document
- 01 Dec. 2000: Updated package availability and additional literature available

**Ordering Information**

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL10K50VQC240-3	Commercial	240-pin Plastic QFP	-3	EPF10K50VQC240-3
CL10K50VQC240-2			-2	EPF10K50VQC240-2
CL10K50VQC240-1			-1	EPF10K50VQC240-1
CL10K50VQI240-2	Industrial		-2	EPF10K50VQI240-2
CL10K50VRC240-4	Commercial	240-pin Power QFP	-4	EPF10K50VRC240-4
CL10K50VRC240-3			-3	EPF10K50VRC240-3
CL10K50VRC240-2			-2	EPF10K50VRC240-2
CL10K50VRC240-1			-1	EPF10K50VRC240-1
CL10K50VRI240-4	Industrial		-4	EPF10K50VRI240-4
CL10K50VRI240-3		-3	EPF10K50VRI240-3	
CL10K50VBC356-4	Commercial	356-pin SBGA	-4	EPF10K50VBC356-4
CL10K50VBC356-3			-3	EPF10K50VBC356-3
CL10K50VBC356-2			-2	EPF10K50VBC356-2
CL10K50VBC356-1			-1	EPF10K50VBC356-1
CL10K50VBI356-4	Industrial		-4	EPF10K50VBI356-4
CL10K50VBI356-3		-3	EPF10K50VBI356-3	

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