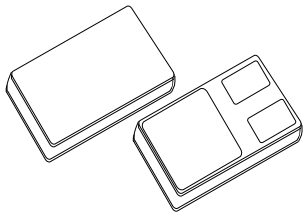
STRH8N10

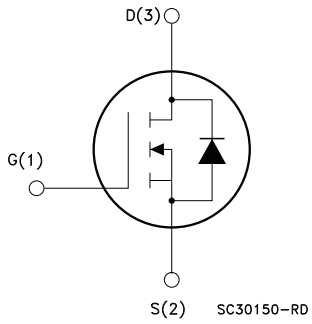
Rad-Hard 100 V, 6 A N-channel Power MOSFET

Datasheet - production data



SMD0.5

Figure 1. Internal schematic diagram



Features

V_{DSS}	I_D	$R_{DS(on)}$	Q_g
100 V	6 A	0.30 Ω	22 nC

- Fast switching
- 100% avalanche tested
- Hermetic package
- 70 krad TID
- SEE radiation hardened

Applications

- Satellite
- High reliability

Description

This N-channel Power MOSFET is developed with STMicroelectronics unique STripFET™ process. It has specifically been designed to sustain high TID and provide immunity to heavy ion effects. This Power MOSFET is fully ESCC qualified.

Table 1. Device summary

Order codes	ESCC part number	Quality level	Package	Lead finish	Mass (g)	Temp. range	EPPL
STRH8N10S1	-	Engineering model	SMD0.5	Gold	1.2	-55 to 150°C	-
STRH8N10SG	5205/023/01	ESCC flight					Target

Contents

1 Electrical ratings

(T_C = 25°C unless otherwise specified)

Table 2. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V_{DS} (1)	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS} (2)	Gate-source voltage	±20	V
I_D (3)	Drain current (continuous) at T_C= 25°C	6	A
I_D (1)	Drain current (continuous) at T_C= 100°C	4.1	A
I_{DM} (4)	Drain current (pulsed)	24	A
P_{TOT} (1)	Total dissipation at T_C= 25°C	62.5	W
P_{TOT}	Total dissipation at T_a= 25°C	2.4	W
dv/dt (5)	Peak diode recovery voltage slope	6.4	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. This rating is guaranteed @ T_J > 25 °C (see *Figure 10: Normalized $V_{DSS(BR)DSS}$ vs temperature*).
2. This value is guaranteed over the full range of temperature.
3. Rated according to the $R_{thj\text{-}case}$ + $R_{thc\text{-}s}$.
4. Pulse width limited by safe operating area.
5. I_{SD} ≤ 6 A, di/dt ≤ 1060 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	52	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	4	A
E_{AS}(1)	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	457	mJ
E_{AS}	Single pulse avalanche energy (starting Tj=110°C, Id=Iar, Vdd=50V)	134	mJ
E_{AR}	Repetitive avalanche (Vdd = 50 V, I_{AR} = 4 A, f = 100 kHz, T_J = 25 °C, duty cycle = 10%)	4.3	mJ
E_{AR}	Repetitive avalanche (Vdd = 50 V, I_{AR} = 4 A, f = 100 kHz, T_J = 110 °C, duty cycle = 10%)	1.4	mJ

1. Maximum rating value.

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified).

2.1 Pre-irradiation

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	100% BV_{Dss}			1	mA
		80% BV_{Dss} 80% BV_{Dss}, T_C = 125 °C			10 100	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V V_{GS} = -20 V V_{GS} = 20 V, T_C = 125 °C V_{GS} = -20 V, T_C = 125 °C	 -100 -200		100 200 	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} =V_{GS}, I_D = 1mA V_{DS} =V_{GS}, I_D = 1mA , T_C = 125 °C V_{DS} =V_{GS}, I_D = 1mA , T_C = -55 °C	2 1.5 2.1		4.5 3.7 5.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12 V, I_D = 4 A V_{GS} = 12 V, I_D = 4 A, T_C = 125 °C			0.30 0.72	W

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} (1) C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0V	527 76 31	659 95 39	791 114 47	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance (2)	V_{DD} = 80 V, V_{GS}=0V		162		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-to-source charge Gate-to-drain (“Miller”) charge	V_{DD} = 50 V, I_D = 4 A, V_{GS}= 12 V	15 2.5 3.5	18.5 3.5 5	22 4.5 6	nC nC nC
R_G (3)	Gate input resistance	f=1MHz gate DC bias=0 test signal level=20mV open drain		1.6		W

1. This value is guaranteed over the full range of temperature.
2. This value is defined as the ratio between the Q_{oss} and the voltage value applied.
3. Not tested, guaranteed by process.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 12 V	5	7.5	10	ns
t_r	Rise time		2	5.5	9	ns
$t_{d(off)}$	Turn-off-delay time		13	21.5	30	ns
t_f	Fall time		2.5	5	7.5	ns

Table 8. Source drain diode(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				6	A
I_{SDM} (2)	Source-drain current (pulsed)				24	A
V_{SD} (3)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0			1.5	V
		I_{SD} = 8 A, V_{GS} = 0, T_C = 125 °C			1.275	
t_{rr}(4)	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 17 V, Tj = 25 °C	196	245	294	ns
Q_{rr}(4)	Reverse recovery charge			1.2		µC
I_{RRM}(4)	Reverse recovery current			10		A
t_{rr}(4)	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD}= 17 V, Tj = 150 °C	282	352	422	ns
Q_{rr}(4)	Reverse recovery charge			1.7		µC
I_{RRM}(4)	Reverse recovery current			10.5		A

1. Refer to the *Figure 16: Source drain diode*.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300 µs, duty cycle 1.5%
4. Not tested in production, guaranteed by process.

3 Radiation characteristics

The technology of the STMicroelectronics rad-hard Power MOSFETs is extremely resistant to radiative environments. Every manufacturing lot is tested, using the SMD0.5 package, in total ionizing dose (irradiation done according to the ESCC 22900 specification, window 1) and Single Event Effect according to the MIL-STD-750E TM1080 up to a fluence level of 3e+5 ions/cm². Both pre-irradiation and post-irradiation performances are tested and specified using the same circuitry and test conditions in order to provide a direct comparison.

(T_{amb}= 22 ± 3 °C unless otherwise specified).

Total dose radiation (TID) testing

One bias conditions using the SMD0.5 package:

– V_{GS} bias: + 15 V applied and V_{DS}= 0 V during irradiation

The following parameters are measured (see *Table 9*, *Table 10* and *Table 11*):

– before irradiation
– after irradiation
– after 24 hrs @ room temperature
– after 168 hrs @ 100 °C anneal

Table 9. Post-irradiation on/off states @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}	+1	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V V_{GS} = -20 V	1.5 -1.5	nA
BV_{DSS}	Drain-to-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	-25%	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	-60% / + 30%	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V; I_D = 4 A	±10%	W

Table 10. Dynamic post-irradiation @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
Q_g	Total gate charge	I_G = 0.2 mA, V_{GS} = 12 V, V_{DS} = 50 V, I_{DS} = 4 A	-5% / + 40%	nC
Q_{gs}	Gate-source charge		±35%	
Q_{gd}	Gate-drain charge		-5% / + 130%	

Table 11. Source drain diode post-irradiation @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))(1)

Symbol	Parameter	Test conditions	Drift values Δ.	Unit
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	±2%	V

1. Refer to *Figure 16*.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Single event effect, SOA

The technology of the STMicroelectronics rad-hard Power MOSFETs is extremely resistant to heavy ion environment for single event effect according to MIL-STD-750E method 1080 (bias circuit in *Figure 3: Single event effect, bias circuit*) SEB and SEGR tests have been performed with a fluence of 3e+5 ions/cm².

The accept/reject criteria are:

– SEB test: drain voltage checked, trigger level is set to V_{ds} = - 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².

– SEGR test: the gate current is monitored every 100 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

The results are:

– SEB immune at 60 MeV/mg/cm2

– SEGR immune at 60 MeV/mg/cm2 within the safe operating area (SOA) given in *Table 12: Single event effect (SEE), safe operating area (SOA)* and *Figure 2: Single event effect, SOA*)

Table 12. Single event effect (SEE), safe operating area (SOA)

Ion	Let (Mev/(mg/cm^2))	Energy (MeV)	Range (µm)	V_{DS} (V)				
				@V_{GS}=0	@V_{GS}= -2 V	@V_{GS}= -5 V	@V_{GS}= -10 V	@V_{GS}= -20 V
Kr	32	768	94	100	80	60	30	10
Xe	60	1217	89	40	30	30	-	0

Figure 2. Single event effect, SOA

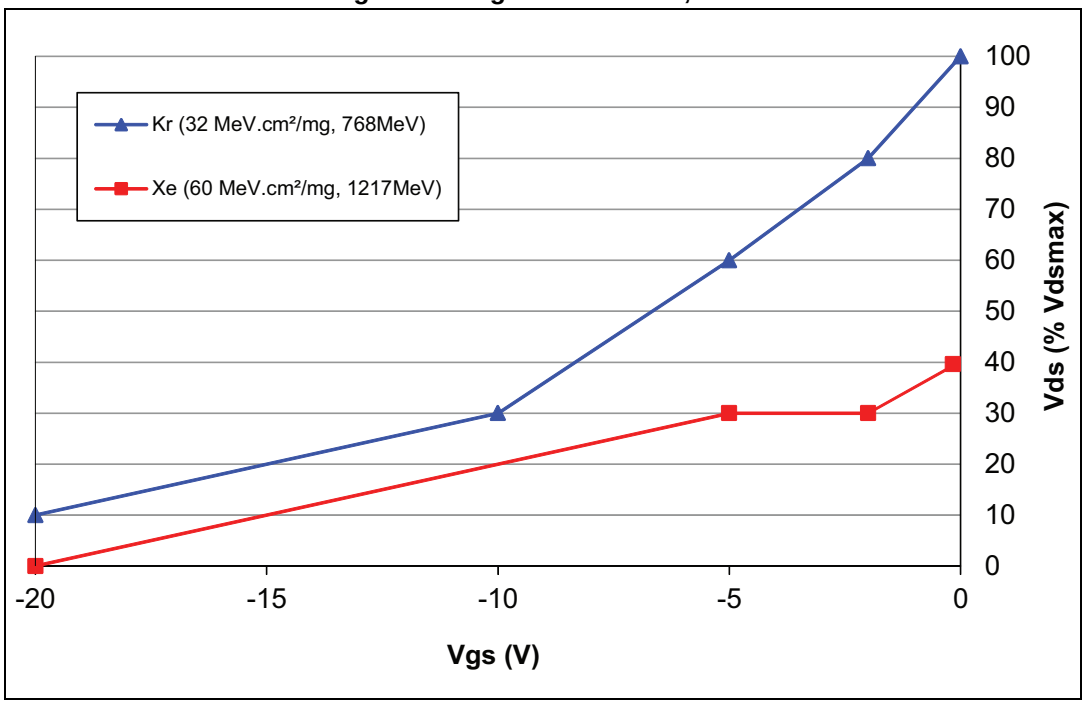
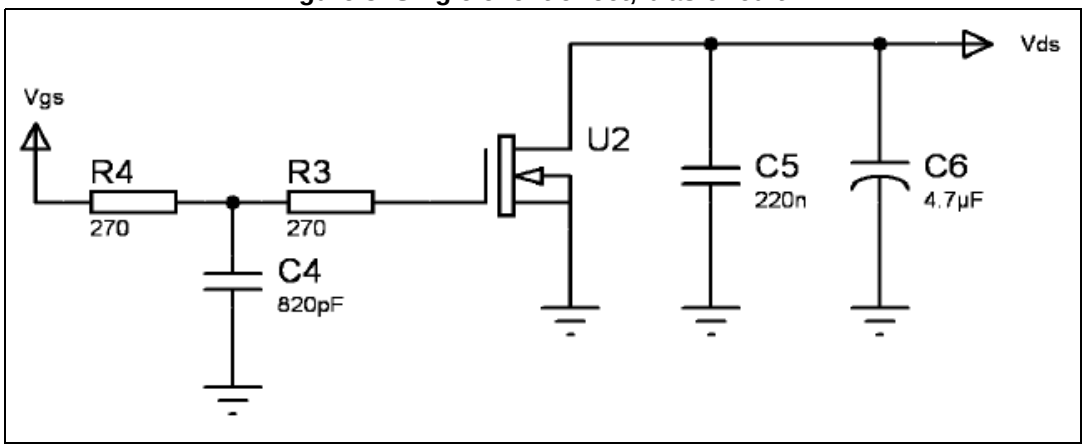


Figure 3. Single event effect, bias circuit(a)



a. Bias condition during radiation refer to *Table 12: Single event effect (SEE), safe operating area (SOA)* .

4 Electrical characteristics (curves)

Figure 4. Safe operating area

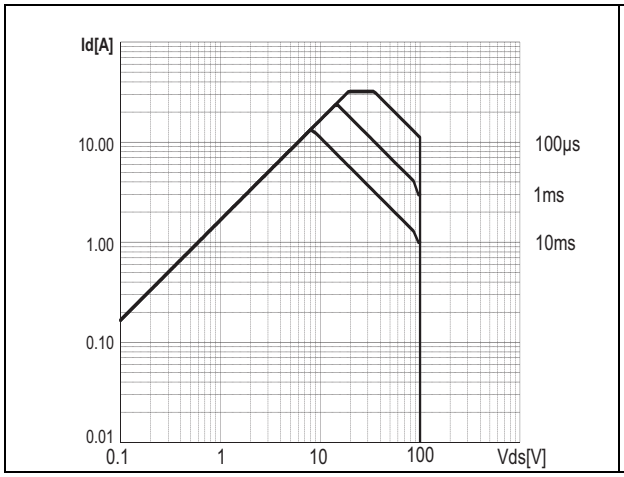


Figure 5. Thermal impedance

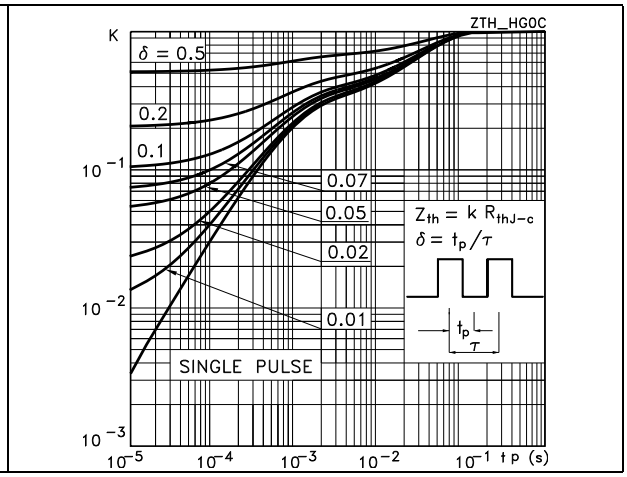


Figure 6. Output characteristics

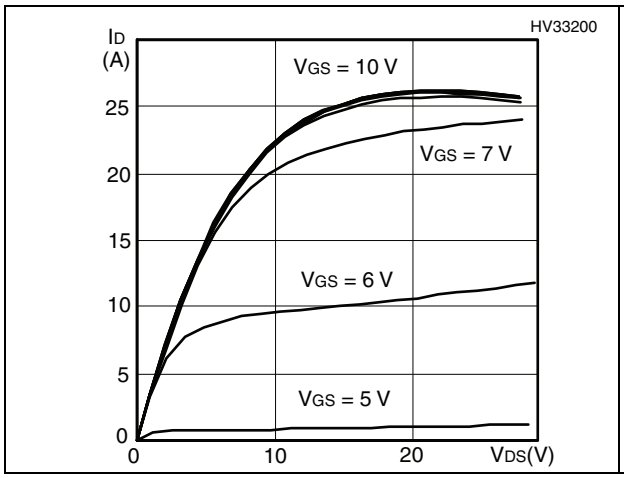


Figure 7. Transfer characteristics

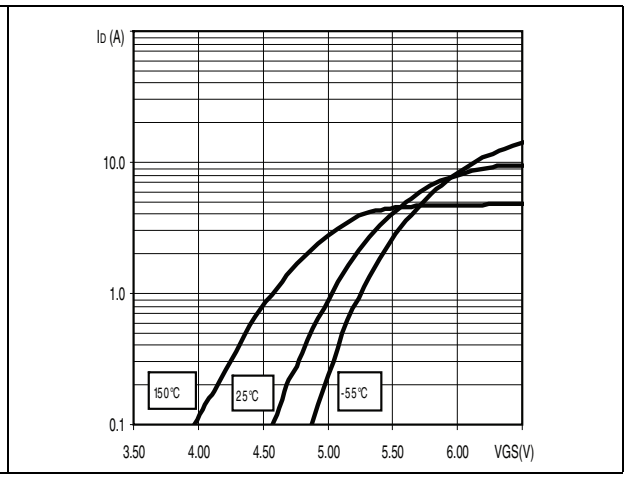


Figure 8. Gate charge vs gate-source voltage

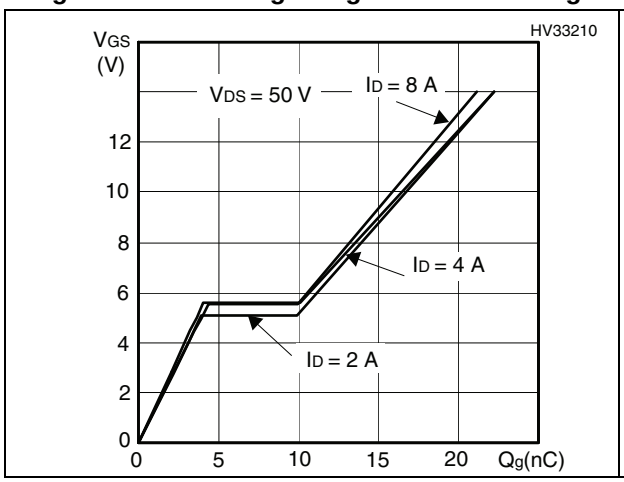


Figure 9. Capacitance variations

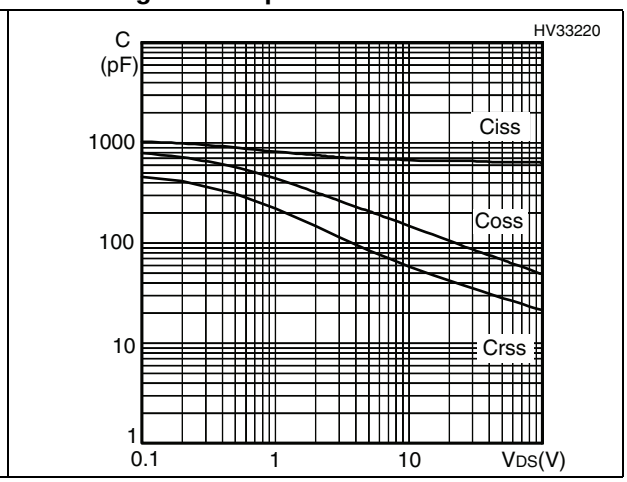


Figure 10. Normalized $V_{DSS(BR)DSS}$ vs temperature

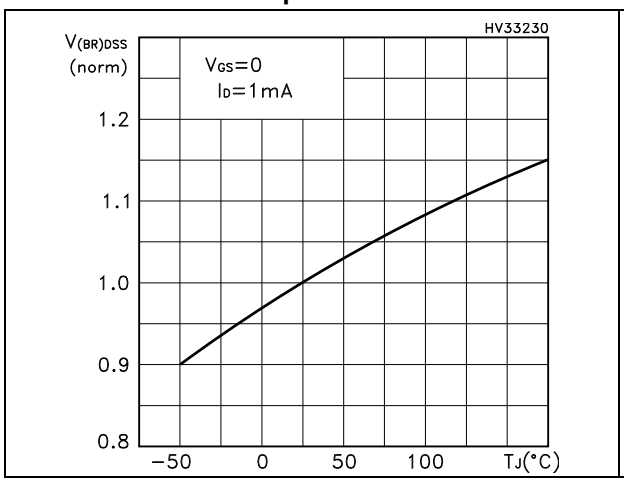


Figure 11. Static drain-source on-resistance

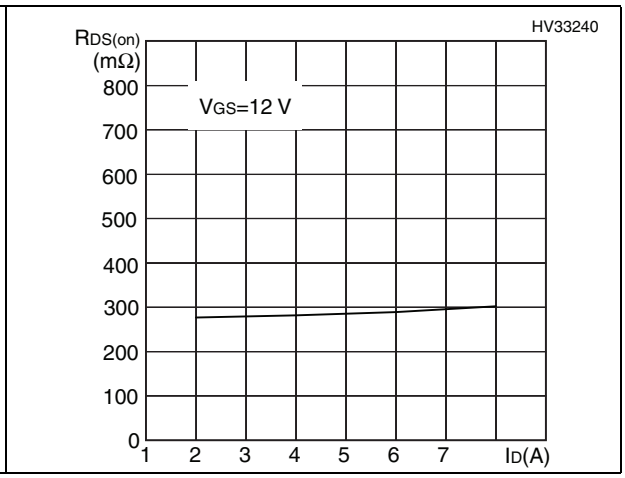


Figure 12. Normalized gate threshold voltage vs temperature

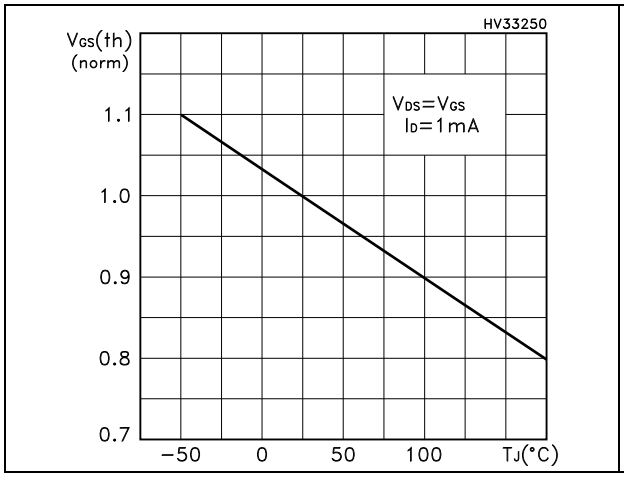


Figure 13. Normalized on-resistance vs temperature

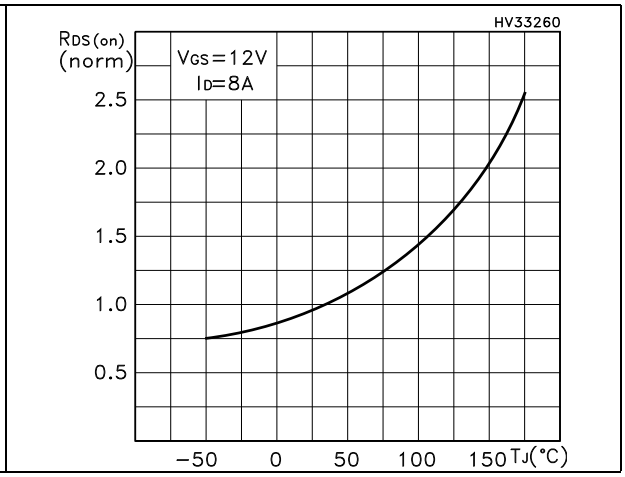
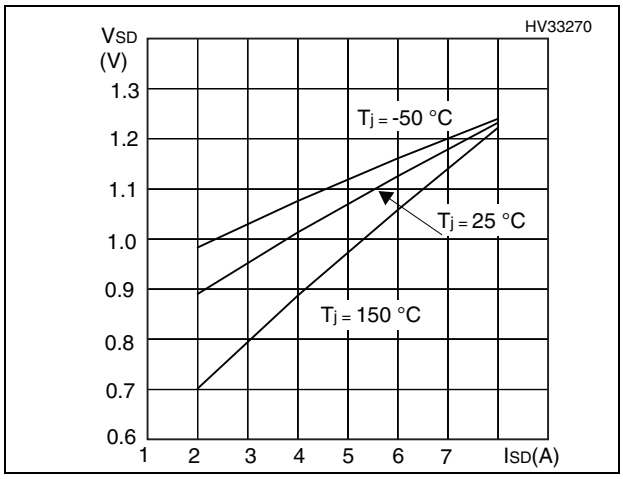
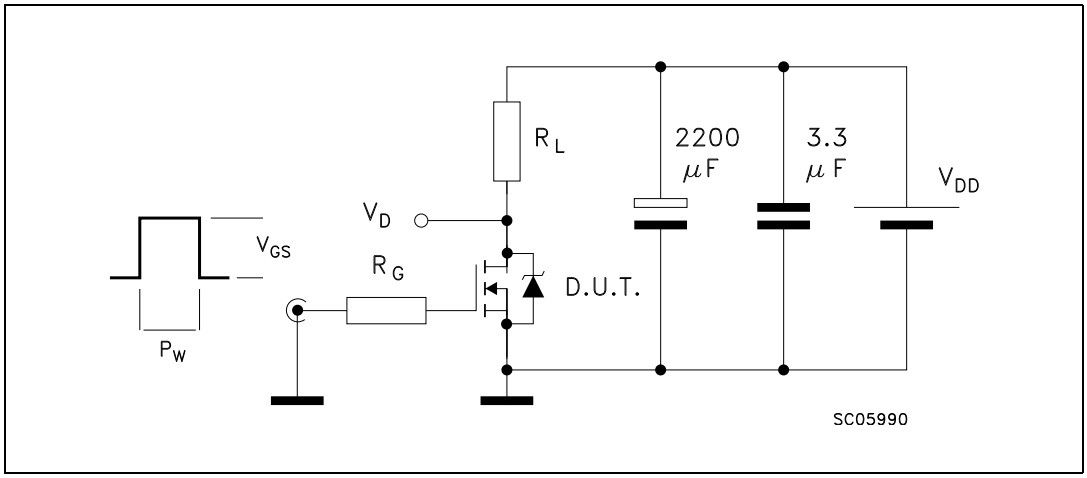


Figure 14. Source drain-diode forward characteristics



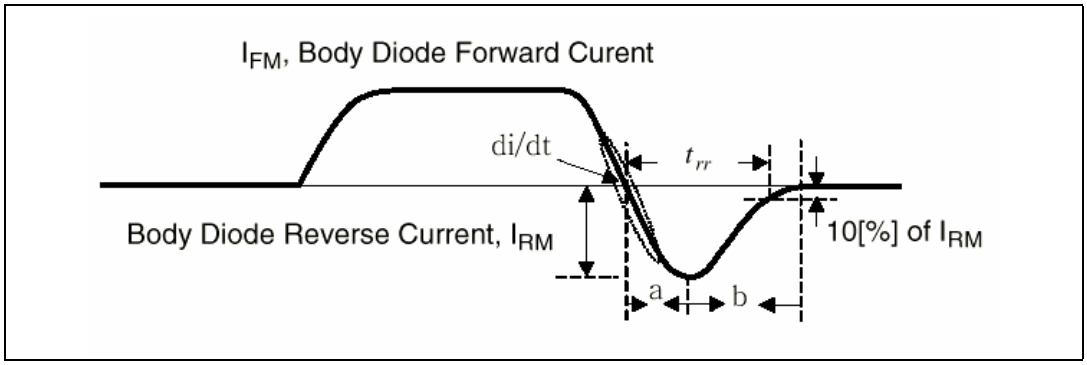
5 Test circuit

Figure 15. Switching times test circuit for resistive load (1)



1. Max driver V_{GS} slope = 1V/ns (no DUT)

Figure 16. Source drain diode



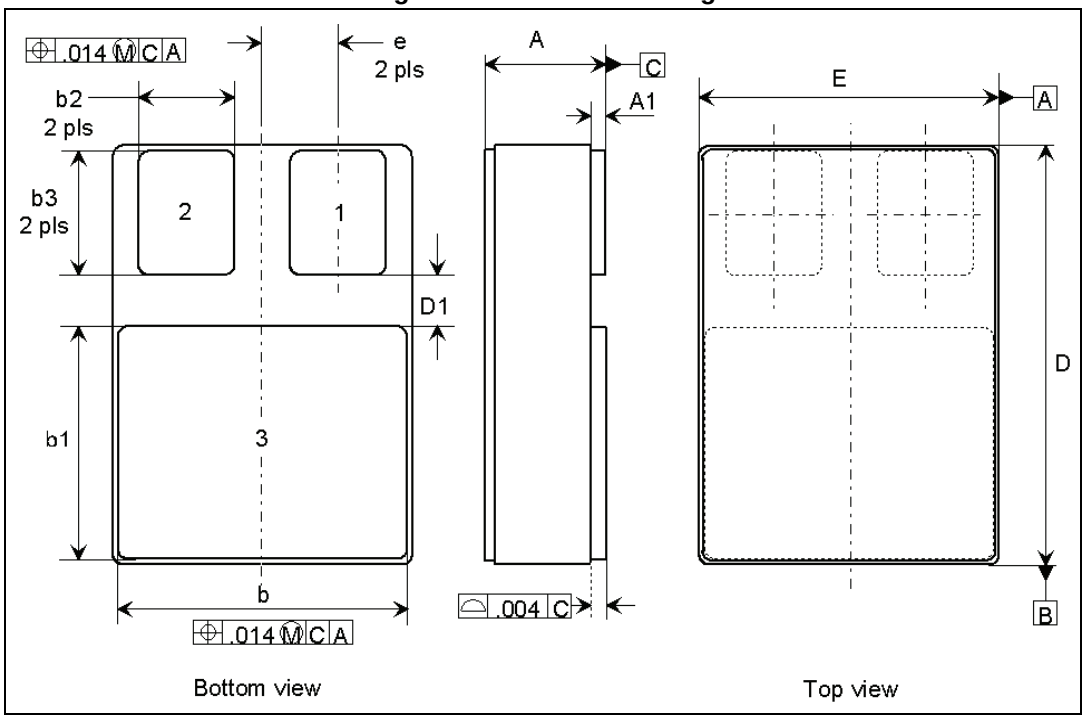
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 13. SMD0.5 mechanical data

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.84	3.00	3.15	0.112	0.118	0.124
A1	0.25	0.38	0.51	0.010	0.015	0.020
b	7.13	7.26	7.39	0.281	0.286	0.291
b1	5.58	5.72	5.84	0.220	0.225	0.230
b2	2.28	2.41	2.54	0.090	0.095	0.100
b3	2.92	3.05	3.18	0.115	0.120	0.125
D	10.03	10.16	10.28	0.935	0.400	0.405
D1	0.76			0.030		0.685
E	7.39	7.52	7.64	0.291	0.296	0.301
e		1.91			0.075	

Figure 17. SMD0.5 drawing



7 Order codes

Table 14. Ordering information

Order codes	ESCC part number	Quality level	EPPL	Package	Lead finish	Marking	Packing
STRH8N10S1	-	Engineering model	-	SMD0.5	Gold	STRH8N10S1	Strip pack
STRH8N10SG	5205/023/01	ESCC flight	Target			520502301F	

For specific marking only the complete structure is:

- ST Logo
- ESA Logo
- Date code (date of sealing of the package) : YYWWA
  - YY: year
  - WW: week number
  - A: week index
- ESCC part number (as mentioned in the table)
- Warning signs (e.g. BeO)
- Country of origin: FR (France)
- Part serial number within in the assembly lot

Contact ST sales office for information about the specific conditions for products in die form and for other packages.

7.1 Other information

Date code

The date code for “ESCC flight” is structured as follows: yywwz

where:

- yy: last two digits of year
- ww: week digits
- z: lot index in the week

Documentation

The table below provide a summary of the documentation provided with each type of products.

Table 15. Documentation provided for each type of product

Quality level	Radiation level	Documentation
Engineering model	-	-
ESCC flight	70 krad	Certificate of conformance
		Radiation verification test report

8 Revision history

Table 16. Document revision history

Date	Revision	Changes
20-May-2011	1	First release.
09-Nov-2011	2	Updated dynamic values on *Table 6: Dynamic*, *Table 7: Switching times*.
03-Jun-2013	3	Added new package and mechanical data: SMD0.5 Removed TO-39 package.
16-Dec-2013	4	Updated *Description* Minor text changes
09-Apr-2014	5	Document status promoted from preliminary data to production data Modified: *Figure 2*. Minor text changes.
26-May-2014	6	Updated *Figure 1*.

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