64Kx16 CMOS, High Speed Programmable, Static RAM Module

The EDH816H64C is a 1024K-bit high speed CMOS Static RAM Module consisting of sixteen (16) 64Kx1 Static RAMs in leadless chip carriers surface-mounted onto a multilayered ceramic substrate. Four Chip Select lines are provided (one for each 64Kx4 array) allowing the user to configure the memory into a 64Kx16, 128Kx8 or 256Kx4 organizations.

The EDH816H64C is available with access times as fast as 35ns. The module is a high density, 40 pin sidebrazed DIP on 900 mil centers.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Dual ground pins are provided for maximum noise immunity.

Fully asynchronous circuitry requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which are compliant to MIL-STD-883, paragraph 1.2.1.

Features

High Density 1024K-bit CMOS Static Random Access Memory Module

- Access Times 35, 45, 55, and 70ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Customer Configured Memory, as 64Kx16, 128Kx8 or 256Kx4

40 Pin Dual-in-line Package, No. 31

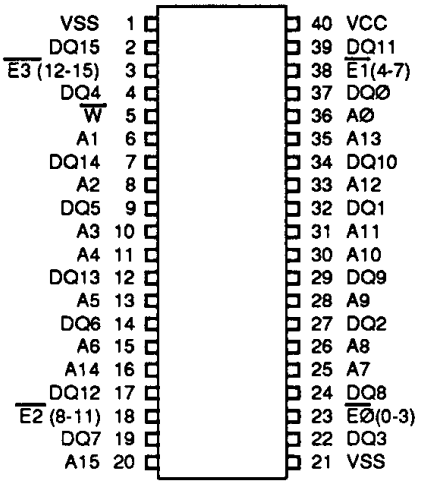
- Dual Ground Pins for Maximum Noise Immunity

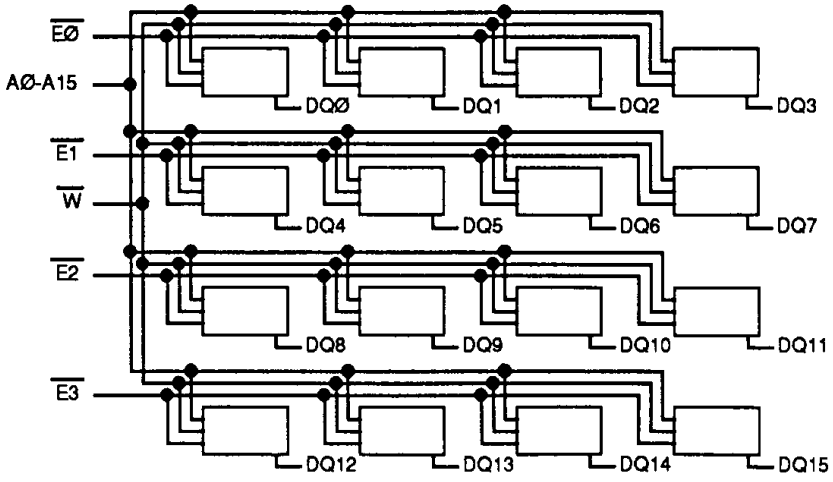
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
$\overline{E}$Ø-$\overline{E}$3	Chip Enables
$\overline{W}$	Write Enable
DQØ-DQ15	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to+70°C
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Storage Temperature, Ceramic ..... -65°C to +150°C
Power Dissipation ..... 8 Watts
Output Current ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Mode	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	x16	--	1120	1380	mA
			x8	--	690	830	
			x4	--	445	555	
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	200	475	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		--	40	250	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	50	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	50	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Input Capacitance (Address, $\overline{W}$)	CI	120	pF
Input Capacitance Enable Line ($\overline{E}$)	CE	40	pF
Output Capacitance	CO	12	pF

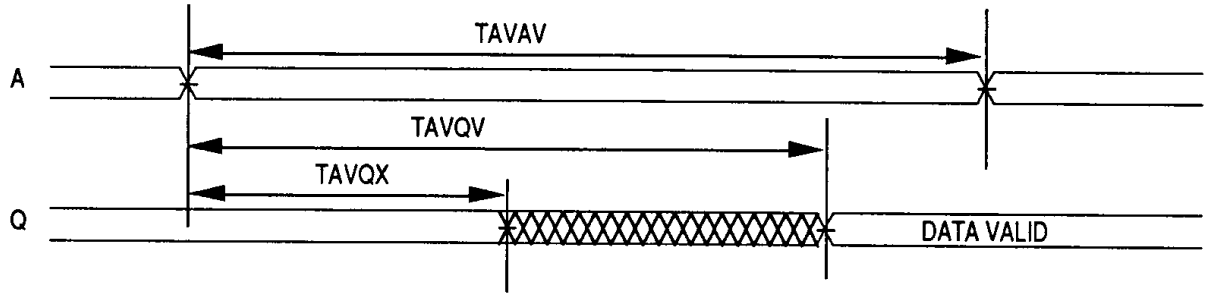
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

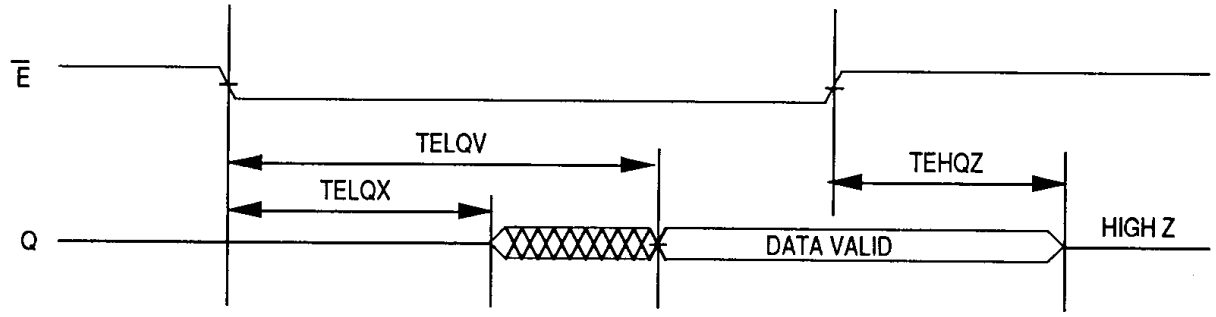
Parameter	Symbol	35ns		45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		70		ns
Address Access Time	TAVQV		35		45		55		70	ns
Chip Enable Access Time	TELQV		35		45		55		70	ns
Chip Enable to Output Low Z (1)	TELQX	10		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	25	0	30	0	30	0	30	ns
Output Hold from Address Change	TAVQX	5		5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		0		ns
Chip Disable to Power Down (1)	TPD	0	30	0	35	0	50	0	55	ns

Note 1: Parameter guaranteed, but not tested.

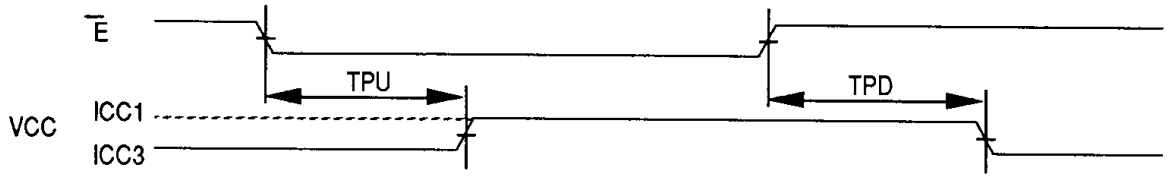
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



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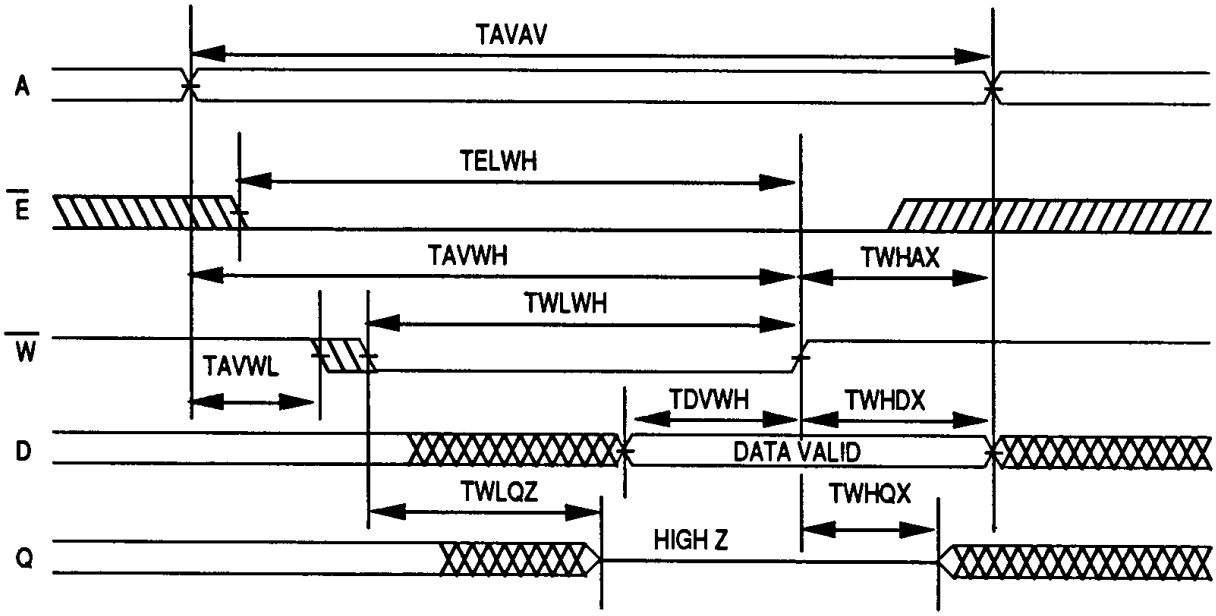
AC Characteristics
Write Cycle

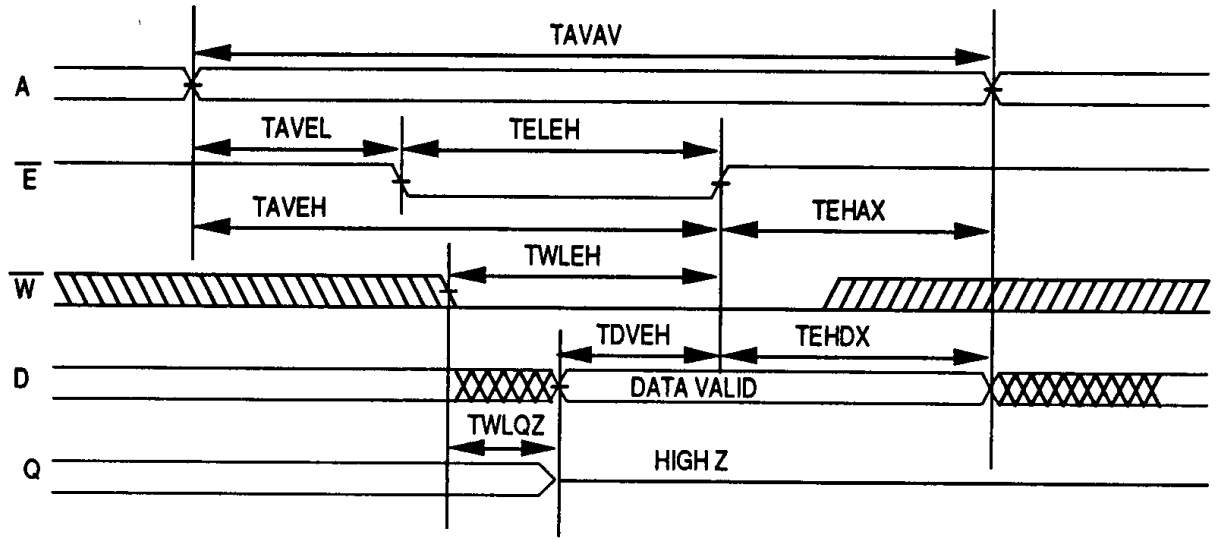
Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		70		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		65		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		65		ns
Address Setup Time	TAVWL	$\overline{W}$	10		10		10		10		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		40		50		65		ns
End of Write	TAVEH	$\overline{E}$	30		40		50		65		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		30		35		40		ns
	TELEH	$\overline{E}$	25		30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	30	0	30	0	35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		30		35		35		ns
	TDVEH	$\overline{E}$	25		30		35		35		ns
Output Active from End of Write (1)	TWHQX		0	20	0	25	0	30	0	40	ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



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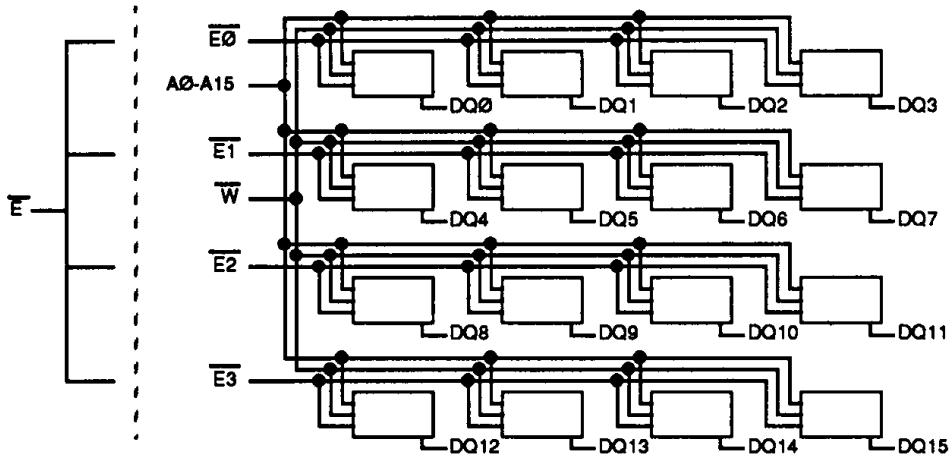
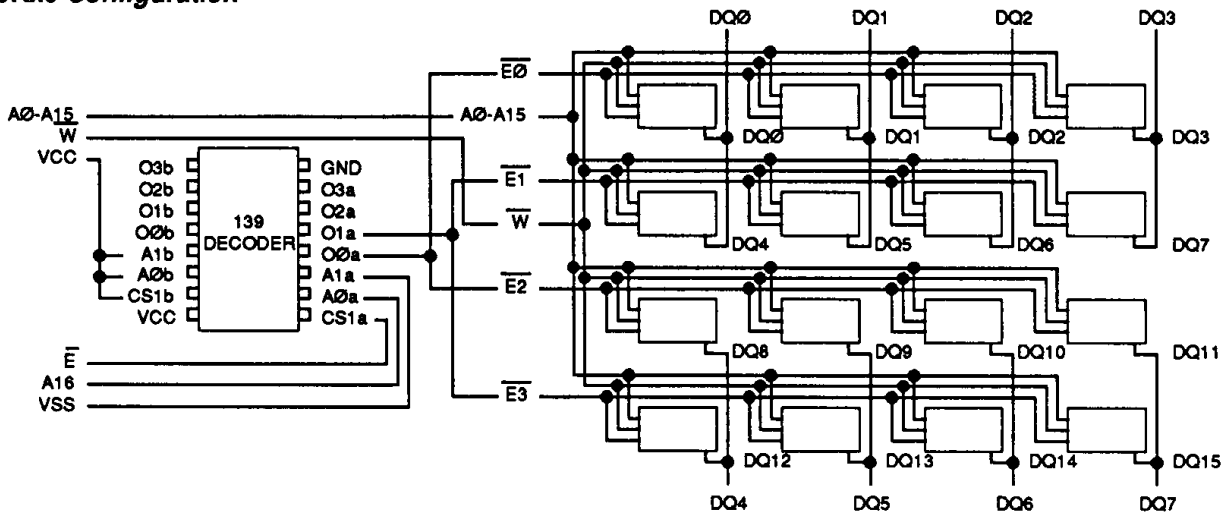
Device Configurations for 139 Decoder Applications

64Kx16 Configuration



128Kx8 Configuration



256Kx4 Configuration