To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

HAT3006R

Silicon N Channel / P Channel Power MOS FET
High Speed Power Switching

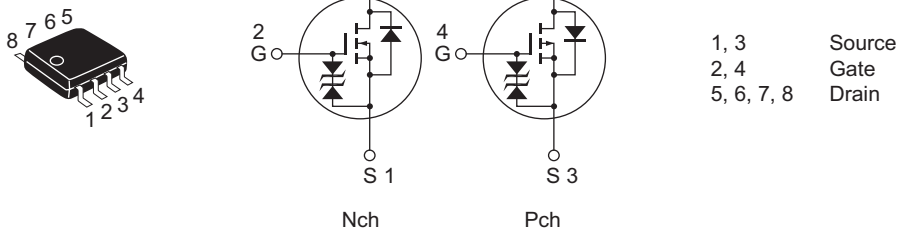
REJ03G1197-0800
(Previous: ADE-208-480F)
Rev.8.00
Sep 07, 2005

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	6.5	–4.5	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	52	–36	A
Body-drain diode reverse drain current	I_{DR}	6.5	–4.5	A
Channel dissipation	Pch Note 2	2		W
Channel dissipation	Pch Note 3	3		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s

Electrical Characteristics

N Channel

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS\ (on)}$	—	0.03	0.045	Ω	I_D = 4 A, V_{GS} = 10 V Note 4
	$R_{DS\ (on)}$	—	0.05	0.08	Ω	I_D = 4 A, V_{GS} = 4 V Note 4
Forward transfer admittance	$\|y_{fs}\|$	5	8	—	S	I_D = 4 A, V_{DS} = 10 V Note 4
Input capacitance	Ciss	—	560	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	380	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	170	—	pF	f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	30	—	ns	V_{GS} = 4 V, I_D = 4 A
Rise time	t_r	—	270	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d\ (off)}$	—	40	—	ns	
Fall time	t_f	—	65	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.9	1.4	V	I_F = 6.5 A, V_{GS} = 0 Note 4
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 6.5 A, V_{GS} = 0 di_F/dt = 20 A/µs

Note: 4. Pulse test

P Channel

(Ta = 25°C)

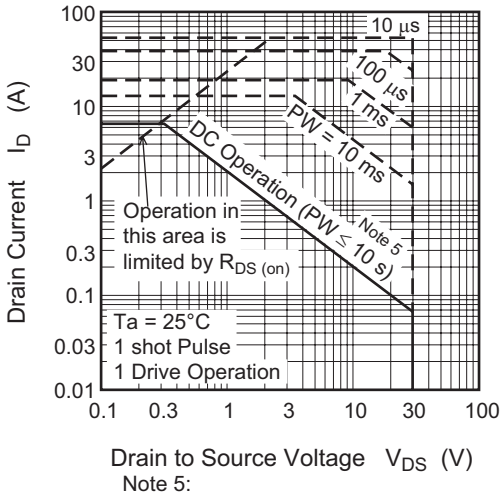
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS\ (on)}$	—	0.07	0.09	Ω	I_D = –3 A, V_{GS} = –10 V Note 5
	$R_{DS\ (on)}$	—	0.11	0.18	Ω	I_D = –3 A, V_{GS} = –4 V Note 5
Forward transfer admittance	$\|y_{fs}\|$	4	6	—	S	I_D = –3 A, V_{DS} = –10 V Note 5
Input capacitance	Ciss	—	660	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	440	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	140	—	pF	f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	24	—	ns	V_{GS} = –4 V, I_D = –3 A
Rise time	t_r	—	165	—	ns	V_{DD} ≅ –10 V
Turn-off delay time	$t_{d\ (off)}$	—	35	—	ns	
Fall time	t_f	—	70	—	ns	
Body-drain diode forward voltage	V_{DF}	—	–0.9	–1.4	V	I_F = –4.5 A, V_{GS} = 0 Note 5
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = –4.5 A, V_{GS} = 0 di_F/dt = 20 A/µs

Note: 5. Pulse test

Main Characteristics

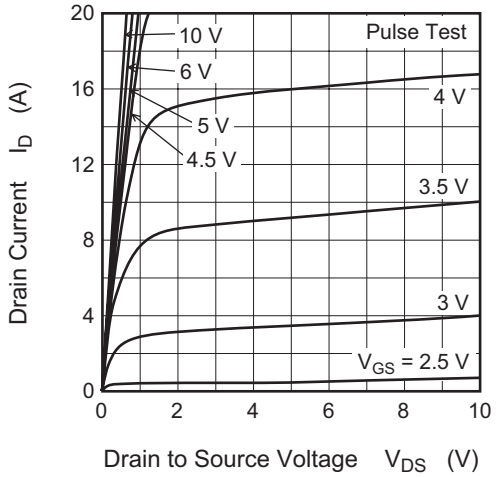
N Channel

Maximum Safe Operation Area

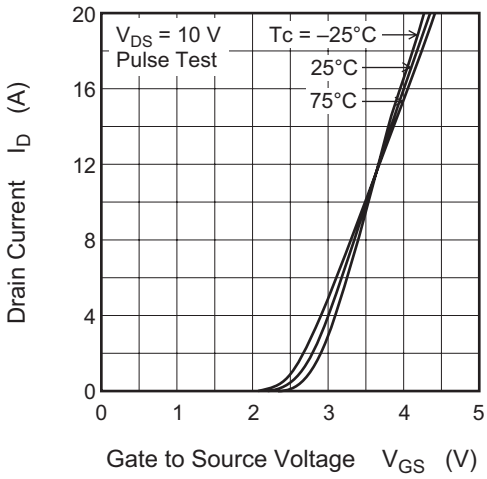


Note 5:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

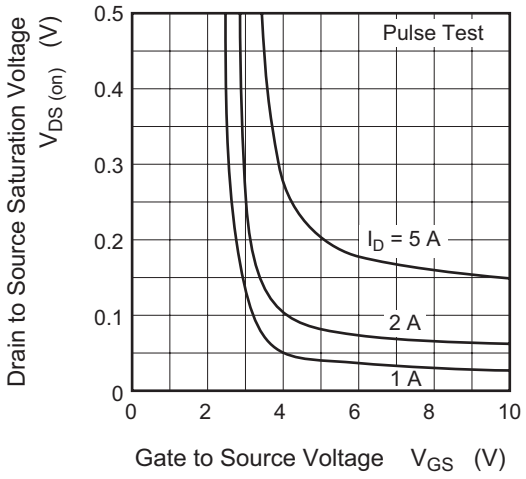
Typical Output Characteristics



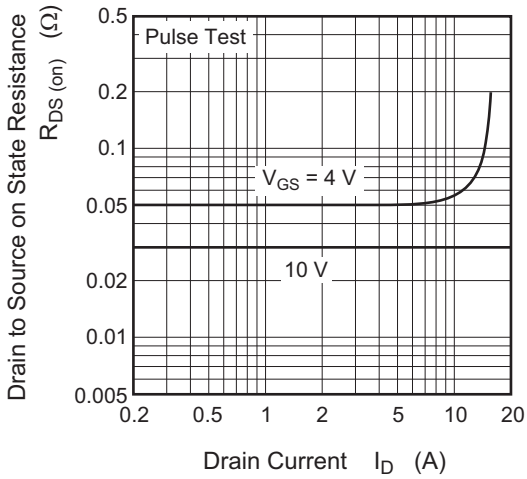
Typical Transfer Characteristics



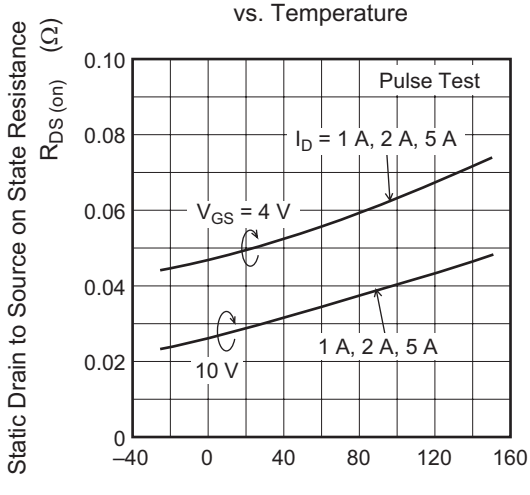
Drain to Source Saturation Voltage vs. Gate to Source Voltage



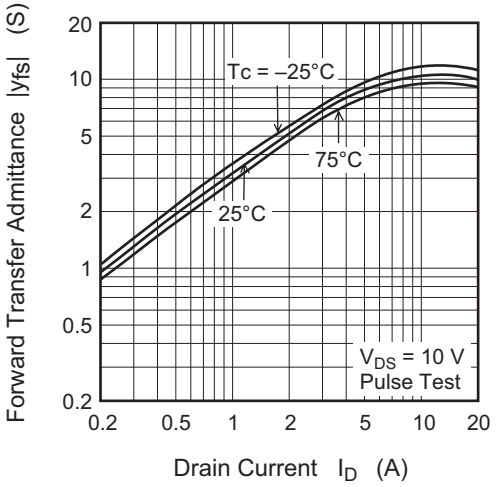
Static Drain to Source on State Resistance vs. Drain Current



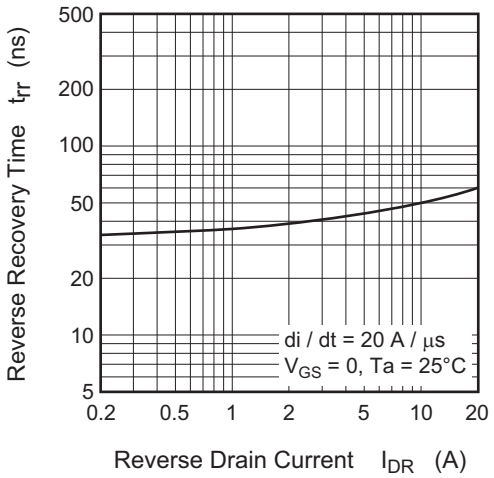
Static Drain to Source on State Resistance vs. Temperature



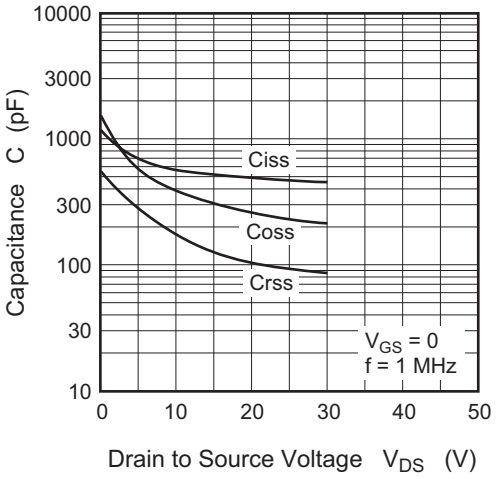
Forward Transfer Admittance vs. Drain Current



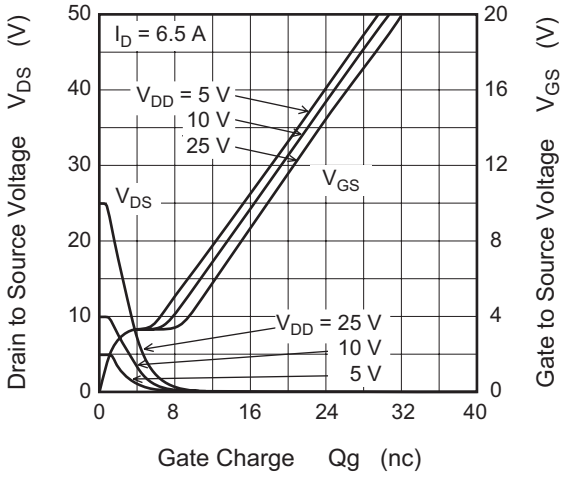
Body-Drain Diode Reverse Recovery Time



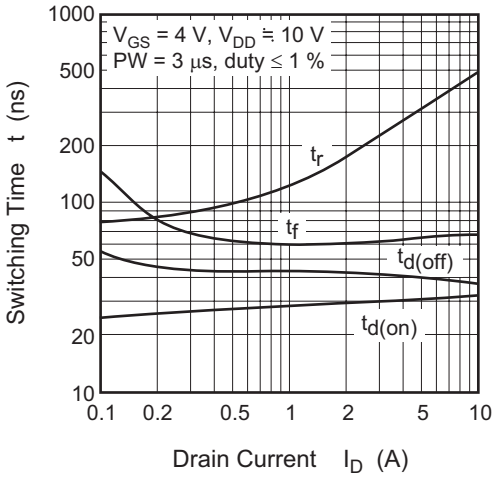
Typical Capacitance vs. Drain to Source Voltage



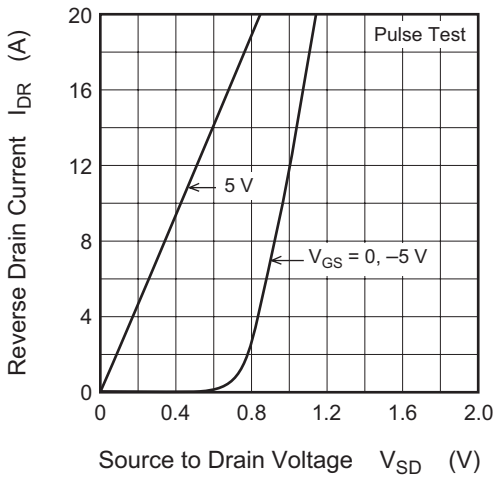
Dynamic Input Characteristics



Switching Characteristics

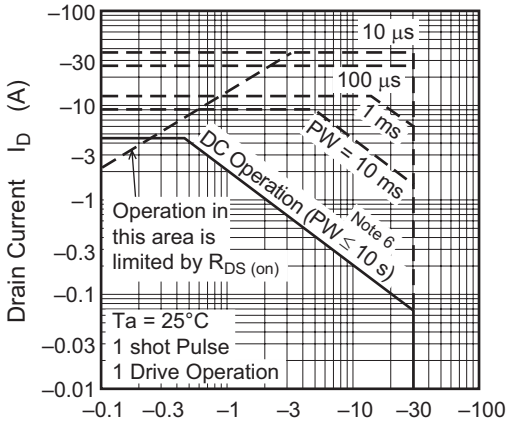


Reverse Drain Current vs. Source to Drain Voltage



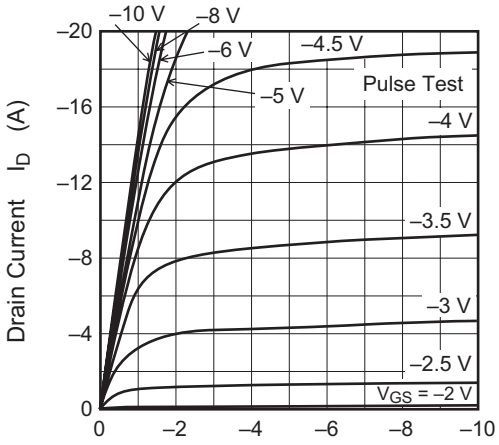
P Channel

Maximum Safe Operation Area

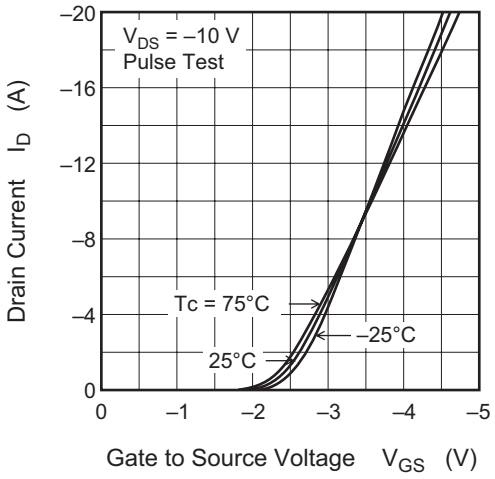


Note 6:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

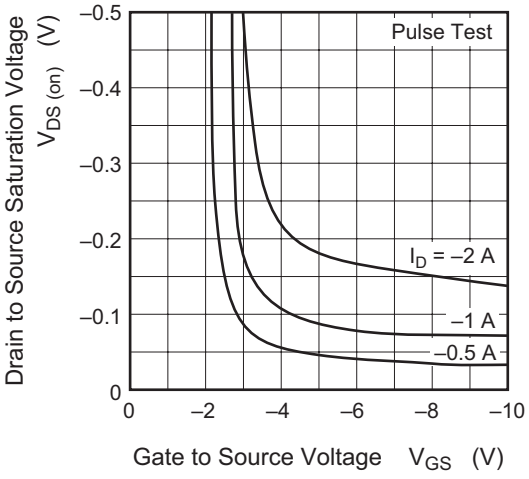
Typical Output Characteristics



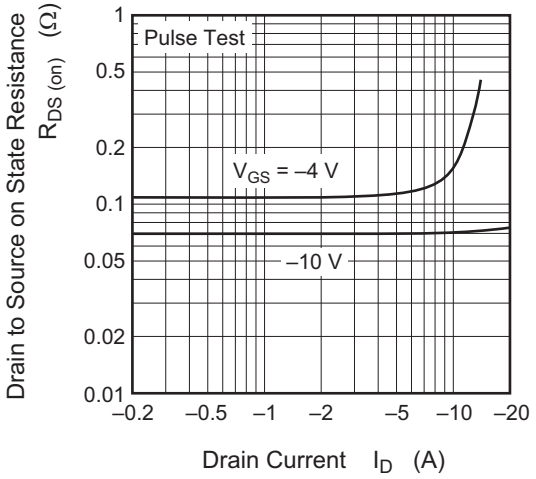
Typical Transfer Characteristics



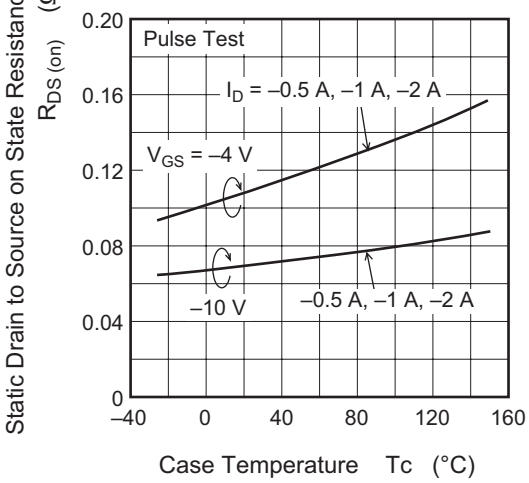
Drain to Source Saturation Voltage vs. Gate to Source Voltage



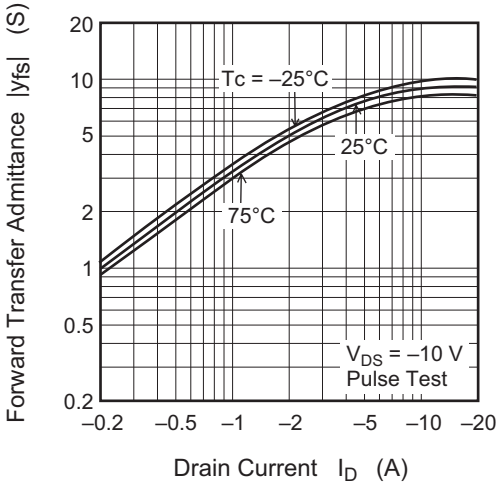
Static Drain to Source on State Resistance vs. Drain Current



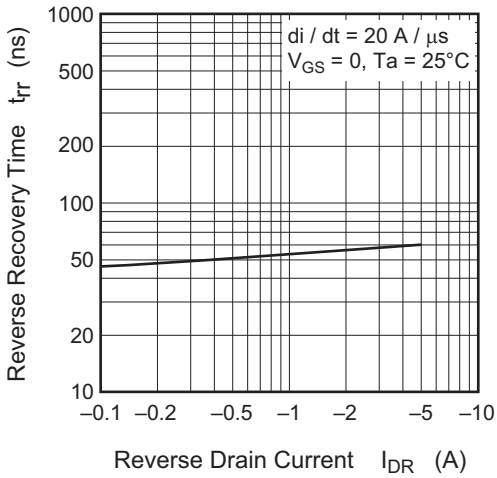
Static Drain to Source on State Resistance vs. Temperature



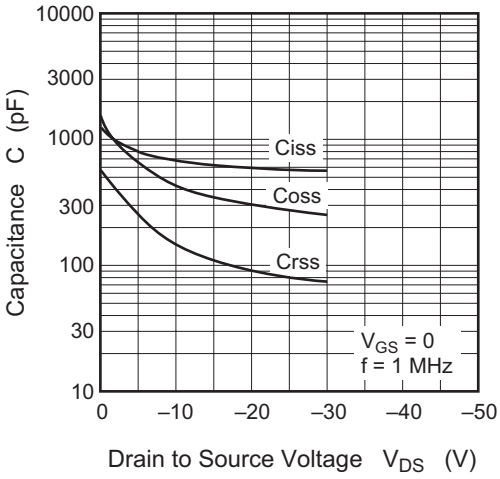
Forward Transfer Admittance vs. Drain Current



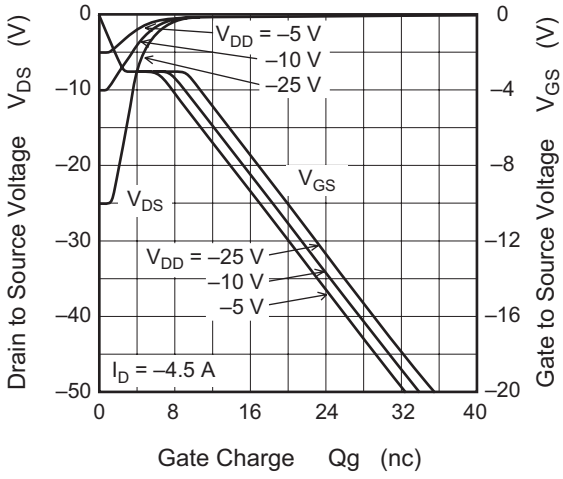
Body-Drain Diode Reverse Recovery Time



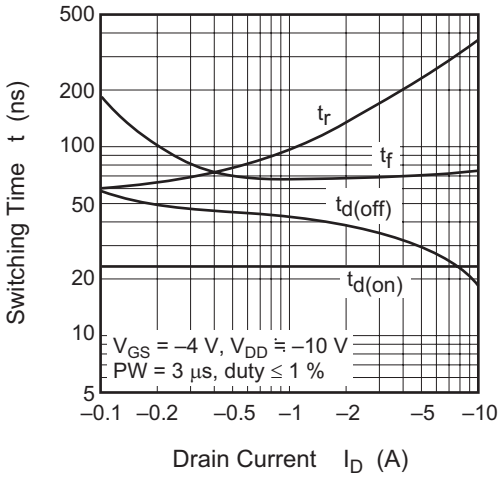
Typical Capacitance vs. Drain to Source Voltage



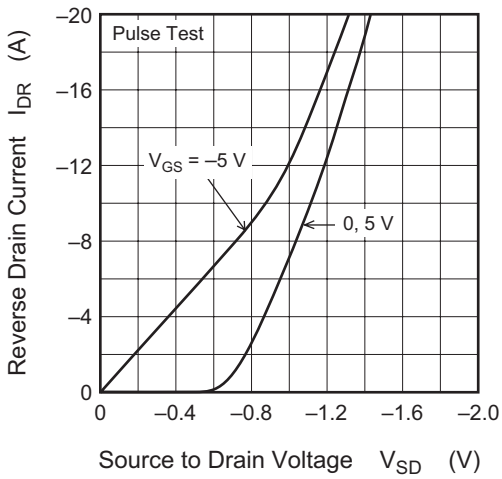
Dynamic Input Characteristics



Switching Characteristics

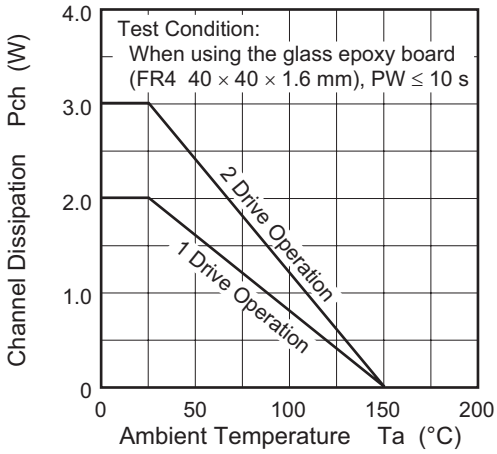


Reverse Drain Current vs. Source to Drain Voltage

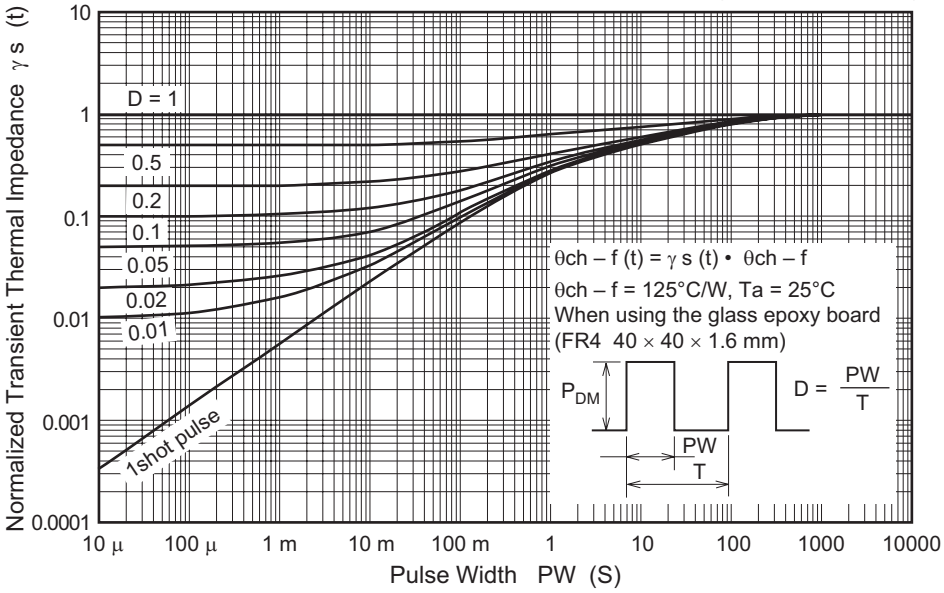


Common

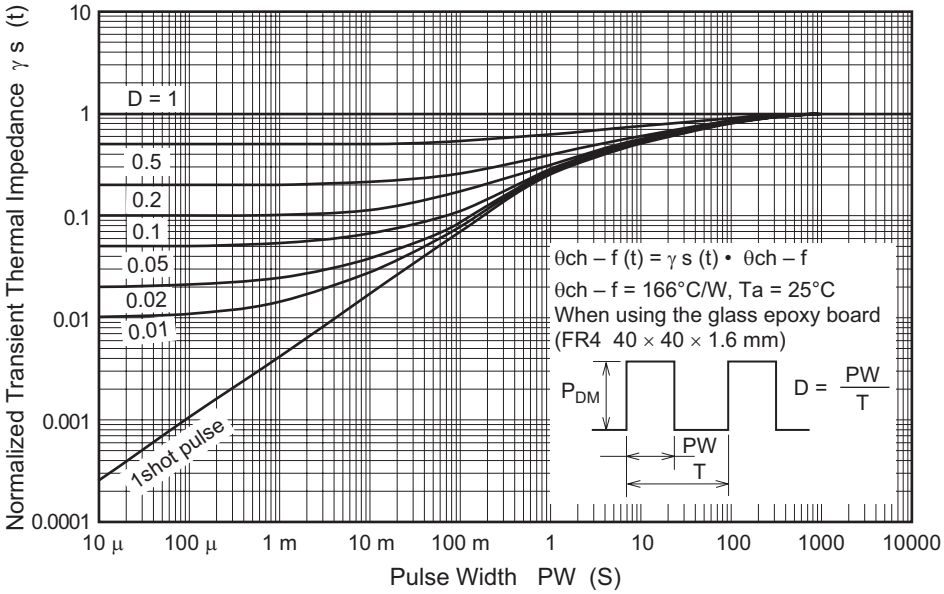
Power vs. Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

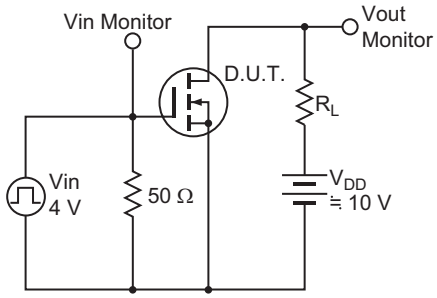


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

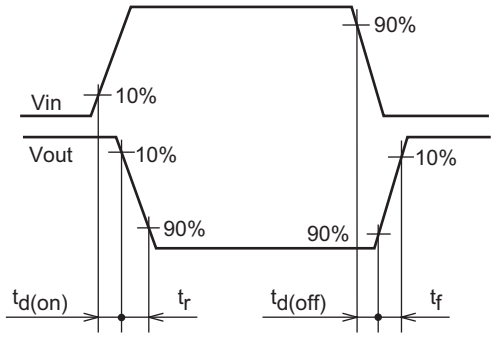


N channel

Switching Time Test Circuit

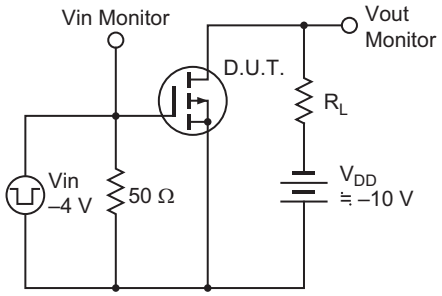


Switching Time Waveform

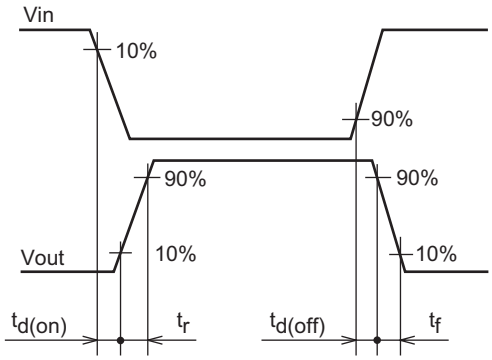


P channel

Switching Time Test Circuit

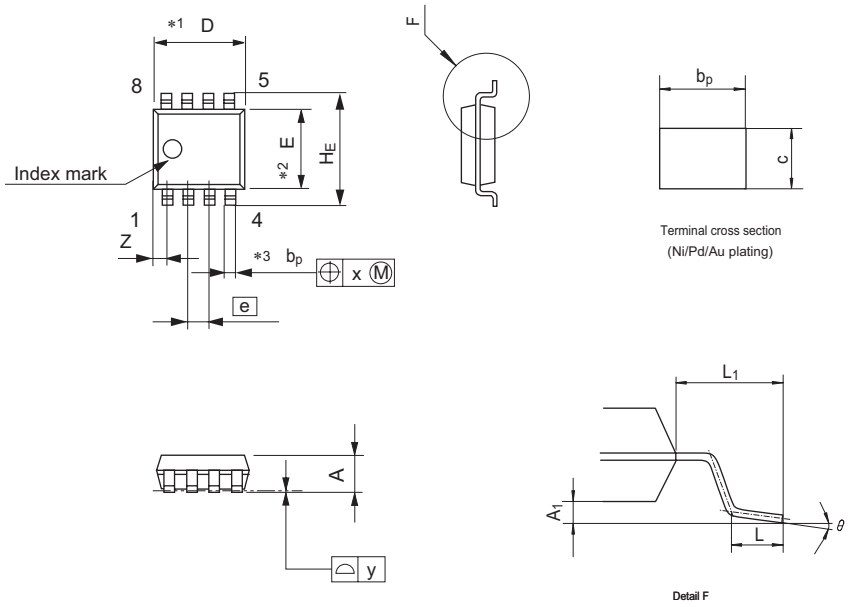


Switching Time Waveform



Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



Terminal cross section
(Ni/Pd/Au plating)

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Part Name	Quantity	Shipping Container
HAT3006R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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