Longest Match Engine

KE5BLME064

Ver. 2.5.4

Kawasaki LSI U.S.A., Inc.

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1. Features

The KE5BLME064 provides the best solution to a high-speed route search with the following functions:

- **64K Route Entries**
  - The device can store 65,528-route prefixes
  - Each entry has 40-bit width
- **Clock**
  - Maximum Clock Frequency: 66 MHz
- **Longest Match Search Capability**
- **Exact Match Search Capability**
- **Search Throughput**
  - 6.7 Mpps (packet per sec. at 66MHz clock) (10 clocks)
- **Search Latency**
  - 270 ns (hit flag; match length output) (18 clocks)
  - 555 ns (associative data output) (37 clocks)
- **Data Insertion/Deletion**
  - 534 entries/sec typical (During Search Operation) (66MHz)
  - 400k entries/sec maximum (During initialization Operation) (66MHz)
- **Triple-Port Architecture**
  - CPU port: 16 bit
  - Input port: 40 bit
  - Output port: 18 bit
- **Embedded External SRAM Control**
  - 3pcs of 2Mbits flow through type Synchronous Burst SRAM
- **Cascade Connection to Increase Density**
- **Interface**
  - LVTTL
- **Voltage**
  - Single 3.3V ± 0.3V Supply
- **Package**
  - 416 BGA (BGA352+TB64, TB:Thermal Ball)
- **CMOS Technology**

2. Block Diagram

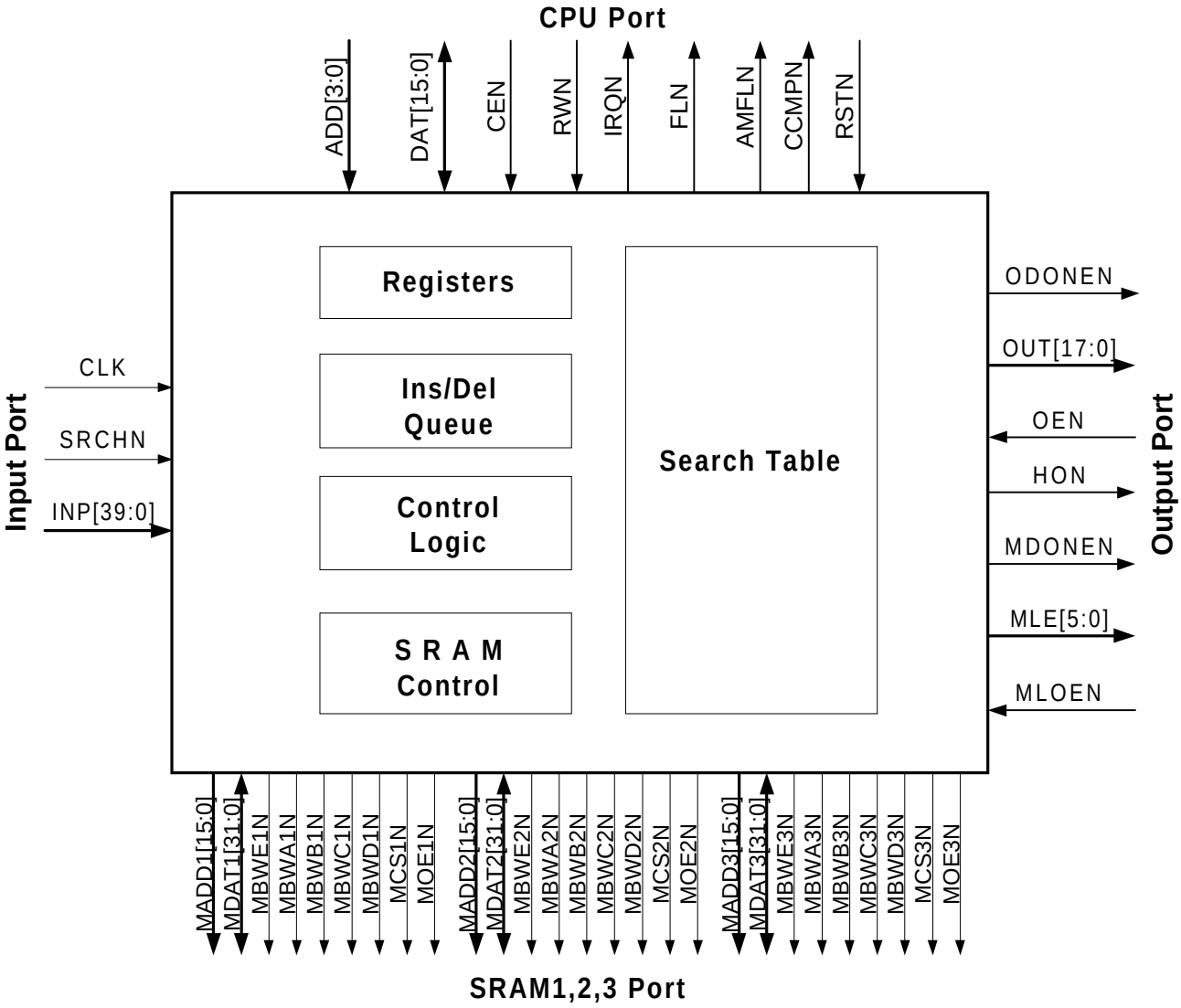


Fig. 2.1 Block Diagram

Pin Assignment and Description

3.1 Pin Assignment: Diagram

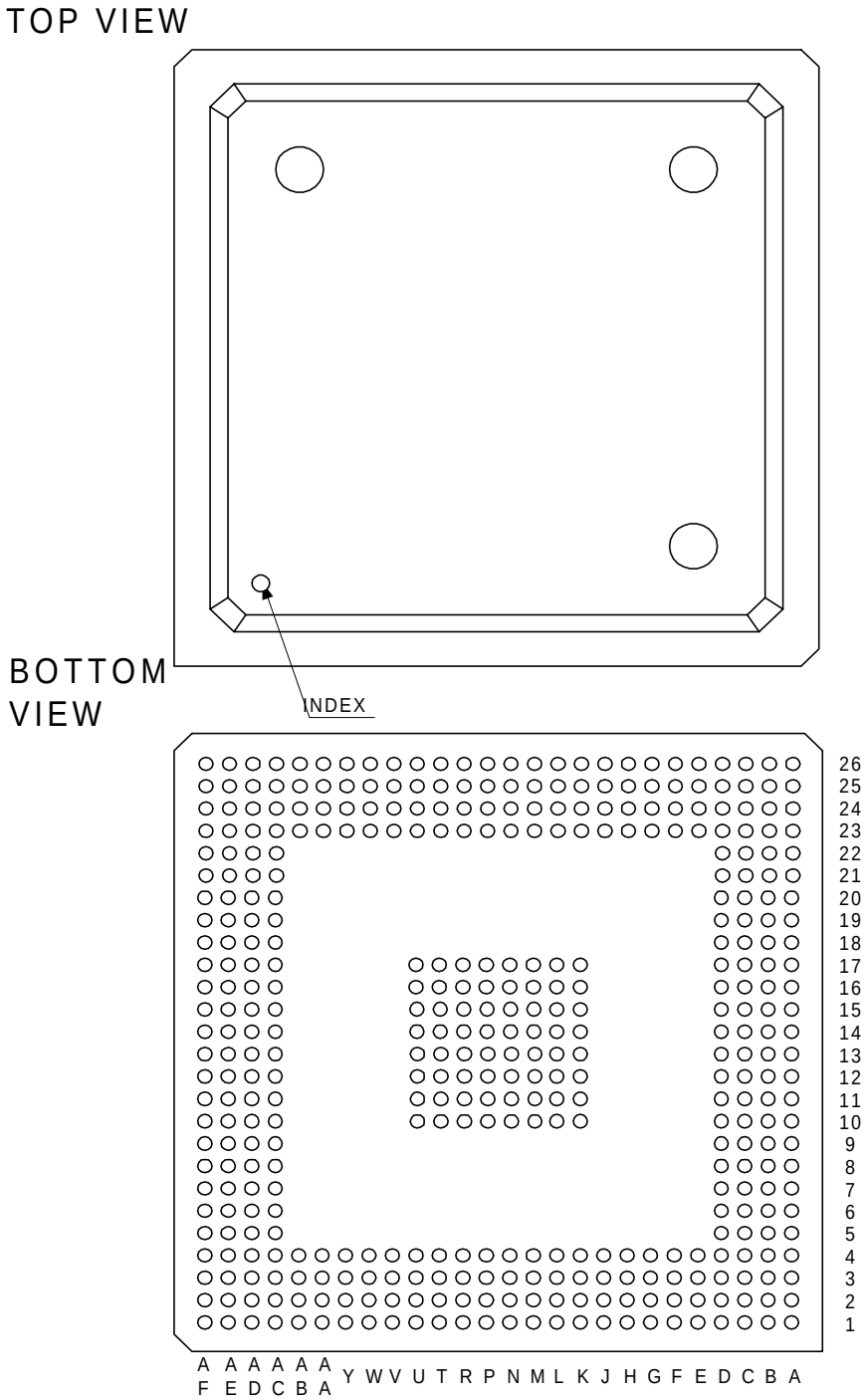


Fig. 3.1 Pin Assignment

3.2 Pin Assignment: List

No.	PIN NAME	I/O	No.	PIN NAME	I/O	No.	PIN NAME	I/O	No.	PIN NAME	I/O
A1	GND	-	B19	MLOEN	in	D11	DAT<15>	io	H23	GND	-
A2	INP<28>	in	B20	OUT<17>	out	D12	GND	-	H24	MADD3<10>	out
A3	INP<21>	in	B21	OUT<16>	out	D13	DAT<8>	io	H25	MADD3<9>	out
A4	INP<16>	in	B22	OUT<13>	out	D14	DAT<4>	io	H26	MADD3<8>	out
A5	INP<12>	in	B23	OUT<10>	out	D15	VDD	-	J1	GND	-
A6	INP<9>	in	B24	OUT<6>	out	D16	RSTN	in	J2	MADD1<1>	out
A7	INP<5>	in	B25	GND	-	D17	GND	-	J3	MADD1<2>	out
A8	INP<2>	in	B26	GND	-	D18	MLE<4>	out	J4	GND	-
A9	IRQN	out	C1	INP<35>	in	D19	VDD	-	J23	VDD	-
A10	CCMPN	out	C2	INP<29>	in	D20	GND	-	J24	MADD3<12>	out
A11	DAT<12>	io	C3	INP<23>	in	D21	GND	-	J25	MADD3<11>	out
A12	DAT<9>	io	C4	INP<18>	in	D22	GND	-	J26	VDD	-
A13	DAT<5>	io	C5	INP<14>	in	D23	GND	-	K1	MADD1<3>	out
A14	DAT<1>	io	C6	INP<11>	in	D24	OUT<8>	out	K2	MADD1<4>	out
A15	DAT<0>	io	C7	INP<7>	in	D25	OUT<4>	out	K3	MADD1<5>	out
A16	ADD<0>	in	C8	INP<4>	in	D26	OUT<1>	out	K4	GND	-
A17	MLE<5>	out	C9	INP<0>	in	E1	INP<37>	in	K23	VDD	-
A18	MLE<1>	out	C10	AMFLN	out	E2	INP<31>	in	K24	MADD3<15>	out
A19	MLE<0>	out	C11	DAT<14>	io	E3	INP<25>	in	K25	MADD3<14>	out
A20	OEN	in	C12	DAT<11>	io	E4	INP<19>	in	K26	MADD3<13>	out
A21	OUT<15>	out	C13	DAT<7>	io	E23	MADD3<2>	out	L1	MADD1<6>	out
A22	OUT<12>	out	C14	DAT<3>	io	E24	MADD3<1>	out	L2	MADD1<7>	out
A23	OUT<9>	out	C15	ADD<3>	in	E25	MADD3<0>	out	L3	MADD1<8>	out
A24	OUT<5>	out	C16	ADD<2>	in	E26	ODONEN	out	L4	MADD1<9>	out
A25	OUT<2>	out	C17	RWN	in	F1	INP<38>	in	L23	GND	-
A26	VDD	-	C18	MLE<3>	out	F2	INP<32>	in	L24	MDAT3<2>	io
B1	INP<34>	in	C19	MDONEN	out	F3	INP<26>	in	L25	MDAT3<1>	io
B2	VDD	-	C20	HON	out	F4	GND	-	L26	MDAT3<0>	io
B3	INP<22>	in	C21	VDD	-	F23	VDD	-	M1	MADD1<10>	out
B4	INP<17>	in	C22	OUT<14>	out	F24	MADD3<5>	out	M2	MADD1<11>	out
B5	INP<13>	in	C23	OUT<11>	out	F25	MADD3<4>	out	M3	MADD1<12>	out
B6	INP<10>	in	C24	OUT<7>	out	F26	MADD3<3>	out	M4	VDD	-
B7	INP<6>	in	C25	OUT<3>	out	G1	INP<39>	in	M23	GND	-
B8	INP<3>	in	C26	OUT<0>	out	G2	INP<33>	in	M24	MDAT3<5>	io
B9	SRCHN	in	D1	INP<36>	in	G3	INP<27>	in	M25	MDAT3<4>	io
B10	FLN	out	D2	INP<30>	in	G4	INP<20>	in	M26	MDAT3<3>	io
B11	DAT<13>	io	D3	INP<24>	in	G23	GND	-	N1	MADD1<13>	out
B12	DAT<10>	io	D4	VDD	-	G24	GND	-	N2	MADD1<14>	out
B13	DAT<6>	io	D5	INP<15>	in	G25	MADD3<7>	out	N3	MADD1<15>	out
B14	DAT<2>	io	D6	VDD	-	G26	MADD3<6>	out	N4	GND	-
B15	GND	-	D7	INP<8>	in	H1	GND	-	N23	MDAT3<9>	io
B16	ADD<1>	in	D8	GND	-	H2	OPEN	-	N24	MDAT3<8>	io
B17	CEN	in	D9	INP<1>	in	H3	MADD1<0>	out	N25	MDAT3<7>	io
B18	MLE<2>	out	D10	VDD	-	H4	VDD	-	N26	MDAT3<6>	io

No.	PIN NAME	I/O	No.	PIN NAME	I/O	No.	PIN NAME	I/O	No.	PIN NAME	I/O
P1	MBWE1N	out	W23	VDD	-	AC17	VDD	-	AE9	MDAT2<9>	io
P2	MCS1N	out	W24	MDAT3<17>	io	AC18	VDD	-	AE10	MDAT2<12>	io
P3	MOE1N	out	W25	MDAT3<16>	io	AC19	GND	-	AE11	MDAT2<15>	io
P4	GND	-	W26	MDAT3<15>	io	AC20	GND	-	AE12	MDAT2<19>	io
P23	GND	-	Y1	MDAT1<10>	io	AC21	VDD	-	AE13	MDAT2<22>	io
P24	GND	-	Y2	MDAT1<11>	io	AC22	VDD	-	AE14	MDAT2<24>	io
P25	MBWD3N	out	Y3	GND	-	AC23	GND	-	AE15	MDAT2<28>	io
P26	GND	-	Y4	GND	-	AC24	MDAT3<27>	io	AE16	MDAT2<31>	io
R1	MBWC1N	out	Y23	MDAT3<20>	io	AC25	MDAT3<26>	io	AE17	MBWB2N	out
R2	MBWD1N	out	Y24	MDAT3<19>	io	AC26	MDAT3<25>	io	AE18	MBWD2N	out
R3	GND	-	Y25	GND	-	AD1	MDAT1<20>	io	AE19	MADD2<14>	out
R4	GND	-	Y26	MDAT3<18>	io	AD2	MDAT1<21>	io	AE20	MADD2<13>	out
R23	VDD	-	AA1	MDAT1<12>	io	AD3	MDAT1<22>	io	AE21	MADD2<10>	out
R24	MBWC3N	out	AA2	MDAT1<13>	io	AD4	MDAT1<23>	io	AE22	MADD2<7>	out
R25	MOE3N	out	AA3	MDAT1<14>	io	AD5	MDAT1<24>	io	AE23	MADD2<4>	out
R26	CLK	in	AA4	VDD	-	AD6	MDAT2<1>	io	AE24	MADD2<2>	out
T1	MBWA1N	out	AA23	GND	-	AD7	MDAT2<4>	io	AE25	MDAT3<31>	io
T2	MBWB1N	out	AA24	MDAT3<22>	io	AD8	MDAT2<7>	io	AE26	MDAT3<30>	io
T3	MDAT1<0>	io	AA25	MDAT3<21>	io	AD9	GND	-	AF1	VDD	-
T4	MDAT1<1>	io	AA26	VDD	-	AD10	MDAT2<13>	io	AF2	MDAT1<29>	io
T23	MCS3N	out	AB1	MDAT1<15>	io	AD11	MDAT2<16>	io	AF3	GND	-
T24	MBWA3N	out	AB2	MDAT1<16>	io	AD12	MDAT2<20>	io	AF4	MDAT1<30>	io
T25	MBWB3N	out	AB3	MDAT1<17>	io	AD13	MDAT2<23>	io	AF5	MDAT1<31>	io
T26	GND	-	AB4	VDD	-	AD14	MDAT2<25>	io	AF6	VDD	-
U1	MDAT1<2>	io	AB23	GND	-	AD15	MDAT2<29>	io	AF7	MDAT2<2>	io
U2	MDAT1<3>	io	AB24	GND	-	AD16	MOE2N	out	AF8	MDAT2<5>	io
U3	MDAT1<4>	io	AB25	MDAT3<24>	io	AD17	MCS2N	out	AF9	MDAT2<8>	io
U4	VDD	-	AB26	MDAT3<23>	io	AD18	MBWE2N	out	AF10	MDAT2<11>	io
U23	GND	-	AC1	MDAT1<18>	io	AD19	MADD2<15>	out	AF11	MDAT2<14>	io
U24	MDAT3<11>	io	AC2	GND	-	AD20	GND	-	AF12	MDAT2<18>	io
U25	MDAT3<10>	io	AC3	MDAT1<19>	io	AD21	MADD2<11>	out	AF13	MDAT2<21>	io
U26	MBWE3N	out	AC4	GND	-	AD22	MADD2<8>	out	AF14	GND	-
V1	GND	-	AC5	GND	-	AD23	MADD2<5>	out	AF15	MDAT2<27>	io
V2	MDAT1<5>	io	AC6	GND	-	AD24	GND	-	AF16	MDAT2<30>	io
V3	MDAT1<6>	io	AC7	GND	-	AD25	MDAT3<29>	io	AF17	MBWA2N	out
V4	VDD	-	AC8	VDD	-	AD26	MDAT3<28>	io	AF18	MBWC2N	out
V23	MDAT3<14>	io	AC9	MDAT2<10>	io	AE1	MDAT1<25>	io	AF19	GND	-
V24	MDAT3<13>	io	AC10	GND	-	AE2	GND	-	AF20	MADD2<12>	out
V25	MDAT3<12>	io	AC11	MDAT2<17>	io	AE3	MDAT1<26>	io	AF21	MADD2<9>	out
V26	GND	-	AC12	VDD	-	AE4	MDAT1<27>	io	AF22	MADD2<6>	out
W1	MDAT1<7>	io	AC13	GND	-	AE5	MDAT1<28>	io	AF23	MADD2<3>	out
W2	MDAT1<8>	io	AC14	MDAT2<26>	io	AE6	MDAT2<0>	io	AF24	MADD2<1>	out
W3	MDAT1<9>	io	AC15	GND	-	AE7	MDAT2<3>	io	AF25	MADD2<0>	out
W4	GND	-	AC16	GND	-	AE8	MDAT2<6>	io	AF26	VDD	-

Table 3.1 Pin Assignment (cont'd)

3.3 Pin Description

Pin Name	Attribute	Description	#of Pins
CLK	Clock Input LVTTL	CLK is the master clock input. Input signals refer to the rising edge of CLK.	1
SRCHN	Search Enable Input LVTTL	SRCHN enables a search operation; search commences when Low is signaled.	1
INP <39:0>	Input Bus Input LVTTL	INP<39:0> is a 40-bit input bus used search key inputs.	40
OUT <17:0>	Output Bus Output LVTTL	OUT<17:0>, a 18-bit output bus, outputs the associate data.	18
OEN	Output Enable Input LVTTL	OEN controls OUT<17:0>. OEN Low enables OUT<17:0> ; and OEN High enables High-Z.	1
ODONEN	Output DONE Output LVTTL	ODONEN Low Active indicates that the associate data is output to the OUT <18:0> after a search.	1
HON	Hit Output Output LVTTL	HON outputs a search result. Low indicates a hit; High indicates a miss hit.	1
MLE <5:0>	Match Length Output LVTTL	MLE outputs match-length information (prefix lengh-1) between the data stored in the table and the relevant search key.	6
MLOEN	Match Length Output Enable Input LVTTL	MLOEN controls MLE<5:0> Output Enable. Low enables MLE<5:0>; High changes it to High-Z.	1
MDONEN	MLE Done Output LVTTL	MDONEN Low indicates that the completion of the search, outputting the match length to MLE<5:0>.	1
RSTN	Reset Input LVTTL	RSTN input Low resets the hardware.	1
IRQN	Interrupt Request Output Open Drain	IRQN indicates Low when an interrupt condition occurs in the CNTL register.	1
CCMPN	Command Execution Completion Output LVTTL	CCMPN signals High during the command operation executed via CPU port, and signals Low upon the completion of its execution.	1
ADD <3:0>	CPU Port Address Input LVTTL	ADD<3:0> is a register address.	4
DAT <15:0>	CPU Port Data Bus Input/Output LVTTL	DAT<15:0> is an input/output data bus for a CPU port.	16

Pin Name	Attribute	Description	#of Pins
CEN	CPU Port Enable Input LVTTL	CEN serves as the CPU port access; CEN Low enables the input operations of data and command.	1
RWN	Read/Write Input LVTTL	RWN determines the direction of the CPU bus; RWN Low selects "write" cycle, and RWN High "read" cycle.	1
FLN	Full Output LVTTL	FLN outputs Low when all entries are filled with valid data.	1
AMFLN	Almost Full Output LVTTL	AMFLN outputs Low when reaching "almost full"; the number of entries is equal to or exceeds the value stored in the Almost Full Register.	1
MADD1 <15:0>	SRAM1 Address Output LVTTL	MADD1 is SRAM1 address output. Ensure that it is connected to SRAM1 address pins.	16
MDAT1 <31:0>	SRAM1 Data Bus Input/Output LVTTL	MDAT1 is a bi-directional Bus for SRAM1. Ensure that it is connected to SRAM1 data pins.	32
MCS1N	SRAM1 Chip Enable Output LVTTL	MCS1N is SRAM1 chip enable signal. Ensure that it is connected to SRAM1 chip enable.	1
MOE1N	SRAM1 Output Enable Output LVTTL	MOE1N is SRAM1 Output Enable signal. Ensure that it is connected to SRAM1 output enable input.	1
MBWE1N	SRAM1 Byte Write Enable Output LVTTL	MBWE1N is SRAM1 Byte Write Enable signal. Ensure that it is connected to SRAM1 Byte write enable input.	1
MBWA1N	SRAM1 Synchronous Byte Write Enable Output LVTTL	MBWA1N is SRAM1 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM1 Synchronous Byte write enable A input.	1
MBWB1N	SRAM1 Synchronous Byte Write Enable Output LVTTL	MBWB1N is SRAM1 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM1 Synchronous Byte write enable B input.	1
MBWC1N	SRAM1 Synchronous Byte Write Enable Output LVTTL	MBWC1N is SRAM1 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM1 Synchronous Byte write enable C input.	1
MBWD1N	SRAM1 Synchronous Byte Write Enable Output LVTTL	MBWD1N is SRAM1 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM1 Synchronous Byte write enable D input.	1
MADD2 <15:0>	SRAM2 Address Output LVTTL	MADD2 is SRAM2 address output. Ensure that it is connected to SRAM2 address pins.	16
MDAT2 <31:0>	SRAM2 Data Bus Input/Output LVTTL	MDAT2 is a bi-directional Bus for SRAM2. Ensure that it is connected to SRAM2 data pins.	32
MCS2N	SRAM2 Chip Enable Output LVTTL	MCS2N is SRAM2 chip enable signal. Ensure that it is connected to SRAM2 chip enable.	1

Pin Name	Attribute	Description	#of Pins
MOE2N	SRAM2 Output Enable Output LVTTL	MOE2N is SRAM2 Output Enable signal. Ensure that it is connected to SRAM2 output enable input.	1
MBWE2N	SRAM2 Byte Write Enable Output LVTTL	MBWE2N is SRAM2 Byte Write Enable signal. Ensure that it is connected to SRAM2 Byte write enable input.	1
MBWA2N	SRAM2 Synchronous Byte Write Enable Output LVTTL	MBWA2N is SRAM2 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM2 Synchronous Byte write enable A input.	1
MBWB2N	SRAM2 Synchronous Byte Write Enable Output LVTTL	MBWB2N is SRAM2 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM2 Synchronous Byte write enable B input.	1
MBWC2N	SRAM2 Synchronous Byte Write Enable Output LVTTL	MBWC2N is SRAM2 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM2 Synchronous Byte write enable C input.	1
MBWD2N	SRAM2 Synchronous Byte Write Enable Output LVTTL	MBWD2N is SRAM2 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM2 Synchronous Byte write enable D input.	1
MADD3 <15:0>	SRAM3 Address Output LVTTL	MADD3 is SRAM3 address output. Ensure that it is connected to SRAM3 address pins.	16
MDAT3 <31:0>	SRAM3 Data Bus Input/Output LVTTL	MDAT3 is a bi-directional Bus for SRAM3. Ensure that it is connected to SRAM3 data pins.	32
MCS3N	SRAM3 Chip Enable Output LVTTL	MCS3N is SRAM3 chip enable signal. Ensure that it is connected to SRAM3 chip enable.	1
MOE3N	SRAM3 Output Enable Output LVTTL	MOE3N is SRAM3 Output Enable signal. Ensure that it is connected to SRAM3 output enable input.	1
MBWE3N	SRAM3 Byte Write Enable Output LVTTL	MBWE3N is SRAM3 Byte Write Enable signal. Ensure that it is connected to SRAM3 Byte write enable input.	1
MBWA3N	SRAM3 Synchronous Byte Write Enable Output LVTTL	MBWA3N is SRAM3 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM3 Synchronous Byte write enable A input.	1
MBWB3N	SRAM3 Synchronous Byte Write Enable Output LVTTL	MBWB3N is SRAM3 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM3 Synchronous Byte write enable B input.	1
MBWC3N	SRAM3 Synchronous Byte Write Enable Output LVTTL	MBWC3N is SRAM3 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM3 Synchronous Byte write enable C input.	1
MBWD3N	SRAM3 Synchronous Byte Write Enable Output LVTTL	MBWD3N is SRAM3 Synchronous Byte Write Enable signal. Ensure that it is connected to SRAM3 Synchronous Byte write enable D input.	1
VDD	Supply	The voltage required is 3.3V.	24
GND	Ground	Ground pin.	49

4. Functional Descriptions

4.1 Overview

KL5BLME064 is a search device for 40-bit IP address searches in IP routing applications. Its capability extends beyond a simple lookup of data entries stored in a routing table. With its compatibility with the CIDR (Classless Inter-Domain Routing), it outputs associated data for the longest match data when there are multiple matching entries. KE5BLME064 also has the search capability of finding the exact 40-bit match for searching the host address.

Moreover, LME064 provides a solution to routes having the same address with different prefix length. Let us assume, for instance, the presence of both 0.192.1.0.0/24 and 0.192.1.0.0/32 in a routing table; the search key of 0.192.1.1.2 outputs associated data relative to 0.192.1.0.0/24 whereas the search key of 0.192.1.0.3 outputs ones relative to 0.192.1.0.0/32.

KL5BLME064 is a triple-port architecture equipped with task-specific ports: Input port conducting a search, Output port effecting a result, and CPU port executing commands and accessing to a register. This triple-port architecture facilities insertion and deletions of entries without interrupting a search operation.

In order to store data, LME064 operates with 3pcs of 2Mbits SRAM.

4.2. Reset

The LME064 device requires a reset after chip power up. A reset can be applied by either supplying a low pulse to the RSTN pins or writing any data onto a Reset register. The values reassigned for both pins and registers are as follows:

Registers		Pins	
CNTL:	0000000b	IRQN:	High-Z
STAT0:	1x00b	FLN:	High
STAT1:	0000000b	AMFLN:	High
PR0 – RR2:	Unknown	CCMPN:	Low
Almost Full constant:	7FFFh	ODONEN:	High
Default Associate Data:	Unknown	MDONEN:	High
Entry Counter constant:	0000h	HON:	High
		MCS#N:	High
		MOE#N:	Low

MBWE#N: High
MBWA#N High
MBWB#N High
MBWC#N High
MBWD#N High
(#: 1, 2, 3)

4.3. Initialization

When the Initialize command is executed, insertion / deletion Queue and search table are initialized, Entry Counter constant becomes 0000h. This command is suitable for constructing a new search table.

As in using other command, before proceeding with the subsequent commands, check anew by monitoring the CCMPN pin whether the initialization process has been completed.

4.4. Data Insertion

To enter data in the table, use the Insert command. Ensure that the IP address is set to WR0-2, the associated data(ASD) to WR3-4, and PL (prefix length –1) to WR2.

Example:

When inserting 0.192.1.2.0/32 with associated data 3456h, enter the following.

WR0: IP[15:0]	0200h (2.0)
WR1: IP[31:16]	C001h (192.1)
WR2: 2'bxx, PL[5:0], IP[39:32]	1F00h (31=32-1.0)
WR3: ASD[15:0]	3456h
WR4: 14'bx..x, ASD[17:16]	0000h

Ensure that the value entered in WR2 is the prefix-length minus 1, not the prefix-length itself. Please put the value of 0 in the host address part.

The completion of the Insert command is confirmed by a low signal on the CCMPN pin. Proceed with the subsequent commands after checking the CCMPN status.

Actually, the data is acknowledged as the data of the search table within 20 clocks after the Insert command is issued and the Entry Counter is increased before the completion of the Insert command.

Notes:

- Even if the signal of the CCMPN pin becomes low level on the completion of the Insert command, the inserted data is not stored in the search table and the Entry Counter is not increased when the search table is full (the signal of FLN pin is low).
- The entry counter does not increase when IP address and PL (prefix length -1) of the inserted data are the same as that of the retrieval table on the completion of the Insert command.
- These status are known as the value of STAT1 register.

LME064 is capable of storing the exact data match, i.e., the entry data hitting only when all the 40 bits coincide with the input key data. When inserting exact match data, set 39 to WR2 (PL[5:0]) because this device considers the prefix length to be a range of the retrieval. This particular function is useful for storing the host address in the table.

4.5. Search

To conduct a longest match search, apply data to INP [39:0], and set a SRCHN pin Low (see Fig.4.1). At the 18th clock after starting a search, MDONEN will be changed to Low, allowing both MLE [5:0] and HON to output. MLE [5:0] output should be equal to the match length minus one. That is to say, MLE [5:0] is the maximum value of the match length of a search key minus 1. The HON status indicates a lookup result, with Low a hit, and High as a miss hit. MDONEN will revert from High to Low after 4 clock cycles, while both MLE [5:0] and HON will be held until the next lookup result.

At the 37th clock after starting a search, ODONEN will be changed into Low, allowing OUT [17:0] to output associated data. If the search results in a miss match, the value pre-registered at the default associated data will be returned and MLE[5:0] output is 00h. ODONEN will revert from High to Low after 4 clock cycles, whereas OUT [17:0] will be held until the next result. For instance, let us assume the presence of the following data in the table:

0.133.5.0.0/24 [associated data: 01111h]
0.133.5.16.0/32 [associated data: 02222h]
Cf. Default associated data: 00000h

The result is as follows:

Search Key	Result	HON status	MLE[5:0]	OUT[17:0]
0.133.5.16.2	Hit at 0.133.5.16.0/32	Low	31 (1Fh)	02222h
0.133.5.17.3	Hit at 0.133.5.0.0/24	Low	23 (17h)	01111h
0.133.6.0.1	Miss hit*	High	0	00000h

Note: **"*"** indicates that0.133.5.0.0 and 0.133.6.0.1 have the matching length of 22bits; a miss hit occurs because the matching length is shorter than the registered value of "24."

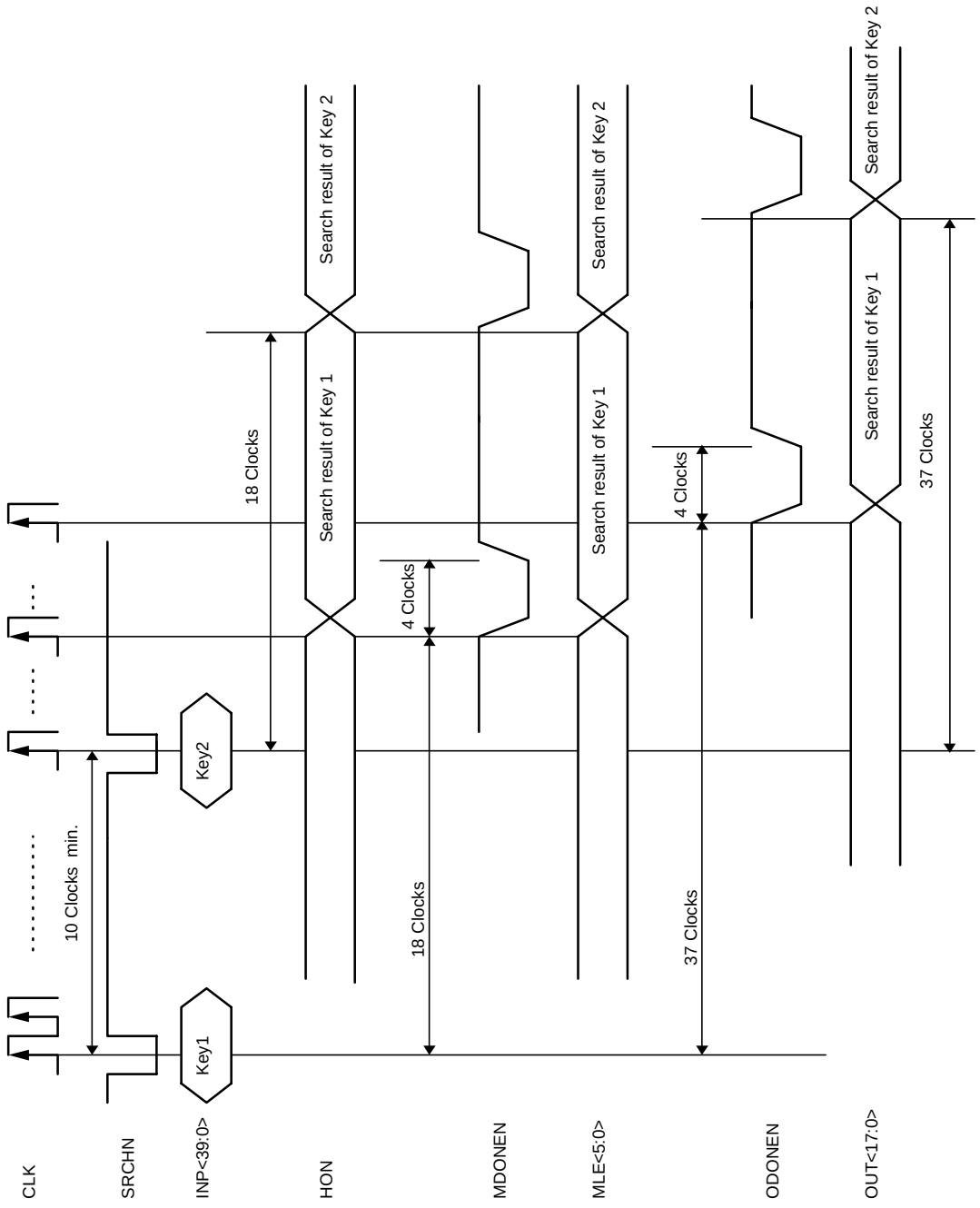


Fig. 4.1 Search Timing

4.6. Data Deletion

To delete data from the table, use the Delete command. Ensure that the IP address is set to WR0-2, and PL to WR2 with a prefix-length minus 1 before executing the commands.

Example:

If deleting 0.192.1.2.0/32, set the registers as follows.

WR0: IP[15:0]	0200h (2.0)
WR1: IP[31:16]	C001h (192.1)
WR2: 2'bxx, PL[5:0], IP[39:32]	1F00h (31=32-1.0)

The completion of the Delete command will be confirmed by a low status of CCMPN pin. Before proceeding with the subsequent commands, check anew to confirm that the Delete command execution has finished.

Actually, the data is acknowledged as the deleted data of the search table within 20 clocks after the Delete command is issued and the Entry Counter is decreased before the completion of the Delete command.

Notes:

- Ensure that the value set to WR2 is the prefix-length minus 1, not the prefix-length itself. No deletion can be performed if the value entered to WR2 differs from that of the initial entry, that is the prefix-length minus 1, and the Entry Counter is not decreased.
- Even if the signal of the CCMPN pin becomes low level on the completion of the Delete command, no deletion can be performed if the value entered to WR0-2 differs from that of the search table entry and the Entry Counter is not decreased.
- These status are known as the value of STAT1 register.

4.7. Data Insertion/Deletion Rate

The maximum Insertion rate is about 400k entries per second (at 66Mhz system clock operation) after the Initialize command is executed. This rate is performed on the condition that each new IP address data is sequentially inserted from the small one to

the large one.

Contrary, the minimum Insertion rate is about 1.4k entries per second after the Initialize command, this is on the condition that each new IP address data is inserted one by one in large the order.

When both of data A and data B have the same IP data, it is preferable to insert the data with the small value of PL (prefix length –1) previously . However, this is not to required.

The typical Insertion/Deletion rate during search operations is about 500 entries per second and worst Insertion/Deletion rate is about 250 entries per second. The maximum waiting time between Insertion/Deletion commands is about 30msec (at 66Mhz system clock operation).

4.8. Search via CPU Port

A search can be performed with the CPU port commands, independently of the Input port operation. Apply a search key data to WR0-2 to execute the Search command. Upon completion of a table lookup, associated data will be written to RR0-1; and both ML (prefix-length minus one) and hit-or-miss-hit information will be written to RR2. The command execution can be confirmed by monitoring the CCMPN pin status; before proceeding with subsequent commands, ensure that the CCMPN pin is changed to Low.

4.9. Interruption

Some statues of interrupt are defined in this device, that can be heard of by reading the STAT1 register. Also the generation of interrupt can be known according to the signal of IRQN pin when the interrupt with IRQN pin is defined in CNTL register.

When the STAT1 register is red, the value of STAT1 register should revert each bit to “0” and Interrupt with IRQN pin should be cleared.

Refer to “6.2. Register Description” for the interrupt event with IRQN pin which can concretely be defined. Interruption is not accomplished unless one of the conditions is met, as described in “6.2. Register Description.” For instance, setting both bit 2 and bit 0 of the CNTL register to “1” activates the Interrupt operation upon completion of either the Initialize command or the table fulfillment process.

Notes:

- The Interrupt operation set to the bit 6 occurs ONLY after the data is not deleted from Search Table against Deletion command, because there isn't that data in Search Table. No other commands are valid.
- The Interrupt operation set to the bit 5 occurs ONLY after a new data is stored in Search Table by Insertion command but the Entry Counter is not increased, because a data as which IP address and PL (prefix length –1) are the same already exists in Search Table. No other commands are valid.
- The Interrupt operation set to the bit 4 occurs ONLY after a new data is not stored in Search Table against Insertion command, because Search Table is full. No other commands are valid.
- The Interrupt operation set to the bit 3 occurs ONLY after the executions of Search/Insert/Delete commands. No other commands are valid.
- The Interrupt operation set to the bit 2 occurs ONLY after the execution of the Initialize command. No other commands are valid.
- The Interrupt operation set to the bit 1 occurs ONLY after the execution of either the Insert or Delete command when the values registered in the Entry Count match those of the Almost Full Register. See the example below:

Example: Entry Count = 999 (3E7h)/Almost Full Register = 1000 (3E8h)

Command	Entry Count	Interruption	AMFLN
Insert	**1000**	**Generated**	**Low**
↓			
Read STAT1	**1000**	**Not generated**	**Low**
↓			
Insert	1001	Not generated	Low
↓			
Insert	1002	Not generated	Low
↓			
Delete	1001	Not generated	Low
↓			
Delete	**1000**	**Generated**	Low
↓			
Delete	999	Not generated	High

- The Interrupt operation set to the bit 0 occurs ONLY after the table becomes full.

4.10. Typical Operational Flow

(1) Turn on the power.
(2) Reset
Input a Low pulse to a RSTN.
(3) Initialize.
Write “Initialize” (0004h) onto the COM register (00h).
Wait for CCMPN to turn to Low.

(4) Set the default associate data:
(a) Write “FFFFh” onto WR0 (04h).
(b) Write “0000h” onto WR1(05h).
Write “Set Default Associated Data” (0007h) onto the COM register (00h).
(c) Wait for the CCMPN to Low.

(5) Data Insertion 1
(a) Write “0000h” onto WR0 (04h).
(b) Write “C018h” onto WR1 (05h).
(c) Write “1C00h” onto WR2 (06h).
(d) Write “1111h” onto WR3 (07h).
(e) Write “xxx0h” onto WR4 (08h).
(f) Write “Insert” (0002h) onto the COM register (00h).
(g) Wait for CCMPN to turn to Low

0.192.24.0.0/29 will be registered with associated data 01111h in a table
Entry Counter becomes 1.

(6) Data Insertion 2
(a) Write “0800h” onto the WR0 (04h).
(b) Write “C018” onto the WR1 (05h).
(c) Write “1D00h” onto the WR2 (06h).
(d) Write “2222h” onto the WR3 (07h).
(e) Wrote “xxx0h” onto the WR4 (08h).
(f) Write “Insert” (0002h) onto the COM register (00h).

(g) Wait for CCMPN to turn to Low.

0.192.24.8.0 /30 will be registered with associated data 02222h in the table. Entry Counter becomes 2.

(7) Data Insertion 3

(a) Write “0000h” onto the WR0 (04h).
(a) Write “C018h” onto the WR1 (05h).
(b) Write “1400h” onto the WR2 (06h).
(c) Write “0000h” onto the WR3 (07h).
(d) Write “xxx0h” onto the WR4 (08h).
(e) Write “Insert” (0002h) onto the COM register (00h).
(f) Wait for the CCMPN to turn to Low.

0.192.24.0.0/21 will be registered in the table with associated data 00000h. Entry Counter becomes 3.

(8) Data lookup 1

(g) Start with 0.192.24.1.2 (00C0180102h):

Result	Hit
HON	Low
MLE [5:0]	1Ch
OUT [17:0]	01111h

(9) Data Lookup 2

Start with 0.192.25.1.2 (00C0190102h):

Result:	Hit
HON:	Low
MLE [5:0]	14h
OUT [17:0]	00000h

(10) Data Lookup 3

Start with 0.192.24.10.11(00C0180A0Bh):

Result: Hit

HON: Low
MLE [5:0] 1Dh
OUT [17:0] 02222h

(11) Data Lookup 4

Start with 0.193.24.10.11 (00C1180A0Bh):

Result: Miss Hit
HON: High
MLE [5:0] 00h
OUT [17:0] 0FFFFh

(12) Data Insertion 4

(a) Write “0102h” onto the WRO (04h).
(b) Write “C018h” onto the WR1 (05h).
(c) Write “2700h” onto the WR2 (06h).
(d) Write “1234h” onto the WR3 (07h).
(e) Write “xxx0h” onto the WR4 (08h).
(f) Write “Insert” (0002h) onto the COM register (00h).

The Host Address 0.192.24.1.2/40 will be stored with associated data 01234h.
Entry Counter becomes 4.

(13) Data Insertion 5

(a) Write “0000h” onto WR0 (04h).
(b) Write “C018h” onto WR1 (05h).
(c) Write “1C00h” onto WR2 (06h).
(d) Write “3333h” onto WR3 (07h).
(e) Write “xxx0h” onto WR4 (08h).
(f) Write “Insert” (0002h) onto the COM register (00h).
(g) Wait for CCMPN to turn to Low

0.192.24.0.0/29 will be registered with associated data 03333h in a table
Entry counter maintains the value of 4, because there is already the data which has the same IP address and PL(prefix length - 1).

(14) Data Lookup 5

Start with 0.192.24.1.2 (00C0180102h):

Result: Hit
HON: Low
MLE [5:0] 27h
OUT [17:0] 01234h

(15) Data Lookup 6
Start with 0.192.24.1.3 (00C0180103h):

Result: Hit
HON: Low
MLE [5:0] 1Ch
OUT [17:0] 03333h

(16) Data Deletion
(a) Wait for the CCMPN to turn to Low.
(b) Write “0000h” onto the WR0 (04h).
(c) Write “C018h” onto the WR1 (05h).
(d) Write “1400h” onto the WR2 (08h).
(e) Write “Delete” (0003h) onto the COM register (00h).
0.192.24.0.0/21 will be deleted.
Entry Counter becomes 3.

(17) Data Lookup 7
Start with 0.192.25.1.2 (00C0190102h):
Result: Miss Hit
HON: High
MLE [5:0] 00h
OUT [17:0] 0FFFFh

4.11. Cascade Connection

To compose a bigger search table, two or more devices can be connected. The example is shown in Figure 4.11. Each device has a different search table basically, and works completely independently.

When the search operates, data to which each device matches longest in the table is output. The values of MLE[5:0] from each device should be compared respectively. After that, OUT[17:0] of the device with the largest the MLE[5:0] value only has to be selected.

The command of each device from CPU port is often executed respectively . Therefore, the CEN signal of each device should be made optional independently.

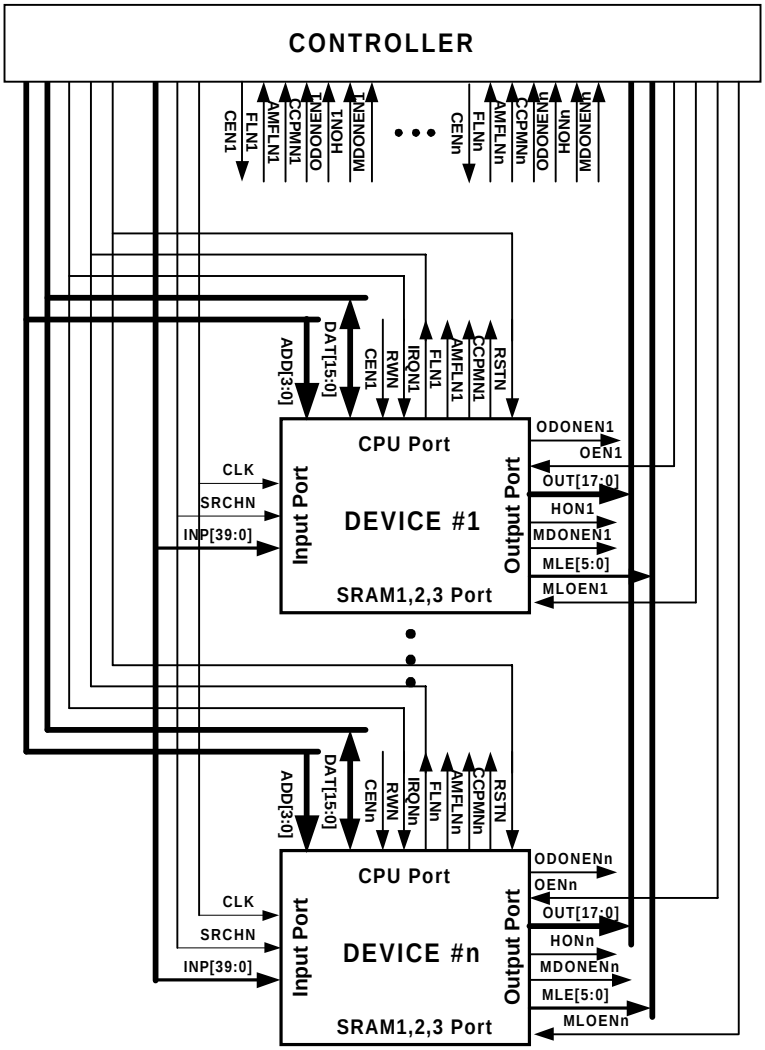


Figure 4.11 Cascade Connection

5. SRAM

5.1. SRAM Specification

When using KE5BLME064, ensure that the corresponding SRAM meets the following requirements:

2Mbits Flow through type Synchronous Burst SRAM (64k-word x 32bits)

- Voltage: 3.3V
- Access time: 9ns

Eg. Micron MT58LC64K32B4

5.2. Connecting to SRAM

For the connection of LME064 to SRAM, see Fig. 5.1 below.

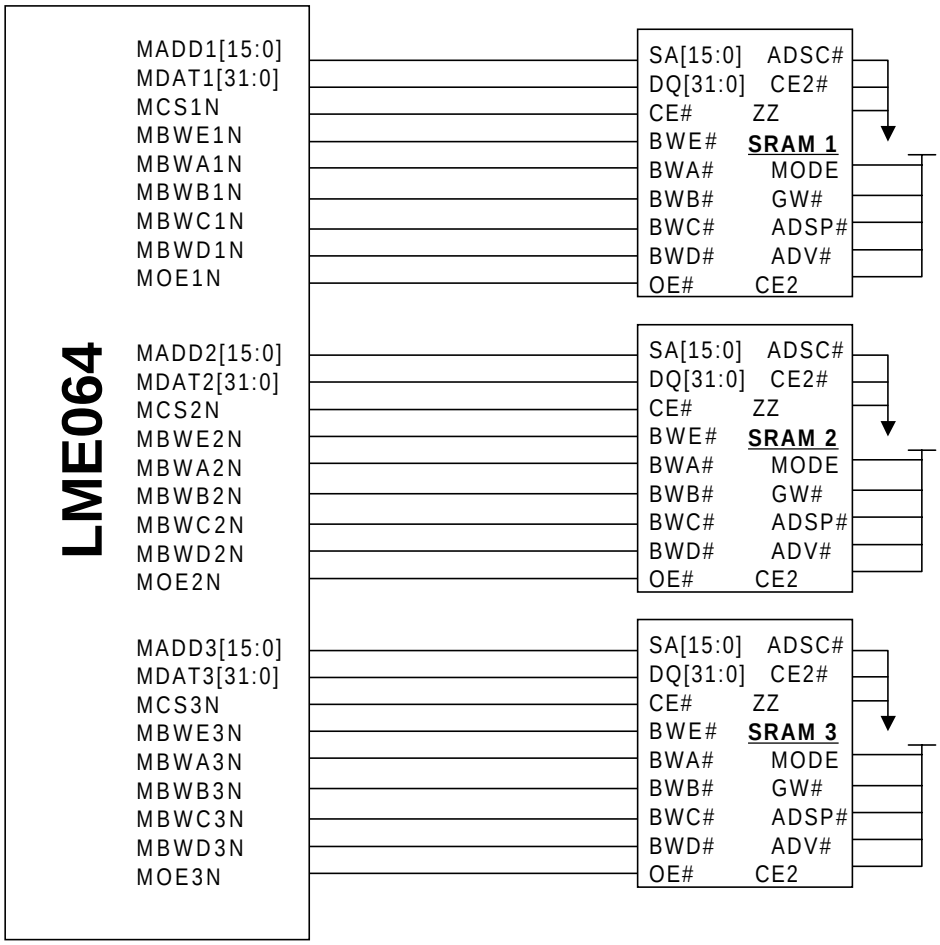


Fig. 5.1 Connection to SRAM

6. Register

6.1. Register Map

Register name	Address	Type
COM	0h	Write
CNTL	1h	R/W
STAT0	2h	Read
STAT1	3h	Read
WR0	4h	Write
WR1	5h	Write
WR2	6h	Write
WR3	7h	Write
WR4	8h	Write
RR0	9h	Read
RR1	Ah	Read
RR2	Bh	Read
RESET	Fh	Write

Table 6.1 Register Address

6.2. Register Description

COM (Command Register) Write Only

ADD [3:0] = 0h:

Write the 16-bit OP code below in the COM register for a command execution:

Command	OP Code	Use Register
NOP	0000h	-
Search	0001h	WR0,WR1,WR2, RR0, RR1,RR2
Insert	0002h	WR0, WR1, WR2, WR3, WR4
Delete	0003h	WR0, WR1,WR2
Initialize	0004h	-
Set Almost Full Register	0005h	WR0
Set Default Associated Data	0007h	WR0, WR1
Write SRAM	0008h	WR0, WR1, WR2, WR3
Read Almost Full Register	0015h	RR0
Read Default Associated Data	0017h	RR0, RR1
Read SRAM	0018h	WR0 , WR1, RR0, RR1
Return Entry Count	001Bh	RR0

Table 6.2 OP Code

CNTL (Control Register):

ADD [3:0] = 01h:

Controls the configuration of an Interrupt operation with the signal of IRQN pin.

bit 6 1: Enables interruption on the data is not deleted from Search Table against Deletion command because there isn't that data in Search Table.

bit 5 1: Enables interruption on a new data is stored in Search Table by Insertion command but the Entry Counter is not increased because a data as which IP address and PL(prefix length –1) are the same already exists in Search Table.

bit 4 1: Enables interruption on a new data is not stored in Search Table against Insertion command because Search Table is full.

bit 3 1: Enables interruption on the Completion of Search/Ins/Del command

bit 2 1: Enables interruption on the Completion of Initialize command

bit 1 1: Enables interruption on Table reaching almost full point

bit 0 1: Enables interruption on Table reaching full

Default Value 0000000b

STAT0 (Status Register):

ADD [3:0] = 02h:

This register stores four kinds of status information during operation.

bit 3	1: Last command complete	/ 0: Not yet complete
bit 2	1: CPU search hit	/ 0: CPU search miss hit
bit 1	1: Table almost full	/ 0:Table not almost full
bit 0	1: Table full	/ 0:Table not full

Default Value 1x00b

Bit 2 is valid after the Search command is executed until the next Search command is engaged.

STAT1 (Interrupt Status Register):

ADD [3:0] = 03h:

This register shows seven kinds of interruption information. The register will be cleared after reading is completed. IRQN will be cleared when this register is read even if the interrupt status is remaining.

bit 6 1: Interruption on the data is not deleted from Search Table against Deletion command because there isn't that data in SearchTable.
bit 5 1: Interruption on a new data is stored in Search Table by Insertion command but the Entry Counter is not increased because a data as which IP address and PL (prefix length –1) are the same already exists in Search Table.
bit 4 1: Interruption on a new data is not stored in Search Table against Insertion command because Search Table is full.
bit 3 1: Interruption on the Completion of Search/Ins/Del command
bit 2 1: Interruption on the Completion of Initialize command
bit 1 1: Interruption on Table reaching almost full point
bit 0 1: Interruption on Table reaching full

Default Value 0000000b

WR0-4 (Write Register):

WR0: ADD[3:0] = 04h
WR1: ADD[3:0] = 05h
WR2: ADD[3:0] = 06h
WR3: ADD[3:0] = 07h
WR4: ADD[3:0] = 08h

Stores the data required for the command executions. See Table 6.2, "OP Code" for registers specific to each command.

RR0-2 (Read Register):

RR0: ADD[3:0] = 09h
RR1: ADD[3:0] = 0Ah
RR2: ADD[3:0] = 0Bh

The data set to RR0-RR2 is valid until the next command is engaged.
RR0-RR2 has unknown values when the command with no return value to these registers is executed.

RESET (Reset Register):

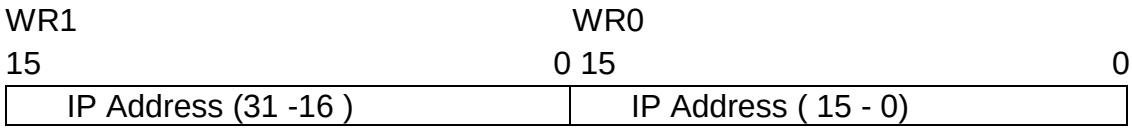
ADD [3:0] =0Fh
Write onto this register to activate the Reset command. This operation is the same as the RSTN pin requiring a low pulse input.

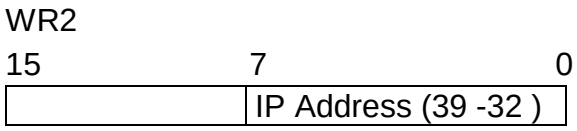
7. Command Description

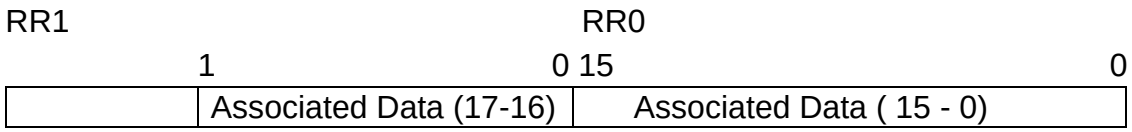
Writing the OP code onto the COM register (00h) enables a command execution. Upon completion of the command execution, bit3 of STAT0 will be changed to 1, and CCMPN to Low. Throughout the execution of a particular command, the execution of the other commands is prohibited; and rewriting to the WR register is also prohibited. Should rewriting to either the WR register or the COM register occur, the proper command execution may not be maintained.

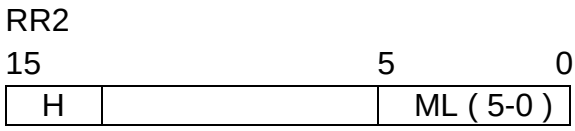
NOP (OP Code: 0000h):
No operation.

Search(OP Code: 0001h):
When this command is executed, a lookup operation starts with a key value in WR0-2. Upon completion of this command, associated data is written to RR0-1, and ML (Match Length minus 1) to RR2, setting a bit 3 (Command Complete) of STAT0 to 1. The bit 15 of RR2(H) shows a lookup result, registering either “1” as a hit or “0” as a miss hit.



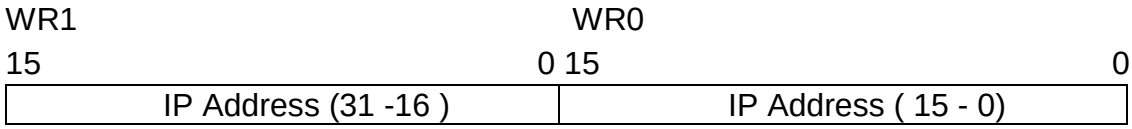


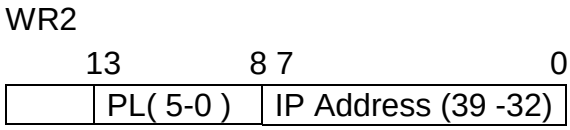


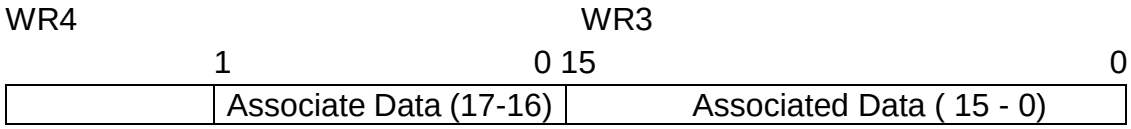


Insert (OP Code: 0002h):

To execute this command, write the entry data (IP address) to WR0-WR2, the associated data to WR3-4, and the PL (Prefix Length minus 1) to WR2. The value of host address part should be all “0”. The execution of this command prompts storing these data to the table. When the insertion is completed, bit3 of STAT0 will be changed to ‘1,’ and CCMPN to Low.

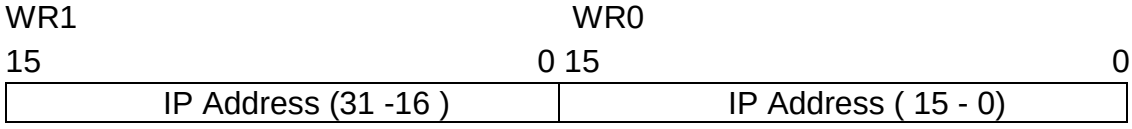


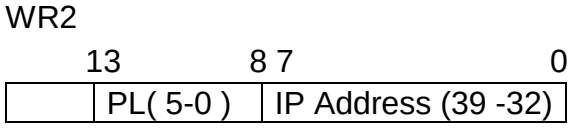




Delete (OP Code: 0003h):

To execute this command, write the entry data (IP address) to WR0-WR2and PL (Prefix Length minus 1) to WR2. The value of host address part should be all “0”. The execution of this command prompts deleting the data from the table. Upon completion of the data deletion, bit3 of STAT0 will be changed to ‘1,’ and CCPMN to Low.





Initialize (OP Code: 0004h):

When this command is executed, the insertion/deletion queue and search table will be cleared. The Entry Counter becomes 0000h.

Upon completion of the command, the CNTL Register, Almost Full Register, and Default Associate Data will maintain their current value, while STAT0 will have the Default. Bit 3 of STAT0 (Command Complete) will be changed to 1, as in using other command, and CCMPN to Low.

Set Almost Full Register (OP Code: 0005h):

The value in WR0 is set to Almost Full Register. Upon completion of the command, bit3 of STAT0 (Command Complete) will be changed to '1,' and CCMPN is changed to Low. When the number of entries is greater than or equal to the Almost Full Register value, AMFLN will be changed to Low with bit1of STAT0 set to '1.' Interrupt is activated when the number of entries is equal to the Almost Full Register value.

WR0

15	0
Almost Full Entry Count (15-0)	

Default Value of Almost Full register is 7FFFh.

Read Almost Full Register (OP Code: 0015h):

The value in Almost Full register is set to RR0.

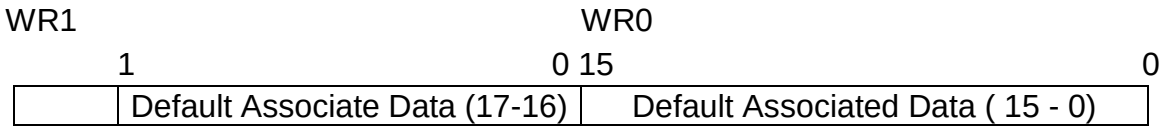
Upon completion of the data setting to RR0, bit3 of STAT0 (Command Complete) is changed to '1,' and CCMPN to Low.

RR0

15	0
Almost Full Entry Count (15-0)	

Set Default Associated Data (OP Code: 0007h):

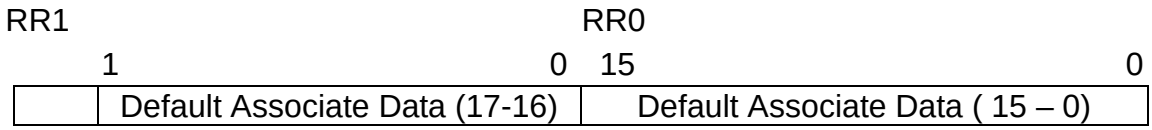
The value in WR0-1 is set as the default associated data, which is output when a miss hit occurs. Upon completion of the data input to the internal register, bit3 of STAT0 will be changed to '1,' and CCMPN to Low.



Read Default Associated Data (OP code: 0017h):

The Default Associate Data is written to RR0-1.

Upon completion of the data setting to RR0-1, bit3 of STAT0 (Command Complete) will be changed to '1,' and CCMPN to Low.



Write SRAM (OP Code: 0008h):

The data in WR2-3 is written to SRAM; in advance, the address of SRAM is specified by the value in WR0-WR1. Upon the completion of the command, bit3 of STAT0 will be changed to ‘1,’ and CCMPN to LOW.

WR1 WR0

1	0	15	0
	SRAM Device ID (17 –16)	SRAM Address (15 – 0)	

00: Reserved
01: SRAM1
10: SRAM2
11: SRAM3

WR2

15	0
SRAM Data (15 – 0)	

WR3

15	0
SRAM Data (31 – 16)	

Read SRAM (OP Code: 0018h):

The data of SRAM is read and written to RR0-1; in advance, the address of DRAM is specified by the value in WR0-WR1. Upon completion of the command, bit3 of STAT0 will be changed to '1,' and CCMPN to Low.

WR1 WR0

1	0	15	0
	SRAM Device ID (17 –16)	SRAM Address (15 – 0)	

00: Reserved
01: SRAM1
10: SRAM2
11: SRAM3

RR0

15	0
SRAM Data(15 – 0)	

RR1

15	0
SRAM Data (31 – 16)	

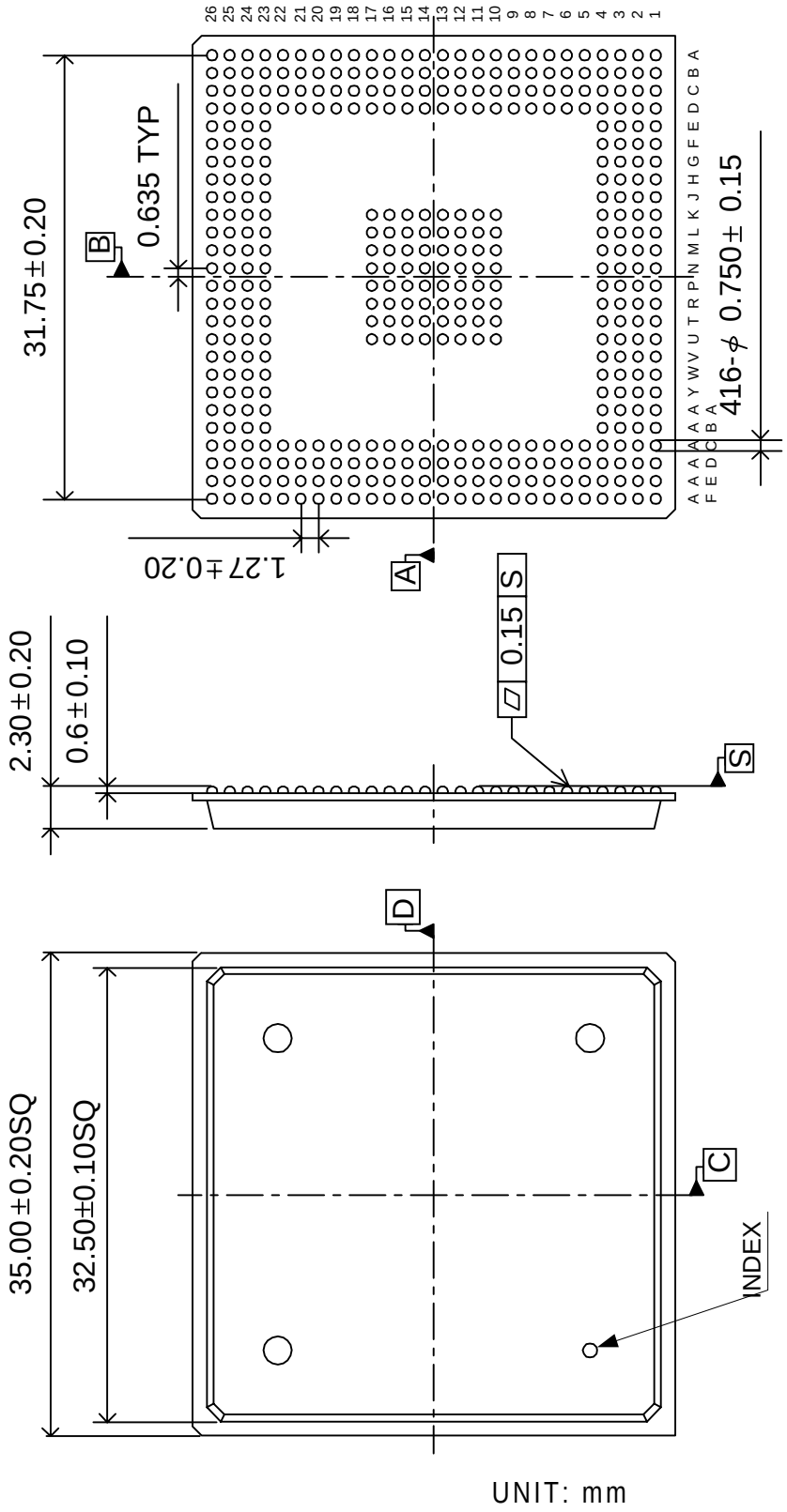
Return Entry Count (OP Code: 001Bh):

The current number of entries in the table is set to RR0.
Upon completion of the data setting to RR0, bit3 of STAT0 will be changed to '1,' and CCMPN to Low.

RR0

15	0
Entry Count (15-0)	

8. Package Outline



9. Electrical Characteristics

9.1. Absolute Maximum Rating

Item	Symbol	Condition	Unit	Note
Supply Voltage	VDD	-0.3 ~ 4.0	V	
Input Voltage	VI	-0.3 ~ VDD+0.3	V	*
Output Voltage	VO	-0.3 ~ VDD+0.3	V	*
I/O Voltage	VIO	-0.3 ~ VDD+0.3	V	*
Storage Temperature	TSTG	-40 ~ +125	°C	

Note: Items with * indicate that Input and Output are NOT 5V tolerant.

9.2. Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	TA	0	+25	+70	°C

9.3. DC Characteristics

Item	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 8mA
Output High Voltage	VOH	2.4			V	IOH = -8mA
Input Leakage Current	IIL	-10			μA	VIN = GND

Output Leakage Current	IIH			10	μA	VIN= -VDD
Output Leakage Current	IOZ	-10		10	μA	High impedance
Standby Current	IDDS			TBD	μA	
Dynamic Operating Current	IDDOP		TBD		mA	

9.4. AC Characteristics

TA = 0~70°C, VDD = 3.3V ± 0.3V

INPUT /OUTPUT Port				
No.	Parameter	Min.	Max.	Unit
1	Clock Cycle Time	15	100	ns
2	CLK High Time	5		ns
3	CLK Low Time	5		ns
4	INP Setup Time to CLK High	4		ns
5	CLK High to INP Hold Time	1		ns
6	SRCHN Setup Time to CLK High	4		ns
7	CLK High to SRCHN Hold Time	1		ns
8	CLK High to OUT Valid	1	15	ns
9	OEN Low to OUT Active	1		ns
10	OEN High to OUT High-Z		10	ns
11	CLK High to ODONEN Low	1	15	ns
12	CLK High to ODONEN High	1	15	ns
13	CLK High to MLE Valid	1	15	ns
14	MLOEN Low to MLE Active	1		ns
15	MLOEN High to MLE High-Z		10	ns
16	CLK High to MDONEN Low	1	15	ns
17	CLK High to MDONEN High	1	15	ns
18	CLK High to HON Valid	1	15	ns

CPU Port				
No.	Parameter	Min.	Max.	Unit
19	ADD Setup Time to CEN Low	8		ns
20	CEN High to ADD Hold Time	3		ns
21	DAT Setup Time to CEN High	8		ns
22	CEN High to DAT Hold Time (Write)	3		ns
23	RWN Setup Time to CEN Low	8		ns
24	CEN High to RWN Hold Time	3		ns
25	CEN Low to DAT Active		22	ns
26	CEN Low to DAT Valid		25	ns
27	CEN High to DAT Hold Time (Read)		1	ns
28	CEN High to CCMPN High		25	ns
29	CLK High to CCMPN Low		25	ns
30	CLK High to FLN Valid		25	ns
31	CLK High to AMFLN Valid		25	ns
32	CLK High to IRQN Low		25	ns
33	CEN Low to IRQN High-Z		4 clks +15	ns
34	CEN Cycle Time	45		ns
35	CEN High Time	15		ns
36	CEN Low Time	30		ns
37	RSTN Low Pulse Width	60		ns
38	RSTN Low to HON High		45	ns
39	RSTN Low to FLN High		45	ns
40	RSTN Low to AMFLN High		45	ns
41	RSTN Low to CCMPN Low		45	ns
42	RSTN Low to IRQN High-Z		45	ns
43	RSTN Low to ODONEN High		45	ns
44	RSTN Low to MDONEN High		45	ns
45	CEN Low to HON High (Reset Reg.)		45	ns
46	CEN Low to FLN High (Reset Reg.)		45	ns
47	CEN Low to AMFLN High (Reset Reg.)		45	ns
48	CEN Low to CCMPN Low (Reset Reg.)		45	ns
49	CEN Low to IRQN High-Z (Reset Reg.)		45	ns
50	CEN Low to ODONEN High (Reset Reg.)		45	ns
51	CEN Low to MDONEN High (Reset Reg.)		45	ns

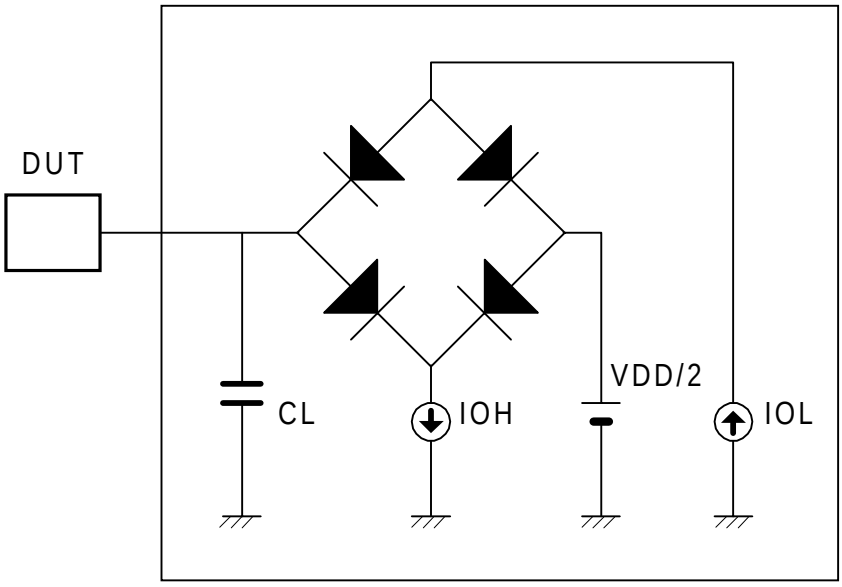
SRAM Port				
No.	Parameter	Min.	Max.	Unit
52*	CLK High to SRAM Control Signal Valid		11	ns
53*	CLK High to SRAM Control Signal Hold Time	2		ns
54*	SRAM Data Setup Time to CLK High	4		ns
55*	CLK High to SRAM Data Hold Time	0.5		ns

Misc			
No.	Parameter		Unit
56	SRCHN Low to SRCHN Low	10N or 40+M N=1,2,3,4 M=1,2,3,....	cycles

Note: Characteristics are measured under the following conditions.
*: In case of No.52, 53, 54, 55 of AC Caracteristics

Input "H" level	3.3V
Input "L" level	0.0V
Input reference voltage	1.5V
Input signal through rate	1.0ns/V
Output judgment level	Vdd/2
Logical capacitance(CL)	50pF(20pF*)
"H" level output loading current(IOH)	-8mA
"L" level output loading current(IOL)	8mA

Test Loads



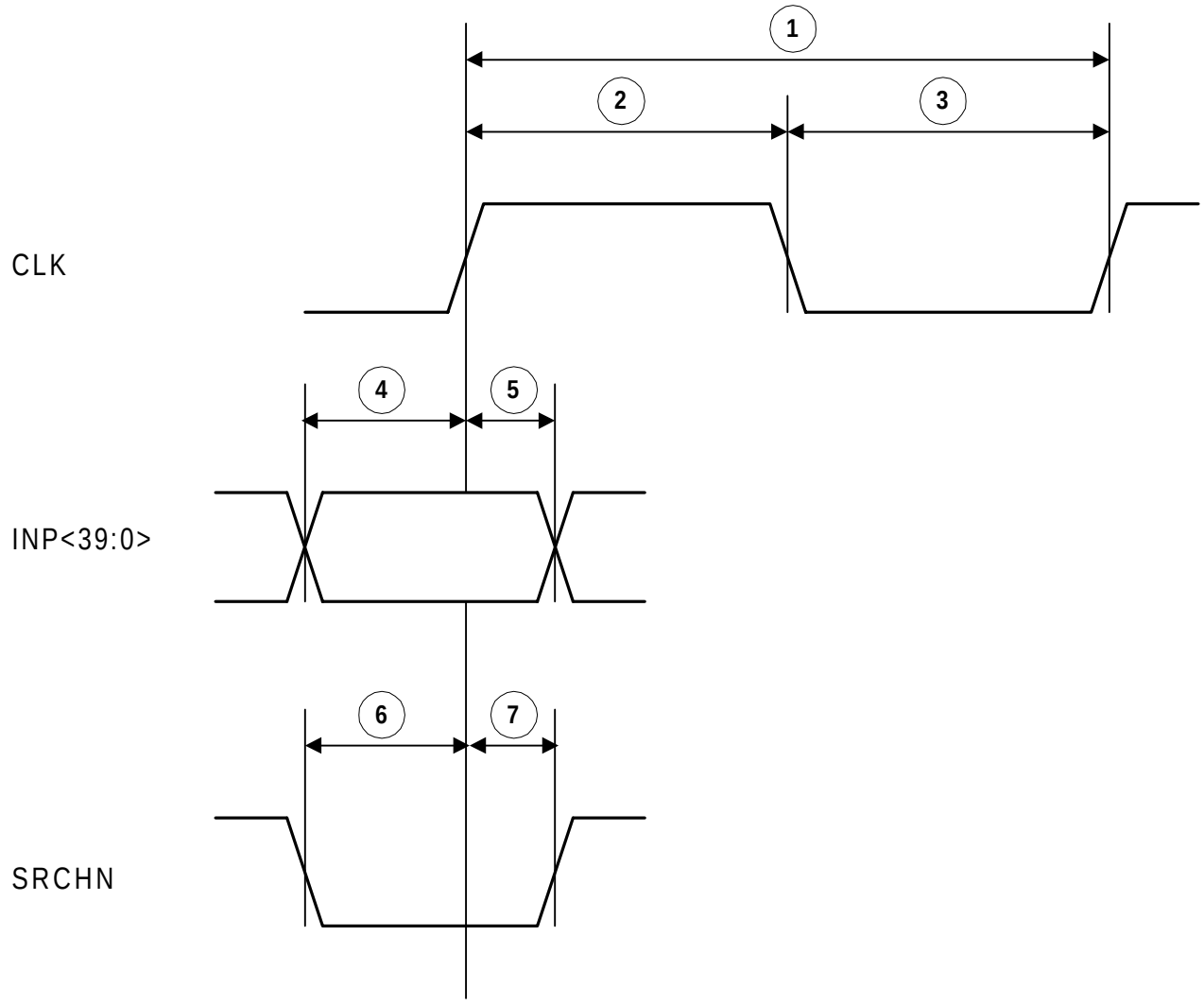


Fig. 9.1 Input Port Timing

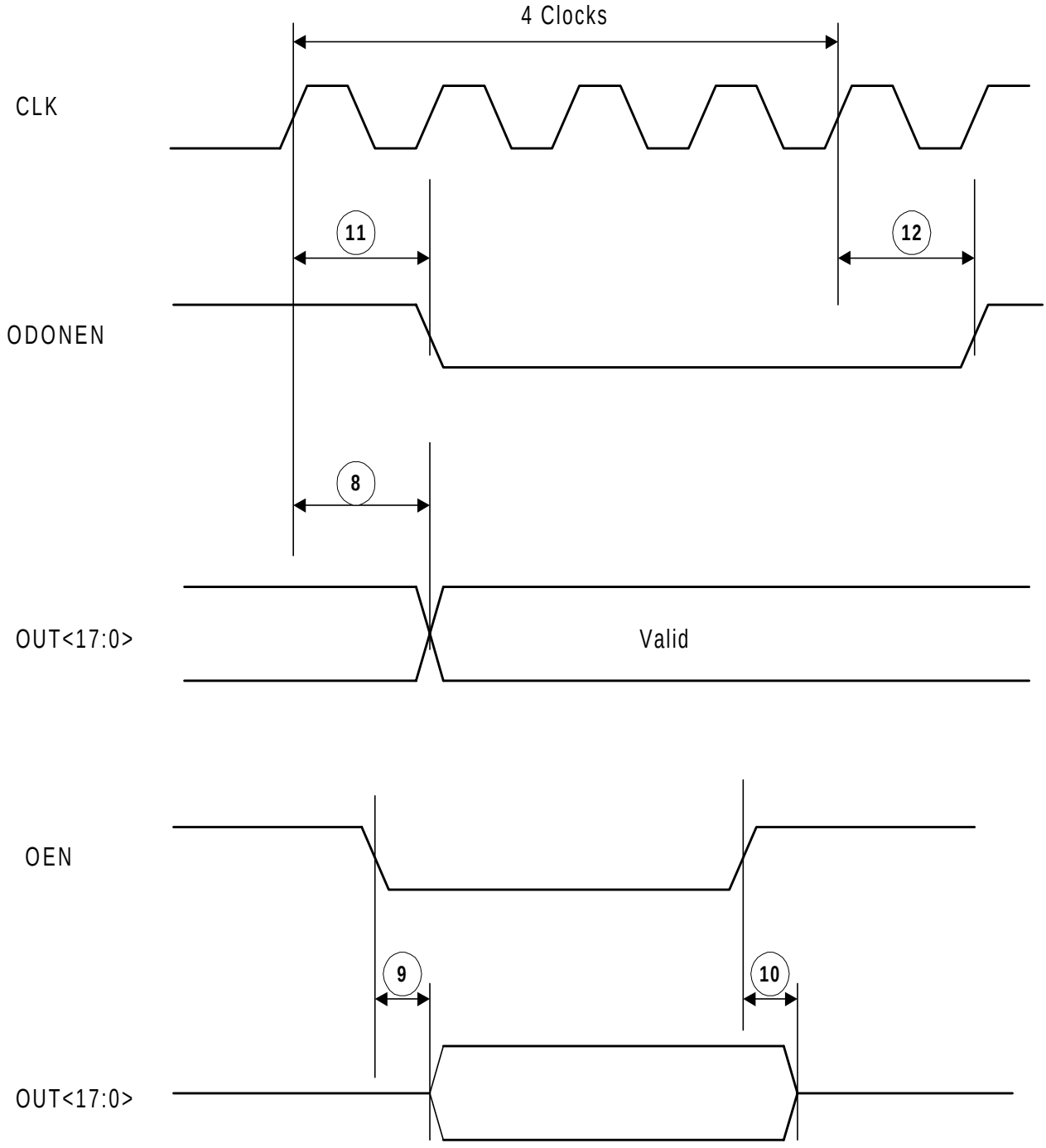


Fig.9.2 Output Port Timing (1)

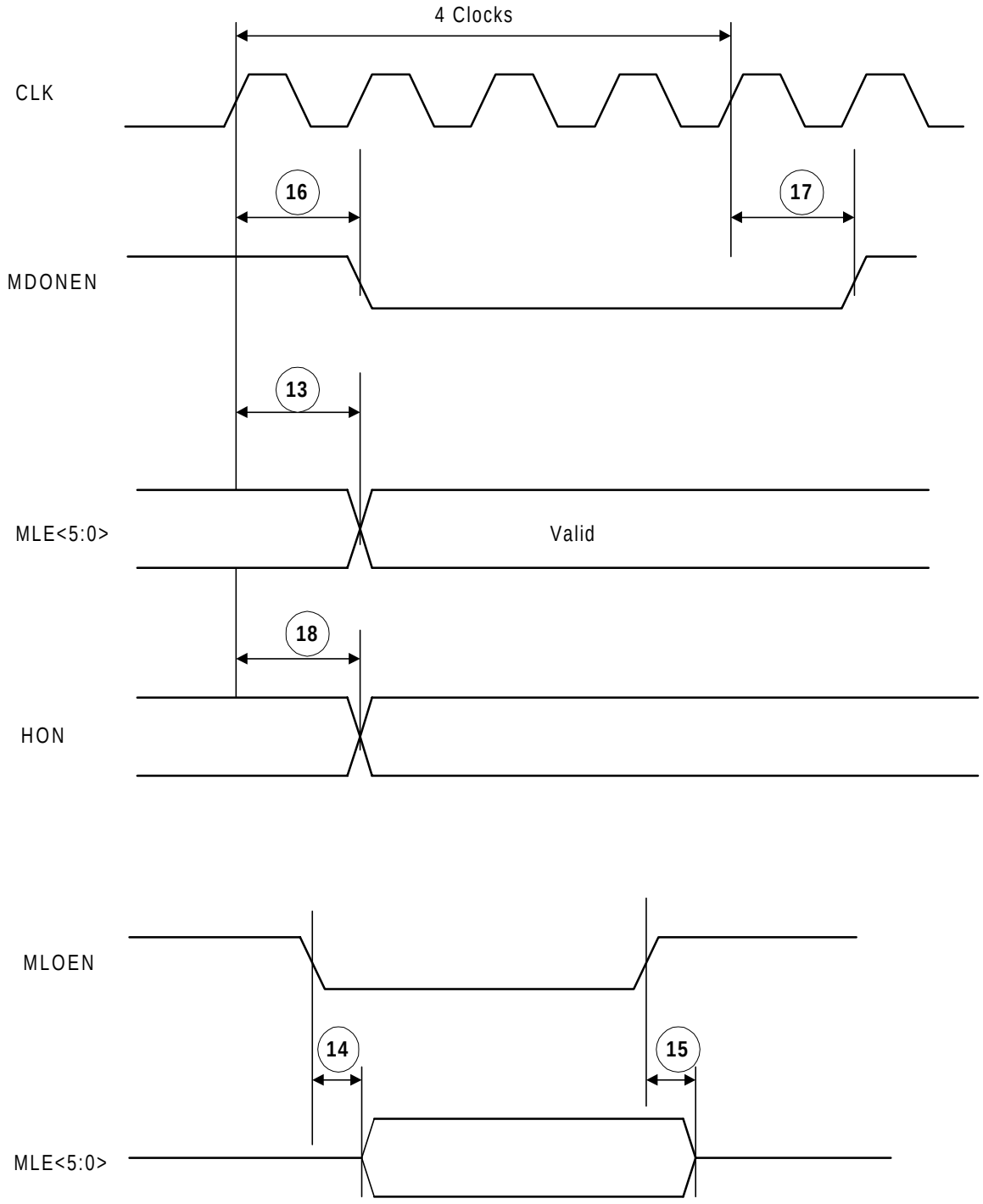


Fig. 9.3 Output Port Timing (2)

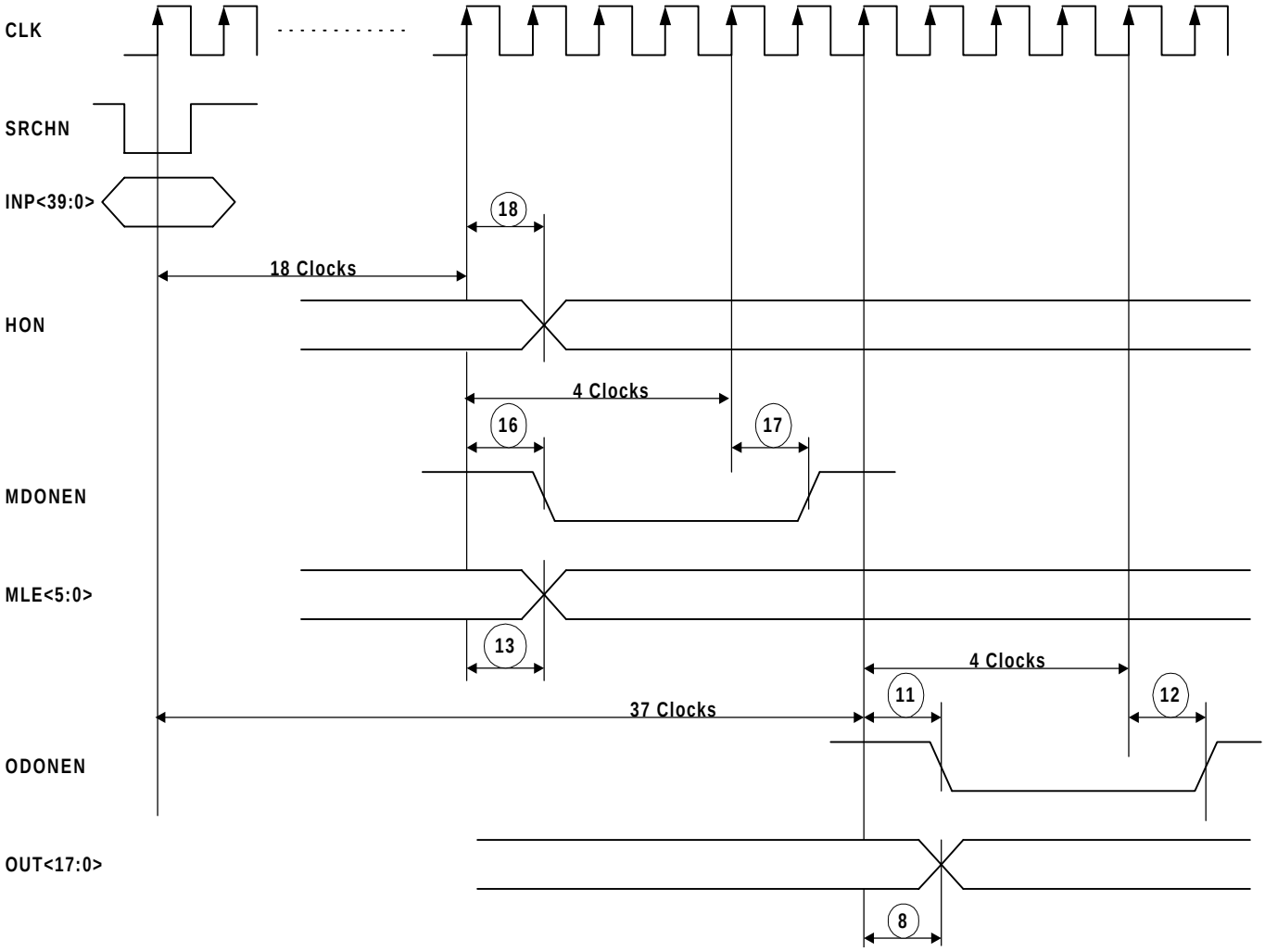


Fig.9.4 Search Timing

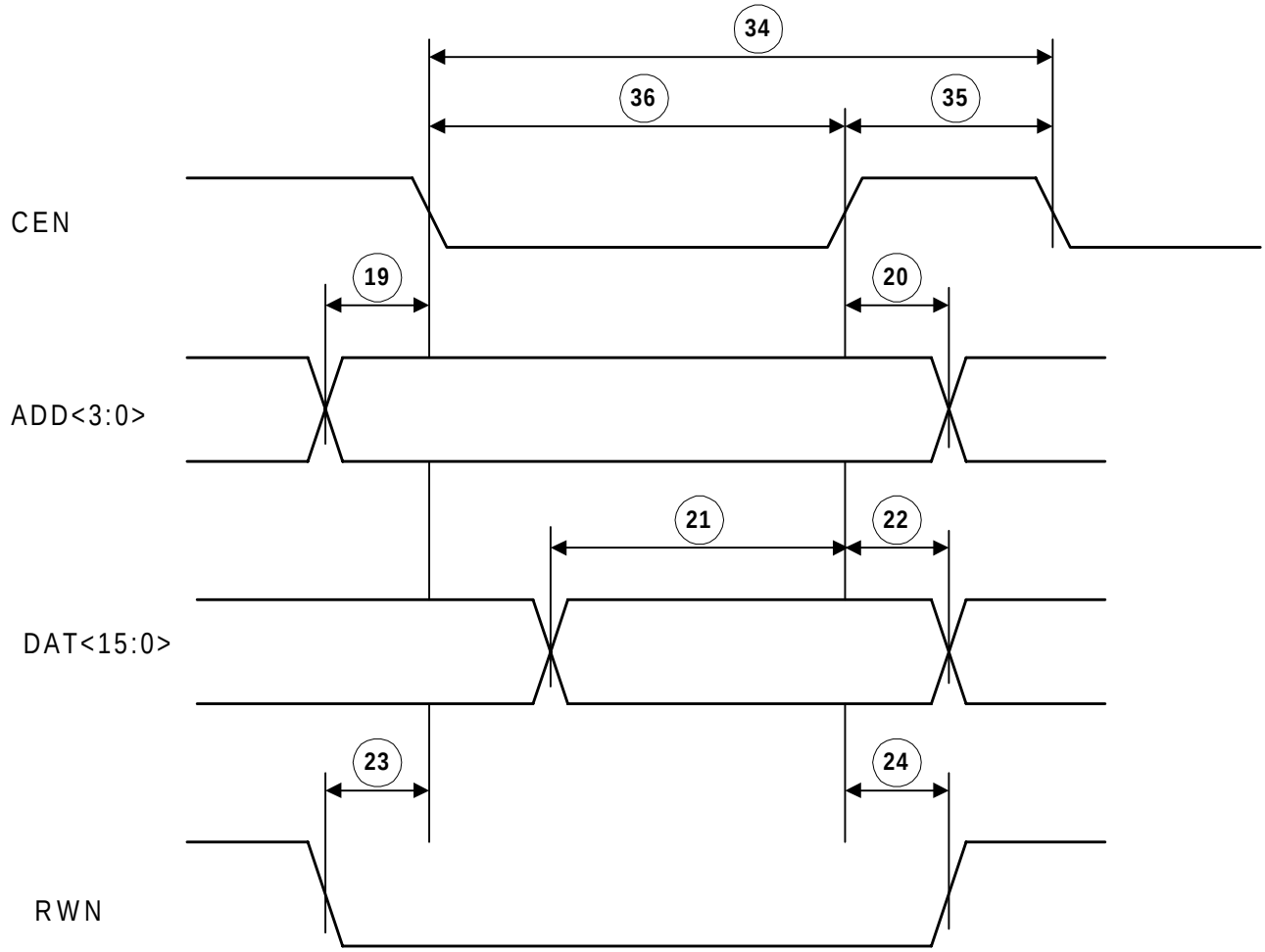


Fig. 9.5 CPU Port Write Timing

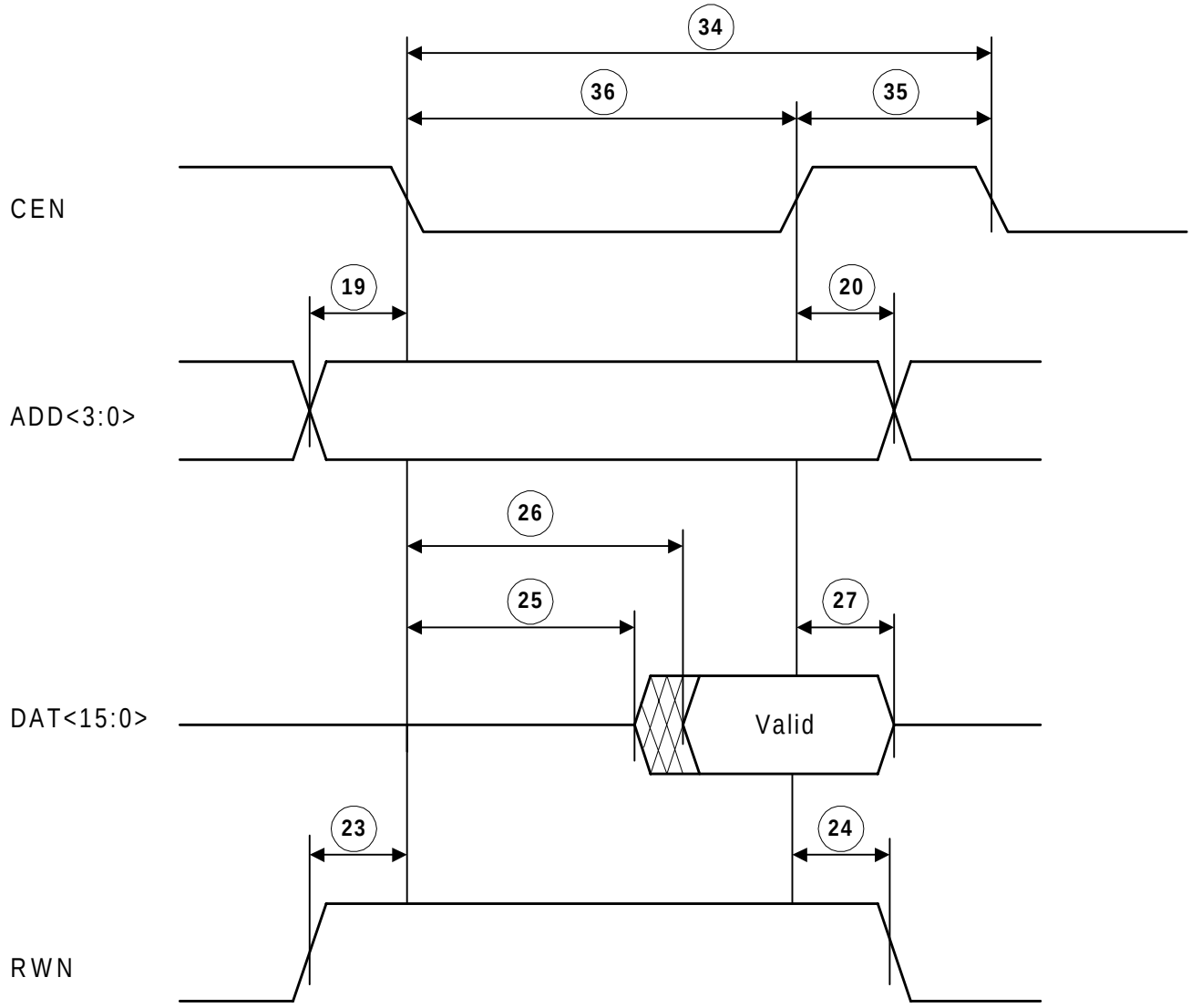


Fig. 9.6 CPU Port Read Timing

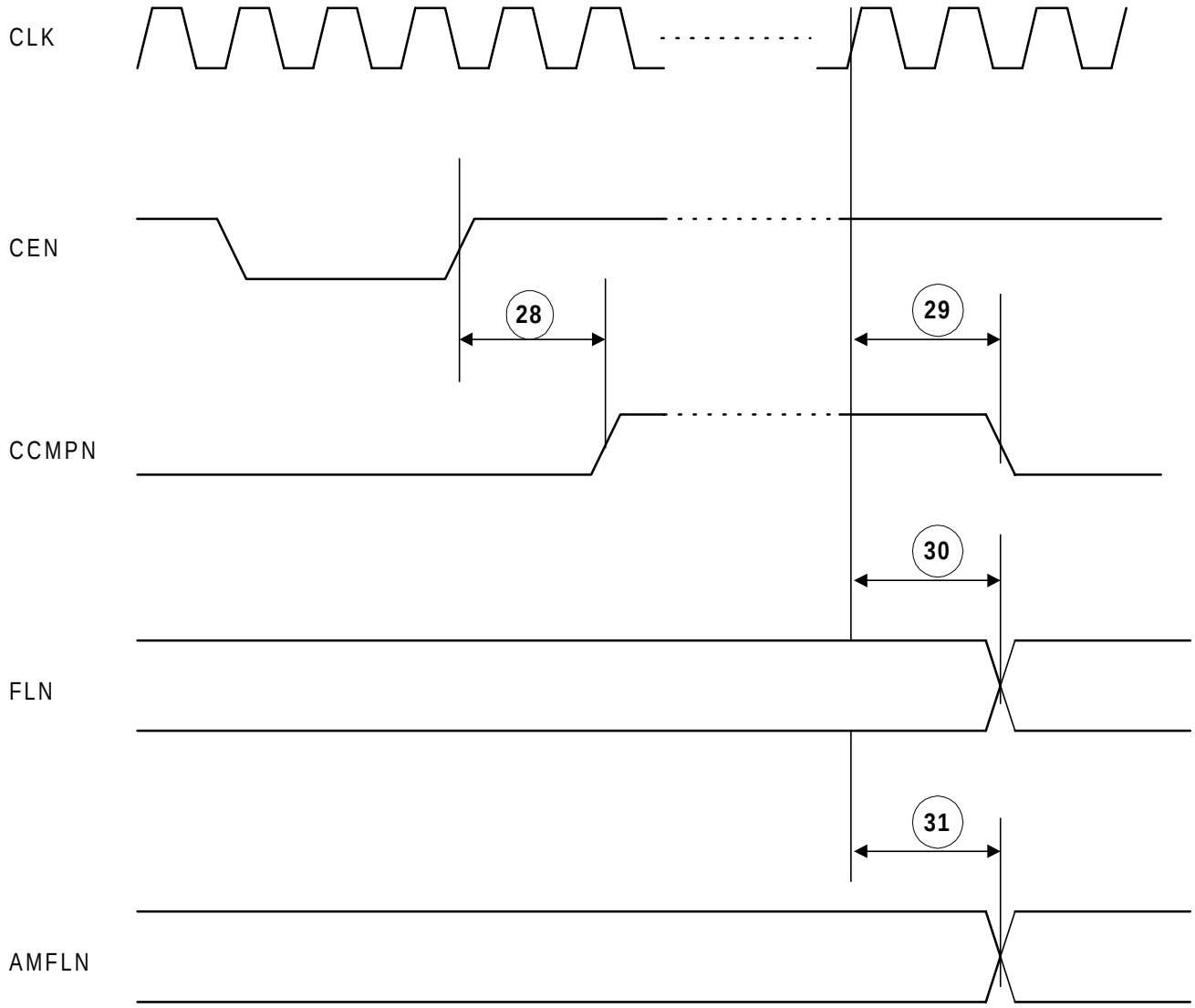


Fig. 9.7 CPU Port Timing (1)

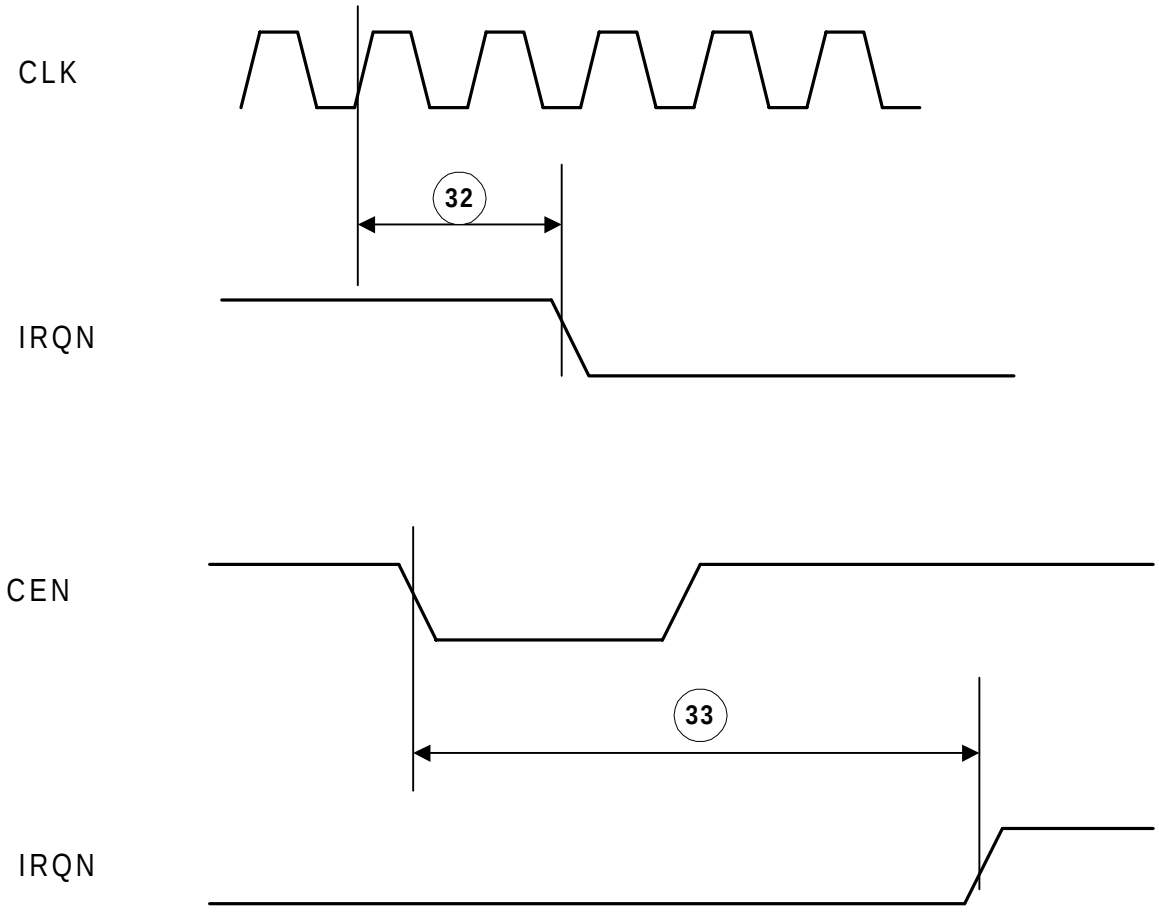


Fig. 9.8 CPU Port Timing (2)

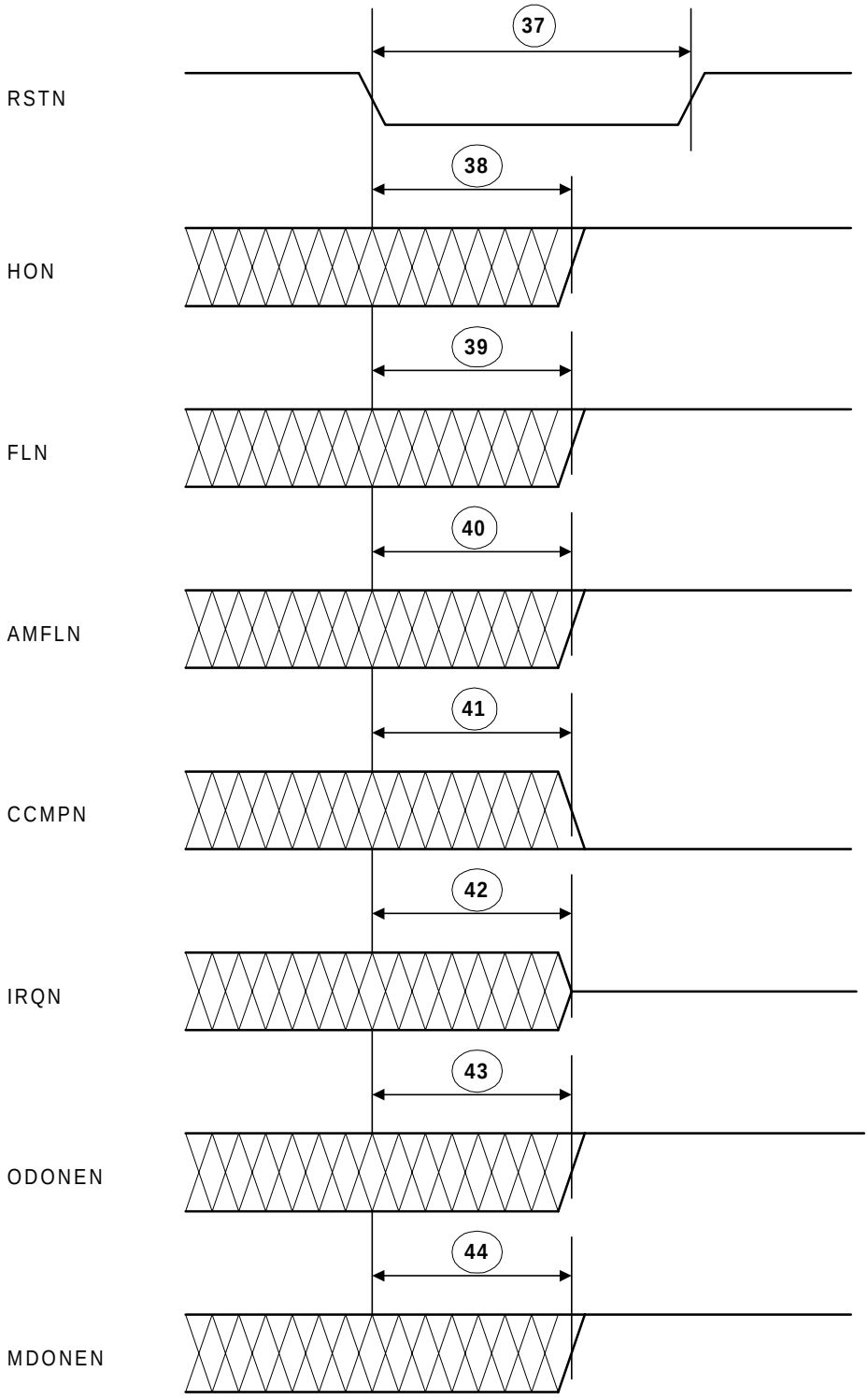


Fig. 9.9 Reset Timing via RSTN Pin

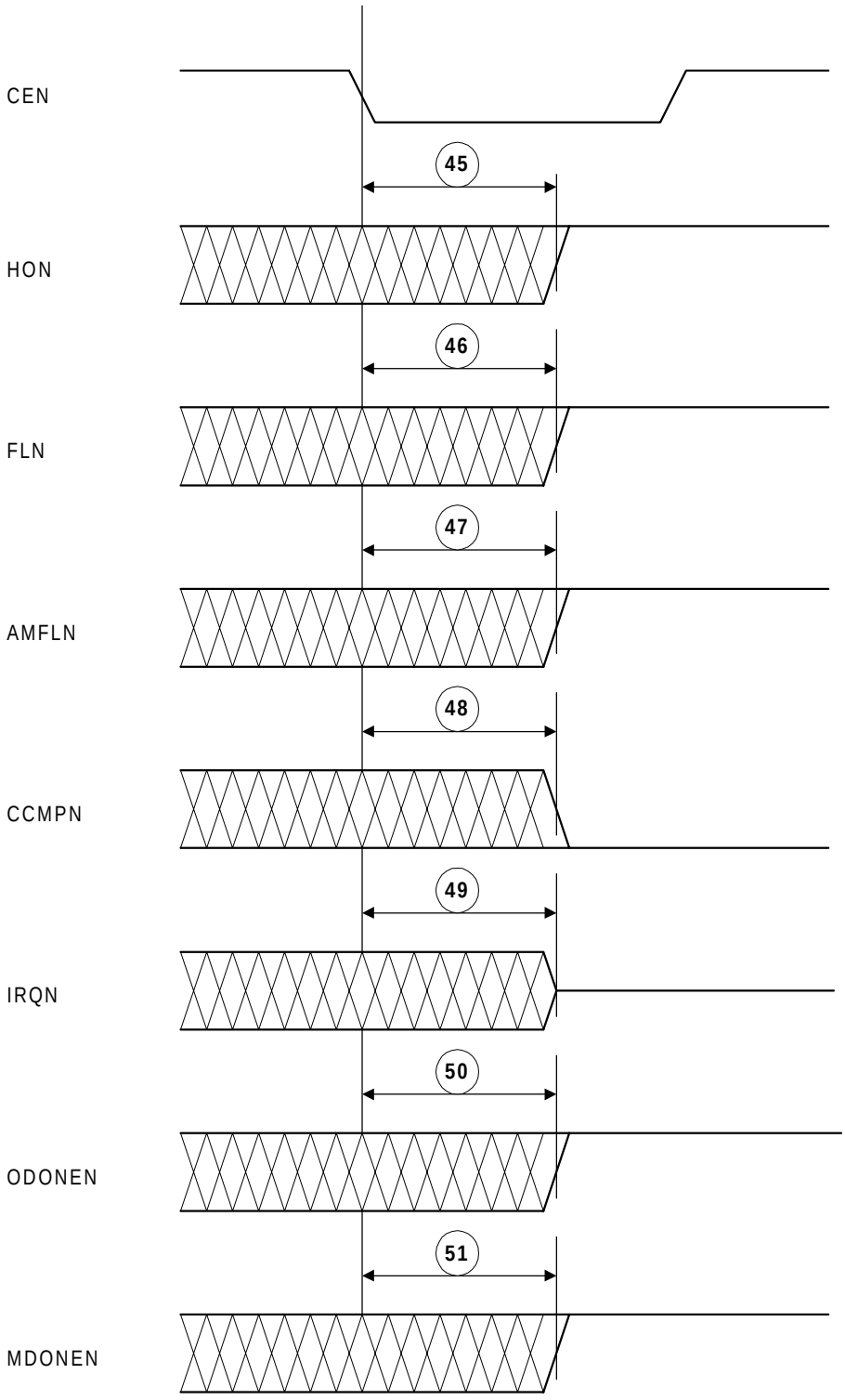


Fig. 9.10 Reset Timing via Reset Register

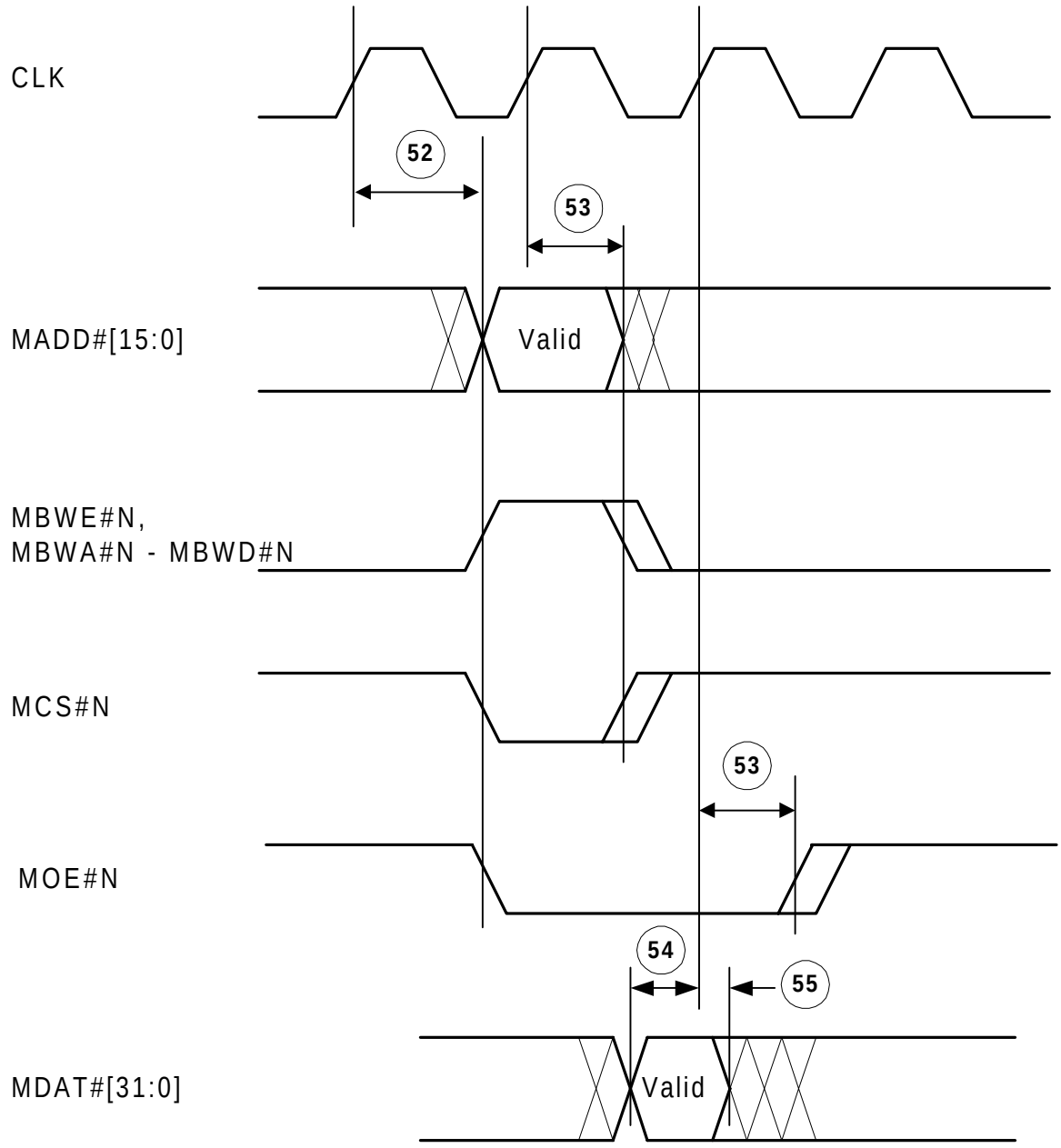


Fig. 9.11 SRAM Read Timing

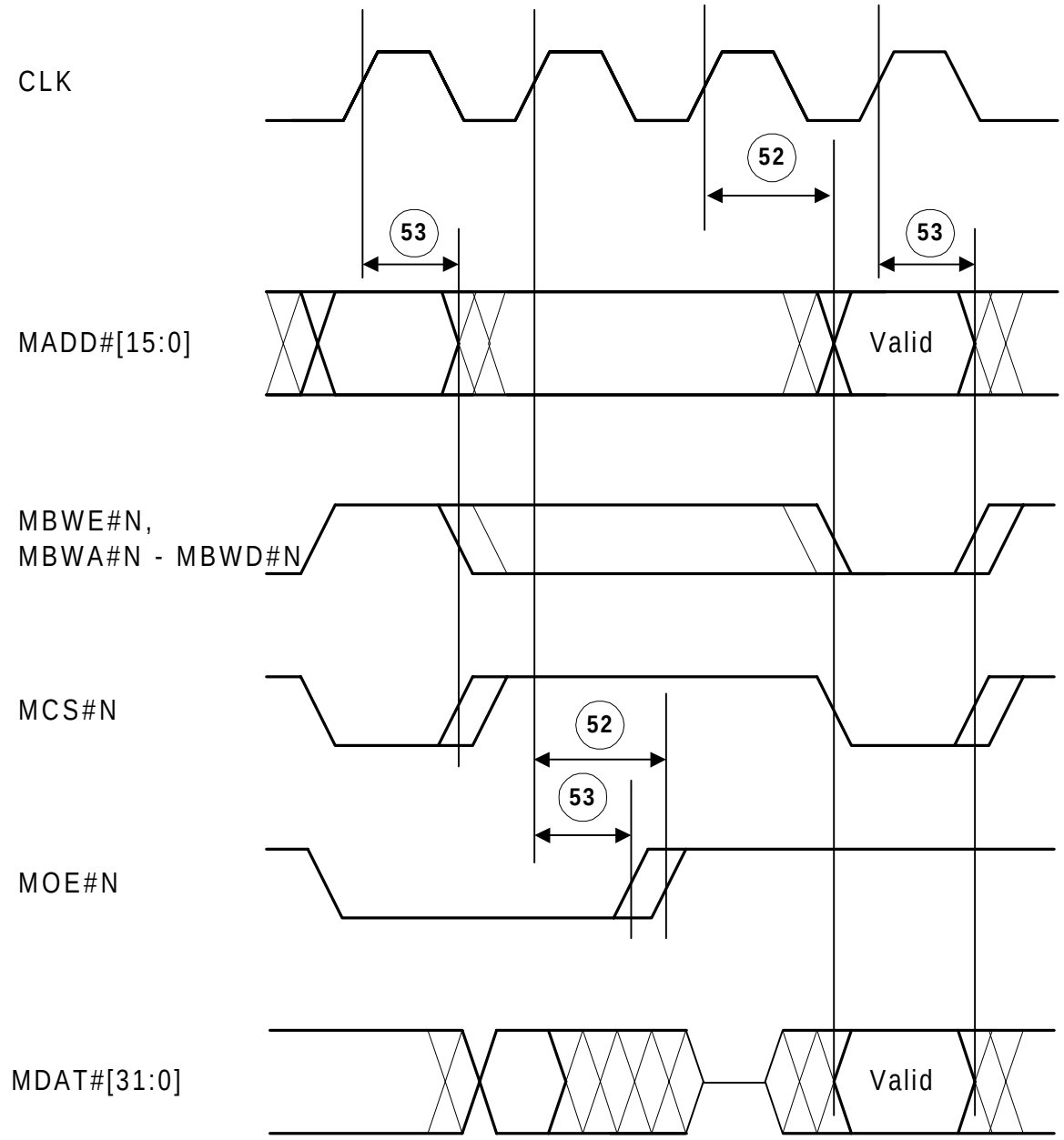


Fig. 9.12 SRAM Write Timing

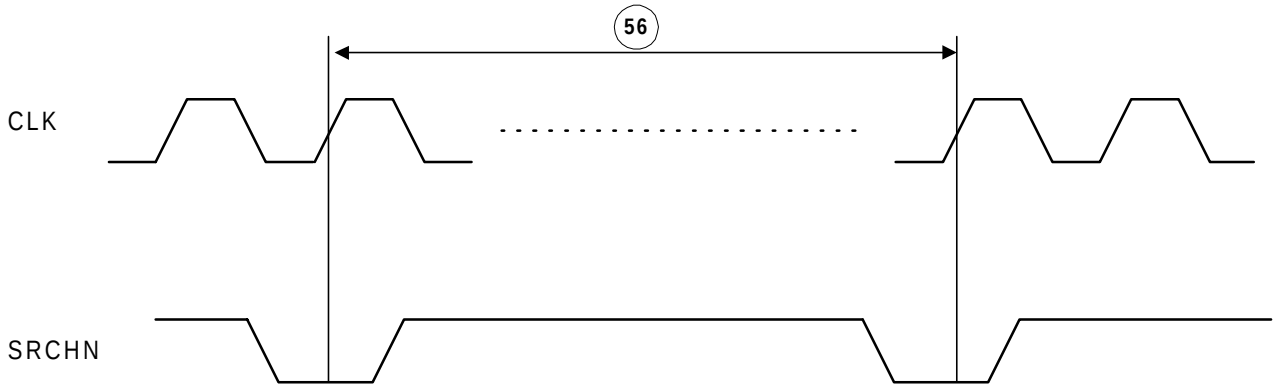


Fig. 9.13 Minimum Search Period

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