RoHS compliant

## Features

- Increases proximity detection range of E909.05/E909.06 by a factor of 5 (*)
- Improves signal to noise ratio by a factor of 3
- Optical receiver with high sensitivity (limiting output): total transimpedance typ. 422MΩ
- Integrated op-amp for buffering, gain or additional active filtering
- Very low phase shift in input overdrive
- High ambient light suppression up to photo currents of 10mA
- Signal bandwidth up to 500kHz
- No current consumption in standby mode
- Automotive qualified according to AEC-Q100

*(*) in systems with highly focused IR beams and optimized optical sensor surfaces*

## Applications

- Optical receivers
- Transimpedance amplifiers
- Multiplex function for channel expander of the chip set E909.05/E909.06

## General Description

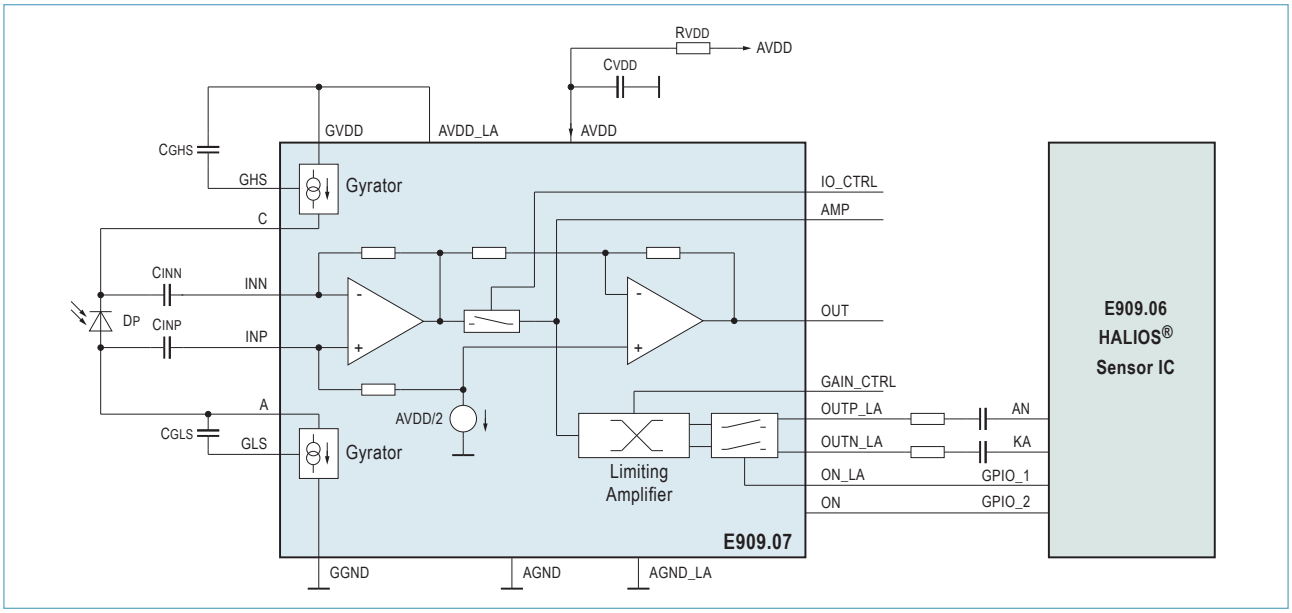
The optical receiver device consists of a first stage transimpedance amplifier (TIA) with differential input, limiting amplifiers with integrated high pass filter characteristics and differential outputs OUTP_LA / OUTN_LA and a secondary linear output OUT.

A very high sensitivity equivalent to a transimpedance resistance of typ. 422MΩ is achieved at the limiting outputs. By using a limiting amplifier no phase shift occurs if the input is overdriven. Ambient light equivalent to a constant photo current up to 10mA is suppressed with an integrated gyrator.

Together with the HALIOS® chip set E909.05/E909.06 motion detectors a detection range of several meters can be realized. By switching the output to high impedance state several optical receivers can be multiplexed to the input of a HALIOS® multi-purpose sensor IC E909.05/E909.06.

## Ordering Information

| Ordering No.: | Temp. Range$_{Amb}$ | Package |
|---|---|---|
| E90907A52C | -40°C to +105°C | QFN20L4 |



# 1 Package and Pinout

## 1.1 Pin Description

| *No* | *Name* | *Type* | *Description* |
|---|---|---|---|
| 1 | INN | A_I | Negative input of transimpedance amplifier (TIA) |
| 2 | INP | A_I | Positive input of transimpedance amplifier (TIA) |
| 3 | A | A_IO | Anode of photodiode connected to high side gyrator |
| 4 | GLS | A_IO | Low pass frequency control (to GGND) |
| 5 | GHS | A_IO | High pass frequency control (to GVDD) |
| 6 | GVDD | S | Supply gyrator |
| 7 | GGND | S | Ground gyrator |
| 8 | AMP | A_IO | Output of TIA or input of limiting amplifier (LA) controlled by IO_CTRL |
| 9 | GAIN_CTRL | D_I | Controls gain of LA, integrated pull down |
| 10 | ON_LA | D_I | Enabling output of LA , active Hi, integrated pull-down |
| 11 | OUTP_LA | A_O | Positive output limiting amplifier |
| 12 | OUTN_LA | A_O | Negative output limiting amplifier |
| 13 | ON | D_I | Activation signal for amplifier-IC, active Hi, integrated pull-down |
| 14 | OUT | A_O | Output of OPAMP |
| 15 | AVDD_LA | S | Supply limiting amplifier (LA) |
| 16 | AGND_LA | S | Ground limiting amplifier (LA) |
| 17 | IO_CTRL | D_I | Controls the input of the limiting amplifier, integrated pull down |
| 18 | AVDD | S | Supply transimpedance amplifier (TIA) and inverting amplifier |
| 19 | AGND | S | Analogue ground |
| 20 | C | A_IO | Cathode of photodiode connected to low side gyrator |
| 21 | EP | S | Exposed Die Pad |

**Table 1: Pin Description**

Explanation of Types:
A = Analogue, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

When connecting the supply pins the requirements of the entire system has to be taken into account.
For highest sensitive it is recommended to use a separate RC filter for every supply input.
The ground pins GGND, AGND_LA and AGND must be soldered together in any application!

Pin EP, IO_CTRL and GAIN_CTRL must be soldered to Ground or VDD. See Chapter 5.7

## 1.2 Package Reference

The device is available in a Pb free, RoHS compliant, 20-lead Quad Flat No Lead QFN20L4 package with 16mm² (0.024 square inch) according to JEDEC standard MO-220- K ; Variant: VGGD-5.

## 1.3 Package Pinout

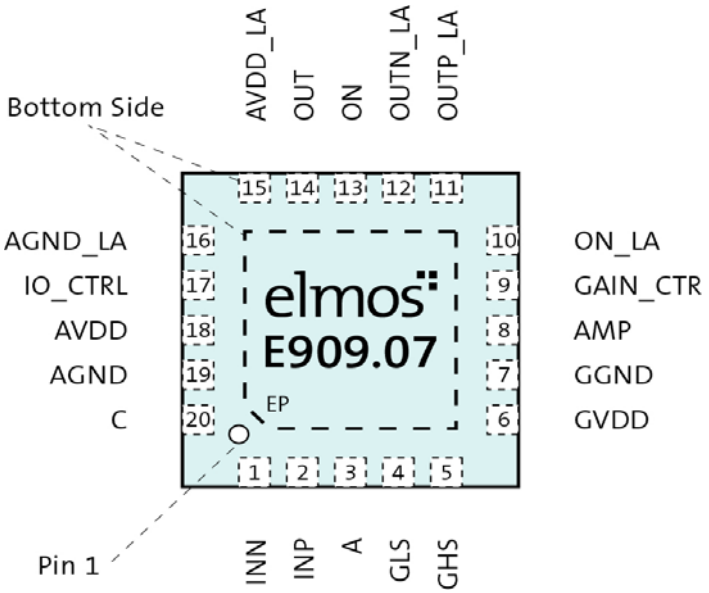



**Fig. 2: Package Pinout E909.07 (Top View)**

# 2 Block Diagram

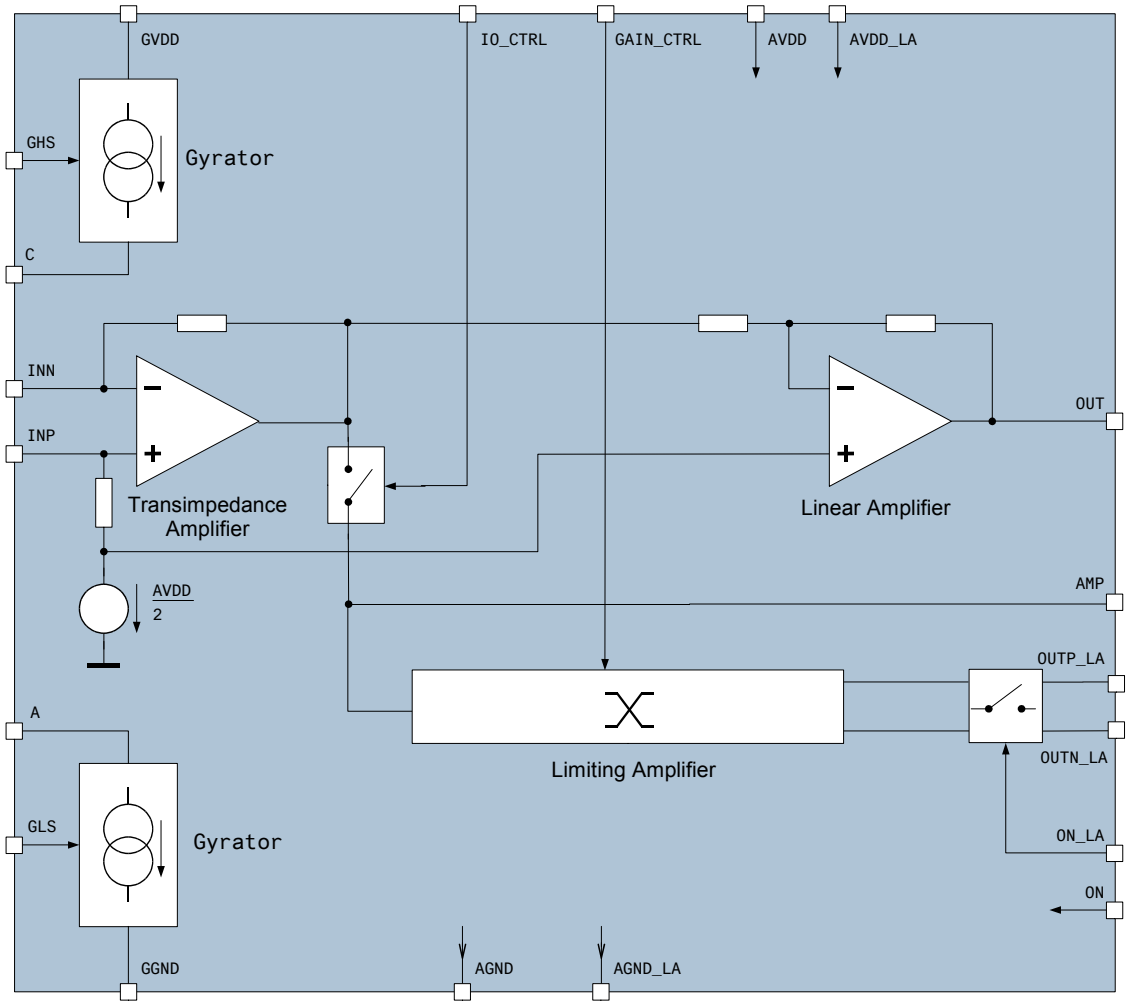



**Fig. 3: Block Diagram E909.07**

# 3 Operating Conditions

## 3.1 Absolute Maximum Ratings

- Operating the device at or beyond these limits may cause permanent damage.
- All voltages are referred to ground (0V).
- Currents flowing into the circuit have positive values.

| *No.* | *Description* | *Condition* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|---|---|
| 1 | Negative supply voltage | | AGND, GGND, AGND_LA | 0 | 0 | V |
| 2 | Positive supply voltage | | AVDD, GVDD, AVDD_LA | -0,3 | +3,6 | V |
| 3 | Voltage digital I/O pins: ON, ON_LA, IO_CTRL, GAIN_CTRL | | V(DPIN) | -0,3 | AVDD + 0,3 | V |
| 4 | Input current at digital pins: ON_LA, IO_CTRL, GAIN_CTRL | | I(DPIN) | -10 | 10 | mA |
| 5 | Voltage at analogue pins | | V(APIN) | -0,3 | AVDD + 0,3 | V |
| 6 | Input current at analogue pins | | I(APIN) | -100 | 100 | mA |
| 7 | Junction temperature | | $T_J$ | -40 | +125 | °C |
| 8 | Ambient temperature | packaged devices | $T_A$ | -40 | +105 | °C |
| 9 | Storage temperature | | $T_{STG}$ | -40 | +150 | °C |
| 10 | Power dissipation | $T_A \leq 85°C$ | $P_{TOT}$ | | 150 | mW |

**Table 2: Absolute Maximum Ratings**

## 3.2 Recommended Operating Conditions

- Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
- All voltages are referred to
- ground (0V).
- Currents flowing into the circuit have positive values.

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Positive supply voltage | | AVDD, GVDD | 3.0 | 3.3 | 3.5 | V |
| 2 | VDD filter and buffer capacitor | Low-ESR type | $C_{VDD}$ | 10 | | | µF |
| 3 | Input coupling capacitors | $C_{INN} = C_{INP}$ | $C_{INN}$, $C_{INP}$ | 0.22 | 0.47 | 10 | nF |
| 4 | Gyrator coupling capacitors | $C_{GLS} = C_{GHS}$ | $C_{GLS}$, $C_{GHS}$ | 10 | 47 | 220 | nF |
| 5 | Capacitive load at output OUT | | $C_{LOAD, OUT}$ | | | 100 | pF |
| 6 | Capacitive load at output AMP | | $C_{LOAD, AMP}$ | | | 100 | pF |
| 7 | Capacitive load at Pin OUTP_LA, OUTN_LA | | $C_{LOAD, OUTx\_LA}$ | | | 100 | pF |
| 8 | Junction Temperature | normal operation | $T_J$ | -40 | | +105 | °C |
| 9 | Thermal resistance, junction to ambient | QFN20L4 | $R_{T,J-A}$ | | 45 | | °C/W |
| 10 | VDD Filter resistor | | $R_{VDD}$ | | 10 | 20 | Ω |
| 11 | Capacitance of photo diode at input C / A | | $C_{DIODE}$ | | 70 | 250 | pF |

**Table 3: Recommended Operating Conditions**

# 4 Detailed Electrical Specification

## 4.1 Supply

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Supply current [1), 2)] | ON = AVDD, ON_LA = AVDD, $I_C = I_A$ = 0mA, | $I_{VDD}$ | | 3.5 | 5.0 | mA |
| 2 | Average supply current [1), 3), 4)] | ON = AVDD, ON_LA = AVDD, $I_C = I_A$ = 0mA, | $I_{VDD,AV}$ | | 0.23 | | mA |
| 3 | Sleep Mode supply current [1), 2)] | ON = 0V, ON_LA = 0V, | $I_{VDD,SLEEP}$ | | | 1 | µA |

**Table 4: Electrical Parameters Supply**

1) Average current from photodiode PD negligible
2) Total supply current to AVDD, AVDD_LA and GVDD
$I_{VDD} = I_{AVDD} + I_{AVDD\_LA} + I_{GVDD}$
3) Power Consumption Calculation
Sample Rate: 10ms
Settling time $T_{SW}$ : 500µs
Measurement time: 250µs
Duty cycle: (500µs + 250µs)/10ms ~ 1/13
$I_{VDD,AV}$ = 5mA * duty cycle ~ 385µA
4) Not tested in production test

## 4.2 Transimpedance Amplifier

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Internal feedback resistance of TIA | Measured from INN to AMP | $R_{TIA}$ | 75 | 100 | 125 | kΩ |
| 2 | Input impedance INP | | $R_{INP}$ | 75 | 100 | 125 | kΩ |
| 3 | Maximum output voltage (TIA drive capability) | $I_{AMP}$ = -500µA AVDD=3.3V | $V_{AMP, max}$ | 2.8 | | | V |
| 4 | Minimum output voltage (TIA drive capability) | $I_{AMP}$ = +500µA | $V_{AMP, min}$ | | | 0.5 | V |
| 5 | Common Mode Rejection Rate $\Delta_{VOUT\_TIA\_cm}$ / $\Delta V_{OUT\_TIA\_dm}$ | @22kHz | CMRR | | 80 | | dB |
| 6 | Internal feedback capacitor of transimpedance amplifier [1)] | | Cf | | 2.25 | | pF |
| 7 | -3dB Corner frequency TIA | | $f_{CS}$ | | 600 | | kHz |

**Table 5: Electrical Parameters Transimpedance Amplifier**

## 4.3 Gyrator

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Voltage drop at low-side gyrator input (A) | $I_A$ = 10mA | $V_A$ - $V_{GGIND}$ | 0.75 | 1.0 | 1.25 | V |
| 2 | Voltage drop at high-side gyrator input (C) | $I_C$ = -10mA | $V_{GVDD}$ - $V_C$ | 0.75 | 1.0 | 1.25 | V |
| 3 | Max. photo current | | $I_{Photo}$ | 10 | | | mA |

**Table 6: Electrical Parameter Gyrator**

## 4.4 Linear Amplifier

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Gain linear amplifier | | $G_{0, lin}$ | | -10 | | V / V |
| 2 | Maximum output voltage | $I_{LIN}$ = -500µA AVDD = 3.3V | $V_{LIN,max}$ | 2.3 | | | V |
| 3 | Minimum output voltage | $I_{LIN}$ = +500µA | $V_{LIN,min}$ | | | 1.0 | V |
| 4 | -3dB Corner frequency | | $f_{CS}$ | | 600 | | kHz |

**Table 7: Electrical Parameters Linear Amplifier**

1) Not tested in production test

## 4.5 High pass filter and limiting amplifier

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Differential gain $A_{VOUT\_LA}$= (OUTP_LA - OUTN_LA) / AMP | GAIN_CTRL = 0 | $AV_{OUTL0}$ | | ($AV_{OUTL1}$)[2] | | V / V |
| 2 | Differential gain $A_{VOUT\_LA}$= (OUTP_LA - OUTN_LA) / AMP | GAIN_CTRL = 1 | $AV_{OUTL1}$ | | 65 | | V / V |
| 3 | Maximum output voltage [2] | $I_{OUTP\_LA}$ = -10µA | $V_{OUTP\_LA,max}$ | | AVDD - 0.1 | | V |
| 4 | Minimum output voltage [2] | $I_{OUTP\_LA}$ = -10µA | $V_{OUTP\_LA,min}$ | | AVDD - 1.1 | | V |
| 5 | Single ended output resistance [1) 2)] | | $R_{OUTN\_LA}$ | | 1.5 | | kΩ |
| 6 | -3dB Corner frequency high pass filter[1)] | | $f_G$ | | 15 | | kHz |
| 7 | Overall gain (TIA +LA) [1)] | GAIN_CTRL=0 IO_CTRL = 0 | G | | $R_{TIA}$* $AV_{OUTL0}$ | | MΩ |

**Table 8: Electrical Parameter High pass filter and limiting amplifier**

## 4.6 Digital Control Inputs

| No. | Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Input low level (Pin ON, ON_LA) | | $V_{IL}$ | | | 0.8 | V |
| 2 | Input high level (Pin ON, ON_LA) | | $V_{IH}$ | AVDD-0.8 | | | V |
| 3 | Settling time after switching on the limiting amplifier[1)] | ON_LA="0" ⟶ "1" | $T_{SON}$ | | 1 | | µs |
| 4 | Settling time after switching from sleep to operating mode[1)] | | $T_{SW}$ | | 500 | | µs |
| 5 | Pull down resistor [1)] | | $R_{PD}$ | | 800 | 1600 | kΩ |

**Table 9: Electrical Parameters Digital Control Inputs**

1) Not tested in production test
2) For proper operation, the output pins OUTN_LA & OUTP_LA must be decoupled with capacitors close to the E909.07. The load at these output pins shall be a load against ground.

# 5 Functional Description

## 5.1 Brief Functional Description

The E909.07 is transimpedance amplifier with high amplification. The differential inputs INN, INP and the differential limiting outputs OUTP_LA, OUTN_LA are forming the main signal path. Within the application field of optical receiver systems it uses a photodiode as input signal source. The differential outputs are designed for use in HALIOS® optical detector systems. The total transimpedance figure in this path is 200MΩ minimum.

Together with the HALIOS® chip set E909.05/ E909.06 motion detectors with a detection range of several meters can be realized. By switching the output to high impedance state several optical receivers for multiple input channels can be multiplexed to one input of a HALIOS® sensor IC E909.05/E909.06, which enables a very economical construction of multi sensor systems with multiple optical detector nodes. These can be operated at minimum power consumption by use of the SLEEP-mode feature of the E909.07 (controlled by pin ON)

## 5.2 Supply

The input GVDD, AVDD should be low pass filtered to increase ambient light suppression and EMC robustness.

## 5.3 Transimpedance Amplifier

The current input signal from an external differential source connected between INN and INP - typically a photodiode - is amplified in a first stage transimpedance amplifier (TIA) with a typical transimpedance figure of 100kΩ. The input photodiode has to be AC-coupled to the inputs by capacitors ($C_{INN}$ , $C_{INP}$). The output of this TIA-stage is accessible at terminal AMP.

In order to achieve a good suppression of common mode disturbances at the pins C and A, the AC coupling capacitors $C_{INN}$, $C_{INP}$ should have a very good matching.

## 5.4 Gyrator

Gyrator input stages at nodes C (cathode) and A (anode) are used to define the input operating point of the input photo diode properly. These gyrators are designed for a maximum DC current of 10mA (photo current) which corresponds to a very high level of ambient light applied to the photo diode. When the device is switched off (ON = 0) the gyrator is also switched off.

## 5.5 Linear Amplifier

Additionally to the limiting amplifier output an inverting amplifier output with an amplification factor of typ. -10 (20dB) is available and can be routed into the signal path. This results in a total transimpedance of typ. 2MΩ at OUT with respect to the input of the TIA.

## 5.6 High Pass Filter and Limiting Amplifier

The limiting amplifier consists of six differential amplifier stages. At the input and after the third stage a high pass filter is placed. Thus the frequency behaviour between the limiting amplifier input IN_LA and the outputs OUTP_LA, OUTN_LA can be described with a second order high pass filter. These stages provide symmetrical outputs at OUTP_LA, OUTN_LA which are inverted with respect to each other. The differential gain (in the linear range) from the input of limiting amplifier (AMP) to the output (OUTP_LA - OUTN_LA) has a typ. value of +4225. In case of input overdrive excessive phase shift is

avoided by the limiting amplifiers.

The outputs OUTP_LA, OUTN_LA are source follower outputs, which buffer the last differential stage of the limiting amplifier. The external load at these outputs should not be smaller than 10k, to avoid reduction of the output swing. The maximum output voltage swing has a typical value of 1V. The limiting outputs can be switched to high impedance by use of control input ON_LA. This allows output multiplexing of several amplifier devices, e.g. in multi-sensor systems.

Using the input ON_LA during multiplex mode to switch between the channels of several E909.07 switching times of 1µs can be realized.

## 5.7 Digital Control Inputs

Four control inputs are provided:

- **ON_LA** enables the limiting amplifier and activates the outputs OUTP_LA, OUTN_LA by closing the switch between the limiting amplifier and the output pins when pulled to high level. An internal pull down keeps the outputs in OFF mode (high impedance) when the pin is left open. If ON_LA is 0 the outputs are in high-impedance state.

- **Input ON** is used to switch the device from OPERATING mode to SLEEP mode. The device is active, when ON is pulled high to supply voltage AVDD. With ON = 0, the all components in the devices are switched off and the current consumption drops to almost zero. An internal pull-down will hold the device in SLEEP mode when the pin is left open.

- **Input GAIN_CTRL** allows to reduce the amplification factor of the limiting amplifier by bypassing one of the two amplification stages.
  - With GAIN_CTRL = 0 both stages are active, the amplification factor has its maximum value.
  - With GAIN_CTRL = 1 one amplifier stage is bypassed thus reducing the amplification factor by a factor of 2.

- **Input IO_CTRL** allows to disconnect the TIA output from the pin AMP. Then it is possible to control the limiting amplifier with an external signal. In all cases, the TIA is connected to the linear amplifier.
  - IO_CTRL = 0: The output of the transimpedance amplifier (TIA) is connected to the input of the limiting amplifier. The TIA output signal is available on the pin AMP which is of type output.
  - IO_CTRL = 1: The output of the transimpedance amplifier is disconnected from the input of the limiting amplifier. Pin AMP is the input of the limiting amplifier.

| *PIN* | *Status* | *Description* |
|---|---|---|
| ON_LA | 0 | Outputs OUTP_LA, OUTN,LA are inactive (high resistance state) |
| | 1 | |
| ON | 0 | SLEEP Mode |
| | 1 | Operating Mode |
| GAIN_CTRL | 0 | Both amplification stages are active, the amplification factor has its maximum value |
| | 1 | The second amplification stage is bypassed |
| IO_CTRL | 0 | TIA Output connected to input of limiting amplifier |
| | 1 | TIA Output disconnected to input of limiting amplifier. Limiting amplifier could be controlled by external signal (AMP) |

**Table 10: Table of Digital Control Inputs**

# 6 ESD, Latch up and EMC

## 6.1 Electro Static Discharge (ESD)

| | |
|---|---|
| Standard | AEC-Q100-002 |
| Model | Human Body Model |
| Capacitance | 100 pF |
| Resistance | 1,5 kΩ |
| Minimum withstand Voltage | +/- 2 kV |
| Supply and interface pins (OUTP_LA, OUTN_LA, GGND, AGND_LA, AGND, GVDD, AVDD_LA, AVDD) | +/- 4 kV |

**Table 11: ESD on IC Level, Human Body Model (HBM)**

| | |
|---|---|
| Standard | AEC-Q100-011 |
| Model | Charged Device Model |
| Resistance | 1 Ω |
| Minimum withstand Voltage | +/- 500 V |
| Pulse rise time (10%-90%) | <400 ps |

**Table 12: ESD on IC Level, Charged Device Model (CDM)**

## 6.2 Latch-up

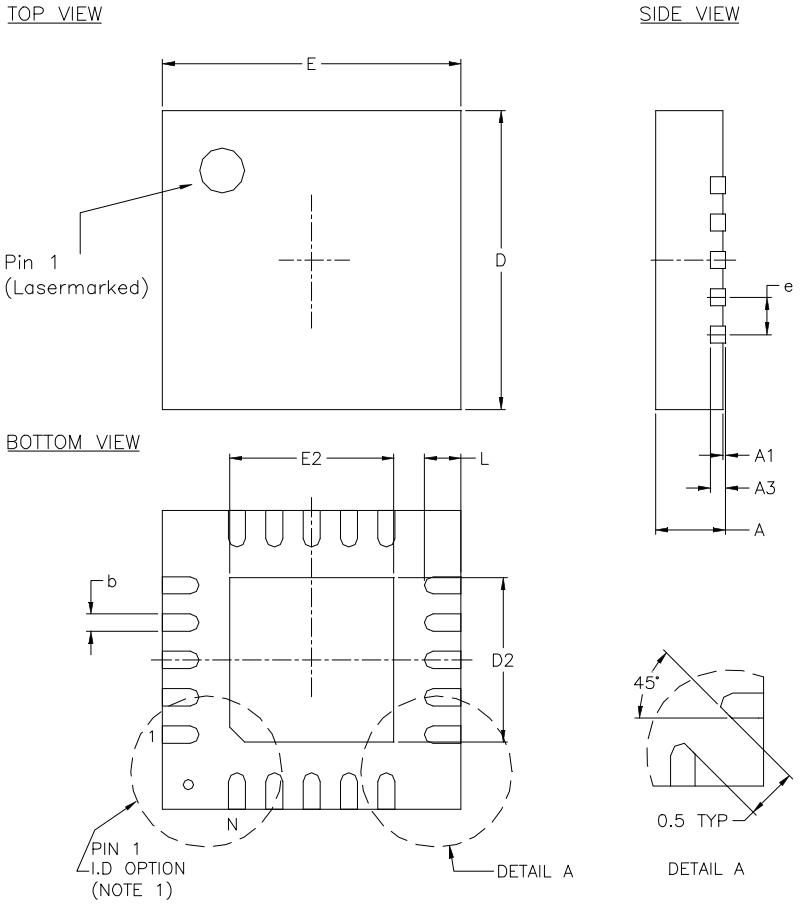
Latch-up performance is validated according JEDEC standard JESD 78 in its valid revision.

## 6.3 EMC

The contents of this chapter were not specified yet!

# 7 Package Information

The E909.07 is available in a Pb free, RoHs compliant QFN20L4 plastic package, for this exposed pad size is no variant within JEDEC MO-220 K available. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.




| Description | Symbol | mm | | | inch | | |
|---|---|---|---|---|---|---|---|
| | | min | typ | max | min | typ | max |
| Package height | A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| Stand off | A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.00079 | 0.002 |
| Thickness of terminal leads, including lead finish | A3 | -- | 0.20 REF | -- | -- | 0.0079 REF | -- |
| Width of terminal leads | b | 0.18 | 0.25 | 0.30 | 0.0071 | 0.0098 | 0.012 |
| Package length / width | D / E | -- | 4.00 BSC | -- | -- | 0.157 BSC | -- |
| Length / width of exposed pad | D2 / E2 | 2.50 | 2.65 | 2.80 | 0.098 | 0.104 | 0.110 |
| Lead pitch | e | -- | 0.50 BSC | -- | -- | 0.020 BSC | -- |
| Length of terminal for soldering to substrate | L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| Number of terminal positions | N | | 20 | | | 20 | |

**Note:** the mm values are valid, the inch values contains rounding errors

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