

LS4119A N-CHANNEL JFET



Linear Systems replaces discontinued Siliconix 2N4119A

The LS4119A is an Ultra-High Input Impedance N-Channel JFET

The LS4119A provides ultra-high input impedance. The device is specified with a 1-pA limit and typically operates at 0.2 pA. The part is ideal for use as a high-impedance sensitive front-end amplifier.

LS4119A Benefits:

- Insignificant Signal Loss / Error Voltage with High-Impedance Source
- Low Power Consumption (Battery)
- Maximum Signal Output, Low Noise
- High Sensitivity to Low-Level Signals

LS4119A Applications:

- High-Impedance Transducer
- Smoke Detector Input
- Infrared Detector Amplifier
- Precision Test Equipment

FEATURES						
DIRECT REPLACEMENT FOR SILICONIX 2N4119A						
LOW POWER	I _{DSS} <90 μA					
MINIMUM CIRCUIT LOADING I _{GSS} <1 pA						
ABSOLUTE MAXIMUM RATINGS						
@ 25°C (unless otherwise noted)						
Maximum Temperatures						
Storage Temperature	-65°C to +175°C					
Operating Junction Temperature	-55°C to +150°C					
Maximum Power Dissipation						
Continuous Power Dissipation	300mW					
MAXIMUM CURRENT						
Gate Current (Note 1)	50mA					
MAXIMUM VOLTAGES						
Gate to Drain or Gate to Source (Note 2)	-40V					

LS4119A ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
BV _{GSS}	Gate to Source Breakdown Voltage	-40		I.	V	$I_{G} = -1\mu A$, $V_{DS} = 0V$
V _{GS(off)}	Gate to Source Cutoff Voltage	-2		-6	V	$V_{DS} = 10V, I_{D} = 1nA$
I _{DSS}	Gate to Sou <mark>rc</mark> e Saturation Current	0.20		0.60	mA	$V_{DS} = 10V, V_{GS} = 0V$
I _{GSS}	Gate Leakage Current	-		-1	pA	$V_{GS} = -20V, V_{DS} = 0V$
				-2.5		$V_{GS} = -20V, V_{DS} = 0V, 150^{\circ}C$
g fs	Forward Transconductance(Note 3)	100		330	μmho	$V_{DS} = 10V$, $V_{GS} = 0V$, $f = 1kHz$
g os	Output Conductance			10		
C _{iss}	Input Capacitance			3		
C _{rss}	Reverse Transfer Capacitance			1.5	pF	$V_{DS} = 10V$, $V_{GS} = 0V$, $f = 1MHz$

NOTES

- 1 . Absolute maximum ratings are limiting values above which LS4119A serviceability may be impaired.
- 2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged
- 3. This parameter is measured during a 2ms interval 100ms after power is applied. (Not a JEDEC condition.)

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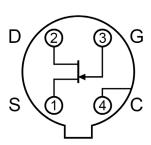
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Available Packages:

LS4119A in TO-71 LS4119A in bare die.

Please contact Micross for full package and die dimensions

TO-71 (Bottom View)



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