

NCP134

500 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

The NCP134 is a 500 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP134 features low I_Q consumption. The XDFN4 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Voltage Versions Available
- Output Voltage Range: 0.8 V to 2.1 V (Fixed)
- $\pm 1.5\%$ Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra-Low Dropout: Typ. 140 mV at 500 mA
- Very Low Bias Input Current of Typ. 80 μ A
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μ A
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 2.2 μ F Ceramic Capacitor
- Available in XDFN4 – 1.2 mm x 1.2 mm x 0.4 mm Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

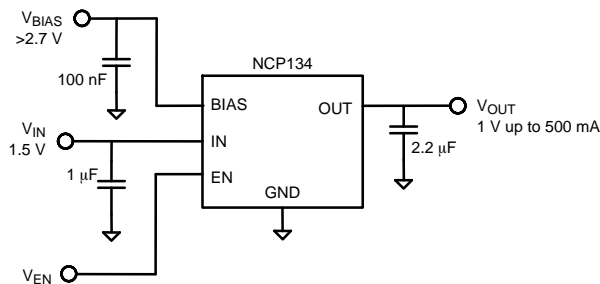


Figure 1. Typical Application Schematics



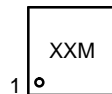
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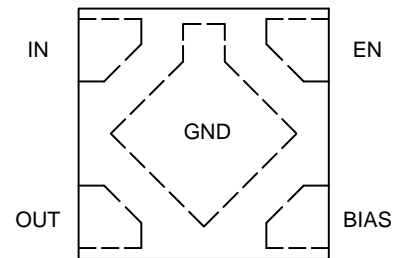
XDFN4
CASE 711BC

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS

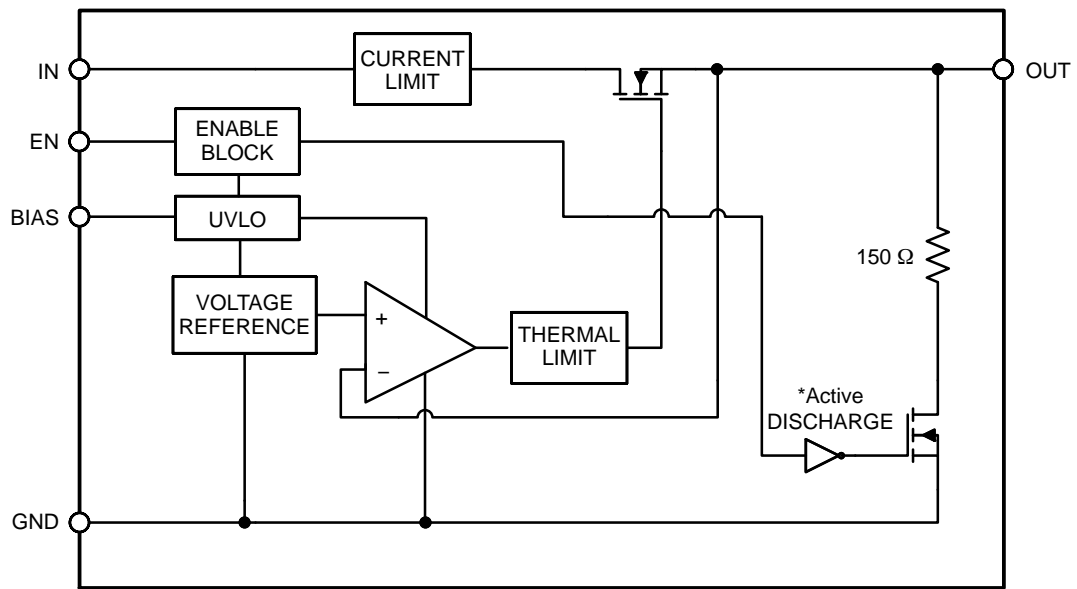


(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

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*Active output discharge function is present only in NCP134AMXyyyTCG devices.
yyy denotes the particular output voltage option.

Figure 2. Simplified Schematic Block Diagram – Fixed Version

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PIN FUNCTION DESCRIPTION

Pin No. XDFN4	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	IN	Input Voltage Supply pin
5	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	-0.3 to 6	V
Output Voltage	V_{OUT}	-0.3 to $(V_{IN}+0.3) \leq 6$	V
Chip Enable, Bias Input	V_{EN}, V_{BIAS}	-0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
 ESD Human Body Model tested per EIA/JESD22-A114
 ESD Machine Model tested per EIA/JESD22-A115
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 1.2 mm x 1.2 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	170	°C/W

3. This data was derived by thermal simulations for a single device mounted on the 40 mm x 40 mm x 1.6 mm FR4 PCB with 2-ounce 800 sq mm copper area on top and bottom.

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ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$; $V_{\text{BIAS}} = 2.7\text{ V}$ or $(V_{\text{OUT}} + 1.6\text{ V})$, whichever is greater, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, $V_{\text{EN}} = 1\text{ V}$, unless otherwise noted. $C_{\text{IN}} = 1\text{ }\mu\text{F}$, $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$. Typical values are at $T_J = +25^{\circ}\text{C}$. Min/Max values are for $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ unless otherwise noted. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V_{IN}	$V_{\text{OUT}} + V_{\text{DO}}$		5.5	V
Operating Bias Voltage Range		V_{BIAS}	$(V_{\text{OUT}} + 1.40) \geq 2.4$		5.5	V
Undervoltage Lock-out	V_{BIAS} Rising Hysteresis	UVLO		1.6 0.2		V
Output Voltage Accuracy		V_{OUT}		± 0.5		%
Output Voltage Accuracy	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, $V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq V_{\text{OUT(NOM)}} + 1.0\text{ V}$, 2.7 V or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$, whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$, $1\text{ mA} < I_{\text{OUT}} < 500\text{ mA}$	V_{OUT}	-1.5		+1.5	%
V_{IN} Line Regulation	$V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq 5.0\text{ V}$	LineReg		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$, whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$	LineReg		0.01		%/V
Load Regulation	$I_{\text{OUT}} = 1\text{ mA}$ to 500 mA	LoadReg		1.5		mV
V_{IN} Dropout Voltage	$I_{\text{OUT}} = 150\text{ mA}$ (Note 5)	V_{DO}		37	75	mV
	$I_{\text{OUT}} = 500\text{ mA}$ (Note 5)	V_{DO}		140	250	
V_{BIAS} Dropout Voltage	$I_{\text{OUT}} = 500\text{ mA}$, $V_{\text{IN}} = V_{\text{BIAS}}$ (Notes 5, 6)	V_{DO}		1.1	1.5	V
Output Current Limit	$V_{\text{OUT}} = 90\% V_{\text{OUT(NOM)}}$	I_{CL}	550	800	1000	mA
Bias Pin Operating Current	$V_{\text{BIAS}} = 2.7\text{ V}$	I_{BIAS}		80	110	μA
Bias Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{BIAS(DIS)}}$		0.5	1	μA
Vinpin Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{VIN(DIS)}}$		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage "H"	$V_{\text{EN(H)}}$	0.9			V
	EN Input Voltage "L"	$V_{\text{EN(L)}}$			0.4	
EN Pull Down Current	$V_{\text{EN}} = 5.5\text{ V}$	I_{EN}		0.3	1	μA
Turn-On Time	From assertion of V_{EN} to $V_{\text{OUT}} = 98\% V_{\text{OUT(NOM)}}$; $V_{\text{OUT(NOM)}} = 1.0\text{ V}$	t_{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} to V_{OUT} , $f = 1\text{ kHz}$, $I_{\text{OUT}} = 150\text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$	PSRR(V_{IN})		70		dB
	V_{BIAS} to V_{OUT} , $f = 1\text{ kHz}$, $I_{\text{OUT}} = 150\text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$	PSRR(V_{BIAS})		80		
Output Noise Voltage	$V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$, $V_{\text{OUT(NOM)}} = 1\text{ V}$, $f = 10\text{ Hz}$ to 100 kHz	V_{N}		40		μV_{RMS}
Thermal Shutdown Threshold	Temperature increasing			160		$^{\circ}\text{C}$
	Temperature decreasing			140		
Output Discharge Pull-Down	$V_{\text{EN}} \leq 0.4\text{ V}$, $V_{\text{OUT}} = 0.5\text{ V}$, NCP134A options only	R_{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$.

Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{\text{OUT(NOM)}}$.

6. For output voltages below 0.9 V , V_{BIAS} dropout voltage does not apply due to a minimum Bias operating voltage of 2.4 V .

TYPICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$, $V_{BIAS} = 2.7\text{ V}$, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)} = 1.0\text{ V}$, $I_{OUT} = 500\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 0.1\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (effective capacitance), unless otherwise noted.

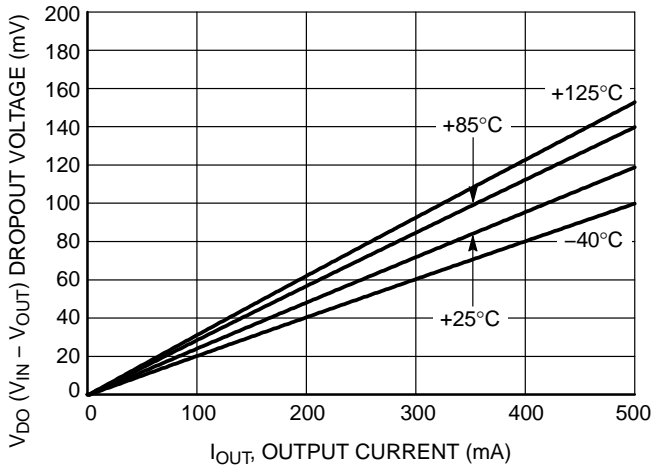


Figure 3. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

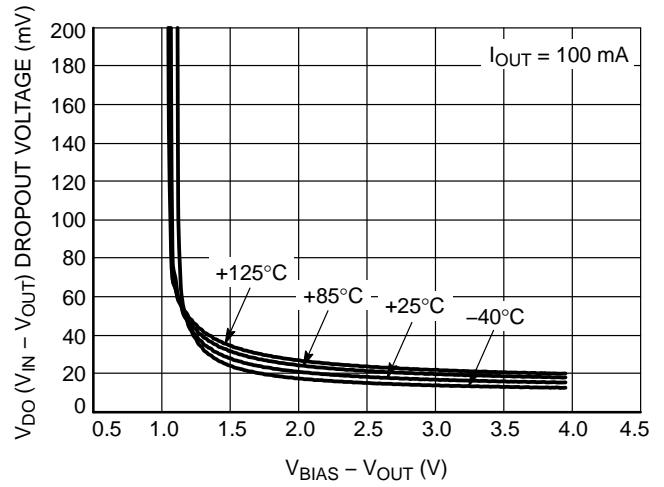


Figure 4. V_{IN} Dropout Voltage vs. $(V_{BIAS} - V_{OUT})$ and Temperature T_J

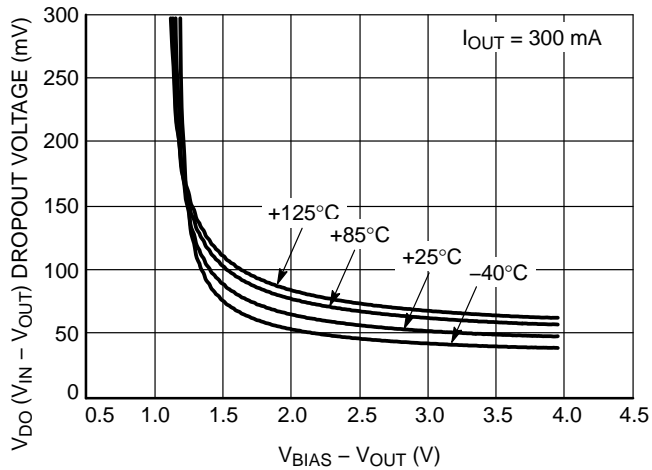


Figure 5. V_{IN} Dropout Voltage vs. $(V_{BIAS} - V_{OUT})$ and Temperature T_J

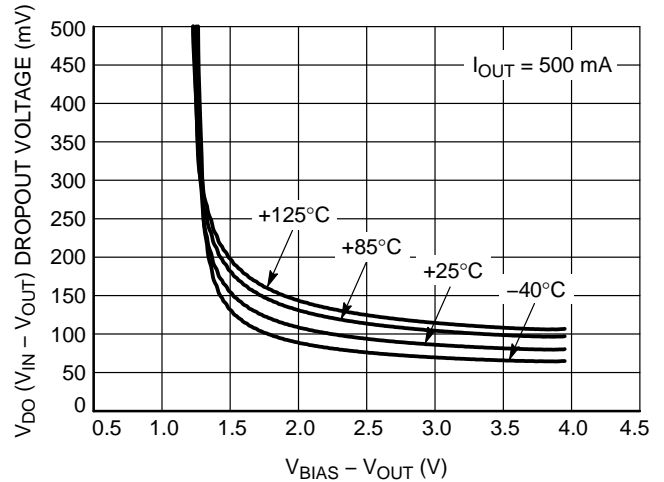


Figure 6. V_{IN} Dropout Voltage vs. $(V_{BIAS} - V_{OUT})$ and Temperature T_J

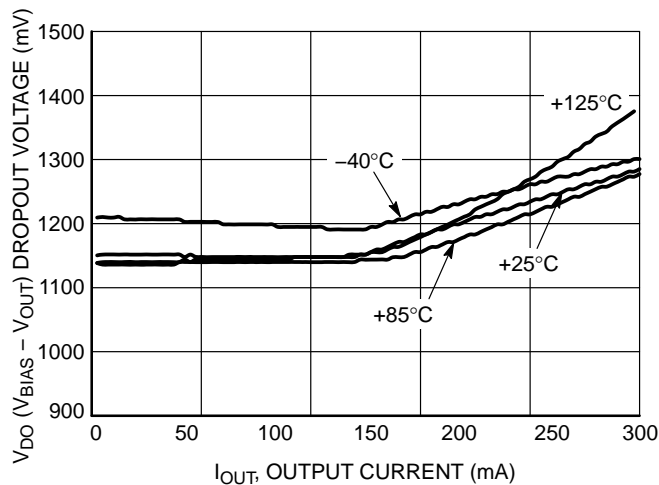


Figure 7. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_J

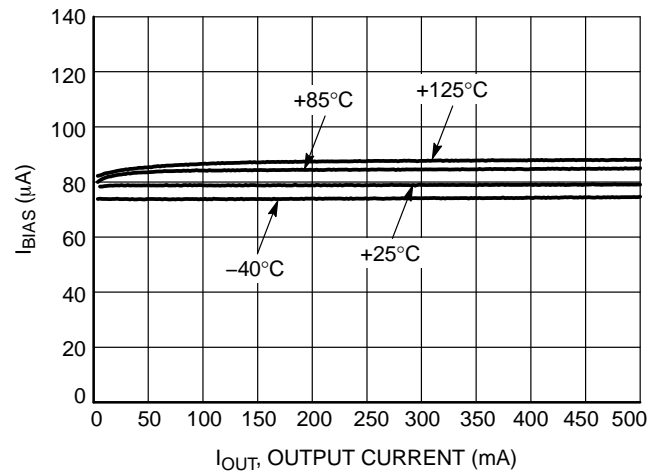


Figure 8. BIAS Pin Current vs. I_{OUT} and Temperature T_J

TYPICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$, $V_{BIAS} = 2.7\text{ V}$, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)} = 1.0\text{ V}$, $I_{OUT} = 500\text{ mA}$,
 $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 0.1\text{ }\mu\text{F}$, and $C_{OUT} = 2.2\text{ }\mu\text{F}$ (effective capacitance), unless otherwise noted.

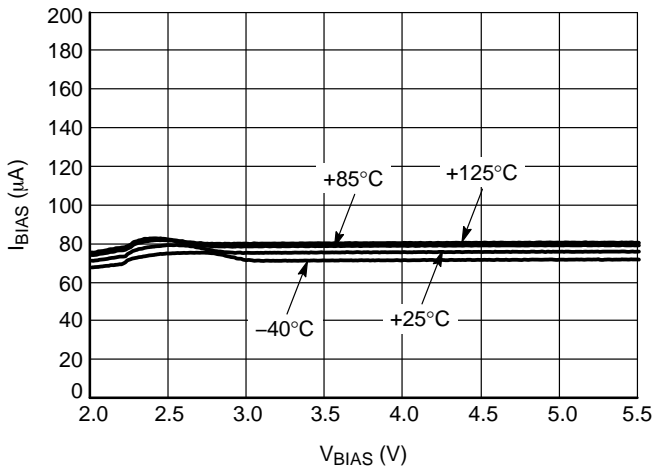


Figure 9. BIAS Pin Current vs. V_{BIAS} and Temperature T_J

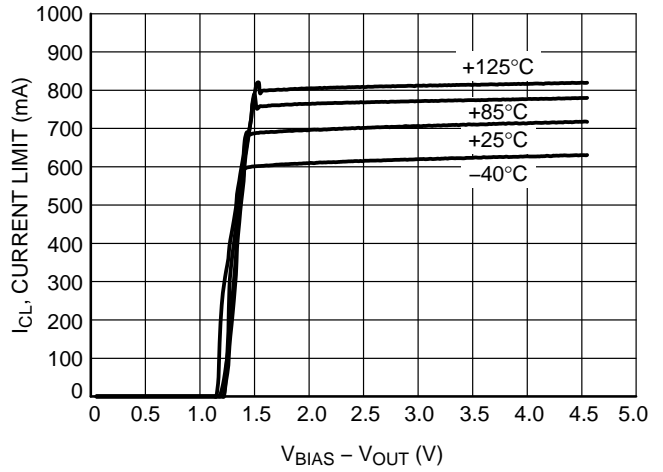


Figure 10. Current Limit vs. $(V_{BIAS} - V_{OUT})$

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ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
NCP134AMX100TCG	1.00 V	GA	Output Active Discharge	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCP134AMX105TCG	1.05 V	GC	Output Active Discharge	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCP134AMX110TCG	1.10 V	GD	Output Active Discharge	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCP134AMX120TCG	1.20 V	GE	Output Active Discharge	XDFN4 (Pb-Free)	3000 / Tape & Reel

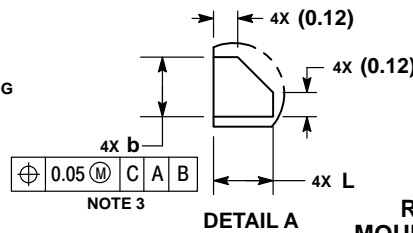
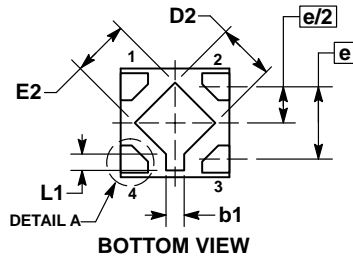
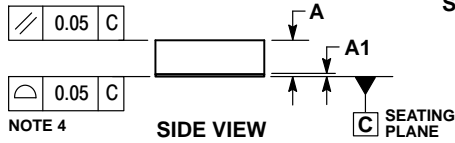
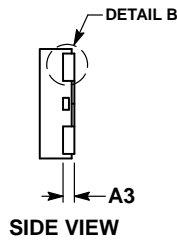
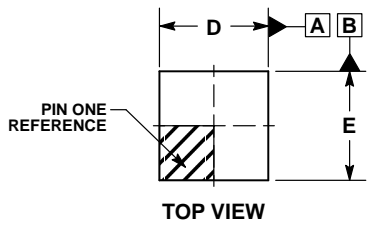
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

NCP134

PACKAGE DIMENSIONS

XDFN4 1.2x1.2, 0.8P CASE 711BC ISSUE O

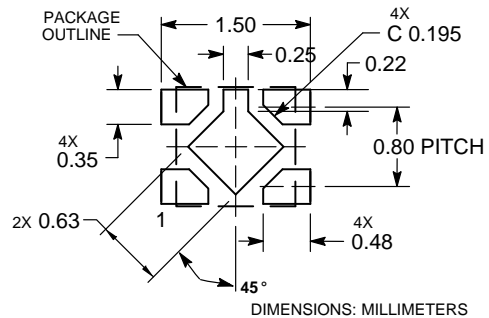


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13	REF
b	0.25	0.35
b1	0.15	0.25
D	1.15	1.25
D2	0.58	0.68
E	1.15	1.25
E2	0.58	0.68
e	0.80	BSC
L	0.25	0.35
L1	0.13	0.23

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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