Pentium/Pro™ System Clock Chip

Features

- Three CPUs @2.5V, up to 100 MHz
- Seven PCIs @ 3.3V (including one free running, 1 early)
- One 48 MHz @ 3.3V fixed
- One REF (3.3V, 14.318 MHz)
- One IOAPIC (2.5V, 14.318 MHz)
- Strong REF clock (1V/ns @50pF load)
- Excellent power management features including Power Down, PCI, and CPU stops
- Spread Spectrum for EMI control (0.5% down spread)
- Early PCI (2.5ns ±700ps)
- Enhanced PCICLK4 (1.5X)
- 28-pin SSOP Packaging (H)

Description

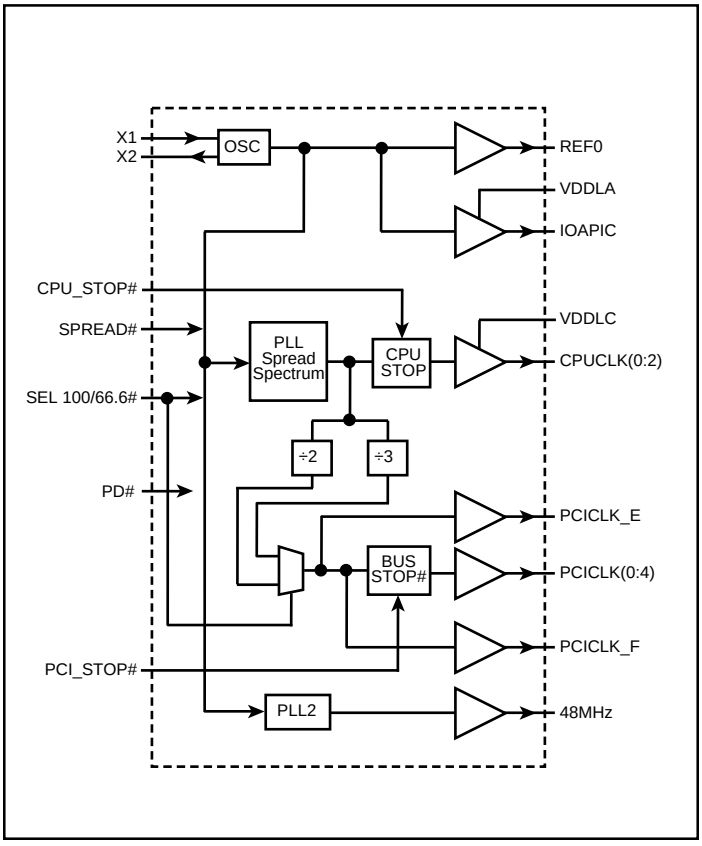
The PI6C106 is part of a reduced pin count two-chip clock solution for designs using an Intel BX style chipset. Companion SDRAM buffers are PI6C182 & PI6C184.

There are two PLLs, with the first PLL capable of spread spectum operation. CPU frequencies up to 100 MHz are supported.

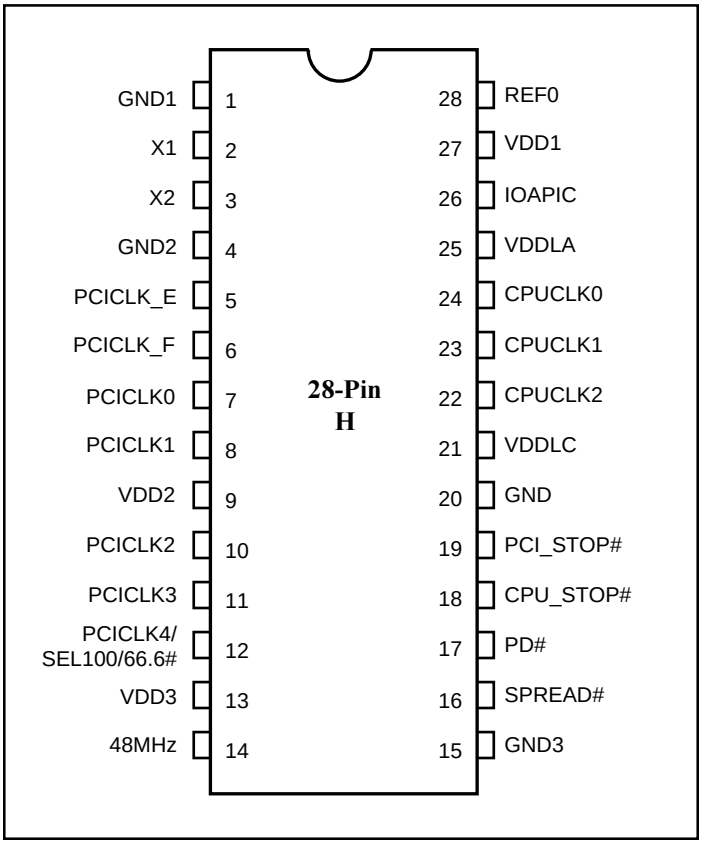
Frequency Table

SEL 100/66.6#	CPU MHz	PCI MHz
1	100	33.3
0	66.6	33.3

Block Diagram



Pin Configuration



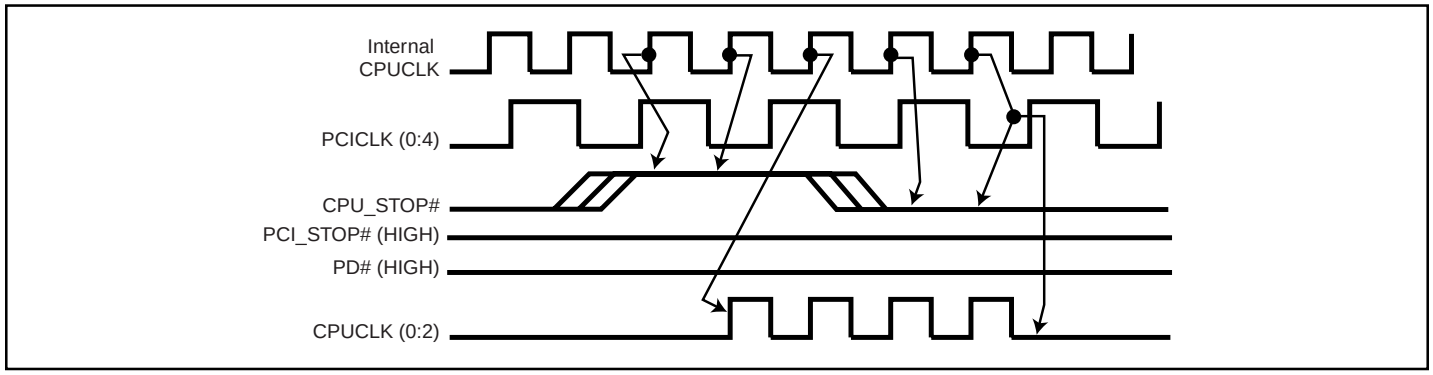
Pin Descriptions

Pin Number	Pin Name	Type	Description
1	GND1	PWR	Ground for REF output, X1, X2.
2	X1	IN	XTAL_IN 14.318 MHz Crystal input, has internal 33pF load cap and feedback resistor from X2.
3	X2	OUT	XTAL_OUT Crystal outut, has internal load cap 33pF
4	GND2	PWR	Ground for PCI outputs
5	PCICLK_E	OUT	Early PCICLK. Leads PCICLK(0:4,_F) by 2ns ±250ps. Not affected by PCI_STOP#.
6	PCICLK_F	OUT	Free Running PCI output. Not affected by PCI_STOP#.
7,8,10,11	PCICLK(0:3)	OUT	PCI clock outputs. TTL compatible 3.3V.
9	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V.
12	PCICLK_4	OUT	PCI clock output. TTL compatible 3.3V. (1.5X)
	SEL100/66.6#	IN	Select pin for enabling 100MHz or 66.6 MHz. H=100 MHz, L=66.6 MHz (PCI always synchronous 33.3 MHz).
13	VDD3	PWR	Power for 48 MHz.
14	48 MHz	OUT	Fixed CLK output @ 48 MHz.
15	GND3	PWR	Ground for 48 MHz.
16	SPREAD#	IN	Turns on Spread Spectrum when active. 0.5% down spread 0.1.
17	PD#	IN	Powers down chip. Internal PLLs, all output are turned off.
18	CPU_STOP#	IN	Halts CPUCLK (2:0) at logic "0" level when input is low.
19	PCI_STOP#	IN	Halts CPUCLK (0:4) at logic "0" level when input is low. Does not affect PCICLK_E and PCICLK_F
20	GND	PWR	Ground for PLL core.
21	VDDLC	PWR	Power for CPU outputs, nominally 2.5V
22,23,24	CPUCLK (2:0)	OUT	CPU and Host clock outputs nominally 2.5V
25	VDDLA	PWR	Power for IOAPIC.
26	IOAPIC	OUT	IOAPIC clock output 14.318MHz.
27	VDD1	PWR	Power for REF outputs.
28	REF0	OUT	14.318 MHz clock output.

Note:
Inactive means outputs are held LOW and are disabled from switching

CPU_STOP# Timing Diagram

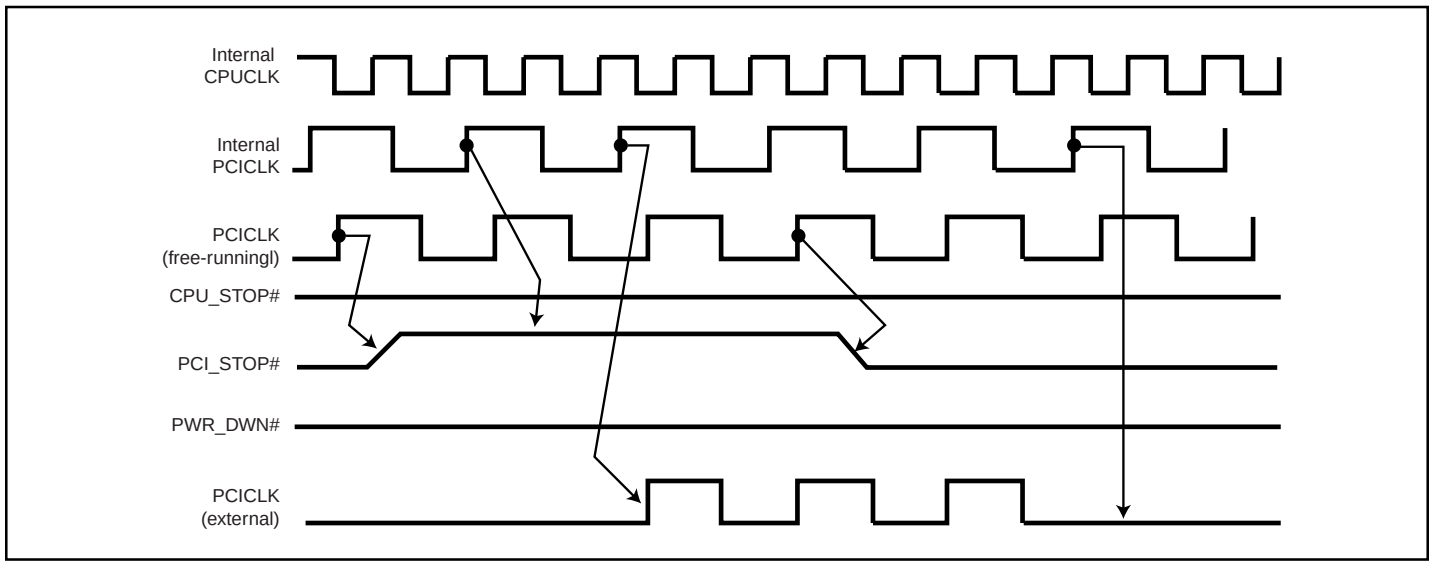
CPUS_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. All other clocks will continue to run while the CPUCLKs clocks are disabled.
The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside PI6C106.
3. All other clocks continue to run undisturbed including SDRAMR.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

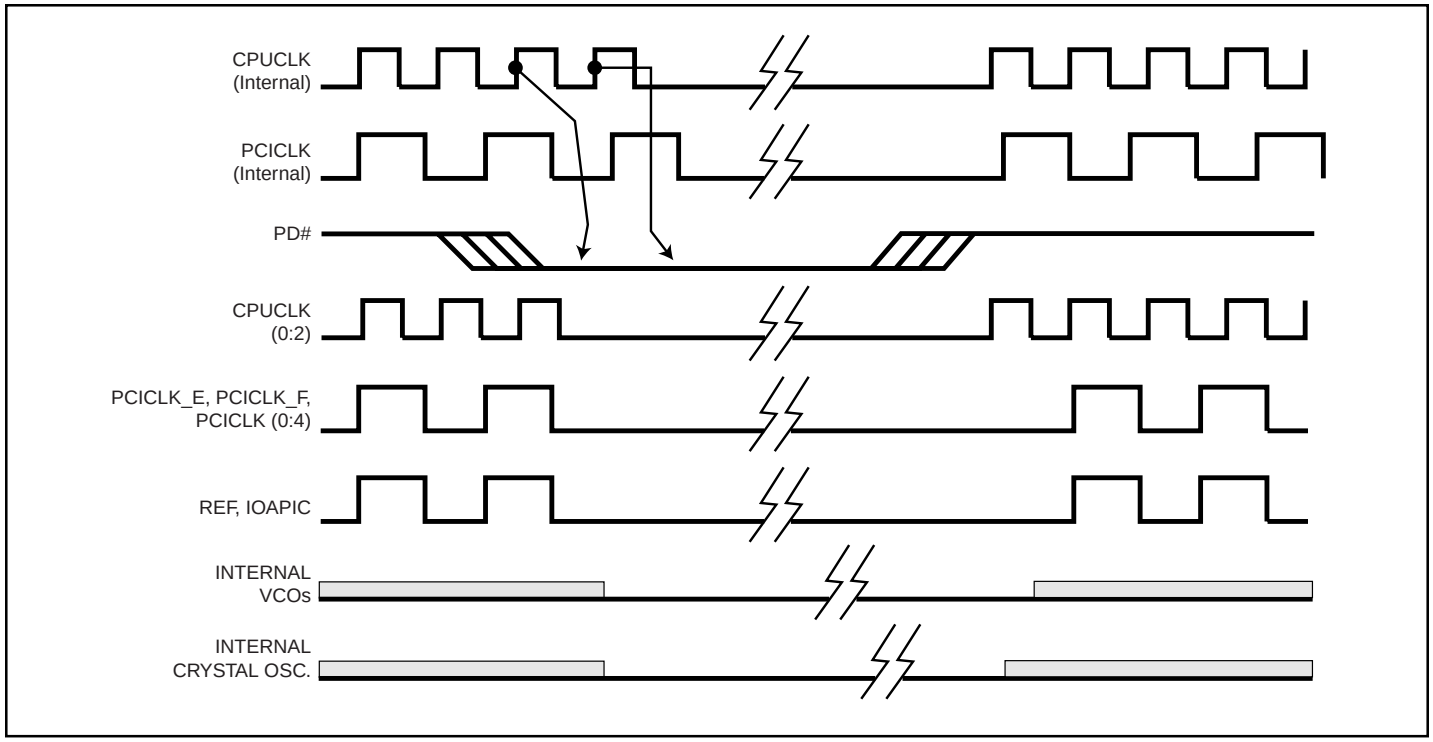
PCI_STOP# is an asynchronous input to the PI6C106. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the PI6C106 internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the PI6C106 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the PI6C106.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the PI6C106 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the PI6C106 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the PI6C106.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage 7.0V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings arestress specifications only and functional operation of the device at these or any other conditions above those listed in theoperational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periodsmay affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0°C - 70°C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V ±5% (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}		2		V_{DD}+0-.3	V
Input Low Voltage	V_{IL}		V_{SS}–0.3		0.8	
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0V; Inputs with no pull-up resistors	–5			
Input Low Current	I_{IL2}	V_{IN} = 0V; Inputs with pull-up resistors	–200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0pF; 66.6 MHz			100	mA
		C_L = 0pF; 100 MHz			100	
Input Frequency	F_i	V_{DD} = 3.3V	12		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	
Transition Time[1]	T_{trans}	To first crossing to 1% target frequency			3	ms
Settling Time[1]	T_S	From first crossing to 1% target frequency			2	
Clock Stabilization[1]	T_{STAB}	From V_{DD} = 3.3V to 1% target frequency			3	

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0°C - 70°C; Supply Voltage V_{DD} = 3.3 V ±5%, V_{DDL} = 2.5V ±5% (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0pF; 66.8 MHz			50	mA
		C_L = 0pF; 100 MHz			50	
Power Down Current	$I_{DD2.5OP}$				100	µA
Skew[1]	$T_{CPU\_PCI(F,0:4)}$	V_T = 1.5V / 1.25V; CPU Leads	1.5		4	ns
	$T_{PCI(E)\ -\ PCIC(F)}$	V_T = 1.5V	1.8		3.2	

Note: 1. Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0°C - 70°C; V_{DD} = 3.3V ±5%, V_{DDL} = 2.5V ±5%; C_L = 10-20pF (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	I_{OH} = –12mA	2			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.4	
Output High Current	I_{OH}	V_{OH} = 1.7V			–16	mA
Output Low Current	I_{OL}	V_{OL} = 0.7V	19			
Rise Time	t_r	V_{OL} = 0.4V, V_{OH} = 2.0V			1.6	ns
Fall Time	t_f	V_{OH} = 2.0V, V_{OL} = 0.4V			1.6	
Duty Cycle	d_t	V_T = 1.25V	45		55	%
Skew	t_{sk}	V_T = 1.25V			175	ps
Jitter, Single Edge Displacement(2)	t_{jsed}	V_T = 1.25V			250	
Jitter, One Sigma	t_{j1}	V_T = 1.25V			150	
jitter, Absolute	t_{jabs}	V_T = 1.25V	–300		300	

Notes:
1. Guaranteed by design, not 100% tested in production.
2. Edge displacement of a period relative to a 10-clock-cycle rolling average period

Electrical Characteristics - PCI

T_A = 0°C - 70°C; V_{DD} = V_{DDL} = 3.3V ±10%, C_L = 30pF (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH1}	I_{OH} = –11mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4mA			0.4	
Output High Current	I_{OH1}	V_{OH} = 2.0V			–22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8V	16			
Rise Time	t_r	V_{OL} = 0.4V, V_{OH} = 2.4V			2	ns
Fall Time	t_f	V_{OH} = 2.4V, V_{OL} = 0.4V			2	
Duty Cycle	d_t	V_T = 1.5V	45		55	%
Skew	t_{sk}	V_T = 1.5V			500	ps
Jitter, Single Edge Displacement(2)	t_{jsed}	V_T = 1.25V			500	
jitter, Absolute	t_{jabs}	V_T = 1.5V	–250		200	
		V_T = 1.5V			250	

Notes:
1. Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0°C - 70°C; V_{DD} = V_{DDL} = 3.3V ±10%, C_L = 50pF (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	I_{OH} = –12mA	2.6			V
Output Low Voltage	V_{OL}	I_{OL} = 9mA			0.4	
Output High Current	I_{OH}	V_{OH} = 2.0V			–22	mA
Output Low Current	I_{OL}	V_{OL} = 0.8V	16			
Rise Time	t_r	V_{OL} = 0.4V, V_{OH} = 2.4V			2	ns
Fall Time	t_f(1)	V_{OH} = 2.4V, V_{OL} = 0.4V			2	
Duty Cycle	d_t	V_T = 1.5V	53		55	%
Jitter, One Sigma	t_{j1s}	V_T = 1.5V			3	ns
Jitter, Absolute	t_{jabs}	V_T = 1.5V	–5		5	

Electrical Characteristics - IOAPIC

T_A = 0°C - 70°C; V_{DD} = V_{DDL} = 3.3V ±10%, C_L = 20pF (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	I_{OH} = –12mA	2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.4	
Output High Current	I_{OH}	V_{OH} = 1.7V			–16	mA
Output Low Current	I_{OL}	V_{OL} = 0.7V	19			
Rise Time	t_{r2}	V_{OL} = 0.4V, V_{OH} = 2.0V			1.6	ns
Fall Time	t_{f2}	V_{OH} = 2.0V, V_{OL} = 0.4V			1.6	
Duty Cycle	d_{t2}	V_T = 1.25V	45		55	%
Jitter, One Sigma(1)	t_{j1s}	V_T = 1.5V			3	ns
Jitter, Absolute(1)	t_{jabs}	V_T = 1.5V	–6		6	

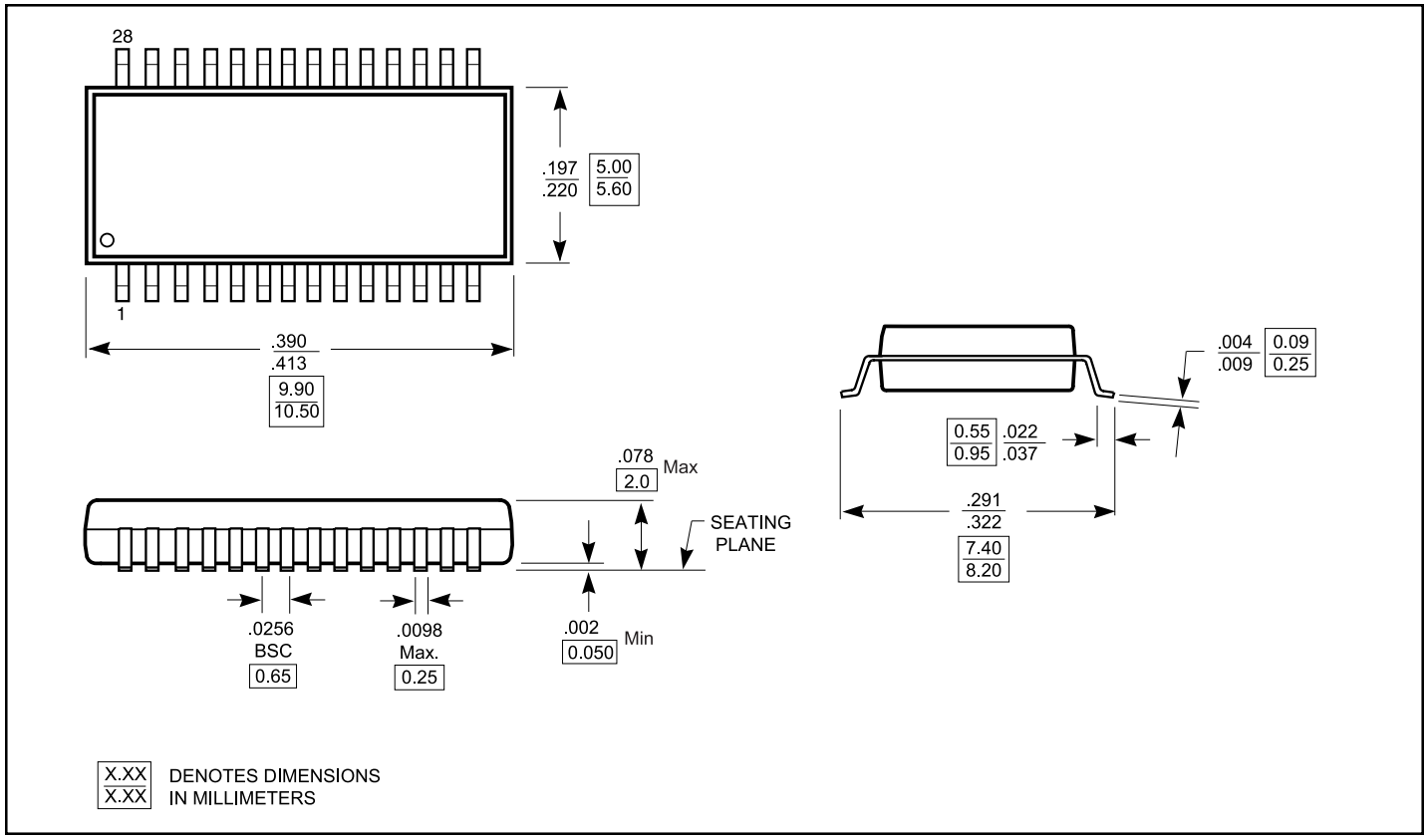
Electrical Characteristics - 48M

T_A = 0°C - 70°C; V_{DD} = V_{DDL} = 3.3V ±5%, C_L = 20pF (unless otherwise stated).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	I_{OH} = –11mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 9.4mA			0.4	
Output High Current	I_{OH}	V_{OH} = 2.0V			–18	mA
Output Low Current	I_{OL}	V_{OL} = 0.8V	12			
Rise Time	t_r	V_{OL} = 0.4V, V_{OH} = 2.4V			2.5	ns
Fall Time	t_f	V_{OH} = 2.4V, V_{OL} = 0.4V			2.5	
Duty Cycle(1)	d_t	V_T = 1.5V	45		55	%
Jitter, One Sigma(1)	t_{j1s}	V_T = 1.5V			3	ns
Jitter, Absolute(1)	t_{jabs}	V_T = 1.5V	–6		6	

Note: 1. Guaranteed by design, not 100% tested in production.

28-Pin SSOP Package (H)



Ordering Information

Part No.	Package	Ordering P/N
PI6C106	SSOP (H-28)	PI6C106-H