TCC-206

Six-Output PTIC Control IC

Introduction

TCC−206 is a six−output high−voltage digital to analog control IC specifically designed to control and bias ON Semiconductor's Passive Tunable Integrated Circuits (PTICs).

These tunable capacitor control circuits are intended for use in mobile phones and dedicated RF tuning applications. The implementation of ON Semiconductor's tunable circuits in mobile phones enables significant improvement in terms of antenna radiated performance.

The tunable capacitors are controlled through a bias voltage ranging from 1 V to 24 V. The TCC−206 high−voltage PTIC control IC has been specifically designed to cover this need, providing six independent high−voltage outputs that control up to six different tunable PTICs in parallel. The device is fully controlled through a multi−protocol digital interface.

Key Features

- Controls ON Semiconductor's PTIC Tunable Capacitors
- Compliant with Timing Needs of Cellular and Other Wireless System Requirements
- Integrated Boost Converter with 6 Programmable DAC Outputs (up to 24 V)
- Low Power Consumption
- Auto−detection of SPI (30− or 32−bit) or MIPI RFFE Interfaces (1.8 V)
- Available in WLCSP (RDL ball arrays)
- Compliant with MIPI 26 MHz Read−Back
- This is a Pb−Free Device

Typical Applications

- Multi−band, Multi−standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Compatible with Closed−loop and Open−loop Antenna Tuner Applications

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WLCSP4
CASE 567JV

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 32 of this data sheet.

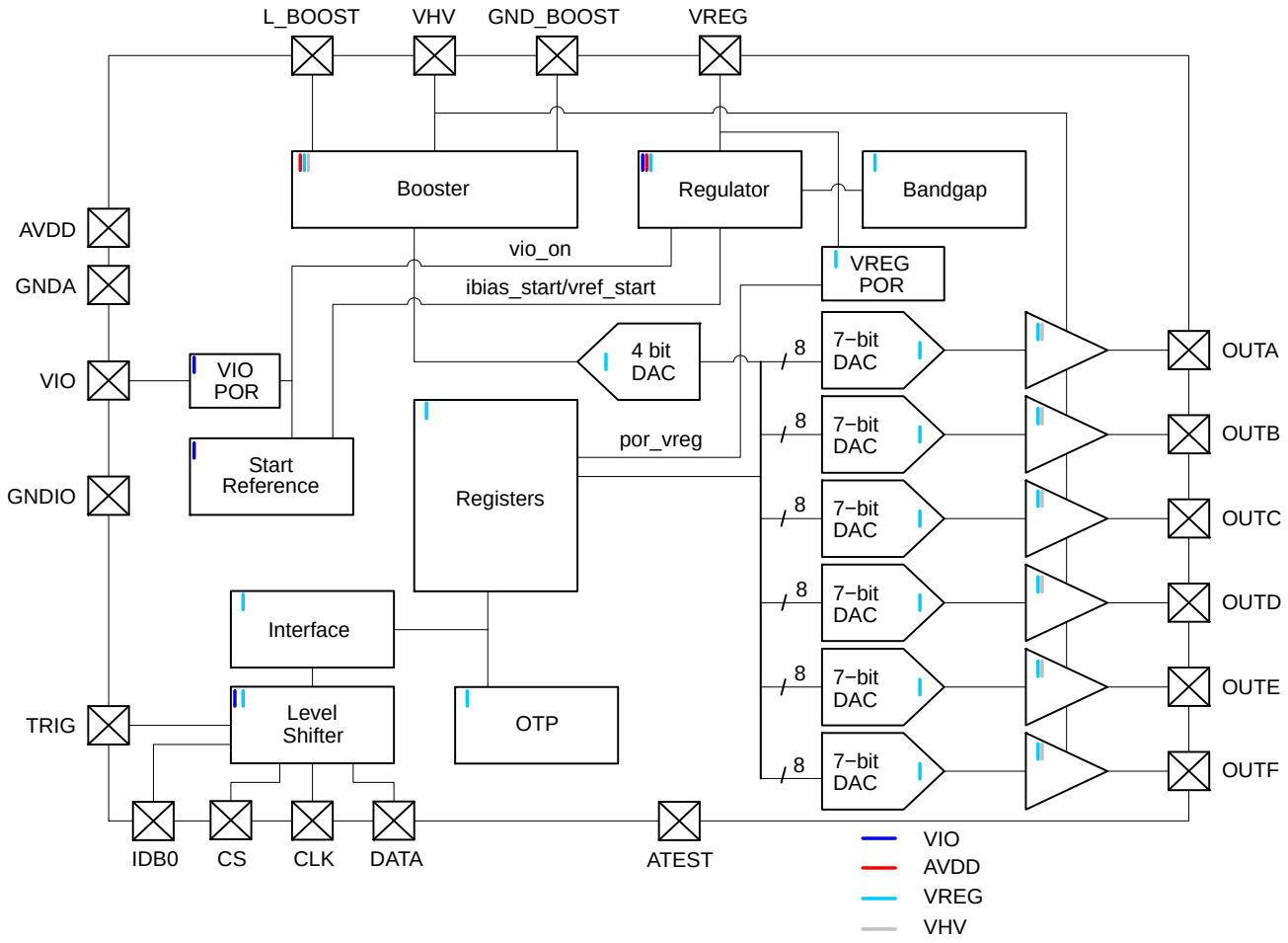


Figure 1. Control IC Functional Block Diagram

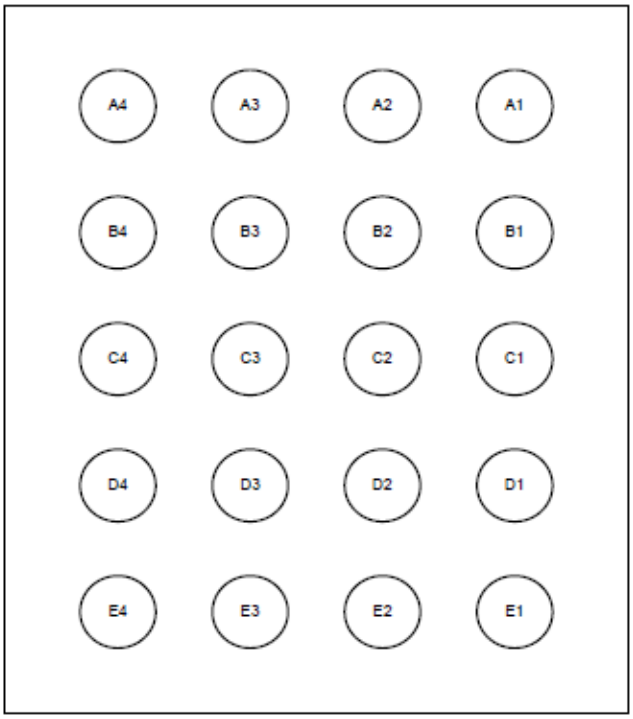


Figure 2. Die Bump Side View

RDL Pin Out

Table 1. PAD DESCRIPTIONS

RDL	Name	Type	Description	Max Voltage (Note 1)
A1	OUTF	AOH	High Voltage Output F	VHV
A2	VREG	AO	Regulator Output	2
A3	GND_BOOST	P	Ground for Booster	0
A4	VHV	AOH / AIH	Boost High Voltage can be Forced Externally	28
B1	OUTE	AOH	High Voltage Output E	VHV
B2	ATEST	AO	Analog Test Out (Note 4)	VREG
B3	AVDD	P	Analog Supply	5.5
B4	L_BOOST	AOH	Boost Inductor	28
C1	OUTD	AOH	High Voltage Output D	VHV
C2	IDB0	DI	MIPI RFFE ID Bit 0 (Note 3)	VIO
C3	GNDA	P	Analog Ground	0
C4	TRIG	DIO	Trigger Signal Input (Note 2)	VIO
D1	OUTC	AOH	High Voltage Output C	VHV
D2	GNDIO	P	Digital IO Ground	VIO
D3	CS	DI	Chip Select for SPI	VIO
D4	CLK	DI	MIPI RFFE / SPI Clock	VIO
E1	OUTB	AOH	High Voltage Output B	VHV
E2	OUTA	AOH	High Voltage Output A	VHV
E3	VIO	P	Digital IO Supply	2
E4	DATA	DIO	Digital IO (SPI and MIPI RFFE)	VIO

1. For information only.
2. To be grounded when not in use.
3. This pin has to be connected to either GNDIO or VIO level, even if only SPI protocol is used. Never let it float.
4. To be grounded in normal operation.

ELECTRICAL PERFORMANCE SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
AVDD	Analog Supply Voltage	−0.3 to +6.0	V
VIO	IO Reference Supply Voltage	−0.3 to +2.2	V
$V_{I/O}$	Input Voltage Logic Lines (DATA, CLK, CS)	−0.3 to VIO + 0.3	V
$V_{(sub)HVH}$	VHV Maximum Voltage	−0.3 to 30	V
$V_{ESD\ (HBM)}$	Human Body Model, JESD22−A114, All I/O	2,000	V
$V_{ESD\ (MM)}$	Machine Model, JESD22−A115	200	V
T_{STG}	Storage Temperature	−55 to +150	°C
$T_{AMB\_OP\_MAX}$	Max Operating Ambient Temperature without Damage	+110	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating			Unit
		Min	Typ	Max	
T_{AMB_OP}	Operating Ambient Temperature	−30	−	+85	°C
T_{J_OP}	Operating Junction Temperature	−30	−	+125	°C
AVDD	Analog Supply Voltage	2.3	−	5.5	V
VIO	IO Reference Supply Voltage	1.62	−	1.98	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC CHARACTERISTICS (T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V<AVDD< 5.5 V; V_{IO} = 1.8 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
SHUTDOWN MODE						
I_{AVDD}	AVDD Supply Current	−	−	1.5	μA	VIO Supply is Low
I_{L_BOOST}	L_BOOST Leakage	−	−	1.5		
I_{BATT}	Battery Current	−	−	2.5		
I_{VIO}	VIO Supply Current	−1	−	1		
I_{CLK}	CLK Leakage	−1	−	1		
I_{DATA}	DATA Leakage	−1	−	1		
ACTIVE MODE						
I_{BATT}	Average battery current, 3 outputs actively switching 16 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs and 3 outputs are @ 16 V steady state	−	1,760	2,350	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS0}	Average battery current, 6 outputs @ 0 V steady state	−	800	1,130		At VHV = 20 V AVDD = 3.3 V
I_{BAT_SS2}	Average battery current, 6 outputs @ 2 V steady state	−	850	1,200	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS16}	Average battery current, 6 outputs @ 16 V steady state	−	1,190	1,560		At VHV = 20 V AVDD = 3.3 V
I_{L_BOOST}	Average inductor current, 3 outputs actively switching 16 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs and 3 outputs are @ 16 V steady state	−	1,480	2,050		At VHV = 20 V AVDD = 3.3 V
$I_{L\_BOOST\_SS0}$	Average inductor current, 6 outputs @ 0 V steady state	−	500	790		At VHV = 20 V AVDD = 3.3 V
$I_{L\_BOOST\_SS2}$	Average inductor current, 6 outputs @ 2 V steady state	−	560	850		At VHV = 20 V AVDD = 3.3 V
$I_{L\_BOOST\_SS16}$	Average inductor current, 6 outputs @ 16 V steady state	−	930	1,270		At VHV = 20 V AVDD = 3.3 V
I_{VIO_INACT}	VIO average inactive current	−	−	3		VIO is high, no bus activity
I_{VIO_ACTIVE}	VIO average active current	−	−	250		VIO = 1.8 V, master sending data at 26 MHz
V_{VREG}		1.7	−	1.9	V	No external load allowed

Table 4. DC CHARACTERISTICS (T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V<AVDD< 5.5 V; V_{IO} = 1.8 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
LOW POWER MODE						
I_{AVDD}	AVDD Supply Current	−	−	8	μA	
I_{L_BOOST}	L_BOOST Leakage	−	−	6		
I_{BATT}	Battery Current	−	−	14		I_{AVDD} + I_{L_BOOST}
I_{VIO}	VIO Supply Current	−	−	3		No bus activity
V_{VREG}		1.6	−	1.9	V	No external load allowed

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. BOOST CONVERTER CHARACTERISTICS
(AVDD from 2.3 V to 5.5 V; V_{IO} = 1.8 V; T_A = –30 to +85°C; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VHV_min	Minimum programmable output voltage (average), DAC Boost = 0h	Active mode	−	13	−	V
VHV_max	Maximum programmable output voltage (average), DAC Boost = Fh	Active mode	−	28	−	
Resolution	Boost voltage resolution	4−bit DAC	−	1	−	
$I_{L\_BOOST\_LIMIT}$	Inductor current limit		−	200	−	mA

Table 6. ANALOG OUTPUTS (OUT A, OUT B, OUT C, OUT D, OUT E, OUT F)
(AVDD from 2.3 V to 5.5 V; V_{IO} = 1.8 V; V_{HV} = 26 V; T_A = –30 to +85°C; R_{load} = ∞ unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
SHUTDOWN MODE						
Z_{OUT}	OUT A, OUT B, OUT C , OUT D, OUT E,OUT F output impedance	7	−	−	MΩ	DAC disabled
ACTIVE MODE						
V_{OH}	Maximum output voltage	−	23.8	−	V	DAC A, B, C, D, E or F = 7Fh, DAC Boost = Fh, I_{OH} < 10 μA
V_{OL}	Minimum output voltage	−	−	1	V	DAC A, B C, D, E or F = 01h, DAC Boost = 0h to Fh, I_{OH} < 10 μA
Slew Rate		−	3	10	μs	2 V to 20 V step, measured at V_{OUT} = 15.2 V, R_{LOAD} = equivalent series load of 2.7 kΩ and 5.6 nF, Turbo enabled
R_{PD}	OUT A, OUT B, OUT C, OUT D, OUT E, OUT F set in pull−down mode	−	−	1000	Ω	DAC A, B C, D, E or F = 00h, DAC Boost = 0h to Fh, selected output(s) is disabled
Resolution	Voltage resolution (1−bit)	−	188	−	mV	(1 LSB = 1−bit)
V_{OFFSET}	Zero scale, least squared best fit	−1	−	+1	LSB	
Error		−3.0	−	+3.0	%V_{OUT}	Over 2 V – 20 V V_O range
DNL	Differential non−linearity least squared best fit	−0.9	−	+0.9	LSB	Over 2 V – 20 V V_O range
INL	Integral non−linearity least squared best fit	−1	−	+1	LSB	Over 2 V – 20 V V_O range
I_{SC}	Over current protection	−	5	65	mA	Any DAC output shorted to ground
V_{RIPPLE}	Output ripple with all outputs at steady state	−	−	40	mV RMS	Over 2 V – 20 V for VHV = 23.5 V

THEORY OF OPERATION

Overview

The control IC outputs are directly controlled by programming the six DACs (DAC A, DAC B, DAC C, DAC D, DAC E and DAC F) through the digital interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high−voltage amplifier supplied from the boost converter (see Figure 1 − Control IC Functional Block Diagram).

The control IC output voltages are scaled from 0 V to 24 V, with 128 steps of 188 mV ((2 x 24 / 255 V) = 0.188235 V). The nominal control IC output can be approximated to 188 mV x (DAC value).

For performance optimization the boost output voltage (VHV) can be programmed to levels between 13 V and 28 V via the DAC_boost register (4 bits with 1 V steps). The startup default level for the boosted voltage is VHV = 24 V.

For proper operation and to avoid saturation of the output devices and noise issues it is recommended to operate the boosted VHV voltage at least 2 V above the highest programmed V_{OUT} voltage of any of the six outputs.

Operating Modes

The following operating modes are available:

1. **Shutdown Mode:** All circuit blocks are off, the DAC outputs are disabled and placed in high Z state and current consumption is limited to minimal leakage current. The shutdown mode is entered upon initial application of AVDD or upon VIO being placed in the low state. The contents of the registers are not maintained in shutdown mode.
2. **Startup Mode:** Startup is only a transitory mode. Startup mode is entered upon a VIO high state. In startup mode all registers are reset to their default states, the digital interface is functional, the boost converter is activated, outputs OUT A, OUT B, OUT C, OUT D, OUT E and OUT F are disabled and the DAC outputs are placed in a high Z state. Control software can request a full hardware and register reset of the TCC−206 by sending an appropriate PWR_MODE command to direct the chip from either the active mode or the low power mode to the startup mode. From the startup mode the device automatically proceeds to the active mode.
3. **Active Mode:** All blocks of the TCC−206 are activated and the DAC outputs are fully controlled through the digital interface, DACs remain off until enabled. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. Active mode is automatically entered from the startup mode. Active mode can also be entered from the low power mode under control software command.
4. **Low Power Mode:** In low power mode the serial interface stays enabled, the DAC outputs are disabled and are placed in a high Z state and the boost voltage circuit is disabled. Control software can request to enter the low power mode from the active mode by sending an appropriate PWR_MODE command. The contents of all registers are maintained in the low power mode.

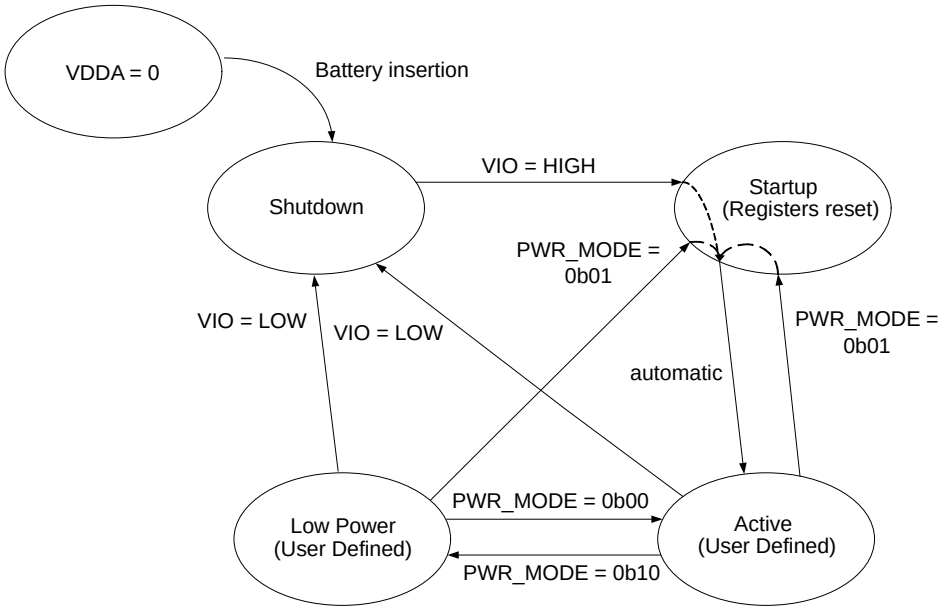


Figure 3. Modes of Operation

AVDD Power−On Reset (POR)

Upon application of AVDD the TCC−206 will be in shutdown mode. All circuit blocks are off and the chip draws only minimal leakage current.

VIO Power−On Reset and Startup Conditions

A high level on VIO places the chip in startup mode which provides a POR to the TCC−206. POR resets all registers to their default settings as described in Table 8. VIO POR also resets the serial interface circuitry. POR is not a brown−out detector and VIO needs to be brought back to a low level to enable the POR to trigger again.

Table 7. VIO POWER−ON RESET AND STARTUP

Register	Default State for VIO POR	Comment
DAC Boost	[1011]	VHV = 24 V
Power Mode	[01]>[00]	Transitions from shutdown to startup and then automatically to active mode
DAC Enable	[000000]	V_{OUT} A, B, C, D, E and F Disabled
DAC A		Output in High−Z Mode
DAC B		Output in High−Z Mode
DAC C		Output in High−Z Mode
DAC D		Output in High−Z Mode
DAC E		Output in High−Z Mode
DAC F		Output in High−Z Mode

VIO Shutdown

A low level at any time on VIO places the chip in shutdown mode in which all circuit blocks are off. The contents of the registers are not maintained in shutdown mode.

Table 8. VIO THRESHOLDS (AVDD from 2.3 V to 5.5 V; T_A = –30 to +85°C unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
VIORST	VIO Low Threshold	−	−	0.2	V	When VIO is lowered below this threshold level the chip is reset and placed into the shutdown state

Power Supply Sequencing

The AVDD input is typically directly supplied from the battery and thus is the first on. After AVDD is applied and before VIO is applied to the chip, all circuits are in the shutdown state and draw minimum leakage currents. Upon application of VIO, the chip automatically starts up using default settings and is placed in the active state waiting for a command via the serial interface.

Table 9. TIMING (AVDD from 2.3 V to 5.5 V; V_{IO} = 1.8 V; T_A = –30 to +85°C; OUT A, OUT B, OUT C, OUT D, OUT E & OUT F; CHV = 22 nF; L_{BOOST} = 15 μH; VHV = 20 V; Turbo−Charge mode off unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
T_{POR_VREG}	Internal bias settling time from shutdown to active mode	−	50	120	μs	For info only
T_{BOOST_START}	Time to charge CHV @ 95% of set VHV	−	130	−	μs	For info only
$T_{SD\_TO\_ACT}$	Startup time from shutdown to active mode	−	180	300	μs	
T_{SET+}	Output A, B, C, D, E, F positive settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 2 V to 20 V; 0Bh (11d) to 55h (85d)	−	50	60	μs	Voltage settling time connected on V_{OUT} A, B, C, D, E, F
$T_{SET−}$	Output A, B, C, D, E, F negative settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 20 V to 2 V; 55h (85d) to 0Bh (11d)	−	50	60	μs	Voltage settling time connected on V_{OUT} A, B, C, D, E, F
T_{SET+}	Output A, B, C, D, E, F positive settling time with Turbo	−	35	−	μs	Voltage settling time connected on V_{OUT} A, B, C, D, E, F
$T_{SET−}$	Output A, B, C, D, E, F negative settling time with Turbo	−	35	−	μs	Voltage settling time connected on V_{OUT} A, B, C, D, E, F

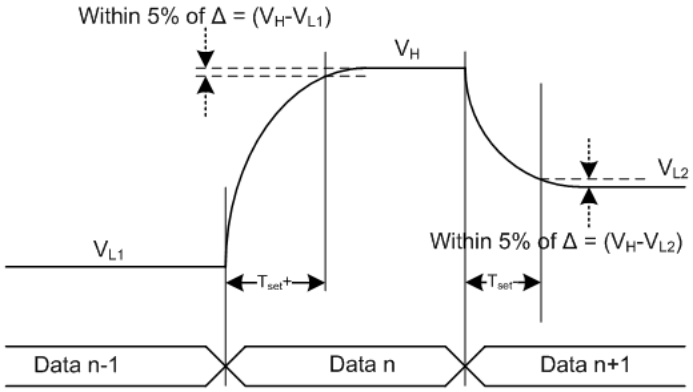


Figure 4. Output Settling Diagram

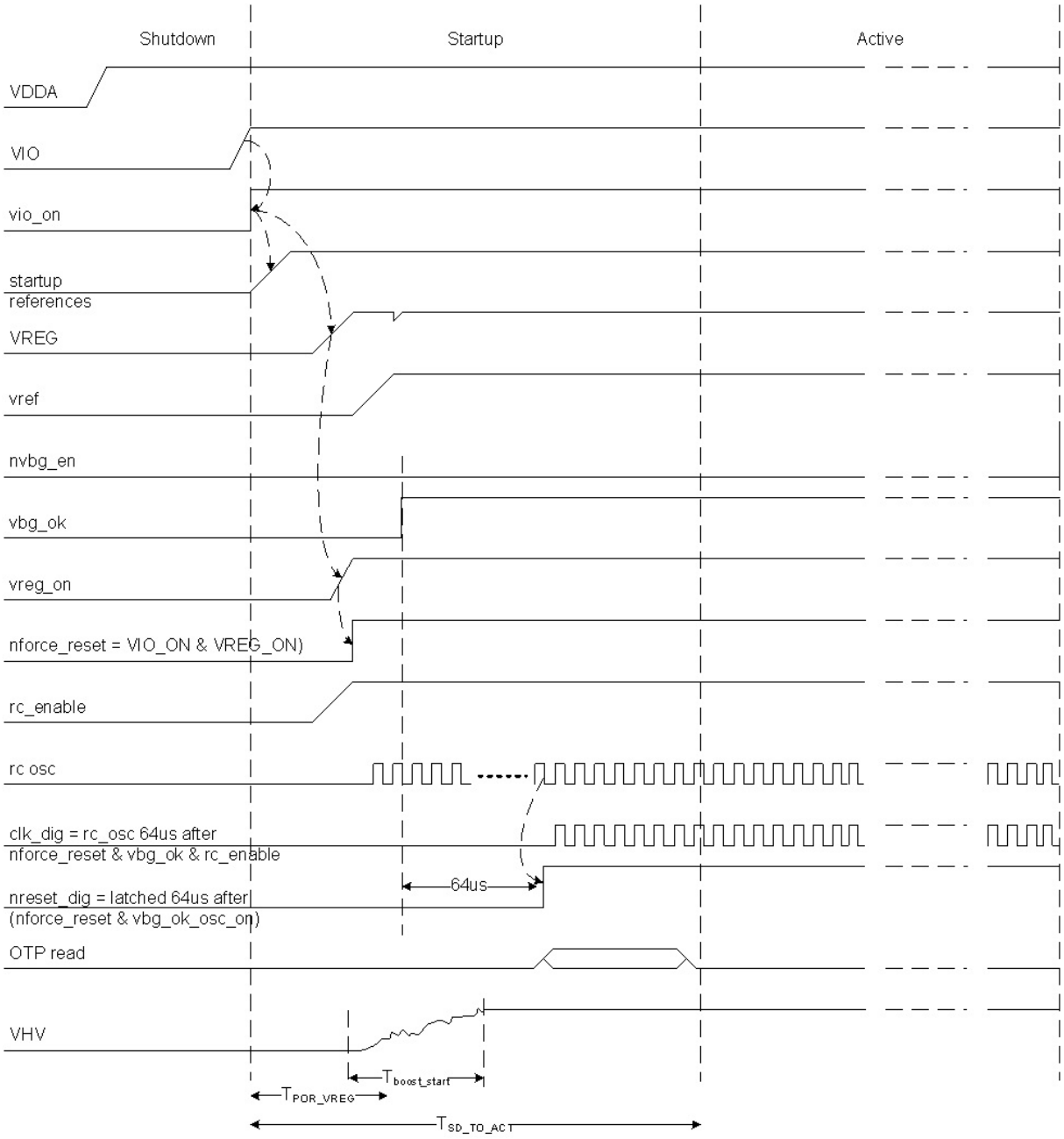


Figure 5. Startup Timing Diagram

Boost Control

The TCC−206 integrates an asynchronous current control boost converter. It operates in a discontinuous mode and features spread−spectrum circuitry for Electro−Magnetic Interference (EMI) reduction. The average boost clock is 2 MHz and the clock is spread between 0.8 MHz and 4 MHz.

Boost Output Voltage (VHV) Control Principle

The asynchronous control starts the boost converter as soon as the VHV voltage drops below the reference set by the 4−bit DAC and stops the boost converter when the VHV voltage rises above the reference again.

Due to the slow response time of the control loop, the VHV voltage may drop below the set voltage before the control loop compensates for it. In the same manner, VHV can rise higher than the set value. This effect may reduce the maximum output voltage available. Please refer to Figure 7 below.

The asynchronous control reduces switching losses and improves the output (VHV) regulation of the DC/DC converter under light load, particularly in the situation where the TCC−206 only maintains the output voltages to fixed values.

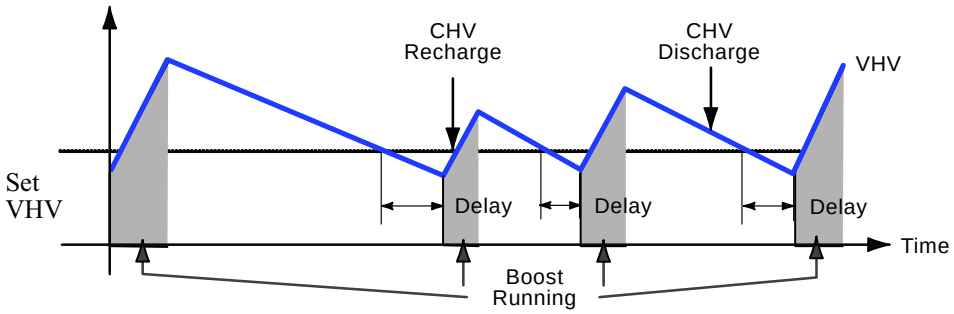


Figure 6. VHV Voltage Waveform

High Impedance (High Z) Feature

In shutdown mode the OUT pins are set to a high impedance mode (high Z). Following is the principle of operation for the control IC:

1. The DAC output voltage V_{OUT} is defined by:

$$V_{OUT} = \frac{\text{DAC code}}{255} \times 24\ V \times 2 \qquad \text{(eq. 1)}$$

2. The voltage VHV defines the maximum supply voltage of the DAC supply output regulator and is set by a 4−bit control.
3. The maximum DAC DC output voltage V_{OUT} is limited to (VHV – 2 V).
4. The minimum output DAC voltage V_{OUT} is 1.0 V max.

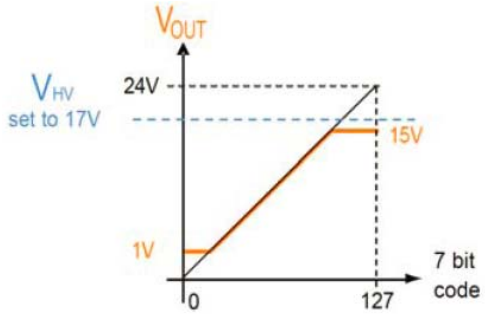


Figure 7. DAC Output Range Example A

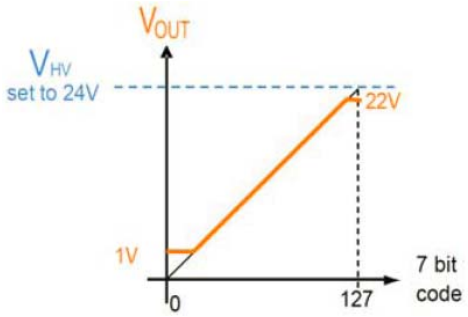


Figure 8. DAC Output Range Example B

Digital Interface

The control IC is fully controlled through a digital interface (DATA, CLK, CS). The digital interface automatically detects and responds to MIPI RFFE interface commands, 3−wire 30−bit serial interface commands or 3−wire 32−bit serial interface commands. Auto−detection is accomplished on a frame by frame basis. The digital interface is described in the following sections of this document, for detailed programming instructions please refer to the programming guide, available by contacting ON Semiconductor.

3−Wire Serial Interface

The 3−wire serial interface operates in a synchronous write−only 3−wire slave mode. 30−bit or 32−bit message length is automatically detected for each frame. If CS changes state before all bits are received then all data bits are ignored. Data is transmitted most significant bit first and DATA is latched on the rising edge of CLK. Commands are latched on the falling edge of CS.

Table 10. 3−WIRE SERIAL INTERFACE SPECIFICATION

(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; V_{IO} = 1.8 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
F_{CLK}	Clock Frequency	−	−	26	MHz	
T_{CLK}	Clock Period	38.4	−	−	ns	
N_{BIT}	Bits Number	−	30/32	−	bits	Auto−detection 30−bit or 32−bit
T_{HIGH}	Clock High Time	13	−	−	ns	
T_{LOW}	Clock Low Time	13	−	−	ns	
TCS_{SETUP}	CS Set−up Time	5	−	−	ns	70% rising edge of CS to 30% rising edge of first clock cycle
TCS_{HOLD}	CS Hold Time	5	−	−	ns	30% falling edge of last clock cycle to 70% falling edge of CS
TD_{SETUP}	Data Set−up Time	4	−	−	ns	Relative to 30% of CLK rising edge
TD_{HOLD}	Data Hold Time	4	−	−	ns	relative to 70% of CLK rising edge
T_{SUCC}	CS Low Time Between Successive Writes	38.4	−	−	ns	70% falling edge of CS to 70% rising edge of CS
T_{SUCC}	CS Low Time Between Successive DAC Update Writes	1,500	−	−	ns	Time between groups of DAC update reg [00000] & [00001] writes
C_{CLK}	Input Capacitance	−	−	5	pF	CLK pin
C_{DATA}	Input Capacitance	−	−	8.3	pF	DATA pin
C_{CS}	Input Capacitance	−	−	5	pF	CS pin
C_{TRIG}	Input Capacitance	−	−	10	pF	TRIG pin
V_{IH}	Input Logic Level High	0.7 x VIO	−	VIO x 0.3	V	DATA, CLK, CS
V_{IL}	Input Logic Level Low	−0.3	−	0.3 x VIO	V	DATA, CLK, CS
I_{IH_DATA}	Input Current High	−2	−	10	μA	DATA
I_{IL_DATA}	Input Current Low	−2	−	1	μA	DATA
$I_{IH\_CLK,CS}$	Input Current High	−1	−	10	μA	CLK, CS
$I_{IL\_CLK,CS}$	Input Current Low	−1	−	1	μA	CLK, CS
V_{TP_TRIG}	Positive Going Threshold Voltage	0.4 x VIO	−	0.7 x VIO	V	TRIG
V_{TN_TRIG}	Negative Going Threshold Voltage	0.3 x VIO	−	0.6 x VIO	V	TRIG
V_{H_TRIG}	Hysteresis Voltage ($V_{TP} – V_{TN}$)	0.1 x VIO	−	0.4 x VIO	V	TRIG
I_{IH_TRIG}	TRIG Input Current High	−2	−	10	μA	TRIG=0.8 x VIO
I_{IL_TRIG}	TRIG Input Current Low	−2	−	1	μA	TRIG=0.2 x VIO

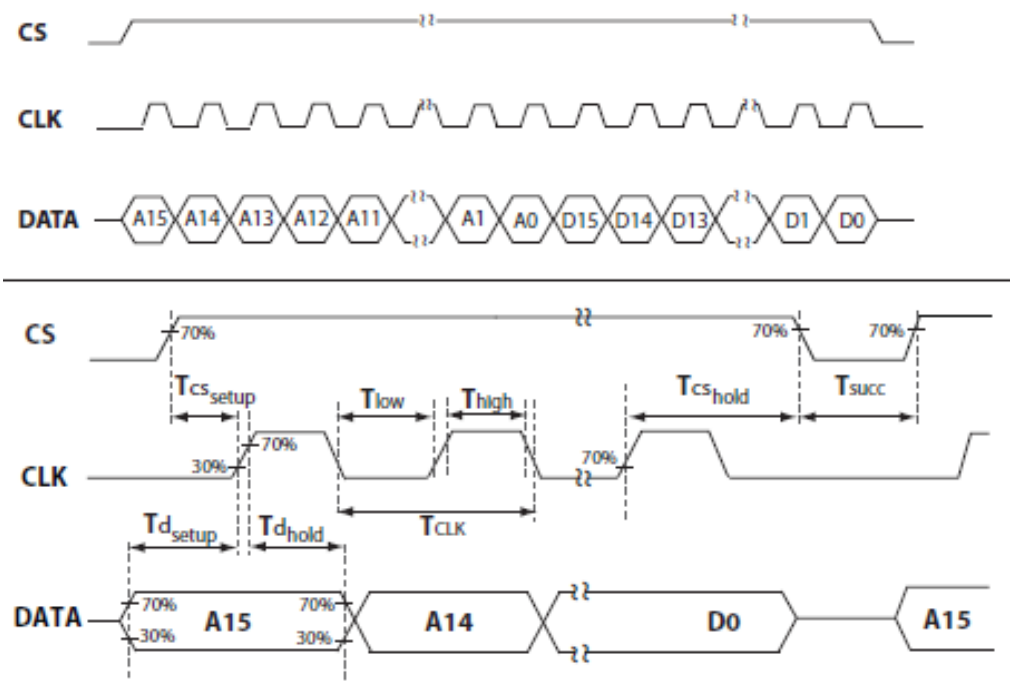


Figure 9. 3−wire Serial Interface Signal Timing

SPI Frame Length Decoding

30−bit or 32−bit frame length is automatically detected. The length of the frame is defined by the number of clock rising edges while CS is kept high. The TCC−206 will not respond to a SPI command if the length of the frame is not exactly 30 bits or 32 bits. SPI registers are write only.

SPI Frame Structure

Table 11. 32 BITS FRAME: ADDRESS DECODING (1, 2, 3, 4, 5 or 6 OUTPUTS)

H0	H1	R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	1	0	0	1	0	0	X	X	X	X	X
ON Semiconductor Header		R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 12. 30 BITS FRAME: ADDRESS DECODING (1, 2, 3, 4, 5 or 6 OUTPUTS)

R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	1	0	0	X	X	X	X	X
R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 13. 3−WIRE SERIAL INTERFACE ADDRESS MAP

A4	A3	A2	A1	A0	Data[15:8]	Data[7:0]
0	0	0	0	0	Turbo−Charge Settings for DAC A, B, C	DAC C
0	0	0	0	1	DAC B	DAC A
0	0	0	1	0	Turbo−Charge Settings for DAC D, E, F	DAC F
0	0	0	1	1	DAC E	DAC D
0	0	1	0	0	Turbo−Charge Delay Parameters for DAC A, B, C	Turbo Threshold Delay Settings for A, B, C
0	0	1	0	1	Turbo−Charge Delay Parameters for DAC D, E, F	Turbo Threshold Delay Settings for A, B, C
1	0	0	0	0	Mode Select + Control IC Setup	

Table 13. 3−WIRE SERIAL INTERFACE ADDRESS MAP

1	0	0	1	0	Reserved	Reserved
to						
1	1	1	1	1		

Turbo−Charge Mode

The TCC−206 control IC has a Turbo−Charge mode that significantly shortens the system settling time when changing programming voltages. In Turbo−Charge mode the DAC output target voltage is temporarily set to either a delta voltage above or a delta voltage below the actual desired target for the TCDLY time. It is recommended that V_{HV} be set to 26 V when using Turbo−Charge mode.

Glide Mode

Unlike turbo mode, which is intended to reduce the charging time, the glide mode extends the transition time of each DAC output. Each DAC has an individual control for turbo mode, glide mode or regular voltage switching. The glide mode can be enabled for a particular DAC through the INDEX register, by setting DAC State to ‘1’ when glide mode is enabled, turbo mode is off for a particular DAC, but one DAC can be gliding while the other is turbo.

During glide mode the output voltage of a DAC is either increased or decreased to its set end point, in max 255 steps, where each DAC time step can be programmed between 2 μs to 64 μs. For programming the glide mode refer to the application note (coming soon). A programming input is not required to maintain a glide transition, all step controls are maintained by the part. Only the inputs to define the glide need to be programmed.

RF Front−End Control Interface (MIPI RFFE Interface)

The TCC−206 is a read/write slave device which is fully compliant to the MIPI Alliance Specification for RF Front−End Control Interface (RFFE) Version 1.10.00 26 July 2011. This device is rated at full−speed operation for 1.65 V<VIO<1.95 V and at half−speed operation for 1.1 V<VIO<1.65 V. When using the MIPI RFFE interface the CS pin must be grounded externally.

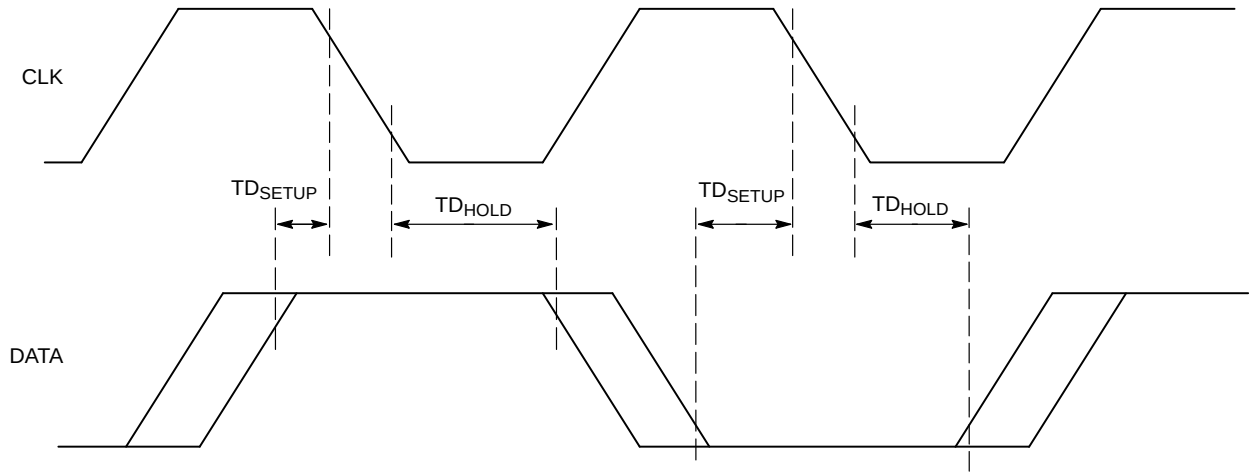


Figure 10. MIPI−RFFE Signal Timing during Master Writes to PTIC Control IC

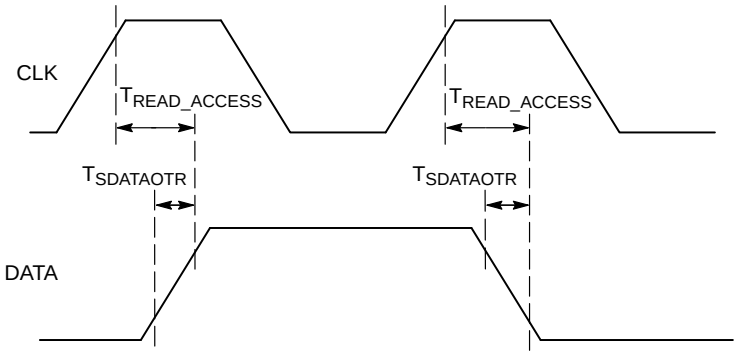


Figure 11. MIPI−RFFE Signal Timing during Master Reads from PTIC Control IC

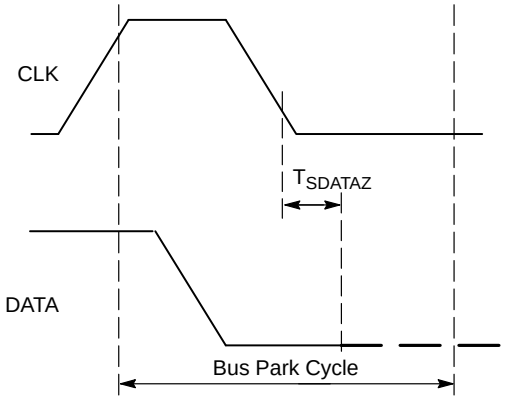


Figure 12. Bus Park Cycle Timing when MIPI−RFFE Master Reads from PTIC Control IC

Table 14. MIPI RFFE INTERFACE SPECIFICATION
(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; 1.1 V < V_{IO} < 1.8 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comments
F_{SCLK}	Clock Full−Speed Frequency	0.032	−	26	MHz	Full−Speed Operation: 1.65 V < V_{IO} < 1.95 V
T_{SCLK}	Clock Full−Speed Period	0.038	−	32	μs	Full−Speed Operation: 1.65 V < V_{IO} < 1.95 V
T_{SCLKIH}	CLK Input High Time	11.25	−	−	ns	Full−Speed
T_{SCLKIL}	CLK Input Low Time	11.25	−	−	ns	Full−Speed
V_{TP}	Positive Going Threshold Voltage	0.4 x VIO	−	0.7 x VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_{TN}	Negative Going Threshold Voltage	0.3 x VIO	−	0.6 x VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_H	Hysteresis Voltage (V_{TP} – V_{TN})	0.1 x VIO	−	0.4 x VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
I_{IH}	Input Current High	−2	−	+10	μA	TRIG,SDATA = 0.8 x VIO
		−1	−	+10	μA	SCLK = 0.8 x VIO
I_{IL}	Input Current Low	−2	−	+1	μA	TRIG,SDATA = 0.2 x VIO
		−1	−	+1	μA	SCLK = 0.2 x VIO
C_{CLK}	Input Capacitance	−	−	5	pF	CLK Pin
C_{DATA}	Input Capacitance	−	−	8.3	pF	DATA Pin
C_{TRIG}	Input Capacitance	−	−	10	pF	TRIG Pin
TD_{SETUP}	Write DATA Setup Time	−	−	1	ns	Full−Speed
TD_{HOLD}	Write DATA Hold Time	−	−	5	ns	Full−Speed
T_{READ_ACCESS}	Read DATA valid from CLK rising edge	−	−	7.11	ns	Full Speed at V_{IO} = 1.80 V, +25°C, and max 15 pF load on DATA pin
T_{READ_ACCESS}	Read DATA valid from CLK rising edge	−	−	9.11	ns	Full Speed at V_{IO} = 1.80 V, +25°C, and max 50 pF load on DATA pin

The control IC contains twenty−four 8−bit registers. Register content is described in Table 15. Some additional registers implemented as provision, are not described in this document.

Table 15. MIPI RFFE ADDRESS MAP

Register Address	Description	Purpose	Access Type	Size (bits)
0x00	DAC Configuration (Enable Mask)	High voltage output enable mask	Write Reg0	7
0x01	Turbo Register DAC A, B & C	Turbo−charge configuration DAC A, B & C	Write	8
0x02	DAC A Register	OUT A value [6:0], Turbo Index [7]**	Write	8
0x03	DAC B Register	OUT B value [6:0], Turbo Index [7]**	Write	8
0x04	DAC C Register	OUT C value [6:0], Turbo Index [7]**	Write	8
0x05	Turbo Register DAC D, E & F	Turbo−charge configuration DAC D,E & F	Write	8
0x06	DAC D Register	OUT D value [6:0], Turbo Index [7]**	Write	8
0x07	DAC E Register	OUT E value [6:0], Turbo Index [7]**	Write	8
0x08	DAC F Register	OUT F value [6:0], Turbo Index [7]**	Write	8
0x09	Wake Up	Wake Up Controls	Write	8
0x10	DAC Boost (VHV)	Settings for the boost high voltage	Write	8
0x11	Trigger register	Trigger configuration	Write	8
0x12	Turbo−Charge Delay DAC A, B, C	Turbo−charge delay steps DAC A, B, C	Write	8
0x13	Turbo−Charge Delay DAC A, B, C	Turbo−charge delay, multiplication DAC A, B, C	Write	8
0X14	Turbo−Charge Delay DAC D, E, F	Turbo−charge delay steps DAC D, E, F	Write	8
0X15	Turbo−Charge Delay DAC D, E, F	Turbo−charge delay multiplication DAC D, E, F	Write	8
0x1A	RFFE_STATUS	RFFE status register	Read/Write	8
0x1B	RFFE_GROUP_SID		Read/Write	8
0x1C	Power Mode and Trigger Register	Power mode & trigger control PWR_MODE [7:6] TRIG_REG [5:0]	Read/Write	8
0x1D	Product ID Register	Product number * Hard coded into ASIC	Read	8
0x1E	Manufacturer ID Register	MN (10 bits long) Manufacturer ID[7:0] Hard Coded into ASIC	Read	8
0x1F	Unique Slave Identifier Register (USID)	Spare [7:6] [5,4] = Manufacturer ID [9:8] USID [3:0]	Read/Write	8
0x2C	Glide Timer Settings	[6:5] Turbo and glide control / [4:0] Glide timer setting / Need extended write for this register	Write	8

*The second least significant bit can be programmed in OTP during manufacture
** The details for configuration of Turbo mode should be ascertained from the Programming Guide, available from ON Semiconductor

Configuration Settings

Table 16. DAC CONFIGURATION (ENABLE MASK) at [0x00] Defaults shown as (x)

Bit 6 (1)	Bit 5 (0)	Bit 4 (0)	Bit 3 (0)	Bit 2 (0)	Bit 1 (0)	Bit 0 (0)
SSE	DAC E	DAC F	DAC A	DAC B	DAC C	DAC D

SSE = 0 spread spectrum disabled, SSE = 1 spread spectrum enabled (default), this controls the average boost clock which is nominally 2 MHz and spread between 0.8 MHz and 3.2 MHz when enabled (default). The hardware does not limit driving more than three DACs at the same time, however it is recommended to have max three DACs changing outputs at one time, no restrictions exist as to which three.

Table 17. DAC MODE SETUP: DAC ENABLE

Bit3	Bit2	Bit1	DAC A	DAC B	DAC C	
0	0	0	Off	Off	Off	(Default)
0	0	1	Off	Off	Enabled	
0	1	0	Off	Enabled	Off	
0	1	1	Off	Enabled	Enabled	
1	0	0	Enabled	Off	Off	
1	0	1	Enabled	Off	Enabled	
1	1	0	Enabled	Enabled	Off	
1	1	1	Enabled	Enabled	Enabled	

Table 18. DAC MODE SETUP: DAC ENABLE

Bit5	Bit4	Bit0	DAC E	DAC F	DAC D	
0	0	0	Off	Off	Off	(Default)
0	0	1	Off	Off	Enabled	
0	1	0	Off	Enabled	Off	
0	1	1	Off	Enabled	Enabled	
1	0	0	Enabled	Off	Off	
1	0	1	Enabled	Off	Enabled	
1	1	0	Enabled	Enabled	Off	
1	1	1	Enabled	Enabled	Enabled	

Table 19. BOOST DAC MODE SETUP (VHV) at [0x10] (Notes 5 and 6)

Bit 7*	Bit 6*	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	VHV (V)
0	0	0	1	0	0	0	0	13
0	0	0	1	0	0	0	1	14
0	0	0	1	0	0	1	0	15
0	0	0	1	0	0	1	1	16
0	0	0	1	0	1	0	0	17
0	0	0	1	0	1	0	1	18
0	0	0	1	0	1	1	0	19
0	0	0	1	0	1	1	1	20
0	0	0	1	1	0	0	0	21
0	0	0	1	1	0	0	1	22
0	0	0	1	1	0	1	0	23
0	0	0	1	1	0	1	1	24 (Default)
0	0	0	1	1	1	0	0	25
0	0	0	1	1	1	0	1	26
0	0	0	1	1	1	1	0	27
0	0	0	1	1	1	1	1	28

*Indicates reserved bits
5. Bit 4 is fixed at logic 1 for reverse software compatibility
6. VHV is recommended to be set at VDac Max + 2 V for non−turbo operation and +4 when turbo is used.* Indicates reserved bits.

MIPI RFFE TRIG Operation

The MIPI RFFE Trigger mode can be used as a synchronization signal to ensure that new DAC settings are applied to the outputs at appropriate times in the overall transceiver system. When the MIPI RFFE TRIG function is enabled via [0x11] bit 4 the requested DAC voltage levels are set up in the shadow registers and not transferred to the destination registers until the trigger condition is met. In this manner the change in output voltage levels are synchronized with the MIPI RFFE TRIG command. If multiple DAC voltage level requests are received before the TRIG event occurs, only the last fully received DAC output voltage level will be applied to the outputs.

The trigger configuration also provides for an additional external TRIG pin to be used as a synchronization signal. The external TRIG is independent from the built−in triggers available within the MIPI RFFE interface. When the TRIG input pin is enabled via [0x11] bit 4 the requested DAC voltage levels are set up in the shadow registers and are not transferred to the destination registers until the external trigger condition is met. In this manner the change in output voltage levels are synchronized with the external TRIG event. The external TRIG input is referenced to VIO. To improve interfacing options the polarity of external TRIG is programmable via [0x11] bit 1.

If the external trigger function is not needed in the application, the TRIG pin should be grounded and the TRIG function disabled. When TRIG pin is disabled by register [0x11] ‘TRIG Select’ = ‘1’ (default) and register [0x10] ‘Trigger Mask 0, 1, 2’ = ‘1’:

- The requested DAC voltage levels for DAC A, B, C are applied to the outputs all together at the same time, after DAC C value is written. This event will not affect the outputs of DAC D, E, F.
- The requested DAC voltage levels for DAC D, E, F are applied to the outputs all together at the same time, after DAC F value is written. This event will not affect the outputs of DAC A, B, C.
- Optionally a configuration register can select the last DAC to be written in order to trigger internally the update of all six DACs at the same time. For example the configuration register can select that a write to DAC B value will trigger internally the update of all six DACs outputs.

Table 20. TRIGGER CONFIGURATION at [0x11]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Res* 0	Res* 0	Res* 0	TRIG Select 0 = Ext TRIG Pin 1 = RFFE Trigger	Reserved 0		TRIG Edge 0 = Active Falling 1 = Active Rising	Mask Ext TRIG 1 = Mask Trig Pin

*Reserved bits

Table 21. EXTERNAL TRIGGER CONFIGURATION BIT SETTING AT [0x11]

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
0	−	−	X	0	External trigger pin is enabled. Sending the RFFE message will load a ‘shadow’ register only. Only upon an active signal on external TRIG pin are the output registers loaded with the new voltage settings which are then applied to the outputs.
1	−	−	X	X	The MIPI RFFE trigger is enabled (Default)
0	−	−	0	0	External TRIG pin signal is active falling
0	−	−	1	0	External TRIG pin signal is active rising (Default)
X	−	−	X	0	External trigger pin is not masked
X	−	−	X	1	Mask external trigger pin (Default)

Table 22. POWER MODE AND TRIGGER REGISTER [0x1C]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PM1	PM0	Trigger Mask 2	Trigger Mask 1	Trigger Mask 0	Trigger 2	Trigger 1	Trigger 0

Writing a logic one (‘1’) to the bits 0, 1 or 2 (Trigger 0, 1 or 2) moves data from the shadow registers into the destination registers. Default for bit 0, 1 and 2 is logic low.

If trigger mask bit 0, 1 or 2 is set (‘1’) the trigger 0, 1 or 2 are disabled respectively and the data goes directly to the destination register. Default for bit 3, 4 and 5 is logic low.

All three triggers behave in the same way as the external pin TRIG. When each of these triggers is set using the MIPI RFFE interface the results are the same as when an active edge is applied to the TRIG pin when external pin TRIG is selected

Table 23. POWER MODE BIT SETTING IN REGISTER [0x1C]

PM1	PM0	State	Description
0	0	Active	Boost Control Active, VHV set by Digital Interface V_{OUT} A, B, C, D, E, F Enabled and Controlled by Digital Interface (Default)
0	1	Startup	Boost Control Active, VHV set by Digital Interface V_{OUT} A, B, C, D, E, F Disabled
1	0	Low Power	Digital Interface is Active While All Other Circuits are in Low Power Mode
1	1	Reserved	State of Hardware Does Not Change

Command Sequences

- **Register 0 Write** (used to access the Register 0 DAC Configuration − Enable Mask). Register 0 can be also be accessed using Register Write or/and Extended Register Write.
- **Register Write** (used to access only one register at the time)
- **Extended Register Write** (used to access a group of contiguous registers with one command)

Register 0 Write Command Sequence

The Command Sequence starts with a Sequence Start Condition (SSC) which is followed by the Register 0 Write Command Frame. This Frame contains the Slave address, a logic one, and the seven bit word that will be written to Register 0. The Command Sequence is depicted below.

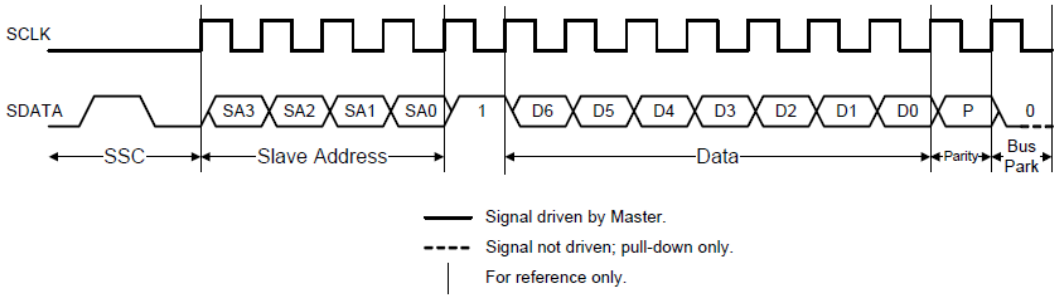


Figure 13. Register 0 Write Command Sequence

Table 24. MIPI RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										BP
SSE & DAC Configuration	1	0	SA [3,0]	1	SSE	DAC_E	DAC_F	DAC_A	DAC_B	DAC_C	DAC_D	P	BP

Register Write Command Sequence

The write register command sequence may be used to access each register (addresses 0−31).

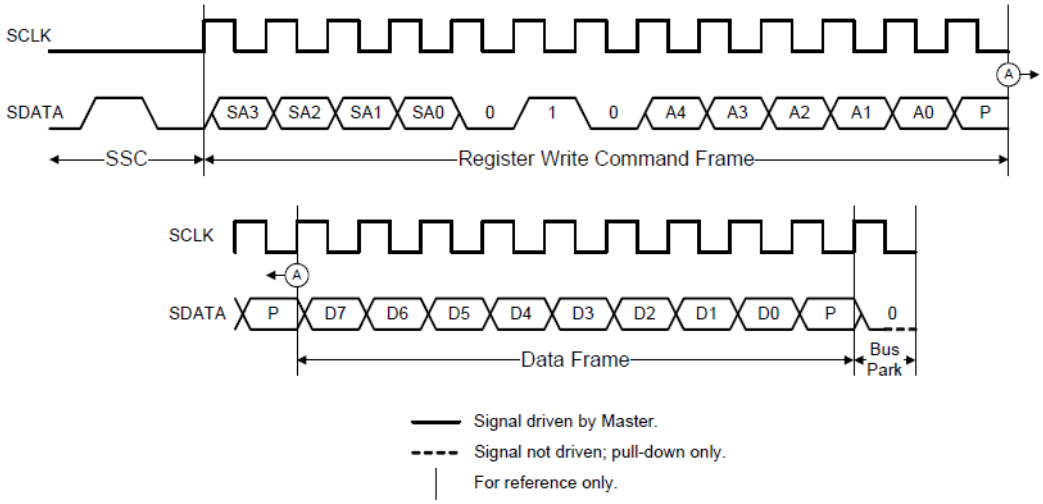


Figure 14. Register Write Command Sequence

Table 25. MIPI RFFE COMMAND FRAME FOR REGISTER WRITE COMMAND SENTENCE

Description	SSC		Command Frame									Data Frame		BP
Turbo−Charge Settings	1	0	SA [3,0]	0	1	0	0	0	0	0	1	P	TC_INDX_L [7:0]	P	BP
Register Write DAC A	1	0	SA [3,0]	0	1	0	0	0	0	1	0	P	TC_INDX_L [8] & DAC_A [6:0]	P	BP
Register Write DAC B	1	0	SA [3,0]	0	1	0	0	0	0	1	1	P	TC_INDX_L [9] & DAC_B [6:0]	P	BP
Register Write DAC C	1	0	SA [3,0]	0	1	0	0	0	1	0	0	P	TC_INDX_L [10] & DAC_C [6:0]	P	BP

Table 26. MIPI RFFE COMMAND FRAME FOR REGISTER WRITE COMMAND SENTENCE

Description	SSC		Command Frame									Data Frame		BP
Turbo−Charge Settings	1	0	SA [3,0]	0	1	0	0	0	1	0	1	P	TC_INDX_U [7:0]	P	BP
Register Write DAC D	1	0	SA [3,0]	0	1	0	0	0	1	1	0	P	TC_INDX_U [8] & DAC_D [6:0]	P	BP
Register Write DAC E	1	0	SA [3,0]	0	1	0	0	0	1	1	1	P	TC_INDX_U [9] & DAC_E [6:0]	P	BP
Register Write DAC F	1	0	SA [3,0]	0	1	0	0	1	0	0	0	P	TC_INDX_U [10] & DAC_F [6:0]	P	BP

Extended Register Write Command Sequence

In order to access more than one register in one sequence this message could be used. Most commonly it will be used for loading three DAC registers at the same time. The four LSBs of the extended register write command frame determine the number of bytes that will be written by the command sequence. A value of 0b0000 would write one byte and a value of 0b1111 would write 16 bytes.

If more than one byte is to be written, the register address in the command sequence contains the address of the first extended register that will be written to and the slave's local extended register address shall be automatically incremented by one for each byte written up to address 0x1F, starting from the address indicated in the address frame.

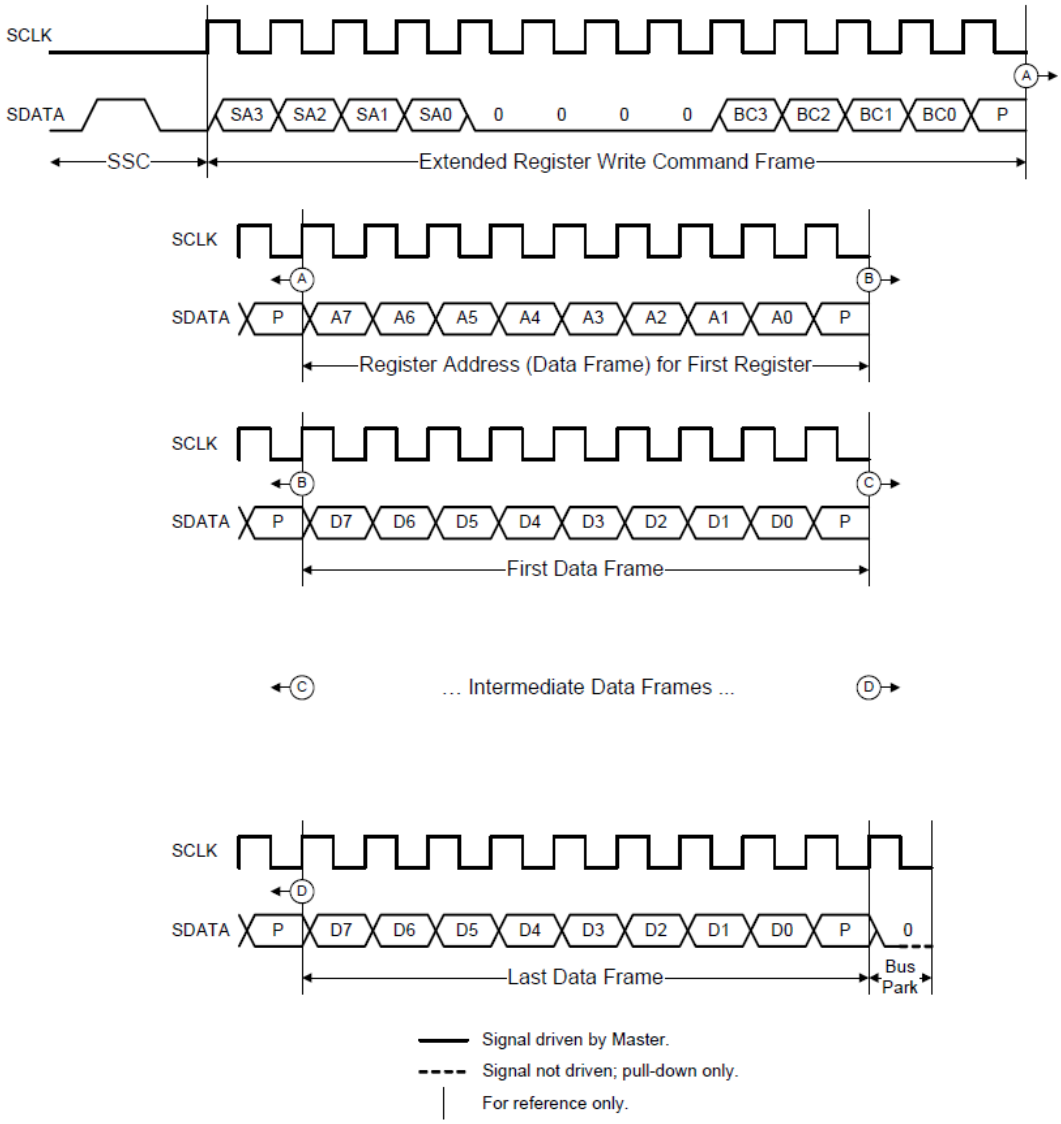


Figure 15. Extended Register Write Command Sequence

Table 27. EXTENDED REGISTER WRITE TO UPDATE DAC A, B, C (Note 7)

Description	SSC		Command Frame										Address Frame								
Extended Register Write TC_INDX_L and DAC A, B, C							Op Code		<Byte Count>			P	<Starting Address>								P
	1	0	SA [3,0]				0	0	0	0	0	0	1	1	P	0	0	0	0	0	0	0	1	P

Data Frame		Data Frame		Data Frame		Data Frame		BP
<Data 8−bit>	P	<Data 8−bit>	P	<Data 8−bit>	P	<Data 8−bit>	P	BP
Turbo−Charge	P	DAC_A [7,0]	P	DAC_B [7,0]	P	DAC_C [7,0]	P	BP

Table 28. EXTENDED REGISTER WRITE TO UPDATE DAC D, E, F (Note 7)

Description	SSC		Command Frame										Address Frame								
Extended Register Write TC_INDX_U and DAC D, E, F							Op Code		<Byte Count>			P	<Starting Address>								P
	1	0	SA [3,0]				0	0	0	0	0	0	1	1	P	0	0	0	0	0	1	0	1	P

Data Frame		Data Frame		Data Frame		Data Frame		BP
<Data 8−bit>	P	<Data 8−bit>	P	<Data 8−bit>	P	<Data 8−bit>	P	BP
Turbo−Charge	P	DAC_D [7,0]	P	DAC_E [7,0]	P	DAC_F [7,0]	P	BP

7. The six DACs can be updated either all together in the same time by using one Extended Register Write command of 8 bytes, or separately by using two Extended Register Write commands of 4 bytes each, where one command is to update DAC A, B, C and the other command to update DAC D, E, F.

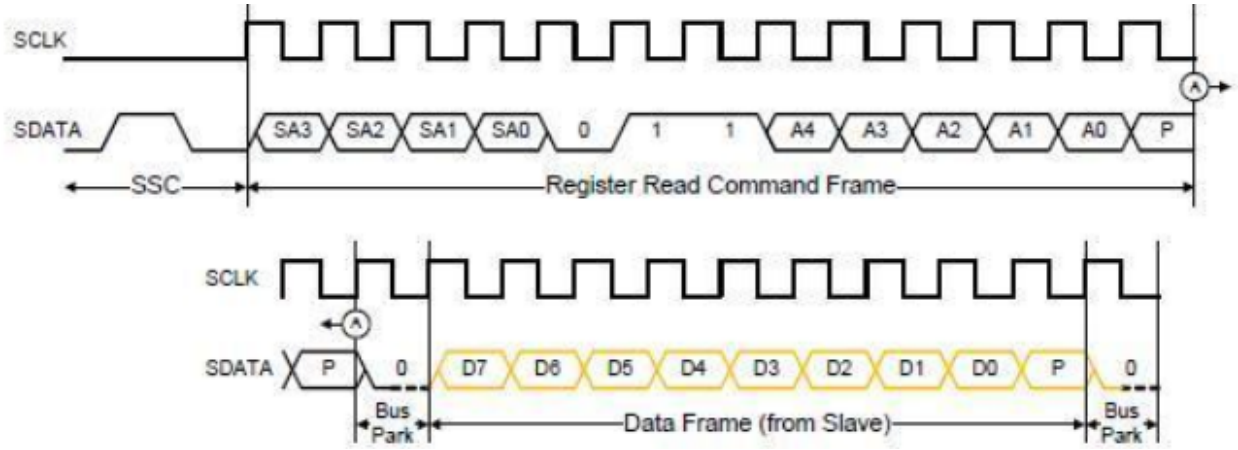


Figure 16. Register Read Command Sequence

Table 29. REGISTER READ COMMAND

Description	SSC		Command Frame										
Read MIPI−RFFE Status Register	1	0	SA[3:0]	0	1	1	1	1	0	1	0	P	BP

Description	Data Frame								
Read MIPI−RFFE Status Register (Continued)	0	CFPE	CLE	AFPE	DFPE	RURE	WURE	BGE	BP

REGISTER DETAILS

Register RFFE:	RFFE_REG_0x00	Address RFFE A[4:0]:	0x00

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	6	5	4	3	2	1	0
Bits	SS Enable	DAC E	DAC F	DAC A (1)	DAC B (1)	DAC C (1)	DAC D
Reset	W−1	W−0	W−0	W−0	W−0	W−0	W−0

(1) When any of the bits [3:1] are written with ‘0’, the corresponding DAC is disabled, but the Turbo−Charge process which is already started, will not be stopped.

(2) If all bits [3:1] are ‘0’, then incoming DAC messages will be ignored, until at least one of [3:1] is set ‘1’.

Bit 6: Spread Spectrum enable
0: SS disabled
1: SS enabled
Bit [1]: Control DAC E
0: off (default)
1: enabled
Bit [1]: Control DAC F
0: off (default)
1: enabled
Bit [3]: Control DAC A
0: off (default)
1: enabled
Bit [2]: Control DAC B
0: off (default)
1: enabled
Bit [1]: Control DAC C
0: off (default)
1: enabled
Bit [1]: Control DAC D
0: off (default)
1: enabled

Register RFFE:	RFFE_REG_0x01	Address RFFE A[4:0]:	0x01

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Bits	TC_INDX_L[7:0]							
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Register RFFE:	RFFE_REG_0x02	Address RFFE A[4:0]:	0x02

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_L [8]	DAC A value [6:0]						
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W−0	W−0

Register RFFE:	RFFE_REG_0x03	Address RFFE A[4:0]:	0x03

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_L [9]	DAC B value [6:0]						
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W−0

Register RFFE:	RFFE_REG_0x04	Address RFFE A[4:0]:	0x04

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_L [10]	DAC C value [6:0]						
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Register RFFE:	RFFE_REG_0x05	Address RFFE A[4:0]:	0x05

(1) Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_U[7:0]							
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Register RFFE:	RFFE_REG_0x06	Address RFFE A[4:0]:	0x06

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_U [8]	DAC D value [6:0]						
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Register RFFE:	RFFE_REG_0x07	Address RFFE A[4:0]:	0x07

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_U [9]	DAC E value [6:0]						
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

Register RFFE:	RFFE_REG_0x08	Address RFFE A[4:0]:	0x08

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	TC_INDX_U [10]	DAC F value [6:0]						
Reset	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Register RFFE:	RFFE_REG_0x9	Address RFFE A[4:0]:	0x09

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	HW Wake-Up Polarity		HW Wake−Up Disable	DAC_WAKEUP_CTRL		Turbo Latency Select	Reserved	boost_en_fast_st (OTP duplicated) (2)
Reset	W-0	W-1	W-0	W-0	W-0	W-0	W-0	W-0

1. Changing RFFE_REG_0x09 bits [7:5] while chip is in LP STD mode does not have effect, until chip returns to ACTIVE mode because bits [7:5] are shadowed when entering LP STD mode.
2. boost_en_fast_st can be set in ACTIVE or in LP mode

Bit [7:6]: HW Wake−Up Polarity

00: HW Wake−Up is always active LOW

01: (default) HW Wake−Up is always active HIGH

10: HW Wake−Up has inverted polarity referred to TRIG pin:

a. when RFFE_REG_0x11/TRIG_SEL = 1, HW Wake−Up is always active LOW

b. when RFFE_REG_0x11/TRIG_SEL = 0, HW Wake−Up is:

i. active LOW if RFFE_REG_0x11/TRIG_EDGE = 0 ii. active HIGH if RFFE_REG_0x11/TRIG_EDGE = 1

11: HW Wake−Up has same polarity as TRIG pin:

a. when RFFE_REG_0x11/TRIG_SEL = 1, HW Wake−Up is always active HIGH

b. when RFFE_REG_0x11/TRIG_SEL = 0, HW Wake−Up is:

i. active HIGH if RFFE_REG_0x11/TRIG_EDGE = 0

ii. active LOW if RFFE_REG_0x11/TRIG_EDGE = 1

Bit [5]: HW Wake−Up Disable

0 : (default) HW Wake−Up is enabled

1: HW Wake−up is disabled

Bit [4:3]: DAC Wake−up Control applicable to Wake−up from LP

00: (default) Don’t apply Turbo when Wake−up from LP

01: Always apply Turbo UP when Wake−up from LP. Turbo UP is calculated based on DAC value prior to enter LP STD mode.

10: Apply Turbo UP when Wake−up from LP when HW Wake−up is applied, but don’t apply Turbo UP when SW Wake−up is applied

11: unused

NOTE 1: Turbo i s NOT appl i ed after Wake−up to the DACs whi ch are programmed with 0x00 in the DAC value register

NOTE 2: When Bi t[4:3] = ‘10’ or ‘01’, then Turbo i s appl i ed after Wake−up regardl ess if:

- **DAC values are updated or not**
- **l ast DAC val ue update i s equal wi th ol d DAC val ue**

NOTE 3: When RFFE_REG_0x31 / Wake−up DAC Ctrl i s ‘0’ (default) Turbo after Wake−Up i s appl i ed after fi rst vhv_too_low fal ling edge is detected. When RFFE_REG_0x31 / Wake−up DAC Ctrl i s ‘1’ Turbo after Wake−up i s appl i ed after rc_clk starts.

Bit [2]: Turbo UP latency Select when Wake−up from LP.

This field has no effect when DAC_WAKEUP_CTRL[1:0] = ‘00’

0 : (default) Turbo UP latency is 50us

1: Turbo UP latency is 100us

Bit [1]: Fast Transition to Active Mode Enable

0: (default) Slow, current as low as possible in LP mode

1 Fast, RC oscillator and bandgap stay on, refer to section 5.6.2.4.2

Bit [0]: Boost Fast Startup Enable

0: (default) Startup with selected boost_il_trim

1: Startup with boost_il_trim_st[2:0], only if OTP[59]=1. The value of boost_il_trim_st[2:0] is applied starting from the moment when RFFE_REG_0x1C / Power Mode filed is written ‘00’ during LP mode, until first vhv_too_low negative edge is detected.

Register RFFE:	RFFE_REG_0x10	Address RFFE A[4:0]:	0x10

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved			Fixed	Boost voltage value			
Reset	U−0	U−0	U−0	U−1	W−1	W−0	W−1	W−1

Bit [3:0]: Boost voltage value
Refer to Table 19 for values

The MIPI RFFE Trigger Modes can be used as a synchronization signal to ensure that new DAC settings are applied to the outputs at appropriate times in the overall transceiver system. When the RFFE TRIG function is enabled via the TRIG SEL bit of RFFE_REG_0x11the requested DAC voltage levels are set up in the shadow registers and not transferred to the destination registers until the trigger condition is met. In this manner the change in output voltage levels are synchronized with the RFFE TRIG command. The trigger configuration also provides for an external TRIG pin to be used as a synchronization signal. When the TRIG input pin is enabled via the TRIG SEL bit of RFFE_REG_0x11the requested DAC voltage levels are set up in the shadow registers and are not transferred to the destination registers until the external trigger condition is met. In this manner the change in output voltage levels are synchronized with the external TRIG event. The external TRIG input is referenced to VIO. To improve interfacing options the polarity of external TRIG is programmable via TRIG_edge bit of RFFE_REG_0x11. When MIPI RFFE trigger and the external TRIG input are disabled by

MASK_EXT_TRIG of RFFE_REG_0x11 and TRIGGER_MASK[5:3] of RFFE_REG_0x1C, the requested DAC voltage levels are immediately applied to the outputs and are not synchronized with the RFFE Trigger Modes or the external TRIG signal.

When valid trigger edge occurs, only the completely received messages are subject to be applied to the outputs.

A message is considered to be completed, if the TRIG edge occurs after TRIG_LAT following last SDL clock falling edge in the frame.

In Figure 17, the last SDL clock cycle in each frame is highlighted gray.

The parameter TRIG_LAT is represented as the latency following the SDL last falling edge in the frame until TRIG edge occurs.

As an example, in Figure 17 TRIG edge 3 occurs before TRIG_LAT, following last SDL falling edge in frame of “MESSAGE A3”, so TRIG edge 3 will move “MESSAGE A2” to output, instead of “MESSAGE A3”. In this case TRIG edge 3 has the same effect as TRIG edge 2, which is described below.

If trigger edge occurs while a message frame is being received by the slave on the serial bus, than the pending message will not be transferred to the output until next trigger edge occurs after frame transfer is completed.

A pending message is considered from the moment SSC cycle starts, until after TRIG_LAT following last SDL falling edge in the frame.

For example, in Figure 17, both TRIG edge 2 and TRIG edge 3 occur while “MESSAGE A3” is pending. In this case both will have same effect, which is to transfer “MESSAGE A2” to the output.

“MESSAGE A3” will be transferred to the output by TRIG edge 4, because it occurs after TRIG_LAT.

If more than one message was received before a trigger edge, than only the last completed message will be transferred to the output.

For example, in Figure 17, between TRIG edge 1 and TRIG edge 2, there have been two messages sent: “MESSAGE A1” and “MESSAGE A2”. In this case, “MESSAGE A1” will be ignored, and only “MESSAGE A2” will be transferred to the output by TRIG edge 2.

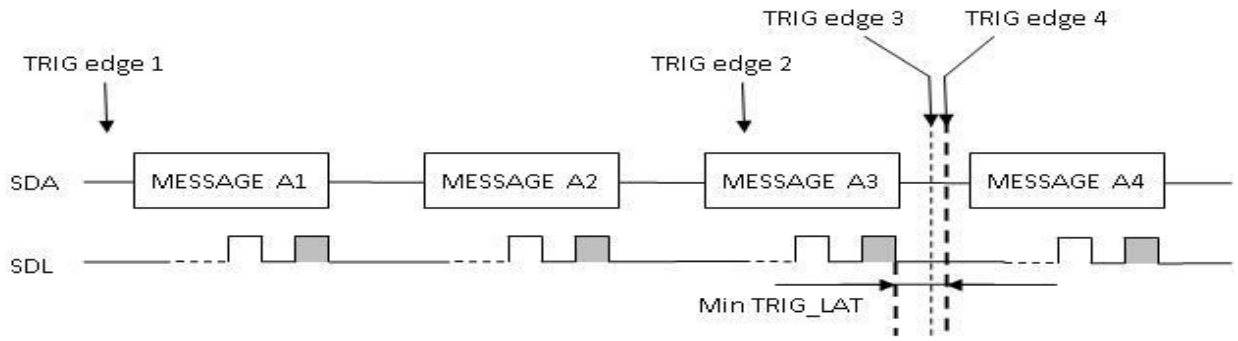


Figure 17. Sequences of Triggers and Messages to Same Output

In Figure 18, TRIG edge 2, will transfer “MESSAGE A2”, “MESSAGE B1”, and “MESSAGE C1” to the respective outputs, but will ignore “MESSAGE A1”.

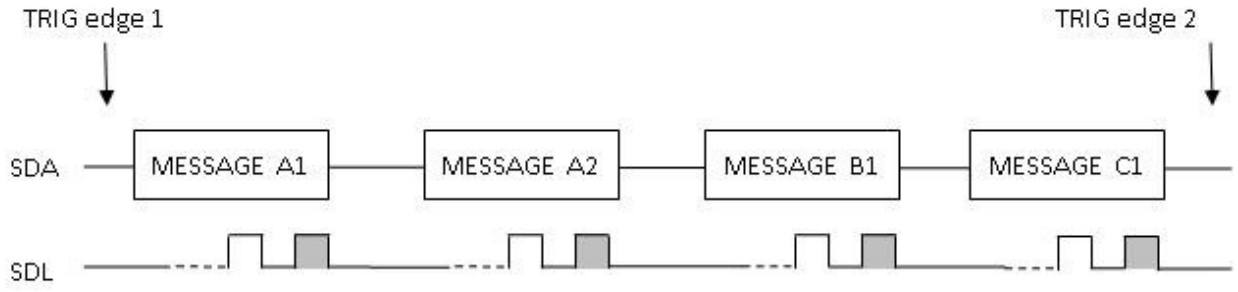


Figure 18. Sequences of Triggers and Messages to Different Outputs

Table 30. TRIG_LAT PARAMETER TIMING

Symbol	Description	Min	Max	Unit
TRIG_LAT	Latency following the falling edge of last clock cycle of a certain message, until the moment a TRIG edge is allowed to update the value sent by that message	5	25	ns

Register RFFE:	RFFE_REG_0x11	Address RFFE A[4:0]:	0x11

	7	6	5	4	3	2	1	0
Bits	Reserved			TRIG SEL	Reserved		TRIG Edge (1) (2)	MASK EXT TRIG
Reset	U-0	U-0	U-0	W-1	U−0	U−0	W−1	W−1

(1) Following sequence is required when changing the expected polarity of TRIG pin:
a) TRIG_SEL = ‘1’ (disable TRIG pin)
b) TRIG_EDGE = new value
c) TRIG_SEL = ‘0’ (enable TRIG pin)

(2) After power−up, first configure TRIG_Edge, then write TRIG_SEL = ‘0’ Bit 4: TRIG Select
0: Use external TRIG pin. Sending the RFFE message will load a ’shadow’ registers only. Only upon an active signal on external TRIG pin are the output registers loaded with the new voltage settings which are then applied to the outputs. Software triggers generated by bits [2:0] of RFFE_REG_0x1C are ignored when external TRIG pin is selected.
1: External TRIG pin will not be used. (default)

Bit [1]: TRIG edge
0: TRIG pin active falling
1: TRIG pin active rising (default)

Bit [0]: MASK EXT TRIG
0: External trigger is not masked
1: Mask external trigger pin (default)

Turbo mode timing is controlled by these registers:

Register RFFE:	RFFE_REG_0x12	Address RFFE A[4:0]:	0x12

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved		TC_STP_DAC_C		TC_STP_DAC_B		TC_STP_DAC_A	
Reset	U−0	U−0	W−0	W−1	W−0	W−1	W−0	W−1

Register RFFE:	RFFE_REG_0x13	Address RFFE A[4:0]:	0x13

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved		TCM_C		TCM_B		TCM_A	
Reset	U−0	U−0	W−0	W−0	W−0	W−0	W−0	W−0

Register RFFE:	RFFE_REG_0x14	Address RFFE A[4:0]:	0x14

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved		TC_STP_DAC_F		TC_STP_DAC_E		TC_STP_DAC_D	
Reset	U−0	U−0	W−0	W−1	W−0	W−1	W−0	W−1

Register RFFE:	RFFE_REG_0x15	Address RFFE A[4:0]:	0x15

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved		TCM_F		TCM_E		TCM_D	
Reset	U−0	U−0	W−0	W−0	W−0	W−0	W−0	W−0

Register RFFE:	RFFE_STATUS_0x1A	Address RFFE A[4:0]:	0x1A

Reset Source: nreset_dig or SWR = ‘1’ or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	SWR	CFPE	CLE	AFPE	DFPE	RURE	WURE	BGE
Reset	W−0	R−0	R−0	R−0	R−0	R−0	R−0	R−0

TC_STP_DAC_x[1:0]	Turbo steps for TCDLY [us]
00	3
01 (default)	5
10	7
11	9

TCM_x[1:0]	Turbo Multiplication Factor
00 (default)	4
01	3
10	2
11	1

Step (μs)	DAC state	0	1	2	3	4	5	6	7	8	9	10	11
9	TCDLY	Turbo OFF		18	27	36	45	54	63	72	81	90	99
7	TCDLY	Turbo OFF		14	21	28	35	42	49	56	63	70	77
5 (default)	TCDLY	Turbo OFF		10	15	20	25	30	35	40	45	50	55
3	TCDLY	Turbo OFF		6	9	12	15	18	21	24	27	30	33

The value of Turbo time is deducted based on the hardware comparison of new DAC value in respect to old DAC value, as follows:

If DAC new > DAC old, then TUP = TCDLY

If DAC new < DAC old, and DAC new_divby2 < 21, then TDOWN = TCDLY + TCM * (21 – DAC_new_divby2) If DAC new < DAC old, and DAC new_divby2 > 21, then TDOWN = TCDLY
If DAC new < DAC old, and DAC new_divby2 = 21, then TDOWN = TCDLY

RFFE_STATUS register can be read any time after power−up without the need to enable the Read Operation as described in section 6.9.5

SWR Soft−Reset MIPI−RFFE registers

Write ‘1’ to this bit to reset all the MIPI−RFFE registers, except RFFE_REG_0x1C, RFFE_USID, and

RFFE_GROUP_SID

This bit will always Read−back ‘0’.

The soft reset occurs in the last clock cycle of the MIPI−RFFE frame which Writes ‘1’ to this bit. Right immediately after this frame, all the MIPI−RFFE registers have the reset value and are ready to be reprogrammed as desired.

The OTP duplicated registers are reset to the values written in OTP.

SWR can be written only by USID messages. GSID and Broadcast frames will be ignored when writing to this register field.

RFFE_STATUS Bits [6:0] are set ‘1’ by hardware to flag when a certain condition is detected, as described below. RFFE_STATUS Bits [6:0] cannot be written, but it is cleared to ‘0’ under following conditions:

- Hardware Self−reset is applied after RFFE_STATUS is READ
- When SWR is written ‘1’ with USID frames
- When power mode transitions through STARTUP mode ‘01’
- After Power−up Reset

CFPE

1: Command frame with parity error received.

On the occurrence of this error, the slave will ignore the entire Command Sequence

CLE

1: Incompatible command length, due to unexpected SSC received before command length to be completed.

On the occurrence of this error, the slave will accept Write data up to the last correct and complete frame. When MIPI−RFFE multi−byte Read command is detected, the slave will always replay with an extended Read command of length of one byte.

AFPE

1: Address frame with parity error received.

On the occurrence of this error, the slave will ignore the entire Command Sequence

DFPE

1: Data frame with parity error received.

RURE

On the occurrence of this error, the slave will ignore only the erroneous data byte (s)

1: Read of non−existent register was detected.

On the occurrence of this error, the slave will not respond to the Read command frame.

When the Read Operation is not enabled according to section 6.9.5, any read from an address other than

0x1A, will set RURE and the slave will not respond to the Read command frame.

When the Read Operation is enabled according to section 6.9.5, any read from an unoccupied RFFE register address will set RURE.

WURE

1: Write to non−existent register was detected.

On the occurrence of this error, the slave discards data being written, and on the next received frame, proceeds as normal

BGE

1: Read using the Broadcast ID was detected

On the occurrence of this error, the slave will ignore the entire Command Sequence

Register RFFE:	RFFE_GROUP_SID_0x1B	Address RFFE A[4:0]:	0x1B

Reset Source: nreset_dig or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved	Reserved	Reserved	Reserved	GSID[3]	GSID[2]	GSID[1]	GSID[0]
Reset	0	0	0	0	W-0	W-0	W-0	W-0

GSID = Group Slave Identifier Register

NOTE: The GSID[3:0] field can be written directly by messages using USID. NOTE: GSID value is NOT retained during SHUTDOWN power mode. NOTE: GSID value is not affected by SWR bit from RFFE_STATUS register

NOTE: Frames using USID = GSID, can write only to RFFE_REG_0x1C [7:6] and [2:0].

NOTE: RFFE READ frames containing GSID will be ignored

Register RFFE:	RFFE_REG_0x1C	Address RFFE A[4:0]:	0x1C

Reset Source: nreset_dig or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Power Mode (5)		Trigger Mask 2 (1) (2) (3) (4)	Trigger Mask 1 (1) (2) (3) (4)	Trigger Mask 0 (1) (2) (3) (4)	Trigger 2	Trigger 1	Trigger 0
Reset	W−0	W−0	W−0	W−0	W−0	W−0	W−0	W−0

(1) Trigger Mask bits [5:3] can be changed, either set or cleared, only with an individual message using USID

(2) During broadcast MIPI−RFFE accesses using GSID = ‘0000’, Trigger bits [2:0] are masked by the pre−existent setting of Trigger Mask Bits [5:3]

(3) During Individual MIPI−RFFE accesses using USID, Trigger bits [2:0] are masked by the incoming Trigger Mask bits [5:3] within the same write message to RFFE_REG_0x1C register. During Individual MIPI−RFFE accesses using USID, pre−existent setting of Trigger Mask Bits [5:3] is ignored.

(4) When RFFE_REG_0x11 / TRIG_SEL = ‘1’ (External TRIG pin will not be used) and RFFE_REG_0x1C/ Trigger_Mask_2 = ‘1’ and Trigger_Mask_1 = ‘1’ and Trigger_Mask_0 = ‘1’, then DAC messages will be sent to DACs immediately after RFFE_REG_0x04 is received, without waiting for any trigger

(5) Power mode field bits [7:6] and Triggers bits [2:0] can be changed by either MIPI−RFFE broadcast messages when USID field within the Register Write Command is 0x0 , or individual messages when USID fields within the Register Write Command is equal with RFFE_REG_0x1F[3:0]

NOTE: All the 8 bits of RFFE_REG_0x1C register bits are NOT affected by SWR bit from RFFE_STATUS register

Bit [7:6]: Power Mode

00: ACTIVE mode, defined by following hardware behavior:
- Boost Control active, VHV set by Digital Interface
- Vout A, B, C enabled and controlled by Digital Interface

01: STARTUP mode, defined by following hardware behavior:
- Boost Control active, VHV set by Digital Interface
- Vout A, B, C disabled

10: LOW POWER mode when TRIG pin = LOW, ACTIVE mode when TRIG pin = HIGH. LOW POWER mode is defined by following hardware behavior:
- Digital interface is active, while all other circuits are in low power mode

11: Reserved (State of hardware does not change)

Bit 5: Mask trigger 2

0:Trigger 2 not masked. Data goes to destination register after bit 2 is written value 1 (default)

1:Trigger 2 is masked. Data goes directly to the destination register

Bit 4: Mask trigger 1

0:Trigger 1 not masked. Data goes to destination register after bit 1 is written value 1(default)

1:Trigger 1 is masked. Data goes directly to the destination register.

Bit 3: Mask trigger 0

0:Trigger 0 not masked. Data goes to destination register after bit 0 is written value 1(default)

1:Trigger 0 is masked. Data goes directly to the destination register.

Bit 2: Trigger 2
Write 1 to this bit, to move data from shadow registers into destination register. This trigger can be masked by bit 5.
Bit 1: Trigger 1
Write 1 to this bit, to move data from shadow registers into destination register. This trigger can be masked by bit 4.
Bit 0: Trigger 0
Write 1 to this bit, to move data from shadow registers into destination register. This trigger can be masked by bit 3.

All three triggers from register [0x1C] behave in the same way as the external pin TRIG. When each of these triggers is set using the MIPI RFFE interface the results are the same as when an active voltage level is applied to the TRIG pin when External pin TRIG is selected.

Register RFFE:	RFFE_PRODUCT_ID_0x1D	Address RFFE A[4:0]:	0x1D

Reset Source: N/A

	7	6	5	4	3	2	1	0
Bits	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0 (1)
Reset	0	0	1	0	0	1	OTP[4]	IDB0 pin

Bits [7:2] are hardcoded in ASIC
Bits [1:0] can be programmed in OTP during manufacturing
The MIPI register RFFE_PRODUCT_ID can be read in SPI mode as described in 6.9.5

Register RFFE:	RFFE_MANUFACTURER_ID_0x1E	Address RFFE A[4:0]:	0x1E

Reset Source: N/A

	7	6	5	4	3	2	1	0
Bits	MPN7	MPN6	MPN5	MPN4	MPN3	MPN2	MPN1	MPN0
Reset	0	0	1	0	1	1	1	0

Register RFFE:	RFFE_USID_0x1F	Address RFFE A[4:0]:	0x1F

Reset Source: nreset_dig or PWR_MODE = ‘01’ (transition through STARTUP mode)

	7	6	5	4	3	2	1	0
Bits	Reserved (2)		MPN9 (2)	MPN8 (2)	USID3 (1)	USID2 (1)	USID1 (1)	USID0 (1)
Reset	0	0	0	1	W−0	W−1	W−1	W−1

USID = Unique Slave Identifier Register
(1) USID field can be changed by:
- MIPI−RFFE broadcast messages when USID field within the Register Write Command is 0b0000
- MIPI−RFFE individual messages when USID field within the Register Write Command equal with content of RFFE_REG_0x1F[3:0]

(2) In the sequence of writing USID field, the upper [7:4] must match the value 0b0001 hard−coded in the RFFE register 0x1F

NOTE: USID value is NOT retained during SHUTDOWN power mode.
NOTE: USID value is not affected by SWR bit from RFFE_STATUS register DAC Update

Following picture shows TCC−206 and all the necessary external components

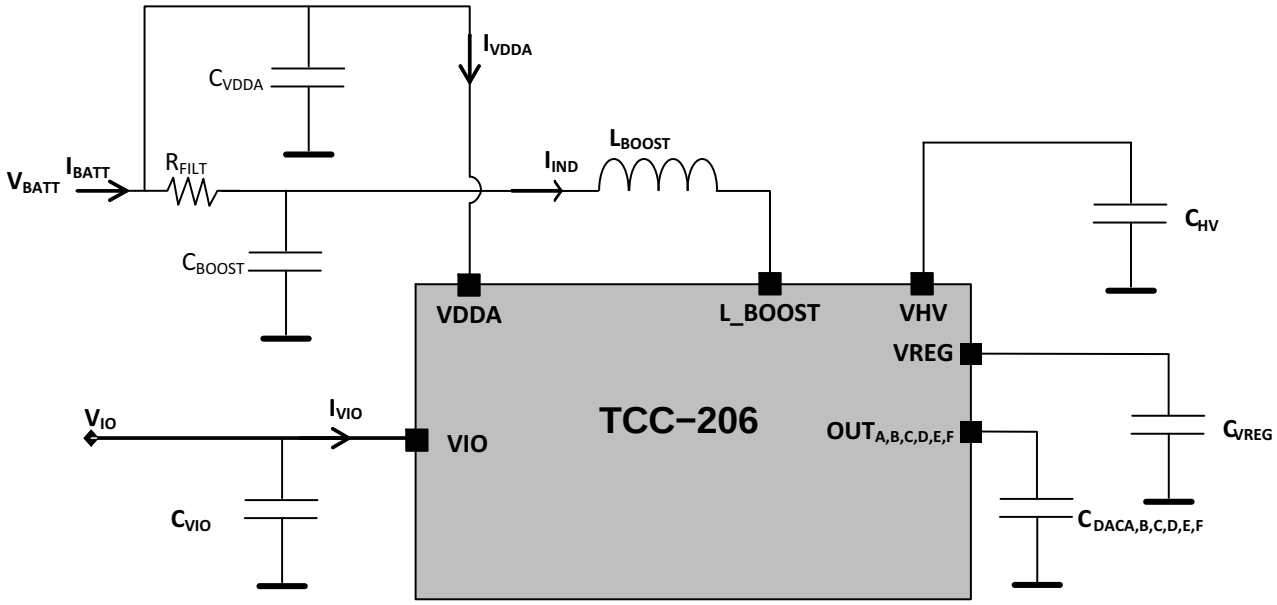


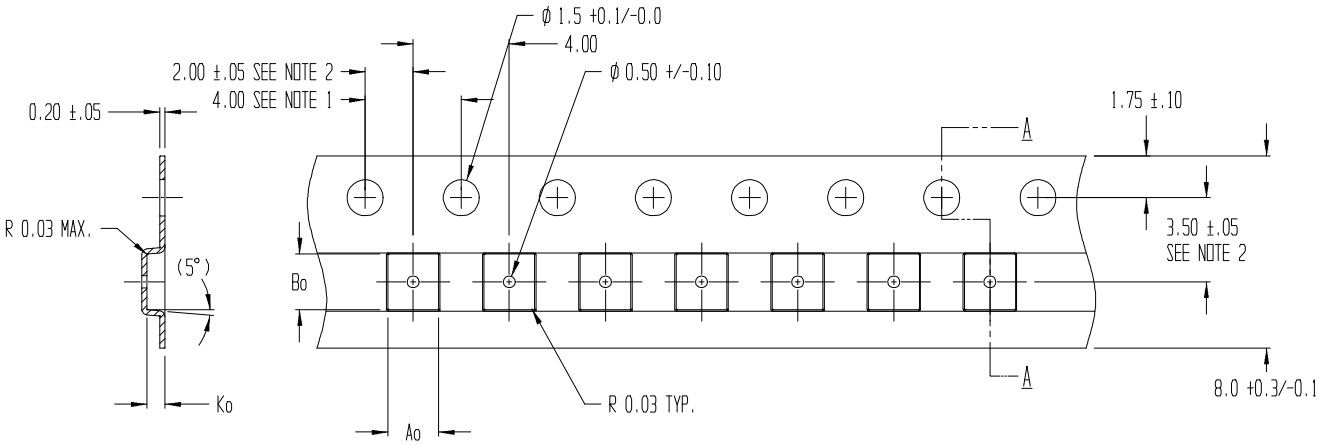
Figure 19. TCC−206 with External Components

Table 31. RECOMMENDED EXTERNAL BOM

Component	Description	Nominal Value	Package	Recommended P/N
C_{BOOST}	Boost Supply Capacitor, 10 V	1 μF	0402	TDK: C1005X5R1A105K
L_{BOOST}	Boost Inductor	15 μH	0603	TDK: VLS2010ET−150M, Sunlord SPH201610H150MT
R_{FILT}	Filtering resistor, 5%	3.3 Ωs	0402	Vishay : CRCW04023R30JNED
C_{VIO}	V_{IO} Supply Decoupling, 10 V	100 nF	0201	Murata: GRM033R61A104ME15D
C_{AVDD}	V_{AVDD} Supply Decoupling, 10 V	1 μF	0402	TDK: C1005X5R1A105K
C_{VREG}	V_{VREG} Supply Decoupling, 10 V	220 nF	0201	TDK: C0603X5R1A224M
C_{HV}	Boost Tank Capacitor, 50 V	47 nF	1005	Murata: GRM155C71H473KE19
$C_{dacA,B,C,D,E,F}$	Decoupling Capacitor, 50 V (Note 8)	100 pF	0201	Murata: GRM0335C1H101JD01D

8. Recommended for noise reduction only – not essential

TAPE & REEL DIMENSIONS



Ao = 2.12 ±.05
Bo = 2.32 ±.05
Ko = 0.75 ±.05

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 20. WLCSP Carrier Tape Drawings

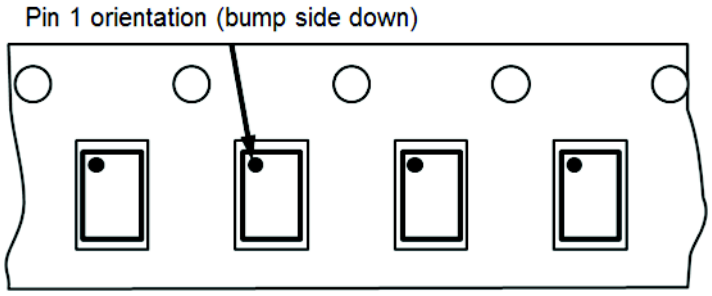


Figure 21. Orientation in Tape

Table 32. ORDERING INFORMATION

Device	Package	Shipping†
TCC−206A−RT	RDL (Pb−Free)	3000 / Tape & Reel

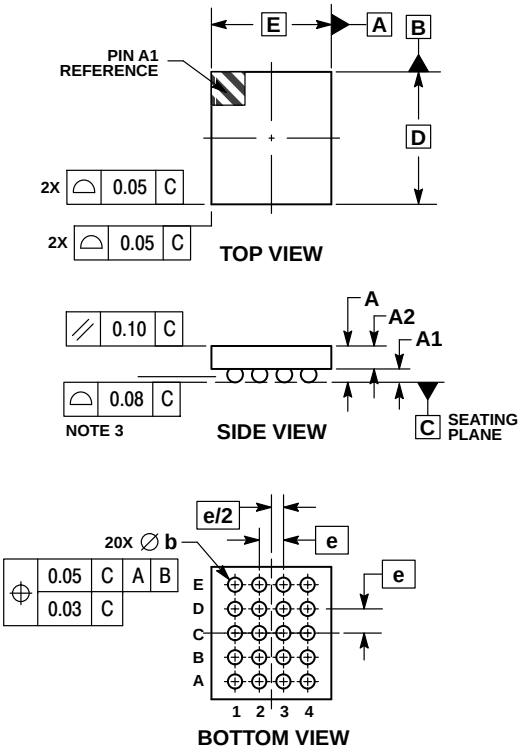
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ASSEMBLY INSTRUCTIONS

Note: It is recommended that under normal circumstances, this device and associated components should be located in a shielded enclosure.

PACKAGE DIMENSIONS

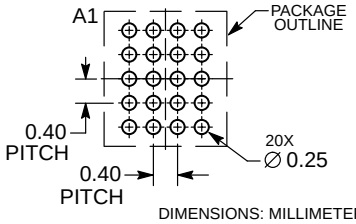
WLCSP20 2.187x1.987
CASE 567JV
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.65
A1	0.17	0.23
A2	0.38 REF	
b	0.23	0.29
D	2.187 BSC	
E	1.987 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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