

To all our customers

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Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2059(L), 2SK2059(S)

Silicon N-Channel MOS FET

RENESAS

ADE-208-1341 (Z)
1st. Edition
Mar. 2001

Application

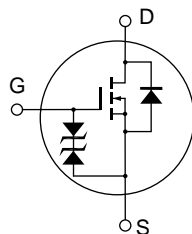
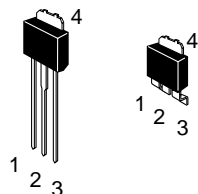
High speed power switching

Features

- Low on-resistance
- High speed switching
- No Secondary Breakdown
- Suitable for Switching regulator, DC - DC converter

Outline

DPAK-1



1. Gate
2. Drain
3. Source
4. Drain

2SK2059(L), 2SK2059(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	600	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	3	A
Drain peak current	I _{D(pulse)} ^{*1}	6	A
Body to drain diode reverse drain current	I _{DR}	3	A
Channel dissipation	Pch ^{*2}	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

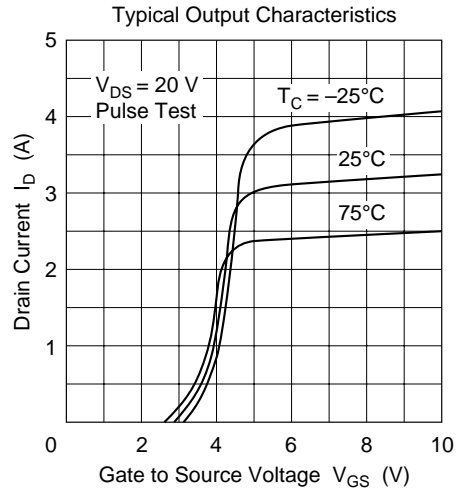
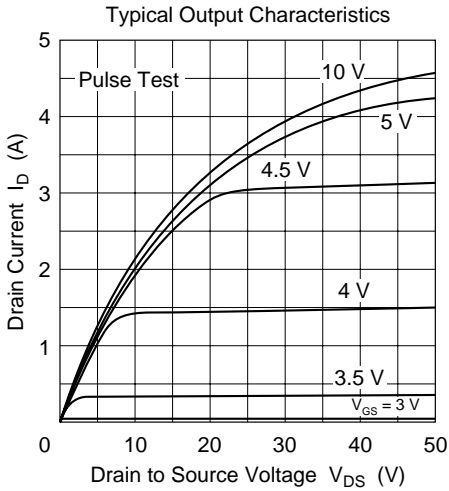
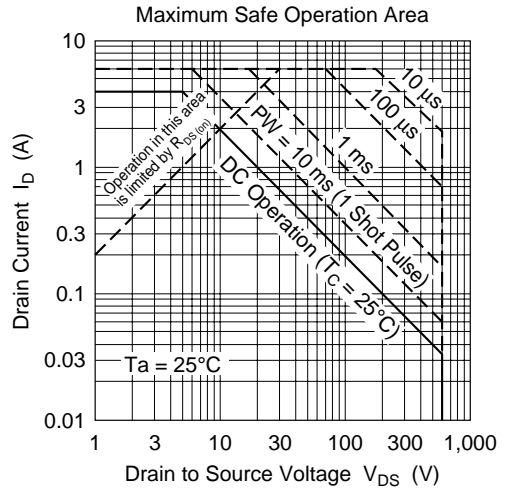
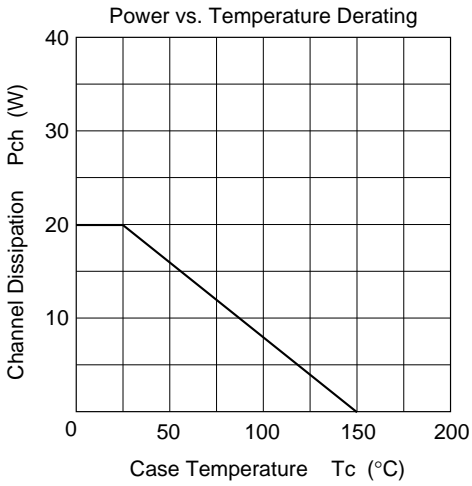
Notes 1. PW 10 μs, duty cycle 1 %

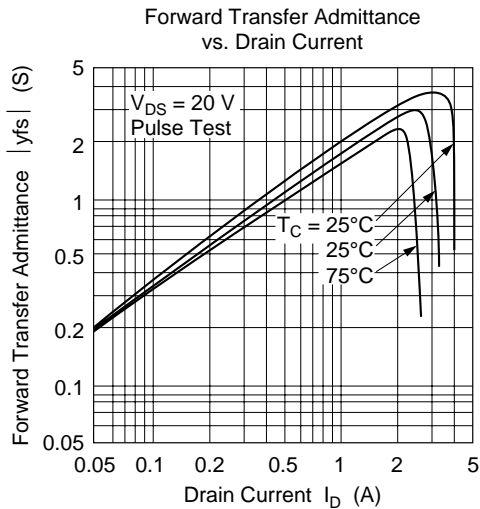
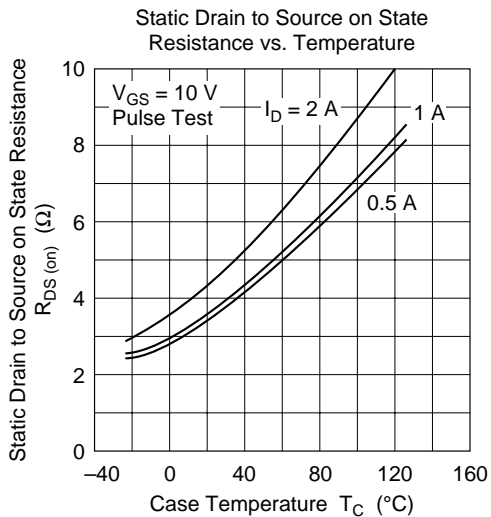
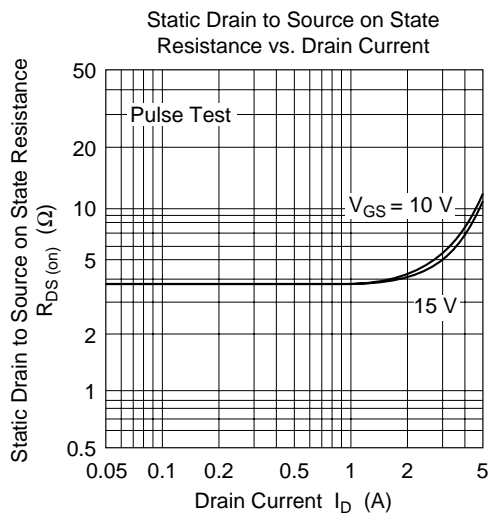
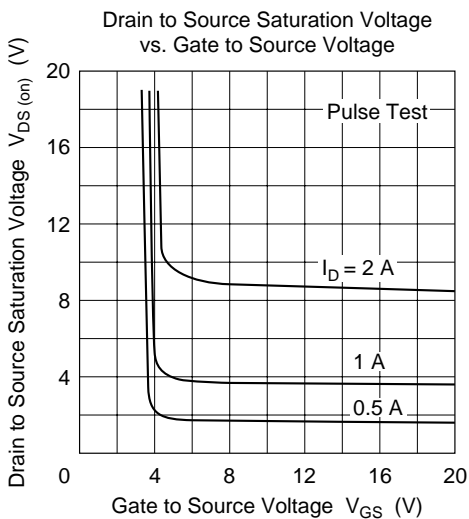
2. Value at Tc = 25°C

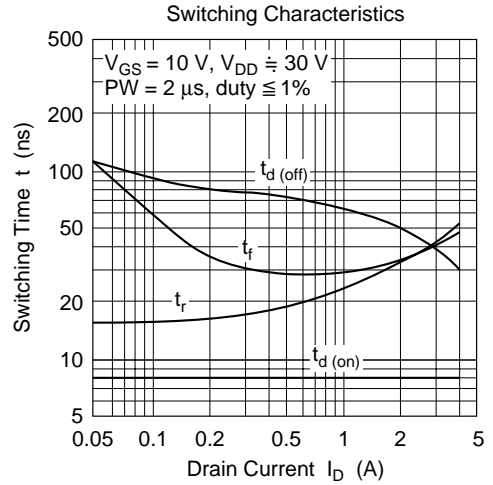
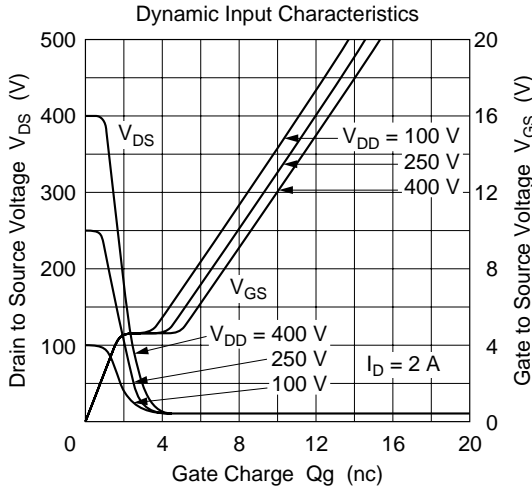
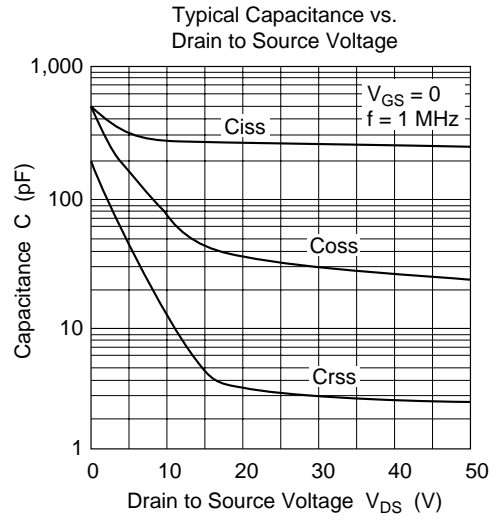
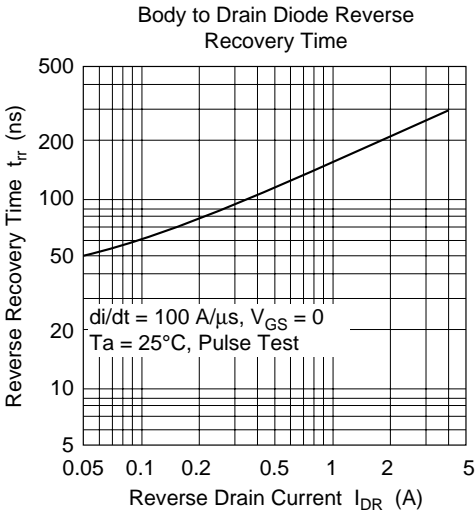
Electrical Characteristics (Ta = 25°C)

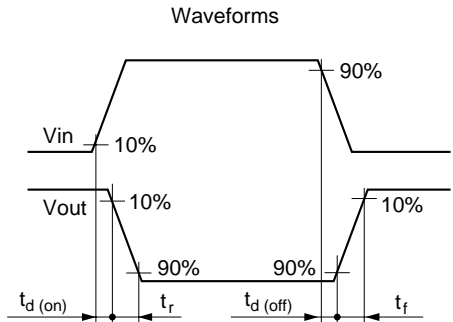
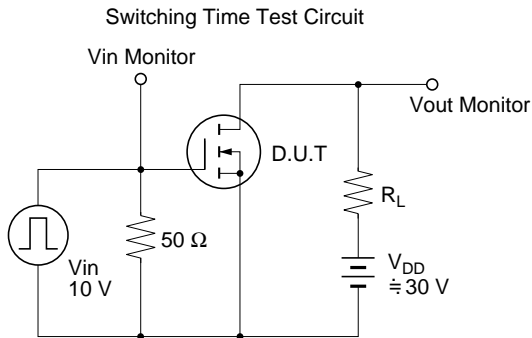
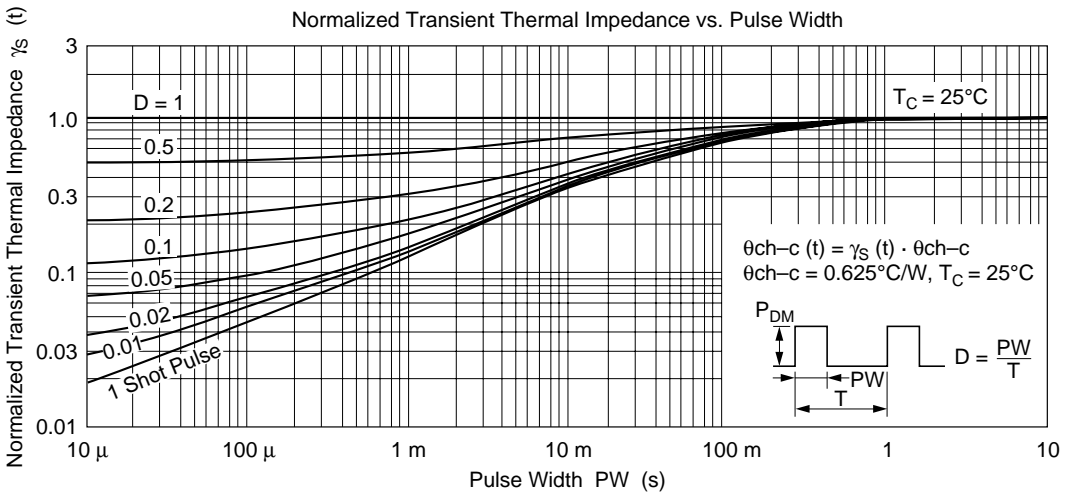
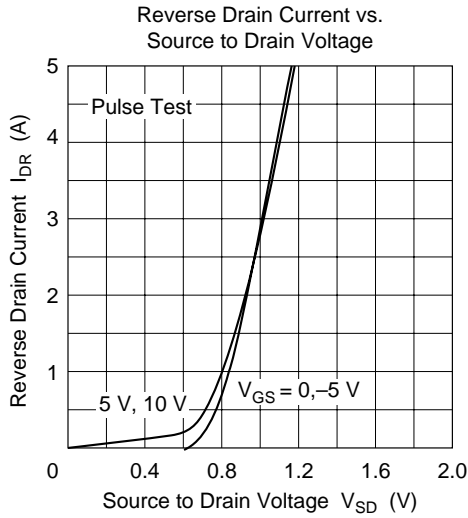
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 30	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	100	μA	$V_{DS} = 500 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	5.0		$I_D = 1 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = 1 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	295	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	70	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	12	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	8	—	ns	$I_D = 1 \text{ A}$
Rise time	t_r	—	25	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	$R_L = 30$
Fall time	t_f	—	30	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 3 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	220	—	ns	$I_F = 3 \text{ A}, V_{GS} = 0,$ $di_F / dt = 100 \text{ A} / \mu\text{s}$

Note 1. Pulse Test



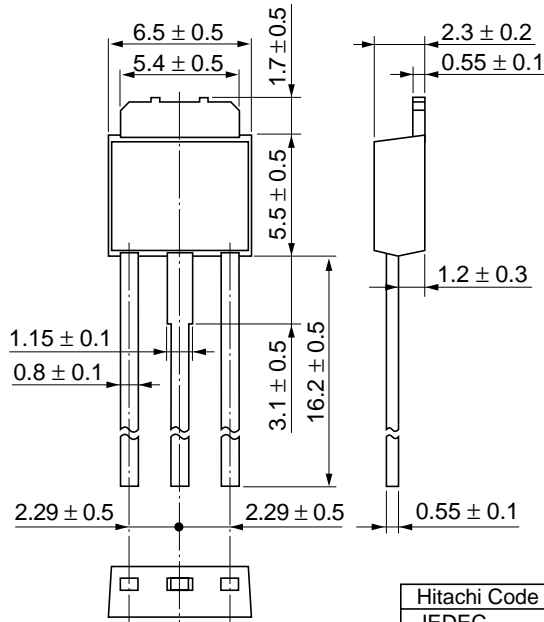






Package Dimensions

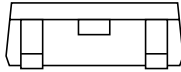
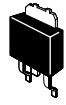
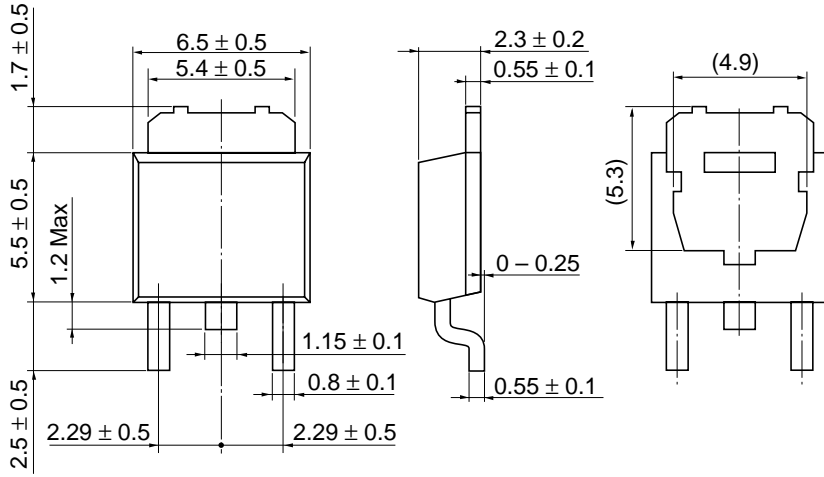
As of January, 2001
Unit: mm



Hitachi Code	DPAK (L)-(1)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.42 g

As of January, 2001

Unit: mm

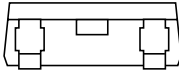
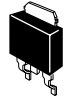
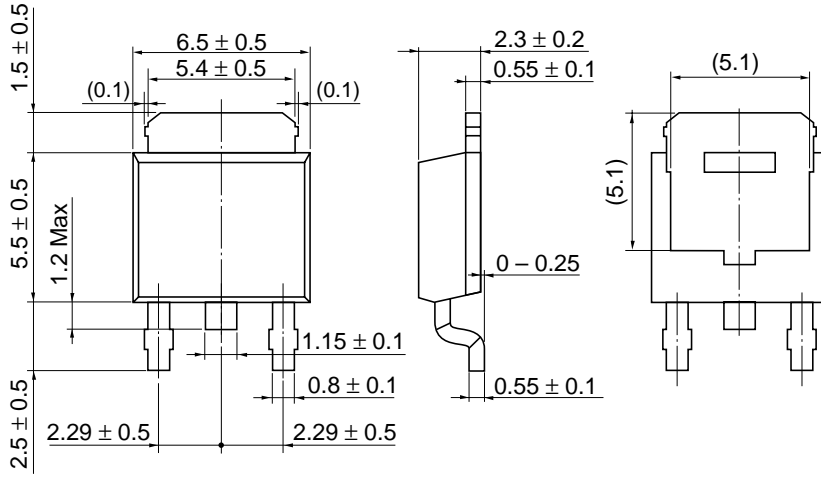


Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

2SK2059(L), 2SK2059(S)

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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