ML9460

Common Driver for Dot Matrix STN Liquid Crystal Display

1. Product Overview

1.1 General Description

The ML9460 is a 240-output common driver for driving a dot matrix LCD panel.
It enables switching between 240 outputs and 200 outputs and 160 outputs and 120 outputs. The ML9460 is used in combination with the segment driver ML9461B.

1.2 Features

- 240-channel common driver
- Display duty: Up to 1/240
- LCD drive voltage: 43 V max.
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage Interface
- Built-in alternating signal generation circuit; pin programmable
- Built-in display OFF control circuit
- Can switch output modes: 240-output mode/200-output mode/160-output mode/120-output mode
- Clock cycle time: 245 ns min. @ 4.5 V 330 ns @ 2.5 V
- Package

Au Bump Chip	Product name: ML9460CVWA
TCP	Product name: ML9460ADVVA

2. Pin Description

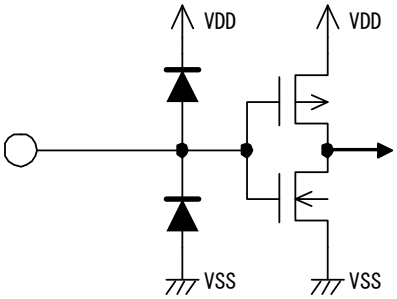
2.1 Pin Description

Pin name	I/O	Polarity	Descripiton	Initial value	Handling when not used	Attribute	Remarks
VDD	—	—	Logic power supply pin	—	—	Power	
VSS	—	—	Logic power supply pin	—	—	VSS	
V2L V2R	—	—	Power supply pins for liquid crystal drive level output. Selective level.	—	—	Power	V2L and V2R are connected internally with each other.
MV2L MV2R	—	—	Power supply pins for liquid crystal drive level output. Selective level.	—	—	Power	MV2L and MV2R are connected internally with each other.
VCL VCR	—	—	Power supply pins for liquid crystal drive level output. Nonselective level.	—	—	Power	VCL and VCR are connected internally with each other.
YSCL	I	↓	Shift clock input pin. Data is shifted in on the falling edge of the shift clock YSCL of the shift register.	Low	—	CLK	
FR	I/O	—	Input-output pin for alternating signal for liquid crystal drive output	Low	—	Digital	See Sections 4.1.1, “Liquid Crystal Drive Circuit,” and 4.2.1, “Timing of Connection with the Segment Driver.”
FRWS0 FRWS1 FRWS2 FRWS3 FRWS4	I	—	Alternating signal (FR signal) period setting pins. Specify the number of lines with an integer from 2 to 31. For operation using an external alternating signal, set the number of lines to 0.	Tied High or Low	—	Digital	See Sections 4.1.4, “Alternating Signal Generation Circuit.”
SEL1 SEL2	I	—	Liquid crystal drive output pin switching pins	Tied High or Low	—	Digital	See Sections 4.1.1, “Liquid Crystal Drive Circuit,” and 4.1.3, “Bidirectional Shift Register.”
DIO1 DIO2	I/O	—	Serial I/O (shift register data input-output) pins	Tied High or Low	—	Digital	See Section 4.1.3, “Bidirectional Shift Register.”
$\overline{\text{FRRES}}$	I	Negative	Pin for initializing the counter for the alternating signal generation circuit. Setting this pin to “L” level sets initializes the altemating signal(FR signal) circuit. A “H” level $\overline{\text{FRRES}}$ is normally used.	Low	—	Digital	
$\overline{\text{DSPOF}}$	I	Negative	A “L” level on this pin sets each of the liquid crystal drive outputs O1–O240 to the VC level. No internal register will be cleared.	Low	—	Digital	
DSPMS	I	—	Pin for selecting the method of processing the $\overline{\text{DSPOF}}$ signal internally	Tied High or Low	—	Digital	See Section 4.1.5, “Control Circuit.”

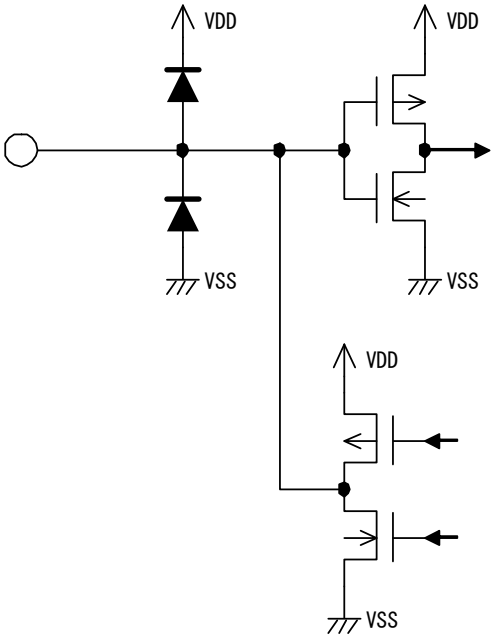
Pin name	I/O	Polarity	Descripiton	Initial value	Handling when not used	Attribute	Remarks
$\overline{DOC}$	O	Negative	DISPOFF signal output pin	Low	—	Digital	See Sections 4.1.5, “Control Circuit,” and 4.2.3, “$\overline{DOC}$ Signal Waveforms.”
SHL	I	—	Shift direction switching pin. Switches the shift direction of the shift register.	Tied High or Low	—	Digital	See Section 4.1.3, “Bidirectional Shift Register.”
O1 to O240	O	—	Liquid crystal drive output pins. When the VDD voltage is input to the $\overline{DSPOF}$ pin, one of the three levels (V2, MV2, VC) is selected and output according to the combination of the FR signal and display data.	—	Pins that are made disabled by the SEL1 and SEL2 pins will output the nonselective level signal (VC).	Analog	See Section 4.1.1, “Liquid Crystal Drive Circuit.”

Note:
In the initial value column,
- A dash “—” for an input pin indicates that the initial value is Don’t Care.
- A dash “—” for an output pin indicates that the initial value is undefined.

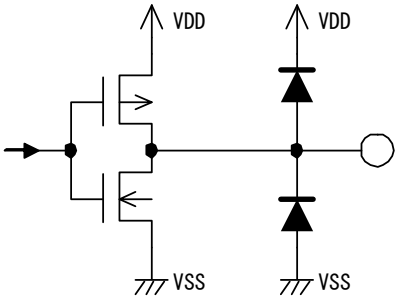
2.2 Inupt and Output Configuration



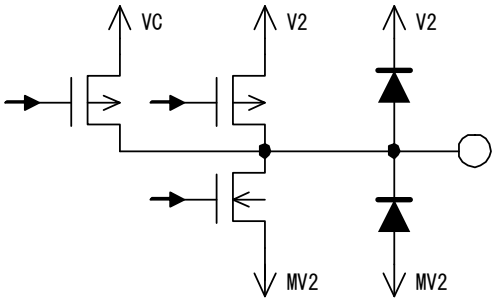
Applicable to pins YSCL, FRWS0～4,SEL1,SEL2, $\overline{\text{FRRES}}$,$\overline{\text{DSPOF}}$,DSPMS, and SHL.



Applicable to pins FR,DIO1,and DIO2.

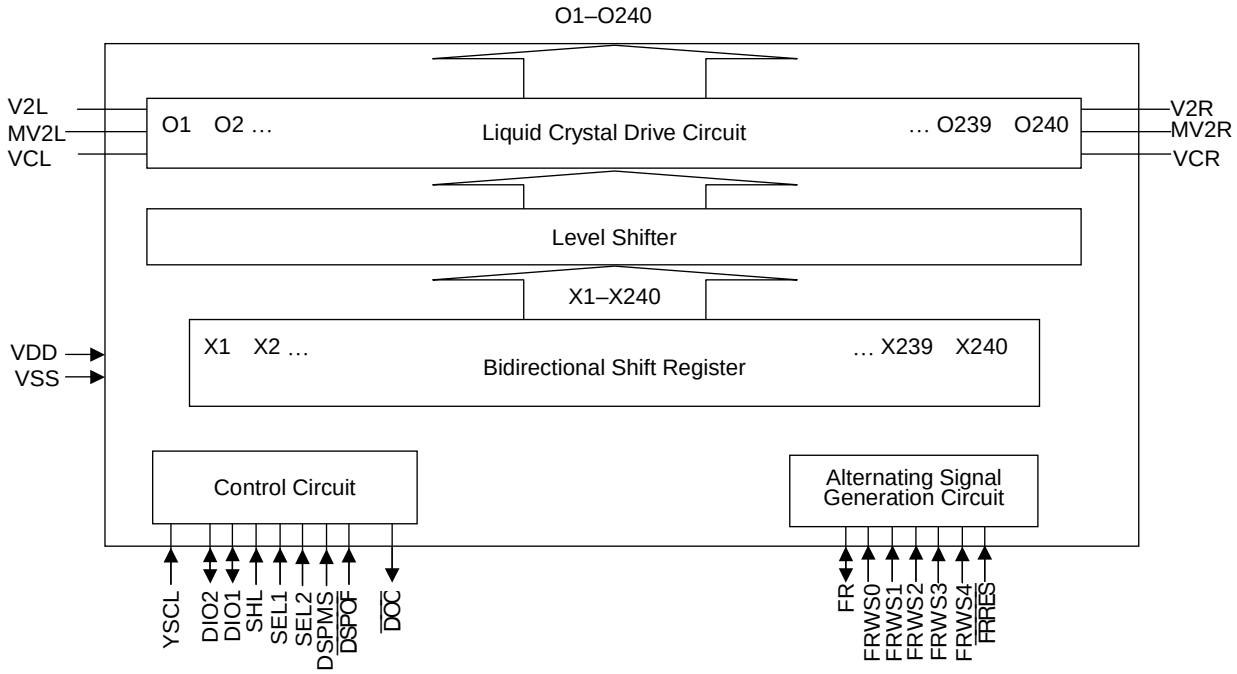


Applicable to pins $\overline{\text{DOC}}$.



Applicable to pins O1～240.

3. Block Diagram



4. Functional Description

4.1 Internal Blocks

4.1.1 Liquid Crystal Drive Circuit

The liquid crystal drive circuit outputs three levels for liquid crystal drive. One of the three liquid crystal drive levels (V2, MV2, VC) is selected and output according to the combination of data stored n the shift register circuit and FR, as shown below.

FR	Display data	$\overline{DSPOF}$	Output level
*	*	"L"	VC
"L"	"L"	"H"	VC
"L"	"H"	"H"	V2
"H"	"L"	"H"	VC
"H"	"H"	"H"	MV2

*: Don't care

The number of output pins is set by the SEL1 and SEL2 settings, as shown below.

SEL1	SEL2	Number of output pins
"H"	"H"	240 outputs (O1, O2, O3, …, O239, O240)
"H"	"L"	200 outputs (O21, O22, O23, …, O219, O220)
"L"	"H"	160 outputs (O41, O42, O43, …, O199, O200)
"L"	"L"	120 outputs (O61, O62, O63, …, O179, O180)

Pins that are made disabled by the SEL1 and SEL2 pins will output the nonselective level signal (VC) synchronized with the FR signal.

4.1.2 Level Shifter

The level shifter converts 5 V signals to high-voltage signals used for liquid crystal drive by multiplying the voltage.

4.1.3 Bidirectional Shift Register

The device is equipped with a 240-bit bidirectional shift register, where the first line signals that are input from the DIO1 and DIO2 pins are shifted sequentially. The shift direction is deterrmined by the SHL pin setting.

Relationship between SHL, DIO1, and DIO2

SHL	DIO1	DIO2
"H"	Serial output	Serial input
"L"	Serial input	Serial output

Relationship between SEL1/SEL2 and Shift Direction

SHL	SEL1	SEL2	Shift direction
"H"	"H"	"H"	DIO2→X1→…→X240→DIO1
	"H"	"L"	DIO2→X21→…→X220→DIO1
	"L"	"H"	DIO2→X41→…→X200→DIO1
	"L"	"L"	DIO2→X61→…→X180→DIO1
"L"	"H"	"H"	DIO1→X240→…→X1→DIO2
	"H"	"L"	DIO1→X220→…→X21→DIO2
	"L"	"H"	DIO1→X200→…→X41→DIO2
	"L"	"L"	DIO1→X180→…→X61→DIO2

4.1.4 Alternating Signal Generation Circuit

The alternating signal generation circuit generates the alternation signal fro liquid crystal display (FR signal). Alternating is enabled by setting each pin from FRWS0 to FRWS4 to VDD or VSS. When inputting alternating signals externally, alternating is enabled by setting all the pins from FRWS0 to FRWS4 to VSS.

Number of lines	FRWS4	FRWS3	FRWS2	FRWS1	FRWS0	Line alternating waveform	FR pin status	Remarks
0	0	0	0	0	0	—	Input	
1	0	0	0	0	1	1 line alternated	Output	(*1)
2	0	0	0	1	0	2 lines alternated		
3	0	0	0	1	1	3 lines alternated		
≀	≀	≀	≀	≀	≀	≀		
31	1	1	1	1	1	31 lines alternated		

*1: This setting is prohitited.

4.1.5 Control Circuit

Based on the DSPMS pin status, the control circuit processes the $\overline{DSPOF}$ signal internally and outputs the generated signal to the $\overline{DOC}$ signal.

DSPMS	$\overline{DSPOF}$ signal and internal processing
"H"	The liquid crystal output is set to the VC level during the “L” period of the $\overline{DSPOF}$ signal.
"L"	Holds the liquid crystal output at the VC level until 16 frames of data are input to DIO1 and DIO2 after a level change from "L" → "H" on the $\overline{DSPOF}$ signal.

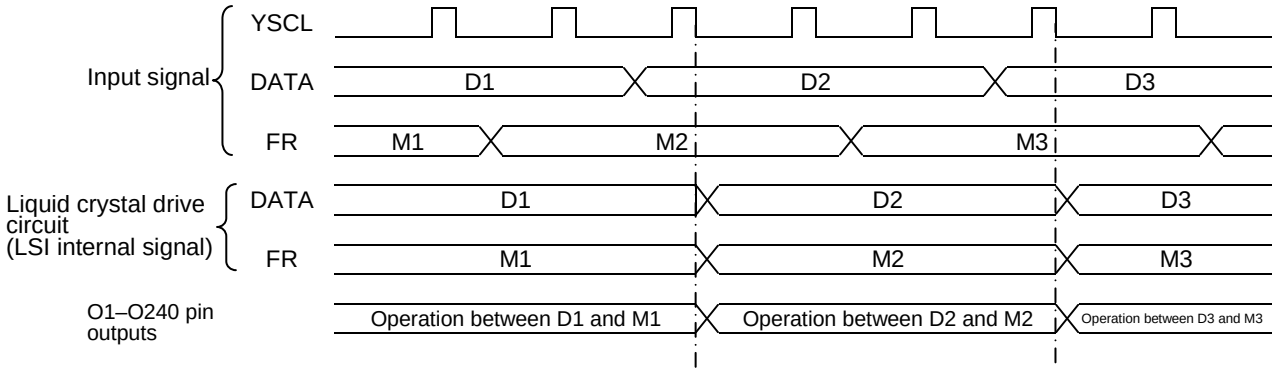
DSPMS	$\overline{DOC}$
"H"	Outputs "L" while the $\overline{DSPOF}$ signal is at “L”.
	Outputs "H" while the $\overline{DSPOF}$ signal is at “H”.
"L"	Even if the $\overline{DSPOF}$ signal level changes from "L" → "H", a "L" level is output until 16 frames of data are input to DIO1 and DIO2.

4.2 Timing Diagram

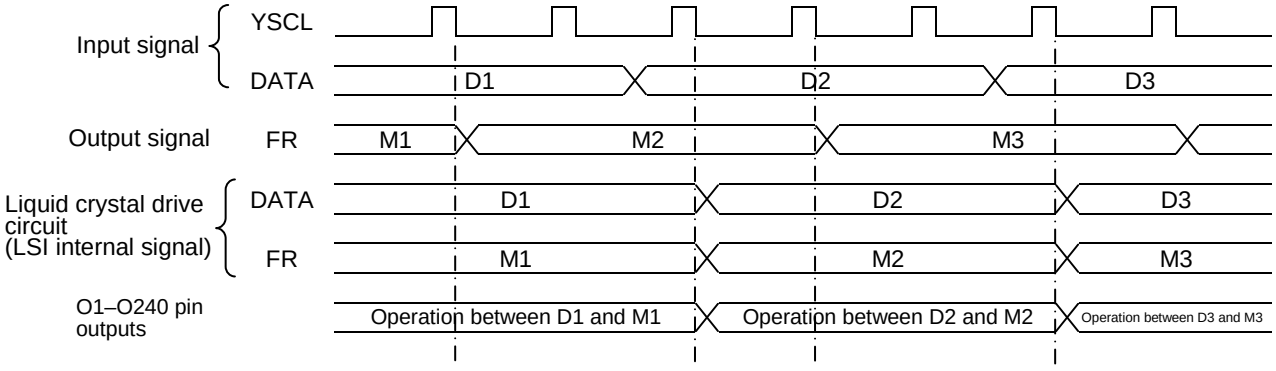
4.2.1 Timing of Connection with the Segment Driver

Input signal FR is latched at the rise of input signal YSCL and is propagated to the liquid crystal drive circuit at the next fall of YSCL. The DATA signal that is input from the DIO1 and DIO2 pins is latched at the fall of the YSCL signal and propagated to the liquid crystal drive circuit. The liquid crystal drive signal level (V2, MC, MV2) is determined by the operation between the FR signal propagated to the liquid crystal drive circuit and the DATA signal.
When using output of the FR signal through the FR signal generation circuit, connect the FR signal to the FR pin of the ML9461B directly. The FR signal inside of the LSI is processed by delaying it by two YSCL signals for the FR signal output from the common driver.

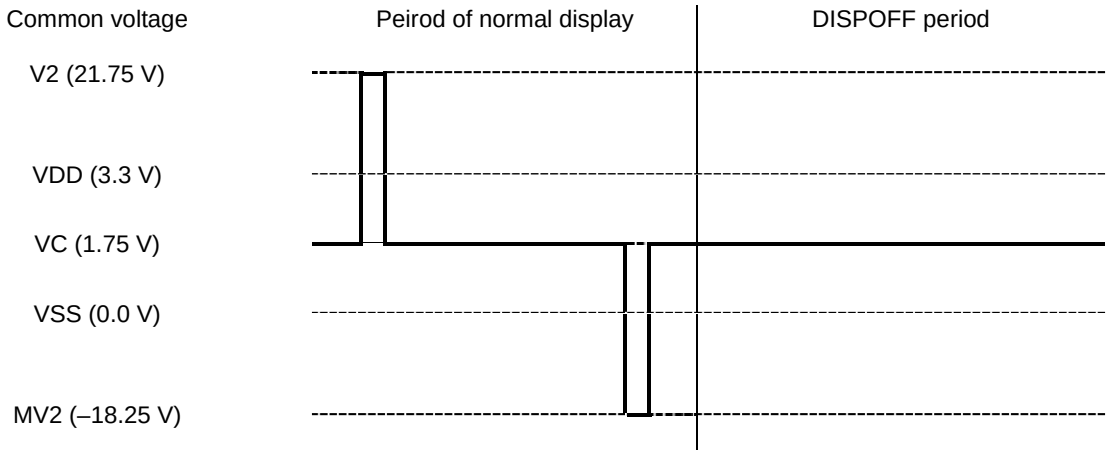
Timing Diagram when the FR pin is configured as input



Timing Diagram when the FR pin is configured as output

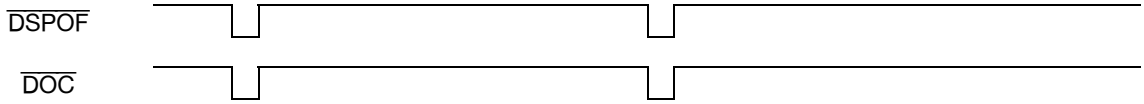


4.2.2 Driver Output Waveform

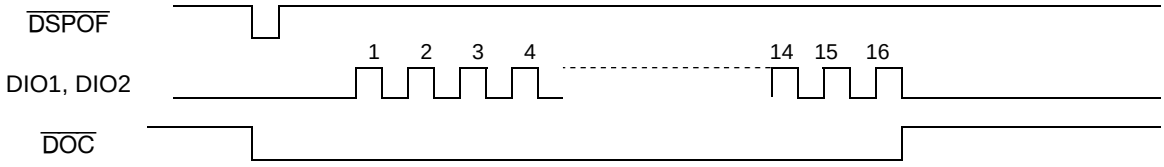


4.2.3 $\overline{DOC}$ Signal Waveforms

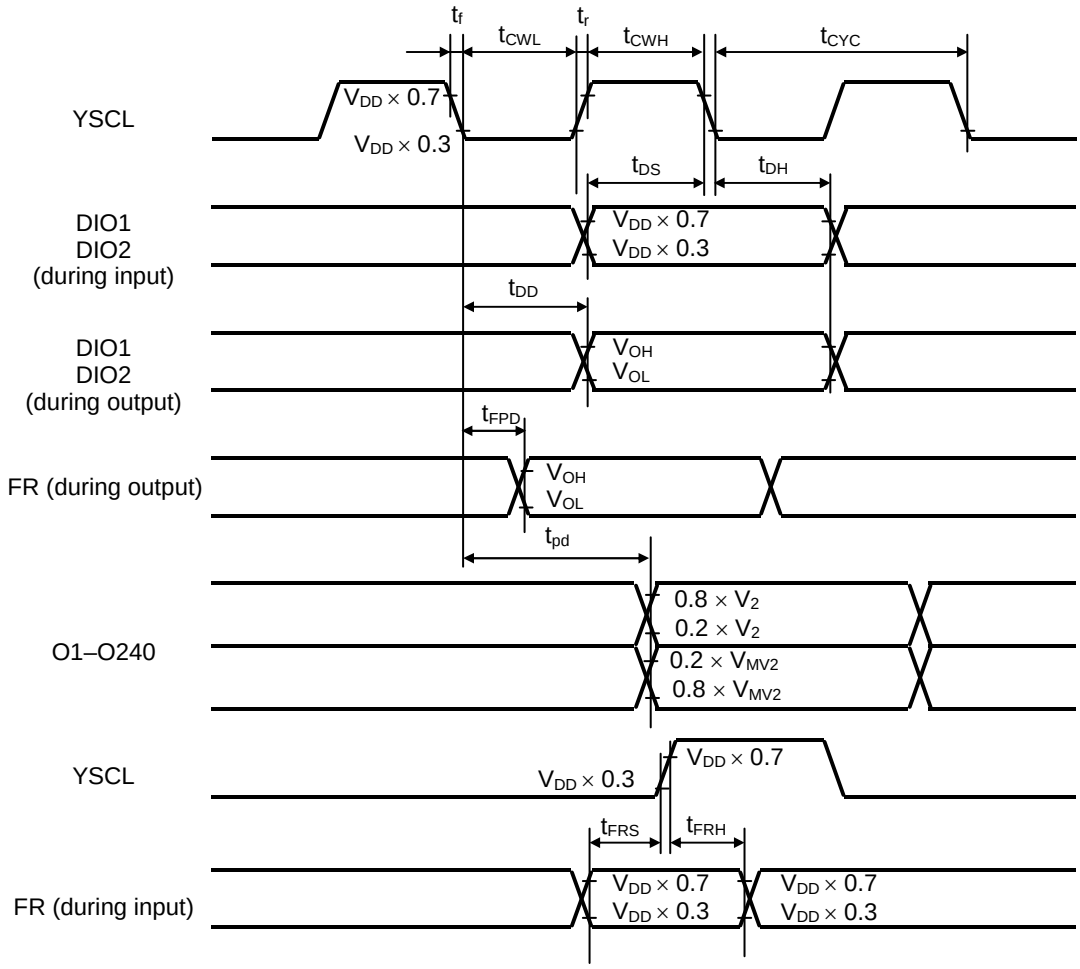
When DSPMS = “H”

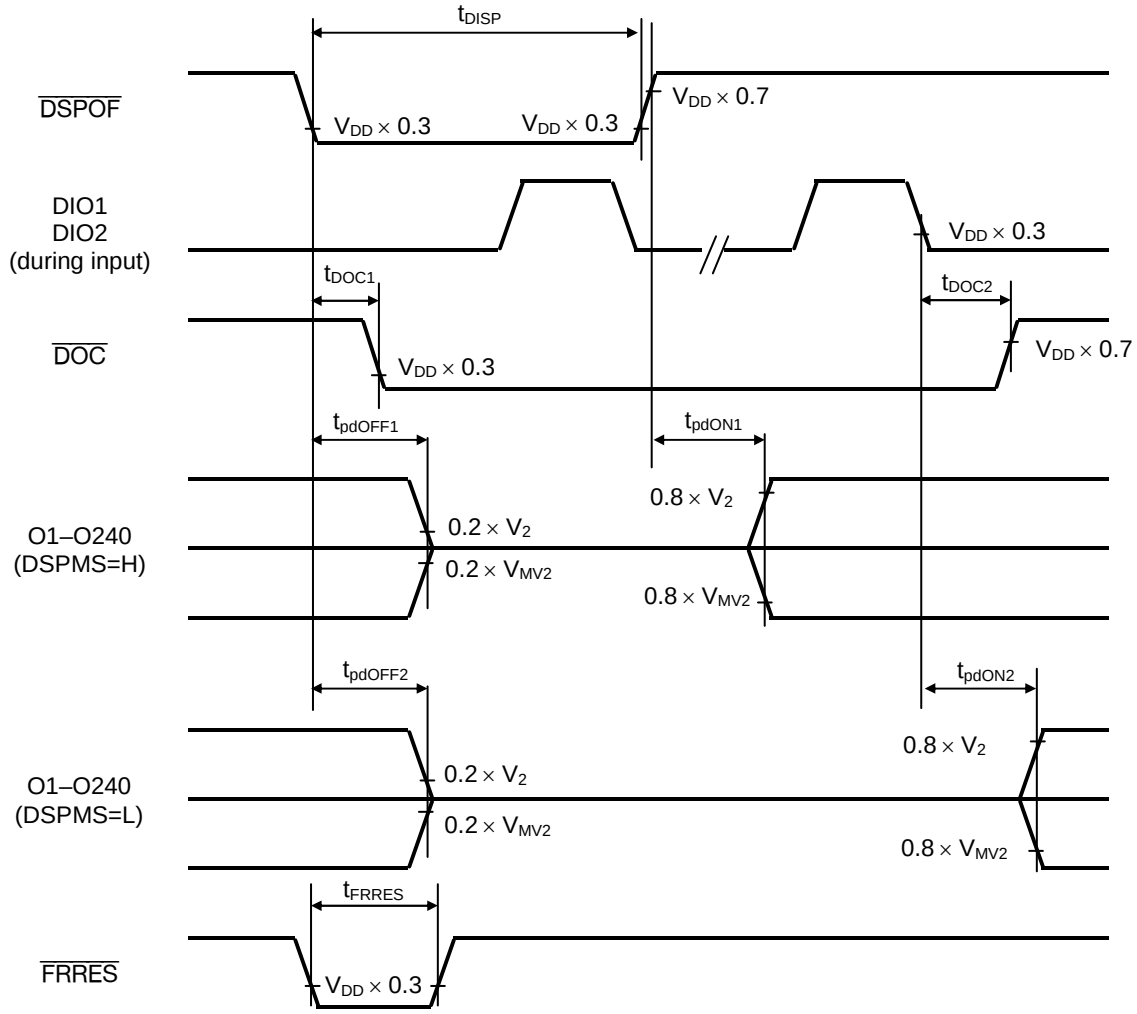


When DSPMS = “L”



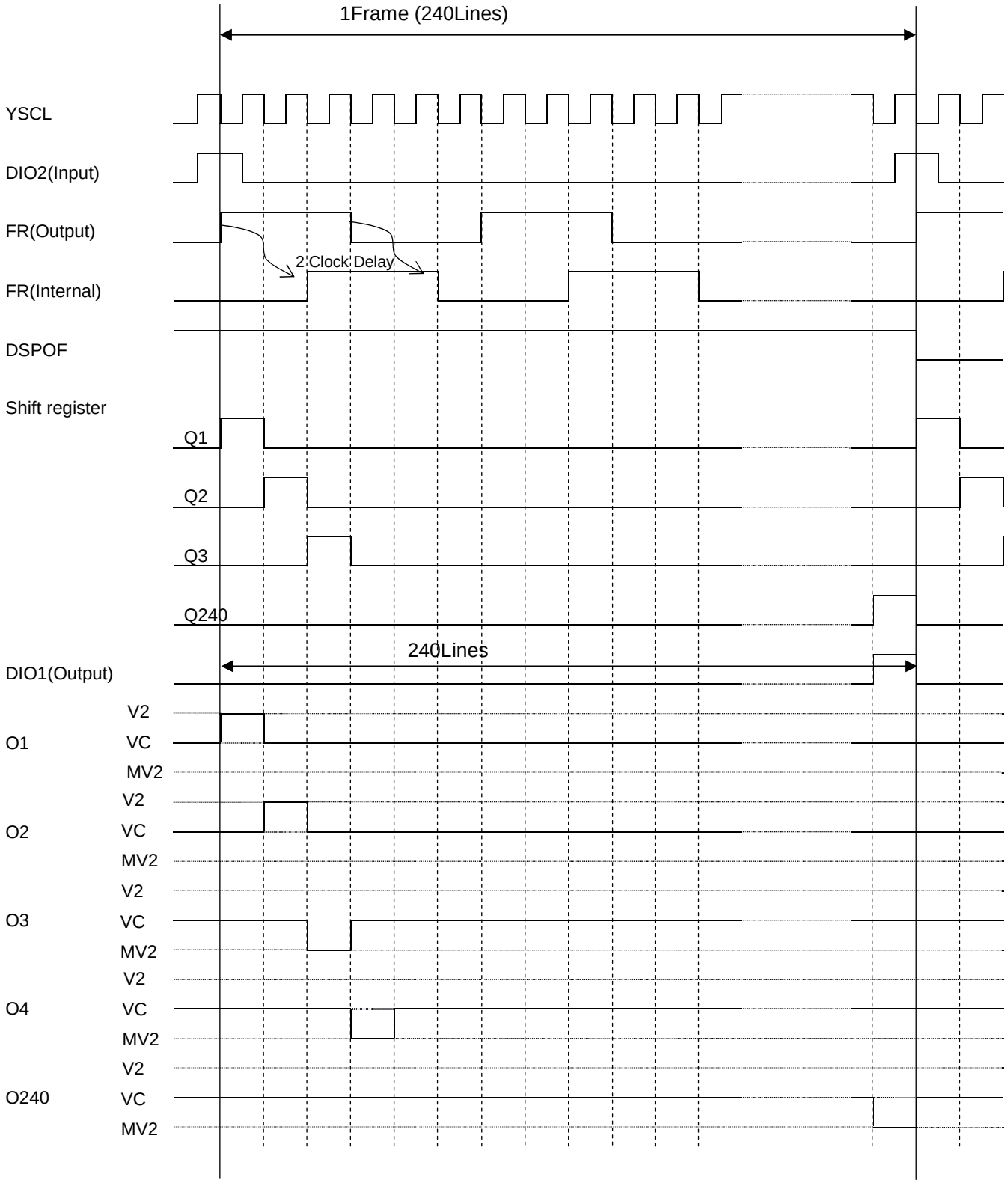
4.2.4 Timing Waveforms of AC Characteristics



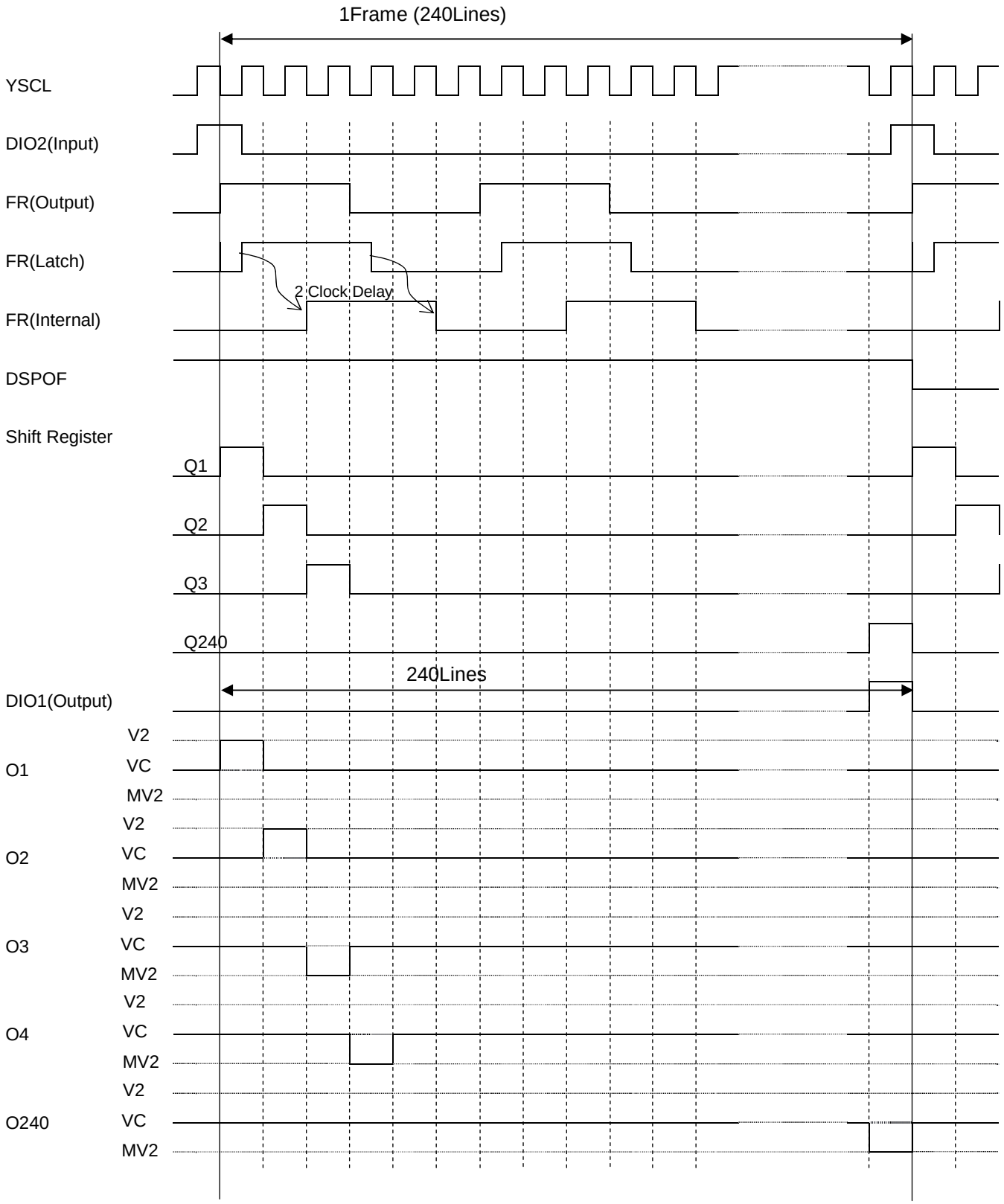

tDISP
DSPOF
VDD × 0.3
VDD × 0.3
VDD × 0.7
DIO1
DIO2
(during input)
VDD × 0.3
tDOC1
tDOC2
DOC
VDD × 0.3
VDD × 0.7
tpdOFF1
tpdON1
0.8 × V2
O1–O240
(DSPMS=H)
0.2 × V2
0.2 × VMV2
0.8 × VMV2
tpdOFF2
tpdON2
0.8 × V2
O1–O240
(DSPMS=L)
0.2 × V2
0.2 × VMV2
0.8 × VMV2
tFRRES
FRRES
VDD × 0.3

4.2.5 Alternating Waveforms

SEL1="H", SEL2="H"(240Output), SHL="H", FR Signal Internal generation, 3 lines inverted

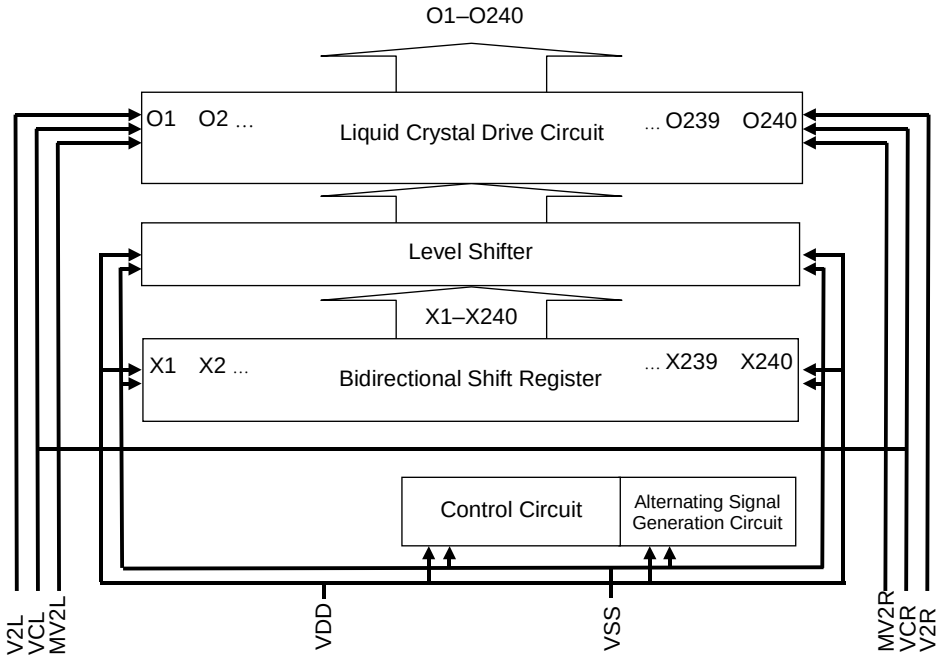


SEL1="H", SEL2="H"(240Output), SHL="H", FR Signal Internal generation, 3 lines inverted



5. Power Supply System

5.1 Power Supply Group



This LSI does completely separate Liquid crystal drive voltage and Operating voltage on its circuit architecture. Please do an anti-noise measure on a panel so that anoise Liquid crystal drive voltage does not round it in Operating voltage.

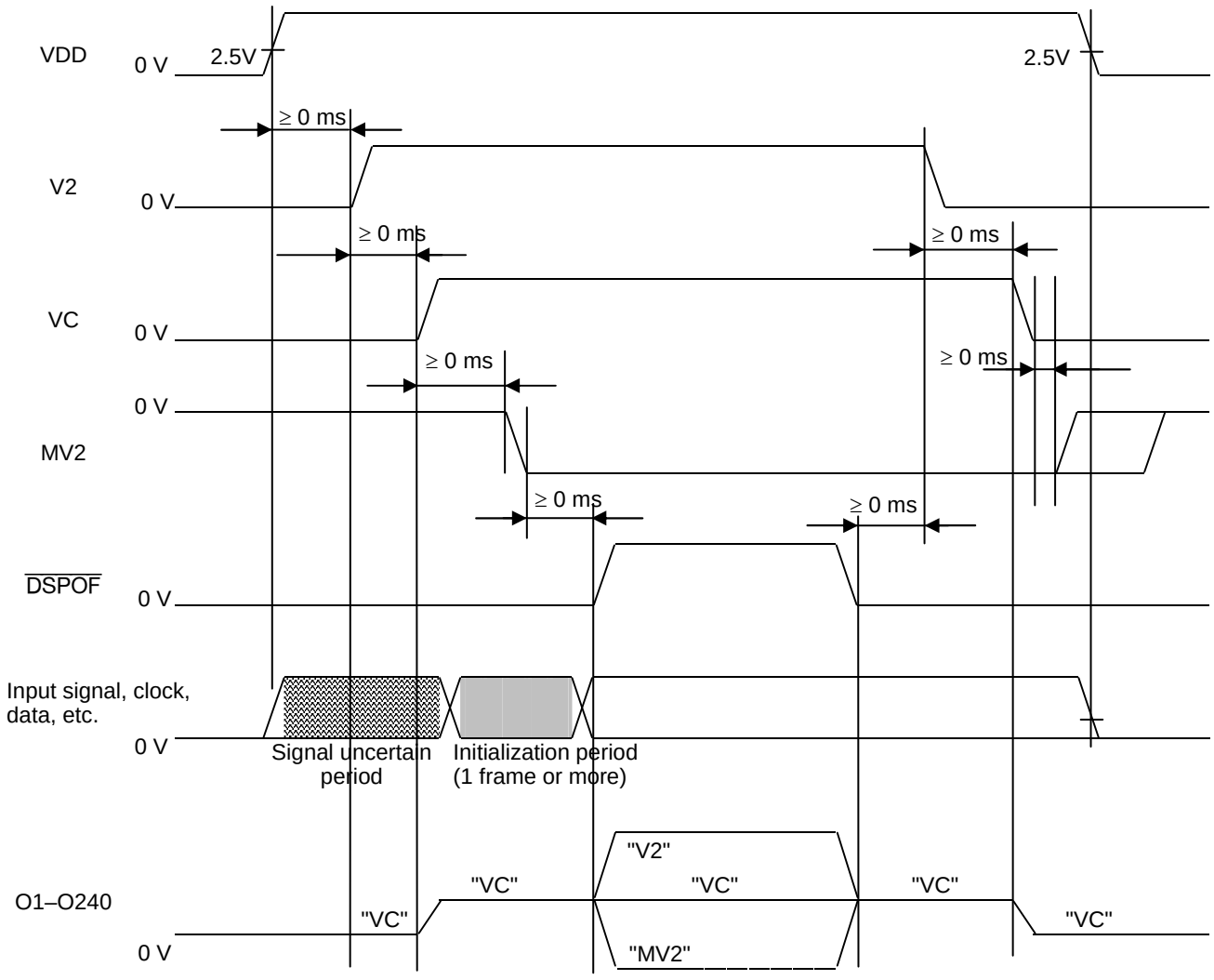
5.2 Power-On/Shutdown Sequence

5.2.1 Power-On Sequence

1. Apply power to (1)VSS–VDD, (2)VSS–V2, (3)VC, and (4)MV2 in this order. Then, input the VSS potential to the $\overline{\text{DSPOF}}$ pin.
2. The O1–O240 pins forcibly outputs the VC level by the DISPOFF function.
3. Even if an input signal is disturbed immediately after VDD is applied, priority is given to the DISPOFF function.
4. Input the predetermined signal(s) to initialize the registers in the driver. In this case, take at least one frame for the initialization period.
5. Input the VDD voltage to the $\overline{\text{DSPOF}}$ pin to release the DISPOFF function. At this point, the levels of the MV2, V2, and VC pin must have reached their respective predetermined potentials.

5.2.2 Shutdown Sequence

1. The $\overline{\text{DSPOF}}$ pin must remain set to the VSS potential.
2. Shut down the power supplies for liquid crystal in the order of (1)VSS–V2, (2)VC, and (3)MV2.
3. Reduce the voltage of VDD and the levels of the input signals to the VSS potential. At this point, the V2 and VC pin must completely drop to 3 V or lower.



6. Electrical Specifications

6.1 Absolute Maximum Ratings

V_{SS} = 0V

Parameter		Symbol	Condition	Rating	Unit	Applicable pins
Power supply voltage	Logic circuit	V_{DD}	Tj = –30°C to +75°C	–0.3 to +7.0	V	VDD
	liquid crystal drive circuit	V_2	Tj = –30°C to +75°C	–0.3 to +25.0	V	V2L, V2R
		V_{MV2}	Tj = –30°C to +75°C	–22.5 to +0.3	V	MV2L, MV2R
		V_M-V_{MV2}	Tj = –30°C to +75°C	–0.3 to +45.0	V	V2L,V2R,MV2L, MV2R
Input voltage (1)		V_{t1}	Tj = –30°C to +75°C	–0.3 to V_{DD}+0.3	V	DIO1, $\overline{\text{DSPOF}}$, SHL, FR, FRWS0, FRWS1, FRWS2, FRWS3, FRWS4, $\overline{\text{FRRES}}$, SEL1, SEL2, YSCL, DSPMS, DIO2
Input voltage (2)		V_2	Tj = –30°C to +75°C	–0.3 to +25.0	V	V2L, V2R
Input voltage (3)		V_{MV2}	Tj = –30°C to +75°C	–22.5 to +0.3	V	MV2L, MV2R
Input voltage (4)		V_C	Tj = –30°C to +75°C	–0.3 to +5.0	V	VCL, VCR
Output current/output short-circuit current		I_O	Tj = –30°C to +75°C	10	mA	$\overline{\text{FR}}$, DIO1, DIO2, $\overline{\text{DOC}}$, O1–O240
Junction temperature		Tj	—	–55 to +110	°C	—
Storate temperature range		T_{stg}	—	–55 to +110	°C	—

6.2 Recommended Operating Conditions (Guaranteed Operating Range)

V_{SS} = 0V, V_2–V_{MV2} = 15 to 43V, Tj = –30 to +75°C

Parameter		Symbol	Condition	Range			Unit	Applicable pins
				Min.	Typ.	Max.		
Power supply voltage	Logic circuit	V_{DD}	—	2.5	—	5.5	V	VDD
	liquid crystal drive circuit	V_2	—	8.8	—	24	V	V2L, V2R
		V_{MV2}	—	–21.5	—	–4	V	MV2L, MV2R
"H" Input voltage		V_{IH}	—	0.7×V_{DD}	—	V_{DD}	V	DIO1, $\overline{\text{DSPOF}}$, SHL, FR, DSPMS, FRWS0, FRWS1, FRWS2, FRWS3, FRWS4, $\overline{\text{FRRES}}$, YSCL, SEL1, SEL2, $\overline{\text{DOC}}$, DIO2
"L" Input voltage		V_{IL}	—	0	—	0.3×V_{DD}	V	
liquid crystal drive Input voltage (1)		V_2	—	8.8	—	24	V	V2L, V2R
liquid crystal drive Input voltage (2)		V_{MV2}	—	–21.5	—	–4	V	MV2L, MV2R
liquid crystal drive Input voltage (3)		V_C	—	0	—	3.5	V	VCL, VCR
Operating frequency		f_{CK}	V_{DD}=5V	(*1)	—	4	MHz	YSCL
			V_{DD}=3V	(*1)	—	3	MHz	YSCL
Operating temperature (Tj)		Topr	—	–30	—	75	°C	—
Load condition 1		C_{L1}	—	—	—	30	pF	DIO1, DIO2
Load condition 2		C_{L2}	—	—	—	100	pF	$\overline{\text{DOC}}$, O1–O240
Input rise waveform		t_r	—	—	—	30	ns	YSCL
Input fall waveform		t_f	—	—	—	30	ns	YSCL
Clock "High" period		t_{CWH}	—	20	—	—	ns	YSCL
Clock "Low" period		t_{CWL}	—	250	—	—	ns	YSCL
Data setup time		t_{DS}	—	70	—	—	ns	DIO1, DIO2, YSCL
Data hold time		t_{DH}	—	10	—	—	ns	DIO1, DIO2, YSCL
FR setup time		t_{FRS}	—	20	—	—	ns	FR, YSCL
FR hold time		t_{FRH}	—	20	—	—	ns	FR, YSCL

"—" indicates that no particular value is specified.

*1: 5kHz is specified for the test condition.

Note:

Insert bypass capacitors by referring to the Application Circuit described later so that power supplies will be stabilized. It is recommended that 0.1 μF CA capacitors (JIS (Japanese Industrial Standards) FJ(F) equivalent) be used.

6.3 DC Characteristics

V_{DD} = 2.5 to 5.5V, V_{SS} = 0V, V_2–V_{MV2} = 15 to 43V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	"H" level input voltage	V_{IH}	—	V_{DD}×0.7	—	V_{DD}	V	DIO1, $\overline{\text{DSPOF}}$, SHL, FR, DSPMS, FRWS0, FRWS1, FRWS2, FRWS3, FRWS4, $\overline{\text{FRRES}}$, YSCL, SEL1, SEL2, DIO2
2	"L" level input voltage	V_{IL}	—	0	—	V_{DD}×0.3	V	
3	"H" level output voltage	V_{OH}	I_{OH} = –0.4mA	V_{DD}–0.4	—	—	V	FR, DIO1, DIO2, $\overline{\text{DOC}}$
4	"L" level output voltage	V_{OL}	I_{OL} = 0.4mA	—	—	0.4	V	
5	Supply current (1)	I_{CC1}	V_{DD} = 3.3V V_2–V_{MV2} = 40V fYSCL = 19.2kHz f_{FR} = 1.5kHz 240-output mode Ta = 25°C No load	—	10	40	μA	VDD
6	Supply current (2)	I_{CC2}	V_{DD} = 5.0V V_2–V_{MV2} = 40V f_{YSCL} = 19.2kHz f_{FR} = 1.5kHz 240-output mode Ta = 25°C No load	—	20	50	μA	VDD
7	Supply current (3)	I_{CC3}	V_{DD} = 3.3V V_2–V_{MV2} = 40V f_{YSCL} = 19.2kHz f_{FR} = 1.5kHz 240-output mode Ta = 25°C No load	—	25	50	μA	V2
8	Static supply current	I_{DDS}	Ta = 25°C	—	—	10	μA	VDD
9	Input leakage current 1	I_{IL1}	V_{IN} = V_{DD} to V_{SS}	–5	—	5	μA	DIO1, $\overline{\text{DSPOF}}$, SHL, FR, DSPMS, FRWS0, FRWS1, FRWS2, FRWS3, FRWS4, $\overline{\text{FRRES}}$, YSCL, SEL1, SEL2, DIO2
10	Input leakage current 2	I_{IL2}	—	–25	—	25	μA	VCL, VCR
11	ON resistance between Vi and Oj	R_{ON}	ΔVON = 0.5V V_2 = 21.75V V_{MV2} = –18.25V V_C = 1.75V	—	0.7	2.0	kΩ	O1–O240
			ΔVON = 0.5V V_2 = 11.75V V_{MV2} = –8.25V V_C = 1.75V	—	1.2	3.3	kΩ	O1–O240

Values in the Typ. column are for reference only.
"—" indicates that no particular value is specified.

6.4 AC Characteristics

6.4.1 AC Characteristics 1

V_{DD} = 2.5 to 4.5V, V_{SS} = 0V, V_2 = 21.5V, V_C = 0V, V_{MV2} =-21.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Clock cycle time	t_{CYC}	—	330	—	—	ns	YSCL
2	YSCL “H” level width	t_{CWH}	—	20	—	—	ns	YSCL
3	YSCL “L” level width	t_{CWL}	—	250	—	—	ns	YSCL
4	YSCL rise time	t_r	—	—	—	30	ns	YSCL
5	YSCL fall time	t_f	—	—	—	30	ns	YSCL
6	Data setup time	t_{DS}	—	70	—	—	ns	DIO1, DIO2, YSCL
7	Data hold time	t_{DH}	—	10	—	—	ns	DIO1, DIO2, YSCL
8	Data output delay time	t_{DD}	(*1)	—	—	200	ns	DIO1, DIO2, YSCL
9	FR output delay time	t_{FRD}	(*1)	—	—	140	ns	FR, YSCL
10	FR setup time	t_{FRS}	—	20	—	—	ns	FR, YSCL
11	FR hold time	t_{FRH}	—	20	—	—	ns	FR, YSCL
12	$\overline{DOC}$ output delay time 1	t_{DOC1}	DSPMS = H (*2)	—	—	200	ns	$\overline{DSPOF}$, $\overline{DOC}$
			DSPMS = L (*2)	—	—	1500	ns	$\overline{DSPOF}$, $\overline{DOC}$
13	$\overline{DOC}$ output delay time 2	t_{DOC2}	(*2)	—	—	300	ns	DIO1, DIO2, $\overline{DOC}$
14	Common output delay time from $\overline{DSPOF}$ fall	t_{pdFF1}	DSPMS = H (*2)	—	—	1200	ns	$\overline{DSPOF}$, O1 to O240
		t_{pdOFF2}	DSPMS = L (*2)	—	—	2500	ns	$\overline{DSPOF}$, O1 to O240
15	Common output delay time from $\overline{DSPOF}$ rise	t_{pdON1}	DSPMS = H (*2)	—	—	1200	ns	$\overline{DSPOF}$, O1 to O240
16	Common output delay time from DIO fall	t_{pdON2}	DSPMS = L (*2)	—	—	1200	ns	DIO1, DIO2, O1 to O240
17	$\overline{DSPOF}$ “L” level width (*3)	t_{DISP}	DSPMS = L	100	—	—	ns	$\overline{DSPOF}$
18	$\overline{FRRES}$ “L” level width (*3)	t_{FRRES}	—	100	—	—	ns	$\overline{FRRES}$

Values in the Typ. column are for reference only.
“—” indicates that no particular value is specified.

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, V_2 = 21.5V, V_C = 0V, V_{MV2} =-21.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Clock cycle time	t_{CYC}	—	245	—	—	ns	YSCL
2	YSCL “H” level width	t_{CWH}	—	15	—	—	ns	YSCL
3	YSCL “L” level width	t_{CWL}	—	170	—	—	ns	YSCL
4	YSCL rise time	t_r	—	—	—	30	ns	YSCL
5	YSCL fall time	t_f	—	—	—	30	ns	YSCL
6	Data setup time	t_{DS}	—	50	—	—	ns	DIO1, DIO2, YSCL
7	Data hold time	t_{DH}	—	10	—	—	ns	DIO1, DIO2, YSCL
8	Data output delay time	t_{DD}	(*1)	—	—	150	ns	DIO1, DIO2, YSCL
9	FR output delay time	t_{FRD}	(*1)	—	—	100	ns	FR, YSCL
10	FR setup time	t_{FRS}	—	15	—	—	ns	FR, YSCL
11	FR hold time	t_{FRH}	—	15	—	—	ns	FR, YSCL
12	$\overline{DOC}$ output delay time 1	t_{DOC1}	DSPMS = H (*2)	—	—	140	ns	$\overline{DSPOF}$, $\overline{DOC}$
			DSPMS = L (*2)	—	—	1000	ns	$\overline{DSPOF}$, $\overline{DOC}$
13	$\overline{DOC}$ output delay time 2	t_{DOC2}	(*2)	—	—	200	ns	DIO1, DIO2, $\overline{DOC}$
14	Common output delay time from $\overline{DSPOF}$ fall	t_{pdOFF1}	DSPMS = H (*2)	—	—	700	ns	$\overline{DSPOF}$, O1 to O240
		t_{pdOFF2}	DSPMS = L (*2)	—	—	2000	ns	$\overline{DSPOF}$, O1 to O240
15	Common output delay time from $\overline{DSPOF}$ rise	t_{pdON1}	DSPMS = H (*2)	—	—	700	ns	$\overline{DSPOF}$, O1 to O240
16	Common output delay time from DIO fall	t_{pdON2}	DSPMS = L (*2)	—	—	700	ns	DIO1, DIO2, O1 to O240
17	$\overline{DSPOF}$ “L” level width(*3)	t_{DISP}	DSPMS = L	100	—	—	ns	$\overline{DSPOF}$
18	$\overline{FRRES}$ “L” level width(*3)	t_{FRRES}	—	100	—	—	ns	$\overline{FRRES}$

Values in the Typ. column are for reference only.
“—” indicates that no particular value is specified.

6.4.2 AC Characteristics 2

V_{DD} = 2.5 to 4.5V, V_{SS} = 0V, V_2 = 21.5V, V_C = 0V, V_{MV2} =-21.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Output delay time	t_{pd}	(*2)	—	—	1.2	μs	O1–O240, FR

"—" indicates that no particular value is specified.

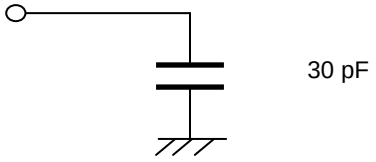
6.4.3 AC Characteristics 3

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, V_2 = 21.5V, V_C = 0V, V_{MV2} =-21.5V, Tj = –30 to +75°C

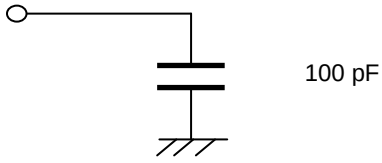
No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Output delay time	t_{pd}	(*2)	—	—	0.7	μs	O1–O240, FR

"—" indicates that no particular value is specified.

*1: Load condition



*2: Load condition



*3: If any signal whose pulse width is shorter than this value, the device may not operate normally.

7. PAD CONFIGURATION

7.1 Pad Coordinates (Au Bump Chip: ML9460CVWA)

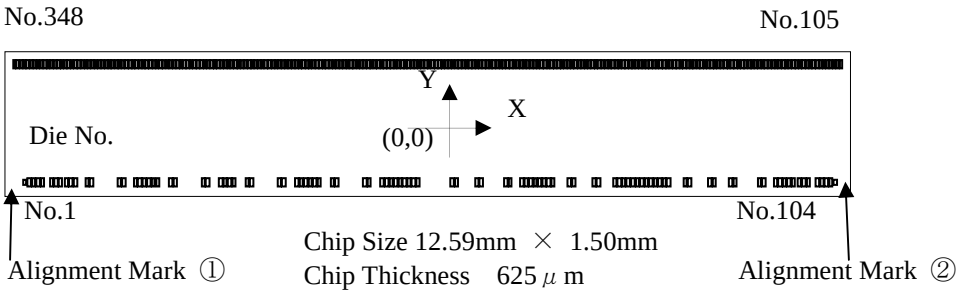
No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]
1	DUMMY	-5936	-604.2	81	DUMMY	3406.8	-604.2	161	O186	3275	606.3	241	O106	-725	606.3
2	DUMMY	-5870	-604.2	82	DUMMY	3472.8	-604.2	162	O185	3225	606.3	242	O105	-775	606.3
3	V2L	-5804	-604.2	83	DUMMY	3538.8	-604.2	163	O184	3175	606.3	243	O104	-825	606.3
4	V2L	-5738	-604.2	84	YSCL	3779	-604.2	164	O183	3125	606.3	244	O103	-875	606.3
5	V2L	-5672	-604.2	85	YSCL	3845	-604.2	165	O182	3075	606.3	245	O102	-925	606.3
6	VCL	-5539.4	-604.2	86	DSPMS	4141.6	-604.2	166	O181	3025	606.3	246	O101	-975	606.3
7	VCL	-5473.4	-604.2	87	DSPMS	4207.6	-604.2	167	O180	2975	606.3	247	O100	-1025	606.3
8	VCL	-5407.4	-604.2	88	DUMMY	4447.8	-604.2	168	O179	2925	606.3	248	O99	-1075	606.3
9	MV2L	-5320.1	-604.2	89	DUMMY	4513.8	-604.2	169	O178	2875	606.3	249	O98	-1125	606.3
10	MV2L	-5254.1	-604.2	90	DIO1	4871	-604.2	170	O177	2825	606.3	250	O97	-1175	606.3
11	MV2L	-5188.1	-604.2	91	DIO1	4937	-604.2	171	O176	2775	606.3	251	O96	-1225	606.3
12	DIO2	-5017.1	-604.2	92	DUMMY	5108	-604.2	172	O175	2725	606.3	252	O95	-1275	606.3
13	DIO2	-4951.1	-604.2	93	DUMMY	5174	-604.2	173	O174	2675	606.3	253	O94	-1325	606.3
14	FR	-4543.2	-604.2	94	MV2R	5240	-604.2	174	O173	2625	606.3	254	O93	-1375	606.3
15	FR	-4477.2	-604.2	95	MV2R	5306	-604.2	175	O172	2575	606.3	255	O92	-1425	606.3
16	DUMMY	-4306.2	-604.2	96	MV2R	5372	-604.2	176	O171	2525	606.3	256	O91	-1475	606.3
17	DUMMY	-4240.2	-604.2	97	VCR	5459.3	-604.2	177	O170	2475	606.3	257	O90	-1525	606.3
18	DUMMY	-4174.2	-604.2	98	VCR	5525.3	-604.2	178	O169	2425	606.3	258	O89	-1575	606.3
19	DUMMY	-4108.2	-604.2	99	VCR	5591.3	-604.2	179	O168	2375	606.3	259	O88	-1625	606.3
20	DUMMY	-4042.2	-604.2	100	V2R	5723.9	-604.2	180	O167	2325	606.3	260	O87	-1675	606.3
21	DUMMY	-3976.2	-604.2	101	V2R	5789.9	-604.2	181	O166	2275	606.3	261	O86	-1725	606.3
22	$\overline{\text{FRRES}}$	-3784.4	-604.2	102	V2R	5855.9	-604.2	182	O165	2225	606.3	262	O85	-1775	606.3
23	$\overline{\text{FRRES}}$	-3718.4	-604.2	103	DUMMY	5921.9	-604.2	183	O164	2175	606.3	263	O84	-1825	606.3
24	FRWS4	-3310.5	-604.2	104	DUMMY	5987.9	-604.2	184	O163	2125	606.3	264	O83	-1875	606.3
25	FRWS4	-3244.5	-604.2	105	DUMMY	6075.1	606.3	185	O162	2075	606.3	265	O82	-1925	606.3
26	DUMMY	-3052.7	-604.2	106	DUMMY	6025.1	606.3	186	O161	2025	606.3	266	O81	-1975	606.3
27	DUMMY	-2986.7	-604.2	107	O240	5975	606.3	187	O160	1975	606.3	267	O80	-2025	606.3
28	DUMMY	-2920.7	-604.2	108	O239	5925	606.3	188	O159	1925	606.3	268	O79	-2075	606.3
29	DUMMY	-2854.7	-604.2	109	O238	5875	606.3	189	O158	1875	606.3	269	O78	-2125	606.3
30	FRWS3	-2663	-604.2	110	O237	5825	606.3	190	O157	1825	606.3	270	O77	-2175	606.3
31	FRWS3	-2597	-604.2	111	O236	5775	606.3	191	O156	1775	606.3	271	O76	-2225	606.3
32	FRWS2	-2189.1	-604.2	112	O235	5725	606.3	192	O155	1725	606.3	272	O75	-2275	606.3
33	FRWS2	-2123.1	-604.2	113	O234	5675	606.3	193	O154	1675	606.3	273	O74	-2325	606.3
34	DUMMY	-1931.3	-604.2	114	O233	5625	606.3	194	O153	1625	606.3	274	O73	-2375	606.3
35	DUMMY	-1865.3	-604.2	115	O232	5575	606.3	195	O152	1575	606.3	275	O72	-2425	606.3
36	DUMMY	-1799.3	-604.2	116	O231	5525	606.3	196	O151	1525	606.3	276	O71	-2475	606.3
37	DUMMY	-1733.3	-604.2	117	O230	5475	606.3	197	O150	1475	606.3	277	O70	-2525	606.3
38	DUMMY	-1667.3	-604.2	118	O229	5425	606.3	198	O149	1425	606.3	278	O69	-2575	606.3
39	DUMMY	-1601.3	-604.2	119	O228	5375	606.3	199	O148	1375	606.3	279	O68	-2625	606.3
40	FRWS1	-1409.4	-604.2	120	O227	5325	606.3	200	O147	1325	606.3	280	O67	-2675	606.3
41	FRWS1	-1343.4	-604.2	121	O226	5275	606.3	201	O146	1275	606.3	281	O66	-2725	606.3
42	FRWS0	-935.6	-604.2	122	O225	5225	606.3	202	O145	1225	606.3	282	O65	-2775	606.3
43	FRWS0	-869.6	-604.2	123	O224	5175	606.3	203	O144	1175	606.3	283	O64	-2825	606.3
44	DUMMY	-677.7	-604.2	124	O223	5125	606.3	204	O143	1125	606.3	284	O63	-2875	606.3
45	DUMMY	-611.7	-604.2	125	O222	5075	606.3	205	O142	1075	606.3	285	O62	-2925	606.3
46	DUMMY	-545.7	-604.2	126	O221	5025	606.3	206	O141	1025	606.3	286	O61	-2975	606.3
47	DUMMY	-479.7	-604.2	127	O220	4975	606.3	207	O140	975	606.3	287	O60	-3025	606.3
48	DUMMY	-413.7	-604.2	128	O219	4925	606.3	208	O139	925	606.3	288	O59	-3075	606.3
49	DUMMY	-347.7	-604.2	129	O218	4875	606.3	209	O138	875	606.3	289	O58	-3125	606.3
50	VDD	-281.7	-604.2	130	O217	4825	606.3	210	O137	825	606.3	290	O57	-3175	606.3
51	VDD	-215.7	-604.2	131	O216	4775	606.3	211	O136	775	606.3	291	O56	-3225	606.3
52	VDD	-149.7	-604.2	132	O215	4725	606.3	212	O135	725	606.3	292	O55	-3275	606.3
53	SEL2	352.6	-604.2	133	O214	4675	606.3	213	O134	675	606.3	293	O54	-3325	606.3
54	SEL2	418.6	-604.2	134	O213	4625	606.3	214	O133	625	606.3	294	O53	-3375	606.3
55	SEL1	715.1	-604.2	135	O212	4575	606.3	215	O132	575	606.3	295	O52	-3425	606.3
56	SEL1	781.1	-604.2	136	O211	4525	606.3	216	O131	525	606.3	296	O51	-3475	606.3
57	$\overline{\text{DOC}}$	1138.2	-604.2	137	O210	4475	606.3	217	O130	475	606.3	297	O50	-3525	606.3
58	$\overline{\text{DOC}}$	1204.2	-604.2	138	O209	4425	606.3	218	O129	425	606.3	298	O49	-3575	606.3
59	DUMMY	1375.8	-604.2	139	O208	4375	606.3	219	O128	375	606.3	299	O48	-3625	606.3
60	DUMMY	1441.8	-604.2	140	O207	4325	606.3	220	O127	325	606.3	300	O47	-3675	606.3
61	DUMMY	1507.8	-604.2	141	O206	4275	606.3	221	O126	275	606.3	301	O46	-3725	606.3
62	DUMMY	1573.8	-604.2	142	O205	4225	606.3	222	O125	225	606.3	302	O45	-3775	606.3
63	DUMMY	1639.8	-604.2	143	O204	4175	606.3	223	O124	175	606.3	303	O44	-3825	606.3
64	DUMMY	1705.8	-604.2	144	O203	4125	606.3	224	O123	125	606.3	304	O43	-3875	606.3
65	DUMMY	1771.8	-604.2	145	O202	4075	606.3	225	O122	75	606.3	305	O42	-3925	606.3
66	DUMMY	1837.8	-604.2	146	O201	4025	606.3	226	O121	25	606.3	306	O41	-3975	606.3
67	$\overline{\text{DSPOF}}$	2078	-604.2	147	O200	3975	606.3	227	O120	-25	606.3	307	O40	-4025	606.3
68	$\overline{\text{DSPOF}}$	2144	-604.2	148	O199	3925	606.3	228	O119	-75	606.3	308	O39	-4075	606.3
69	SHL	2440.6	-604.2	149	O198	3875	606.3	229	O118	-125	606.3	309	O38	-4125	606.3
70	SHL	2506.6	-604.2	150	O197	3825	606.3	230	O117	-175	606.3	310	O37	-4175	606.3
71	DUMMY	2746.8	-604.2	151	O196	3775	606.3	231	O116	-225	606.3	311	O36	-4225	606.3
72	DUMMY	2812.8	-604.2	152	O195	3725	606.3	232	O115	-275	606.3	312	O35	-4275	606.3
73	VSS	2878.8	-604.2	153	O194	3675	606.3	233	O114	-325	606.3	313	O34	-4325	606.3
74	VSS	2944.8	-604.2	154	O193	3625	606.3	234	O113	-375	606.3	314	O33	-4375	606.3
75	VSS	3010.8	-604.2	155	O192	3575	606.3	235	O112	-425	606.3	315	O32	-4425	606.3
76	DUMMY	3076.8	-604.2	156	O191	3525	606.3	236	O111	-475	606.3	316	O31	-4475	606.3
77	DUMMY	3142.8	-604.2	157	O190	3475	606.3	237	O110	-525	606.3	317	O30	-4525	606.3
78	DUMMY	3208.8	-604.2	158	O189	3425	606.3	238	O109	-575	606.3	318	O29	-4575	606.3
79	DUMMY	3274.8	-604.2	159	O188	3375	606.3	239	O108	-625	606.3	319	O28	-4625	606.3
80	DUMMY	3340.8	-604.2	160	O187	3325	606.3	240	O107	-675	606.3	320	O27	-4675	606.3

Note: Leave DUMMY pads open.

No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]
321	O26	-4725	606.3	331	O16	-5225	606.3	341	O6	-5725	606.3
322	O25	-4775	606.3	332	O15	-5275	606.3	342	O5	-5775	606.3
323	O24	-4825	606.3	333	O14	-5325	606.3	343	O4	-5825	606.3
324	O23	-4875	606.3	334	O13	-5375	606.3	344	O3	-5875	606.3
325	O22	-4925	606.3	335	O12	-5425	606.3	345	O2	-5925	606.3
326	O21	-4975	606.3	336	O11	-5475	606.3	346	O1	-5975	606.3
327	O20	-5025	606.3	337	O10	-5525	606.3	347	DUMMY	-6025	606.3
328	O19	-5075	606.3	338	O9	-5575	606.3	348	DUMMY	-6075	606.3
329	O18	-5125	606.3	339	O8	-5625	606.3				
330	O17	-5175	606.3	340	O7	-5675	606.3				

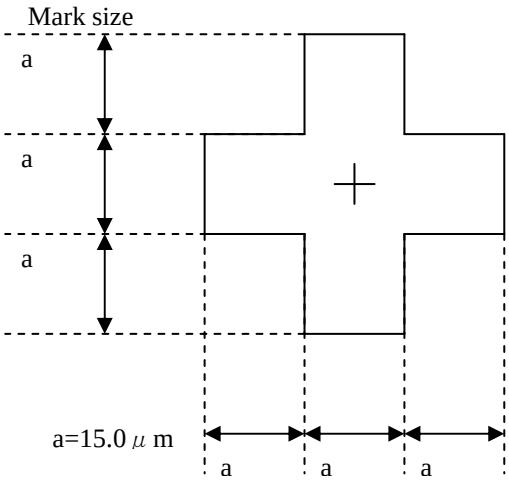
Note: Leave DUMMY pads open.

Alignment Mark Information



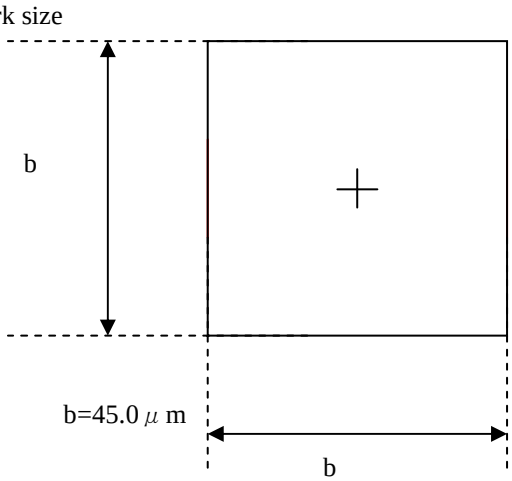
Alignment Mark①

Center Coordinate (-6074.4, -588.1)



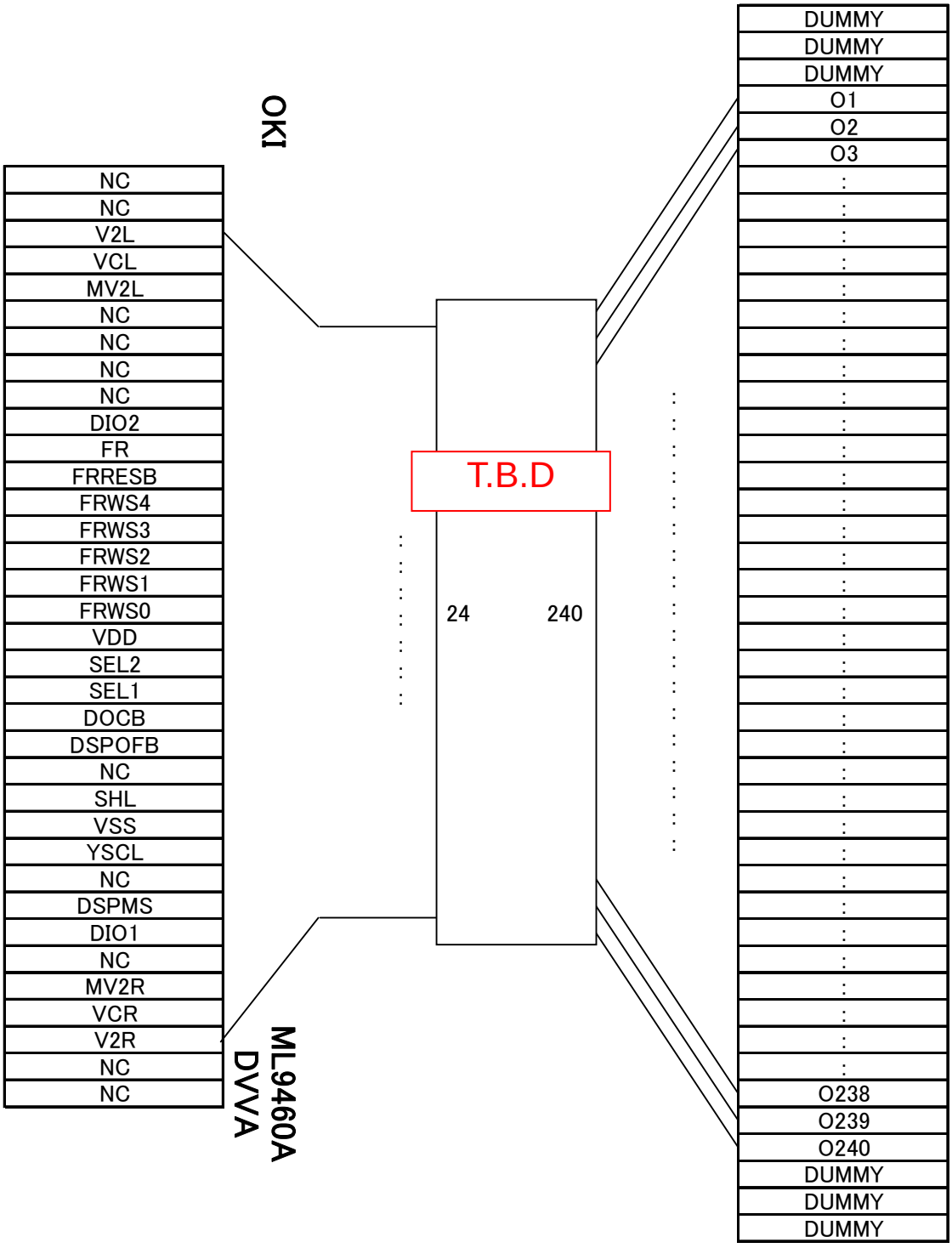
Alignment Mark②

Center Coordinate (6074.4, -588.1)



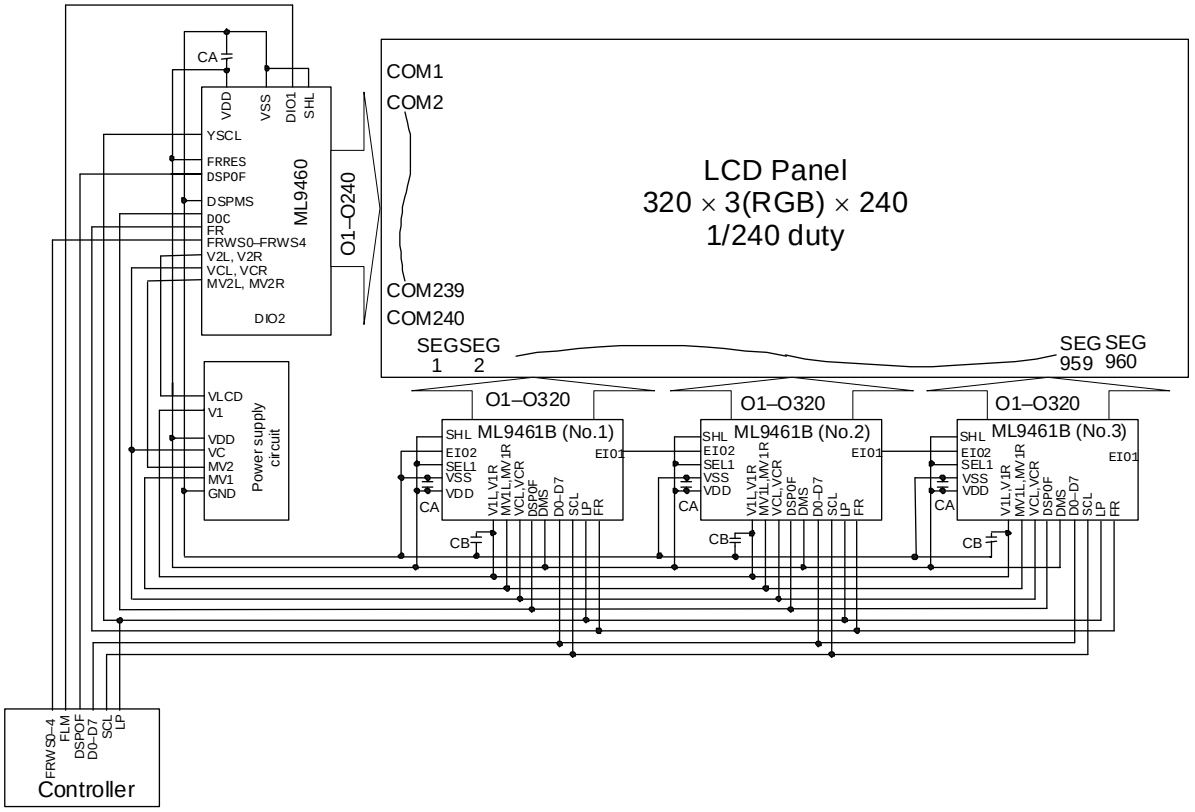
7.2 Pin Configuration (TCP: ML9460ADVVA)

TOP VIEW



The drawing shown does not specify the exact outline of the TCP;it only specifies the pin layout.

8. Application Circuit (With External Components Connected)



Insert a capacitor CA,CB specified in the Recommended Operating Conditions (Guaranteed Operating Range). It is recommended that 0.1 μF CA capacitors (JIS (Japanese Industrial Standards) FJ(F) equivalent) be used.

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9460-01	May 21, 2007	–	–	Preliminary edition 1
PEDL9460-02	Dec 5, 2007	1	1	Au Bump Chip product name DVWA→CVWA
		13	13	Additional comment.
		–	23	Additional 7.2 Pin Configuration.
		23	24	Changed Application Circuit.
PEDL9460-03	Dec 17,2008	–	–	Changed to OKI Semiconductor's format
		1,7,24	1,7,24	ML9461→ML9461B
FEDL9460-01	Jan 29,2009	–	–	Final edition 1
		2	2	Additional comment for $\overline{\text{FRRES}}$ pin
		–	4	Additional 2.2 Inupt and Output Configuration
		13	14	Changed explanation
		22	23	Additional Alignment Mark Information

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