SM3-8RG5
8 REFERENCE
STRATUM 3 MODULE

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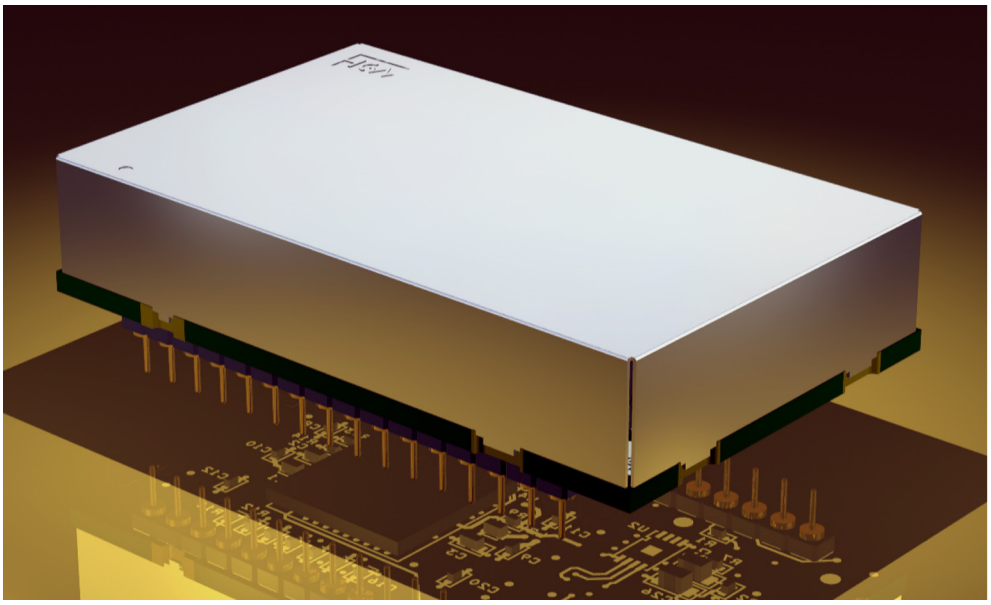

Application

The SM3-8RG5 Timing Module is a complete system clock module for Stratum 3 timing applications and conforms to GR-1244-CORE (Issue 2), GR-253-CORE (Issue 3) and ITU-T G.812 (Option 3). Applications include shared port adapters, data digital cross connects, ADM's, DSLAM's, multiservice platforms, switches and routers in TDM, SDH and SONET environments.

The SM3-8RG5 Timing Module guarantees full Stratum 3 compliance with a minimum of effort and cost in the smallest complete package available.

This product is ROHS-5 compliant. ROHS-5 indicates that this product is ROHS compliant except for lead from those manufacturers wishing to take the lead exemption.

Features

- Small Package Size: 2.05" x 1.25" x 0.515"
- Eight Auto Select Input References, 8 kHz - 77.76 MHz
- Frequency Qualification and Loss of Reference detection for each input
- Hitless Reference Switching
- Master/Slave Operation with Phase Adjustment
- Manual/Autonomous Operation
- Bi-Directional SPI Port Control and Status Reporting
- Three CMOS Frequency Outputs - Output1 from 1.544 - 77.76MHz, M/S_Out@8KHz, BITS @2.048 MHz or 1.544 MHz
- 3.3V operation
- ROHS-5 Compliant

RoHS-5/6 COMPLIANT

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General Description

The SM3-8RG5 timing module provides a clock output that meets or exceeds Stratum 3 specifications given in GR-1244-CORE (Issue 2), GR-253-CORE (Issue 3) and ITU-T G.812 (option 3). The SM3-8RG5 features eight reference inputs. Each input will auto-detect the following reference frequencies: 8 kHz, 1.544 MHz, 2.048 MHz, 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz and 77.76 MHz.

The SM3-8RG5 timing module can be configured during production to produce an output up to 77.76MHz. This output is derived from an onboard VCXO and must be specified when ordering. The second output is a BITS output selectable for either 1.544 or 2.048 MHz. The master/slave output is 8KHz. The user communicates with the SM3-8RG5 module through a SPI port. The user controls the SM3-8RG5 operation by writing to the appropriate registers. The user can also enable or disable SPI operation through a SPI_Enable pin.

The SM3-8RG5 offers a wide range of options for the system designer. The bandwidth is SPI Port-selectable from 0.025 Hz to 1.6 Hz. 0.098 Hz is the recommended operational bandwidth for Stratum 3 applications. The 8 kHz output has an adjustable pulse width. The pull-in range is also adjustable to establish the desired reference frequency rejection limits. A Free Run frequency calibration value can be written to the module to provide a high degree of accuracy in the free run mode. The reference frequency for any given reference input is automatically detected. A wealth of status information is available through the SPI Port registers. The user also has a choice between autonomous or full manual control operation.

In manual mode, the user controls the module operating modes Free Run, Hold Over or locked to a specific reference. If the chosen reference is unavailable or disqualified the module automatically enters Hold Over.

In autonomous control mode, operational mode selection occurs automatically based on reference priority and qualification status. When the active reference becomes disqualified, the module will switch to another qualified reference. If none is available, it will switch to Hold Over. In the revertive mode the module will seek to acquire the highest priority qualified reference. In the non-revertive mode the module will not return to the previous reference even after it is re-qualified unless there are no other qualified references.

Switching between references is hitless. Likewise, the output frequency slew rate is minimized during any change of operating mode, including entry into and return from Free Run or Hold Over to protect traffic from transient-induced bit errors.

Reference Status information and the operating mode information is accessed through status registers. The module will set the Interrupt pin (SPI_INT) low to indicate a status change.

Free Run operation guarantees an output within 4.6ppm of nominal frequency and Hold Over operation guarantees the output frequency will not change by more than 0.37ppm during the first 24 hours. Frequency accuracy is based on a precision oven to provide the stabilty required for Stratum 3 compliance.

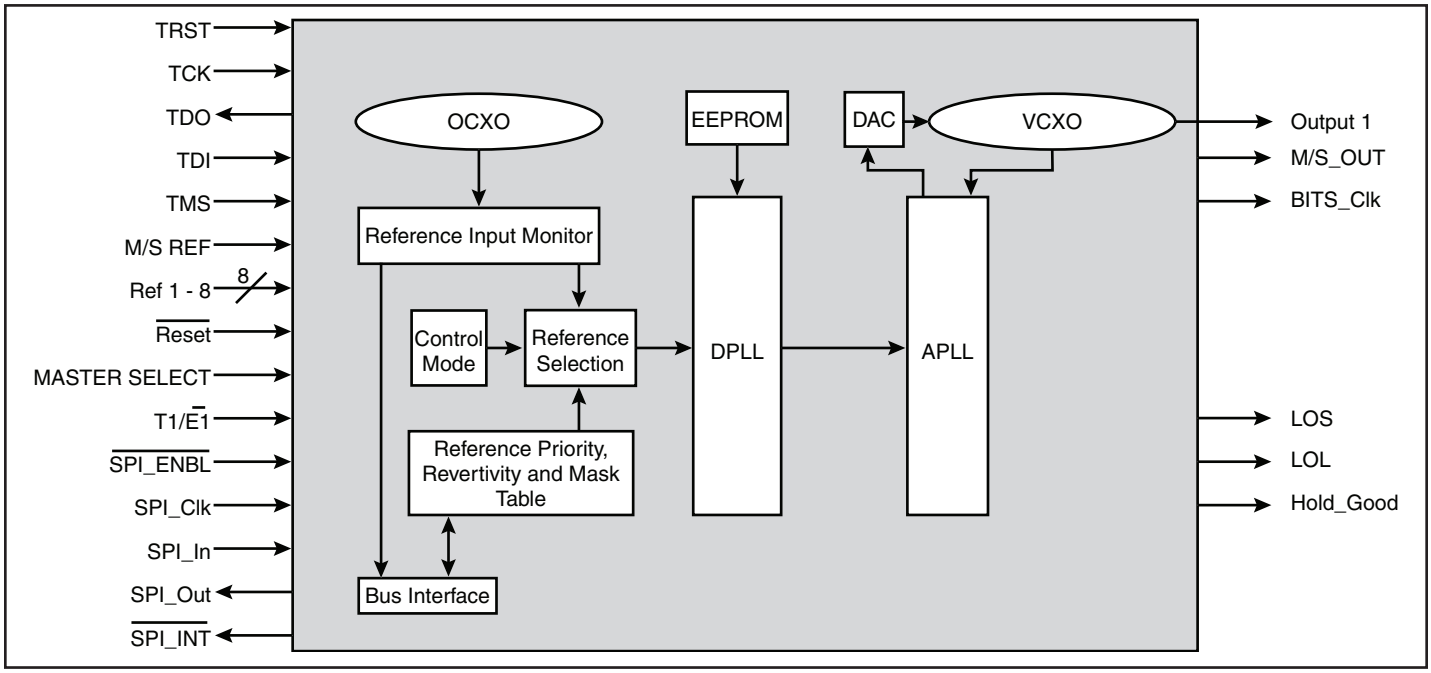
The SM3-8RG5 can be programmed to startup in any mode or bandwidth. The module may even be programmed to operate in an a fully autonomous mode with no further configuration required.

The module operates on 3.3V ± 5% with a typical power drain of less than 1.6W at turn on, dropping to approximately 1W @ room temperature after warming up. The module operates over the 0° to 70° C commercial temperature range.

Phase buildout can be enabled or disabled by means of the SPI port.

Functional Block Diagram

Figure 1



Specifications for Ultra Miniature Stratum 3

Table 1

Parameter	Specification
Voltage	3.3V ± 5%
Power	1.6W Maximum during start up, 1.0W Typical @ room temperature
Operating Temp Range	0° - 70°C
Reference Frequency 1 - 8	8 kHz - 77.76 MHz (Determined by customer's application)
CMOS Output Frequency #1 M/S_Out BITS_Clk	8 kHz - 77.76 MHz 8 kHz 1.544/2.048 MHz (Selectable)
Master/Slave Input Reference	8 kHz - 77.76 MHz
Input Reference Pulse Width	10 ns Min @ 8 kHz, 5 ns Min @ >8 kHz
Free Run Accuracy	4.6 ppm
Hold Over Accuracy	0.37 ppm
Dimensions	2.05 x 1.25 x 0.515 inches (52.07 x 31.75 x 13.08 mm)

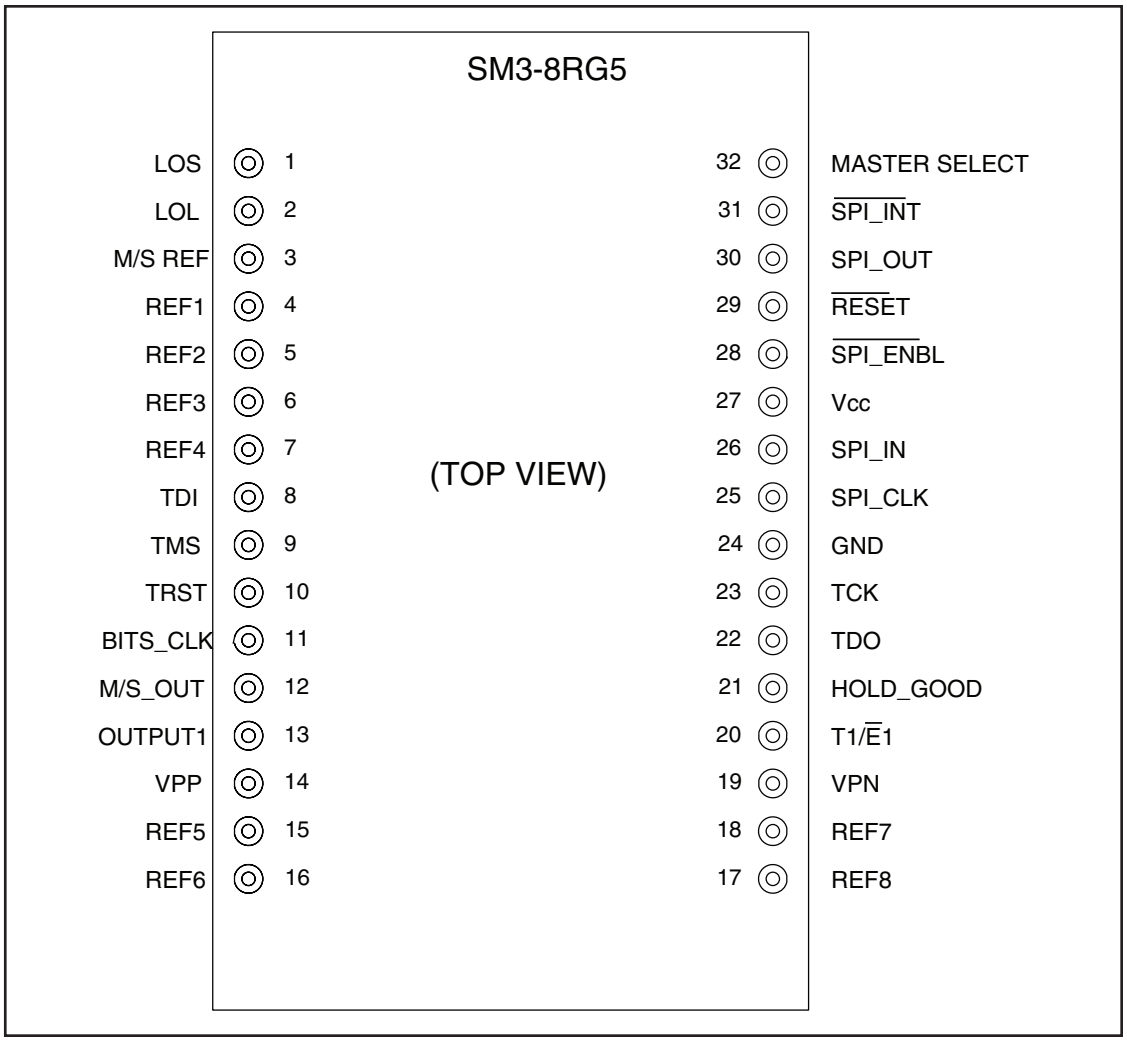
Pin Description

Table 2

Pin #	I/O	Pin Name	Pin Description
1	O	LOS	Alarm Output - Loss of Active Reference Signal
2	O	LOL	Alarm Output - Loss of Lock
3	I	M/S REF	Master/Slave Reference Input
4	I	REF1	Reference Input 1 – 8 kHz to 77.76 MHz auto detected
5	I	REF2	Reference Input 2 – 8 kHz to 77.76 MHz auto detected
6	I	REF3	Reference Input 3 – 8 kHz to 77.76 MHz auto detected
7	I	REF4	Reference Input 4 – 8 kHz to 77.76 MHz auto detected
8		TDI	JTAG TDI pin
9		TMS	JTAG TMS pin
10		TRST	JTAG TRST pin
11	O	BITS_CLK	1.544 or 2.048 MHz output selected by pin 14
12	O	M/S_OUT	Master/Slave 8 kHz output
13	O	OUTPUT1	Synchronous Primary Output
14		VPP	Positive Programming Supply Pin. During normal operation, it is recommended to float this pin.
15		REF5	Reference Input 5 – 8 kHz to 77.76 MHz auto detected
16		REF6	Reference Input 6 – 8 kHz to 77.76 MHz auto detected
17		REF8	Reference Input 8 – 8 kHz to 77.76 MHz auto detected
18		REF7	Reference Input 7 – 8 kHz to 77.76 MHz auto detected
19		VPN	Negative Programming Supply Pin. During normal operation, it is recommended to float this pin.
20	I	T 1/$\overline{E1}$	BITS_CLK select input – 1=1.544 MHz, 0=2.-48 MHz, 4.7k Ohm Pull-up
21	O	HOLD_GOOD	Holdover Good Output Flag – 1=Holdover Available
22		TDO	JTAG TDO pin
23		TCK	JTAG TCK pin
24		GND	Module Ground
25	I	SPI_CLK	SPI Port Clock input
26	I	SPI_IN	SPI Port Data input
27		VCC	3.3 Vdc VCC Supply Input
28	I	$\overline{\text{SPI\_ENBL}}$	SPI Port Enable input – Active Low, 4.7k Ohm Pull-up
29	I	$\overline{\text{RESET}}$	Module Reset – Active Low, 4.7k Ohm Pull-up
30	O	SPI_OUT	SPI Port Data Output
31	O	$\overline{\text{SPI\_INT}}$	SPI Port Interrupt Output
32	I	MASTER SELECT	Master/Slave select input – 1=Master, 0=Slave

Pin Diagram

Figure 2



Register Map

Table 3

Address	Reg Name	Description	Type
0x00	Chip_ID_Low	Low byte of chip ID	R
0x01	Chip_ID_High	High byte of chip ID	R
0x02	Chip_Revision	Chip revision number	R
0x03	Bandwidth_PBO	Bandwidth & Phase Build-Out option	R/W
0x04	Ctl_Mode	Manual or automatic selection of Op_Mode,BITS clock output frequency indication, and frame/multi-frame sync pulse width mode control	R/W
0x05	Op_Mode	Master Free Run, Locked, or Hold Over mode, or Slave mode	R/W
0x06	Max_Pullin_Range	Maximum pull-in range in 0.1 ppm units	R/W
0x07	M/S Input_Activity	Cross Reference activity	R
0x08	Ref_Activity	Activities of 8 reference inputs	R
0x09	Ref_Pullin_Sts	In or out of pull-in range of 8 reference inputs	R
0x0a	Ref_Qualified	Qualification of 8 reference inputs	R
0x0b	Ref_Mask	Availability mask for 8 reference inputs	R/W
0x0c	Ref_Available	Availability of 8 reference inputs	R

Register Map Continued

Table 3

0x0d	Ref_Rev_Delay	Reference reversion delay time, 0 - 255 minutes	R/W
0x0e	Phase_Offset	Phase offset between M/S REF & M/S Output (for the Slave in M/S operation) in 250ps resolution	R/W
0x0f	Calibration	Local oscillator digital calibration in 0.05 ppm resolution	R/W
0x10	Fr_Pulse_Width	Frame sync pulse width	R/W
0x11	DPLL_Status	Digital Phase Locked Loop status	R
0x12	Intr_Event	Interrupt events	R
0x13	Intr_Enable	Enable individual interrupt events	R/W
0x14	Ref1_Frq_Offset	Ref1 frequency offset in 0.2 ppm resolution	R
0x15	Ref2_Frq_Offset	Ref2 frequency offset in 0.2 ppm resolution	R
0x16	Ref3_Frq_Offset	Ref3 frequency offset in 0.2 ppm resolution	R
0x17	Ref4_Frq_Offset	Ref4 frequency offset in 0.2 ppm resolution	R
0x18	Ref5_Frq_Offset	Ref5 frequency offset in 0.2 ppm resolution	R
0x19	Ref6_Frq_Offset	Ref6 frequency offset in 0.2 ppm resolution	R
0x1a	Ref7_Frq_Offset	Ref7 frequency offset in 0.2 ppm resolution	R
0x1b	Ref8_Frq_Offset	Ref8 frequency offset in 0.2 ppm resolution	R
0x1c	Ref1_Frq_Priority	Ref1 frequency and priority	R/W
0x1d	Ref2_Frq_Priority	Ref2 frequency and priority	R/W
0x1e	Ref3_Frq_Priority	Ref3 frequency and priority	R/W
0x1f	Ref4_Frq_Priority	Ref4 frequency and priority	R/W
0x20	Ref5_Frq_Priority	Ref5 frequency and priority	R/W
0x21	Ref6_Frq_Priority	Ref6 frequency and priority	R/W
0x22	Ref7_Frq_Priority	Ref7 frequency and priority	R/W
0x23	Ref8_Frq_Priority	Ref8 frequency and priority	R/W
0x24	FreeRun Priority	Control and Priority for designation of Free Run as a reference	R/W
0x25	History_Policy	Sets policy for Hold Over history accumulation	R/W
0x26	History_CMD	Save, restore and flush comands for Hold Over history	R/W
0x27	HoldOver_Time	Indicates the time since entering Hold Over state	R
0x30	Cfgdata	Configuration data write register	R/W
0x31	Cfgctr_Lo	Configuration data write counter, low byte	R
0x32	Cfgctr_Hi	Configuration data write counter, high byte	R
0x33	Chksum	Configuration data checksum pass/fail indicator	R
0x35	EE_Wrt_Mode	Disables/Enables writing to the external EEPROM	R/W
0x37	EE_Cmd	Read/Write command & ready indication register for ext. EEPROM access	R/W
0x38	EE_Page_Num	Page number for external EEPROM access	R/W
0x39	EE_FIFO_Port	Read/Write data for external EEPROM access	R/W

Detailed Description

The SM3-8RG5 can accept up to 8 external references from 8 kHz to 77.76 MHz and each is monitored for signal presence and frequency offset. Additionally, a cross-couple reference input is provided for master/slave operation. Reference selection may be manual or automatic, according to pre-programmed priorities. All reference switches are performed in a hitless manner, and frequency ramp controls ensure smooth output signal transitions. When references are switched, the device provides an automatic phase build-out to minimize phase transitions in the output clocks.

Three output signals are provided, the first up to 77.76 MHz , the second fixed at 8 kHz for use as a Frame Sync signal as well as a cross-couple reference for master/slave operation. In slave mode, the output phase may be adjusted from -32 to +31.75nS relative to the master, to accommodate downstream system needs, such as different clock distribution path lengths. The third output is a BITS clock, selectable as either 1.544 MHz or 2.048 MHz.

Device operation may be in Free Run, locked, or Hold Over modes. In Free Run, the clock frequencies are simply determined by the accuracy of the calibrated internal clock. In locked mode, the SM3-8RG5 phase locks to the selected input reference. While locked, a frequency history is accumulated. In Hold Over mode, the output frequencies are generated according to this history.

The Digital Phase Locked Loop provides the critical filtering and frequency/phase control that meet or exceed all requirements in critical jitter and accuracy performance parameters. Filter bandwidth may be configured to suit applications requirements.

Control functions are provided via standard SPI bus register interface. Register access provides visibility into a variety of registered information as well as providing extensive programmable control capability.

Operating Modes: The SM3-8RG5 Operates in Either Free Run, Locked, or Hold Over Mode:

Free Run – In Free Run mode, **Output 1, M/S Output,** and **BITS_Clk**, the output clocks, are determined directly from and have the accuracy of the calibrated free running internal clock. Reference inputs continue to be monitored for signal presence and frequency offset, but are not used to synchronize the outputs.

Locked – The **Output 1, M/S Output,** and **BITS_Clk**, outputs are phase locked and track the selected input reference. Upon entering the Locked mode, the device begins an acquisition process that includes reference qualification and frequency slew rate limiting, if needed. Once satisfactory lock is achieved, the “Locked” bit is set in the DPLL_Status register, and a compilation of the frequency history of the selected reference is started. When a usable Hold Over history has been established, the **Hold_Good** pin is set, and the “Hold Over Available” bit is set in the **DPLL_Status** register.

Phase comparison and phase lock loop filtering operations in the SM3-8RG5 are completely digital. As a result, device and loop behavior are entirely predictable, repeatable, and extremely accurate. Carefully designed and proven algorithms and techniques ensure completely hit-less reference switches, operational mode changes, and master/slave switches.

Basic loop bandwidth is programmable from .025 Hz to 1.6 Hz, giving the user a wide range of control over the system response.

When a new reference is acquired, maximum frequency slew limits ensure smooth frequency changes. Once lock is achieved, (<100 seconds for stratum 3), the “Locked” bit is set. If the SM3-8RG5 is unable to maintain lock, Loss of Lock **(LOL)** is asserted. All transitions between locked, Hold Over and Free Run modes are performed with minimal phase events and smooth frequency and phase transitions.

Reference phase hits or phase differences encountered when switching references (or when entering locked mode) are nulled out with an automatic phase build-out function, with a residual phase error of less than 1ns.

Hold Over – Upon entering Hold Over mode, the **Output 1, M/S Output,** and **BITS_Clk**, outputs are determined from the Hold Over history established for the last selected reference. Output frequency is determined by a weighted average of the Hold Over history, and accuracy is determined by the internal clock. Hold Over mode may be entered manually or automatically. Automatic entry into Hold Over mode occurs when operating in the automatic mode, the reference is lost, and no other valid reference exists. The transfer into and out of Hold Over mode is designed to be smooth and free of hits. The frequency slew is also limited to a maximum of ±2 ppm/sec.

The history accumulation algorithm uses a first order frequency difference filtering algorithm. Typical holdover accumulation takes about 15 minutes. When a usable holdover history has been established, the **Hold_Good** pin is set, and the “Holdover Available” bit is set in the **DPLL_Status** register. The holdover history continues to be updated after “Holdover Avaialble” is declared.

The algorithm accumulates the holdover history only when it has locked to either an external reference in Master operation or the **M/S REF** clock in Slave operation, starting 15 minutes after power up. Tracking will be suspended automatically when switching to a new reference and in Hold Over or Free Run mode. A set of registers allows the application to control a holdover history maintenance policy, enabling either a re-build or continuance of the history when a reference switch occurs.

Furthermore, under register access control, a backup holdover history register is provided. It may be loaded from the active holdover history or restored to the active holdover history. The active holdover history may also be flushed.

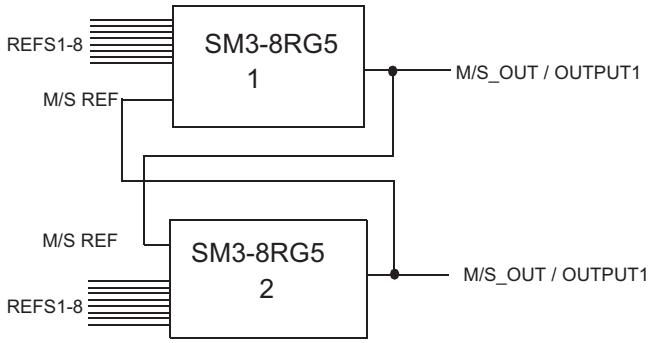
Holdover mode may be entered at any time. If there is no holdover history available, the prior output frequency will be maintained. When in holdover, the application may read (via register access) the time since holdover was enterred.

Master/Slave Operation

Pairs of SM3-8RG5 devices may be operated in a master/slave configuration for redundant timing source applications. A typical configuration is shown below.:

Master / Slave Configuration

Figure 3



The M/S Output or the Output 1 of each device may be cross-connected to the other device's M/S Ref input. The device auto-detects the frequency on the M/S Ref input. Master or slave state of a device is determined by the M/S pin. Thus, master/slave state is always manually controlled by the application. The master synchronizes to the selected input reference, while the slave synchronizes to the M/S Ref input. (Note that 8kHz frame phase alignment is maintained across a master/slave pair of devices only if M/S Output is used as the cross couple signal.)

The unit operating in slave mode locks on and phase-aligns to the cross-reference clock (M/S Output or Output 1) from the unit in master mode. The phase skew between the input cross-reference and the output clock for the slave unit is typically less than ±1ns (under ±3ns in dynamic situations, including reference jitter and wander).

Perfect phase alignment of the two Output 1 output clocks would require no delay on the cross-reference clock connection. To accommodate path length delays, the SM3-8RG5 provides a programmable phase skew feature. The slave's Output 1 or M/S Output may be phase shifted -32nS to +31.75nS relative to M/S Input according to the contents of the MS_Phase_Offset register to compensate for the path length of the M/S Output or Output 1 to M/S Input connection. This offset may therefore be programmed to exactly compensate for the actual path length delay associated with the particular application's cross-reference traces. The offset may further be adjusted to accommodate any output clock distribution path delay differences. Thus, master/slave switches with the SM3 devices may be accomplished with near-zero phase hits.

The first time a unit becomes a slave, such as immediately after power-up, its output clock phase starts out arbitrary, and will quickly phase-align to the cross-reference from the master unit. The phase skew will be eliminated (or converged to the programmed phase offset) step by step. The whole pull-in-and-lock process will complete in about 60 seconds. There is no frequency slew protection in slave mode. In slave mode, the unit's mission is to lock to and follow the master.

Once a pair of units has been operating in aligned master/slave mode, and a master/slave switch occurs, the unit that becomes master will maintain its output clock phase and frequency while a phase build-out (to the current output clock phase) is performed on its selected reference input. Therefore, as master mode operation commences, there will be no phase or frequency hits on the clock output.

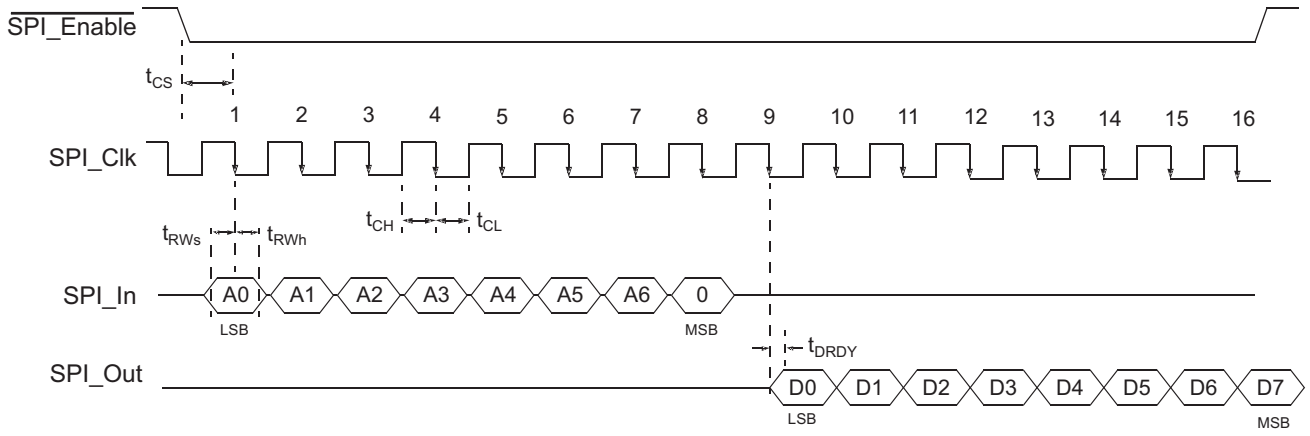
Likewise, the unit that becomes the slave will maintain its output clock frequency and phase for 1 msec before starting to follow the cross-reference, protecting the downstream clock users during the switch. Assuming the phase offset is programmed for the actual propagation delay of this cross-reference path, there will again be no phase hits on the output clock of the unit that has transitioned from master to slave.

Serial Communication

The user can control the operation of the SM3-8RG5 module through the SPI port. Timing diagrams are shown below. This interface is only for point-to-point applications.

Serial Interface Timing, Read Access

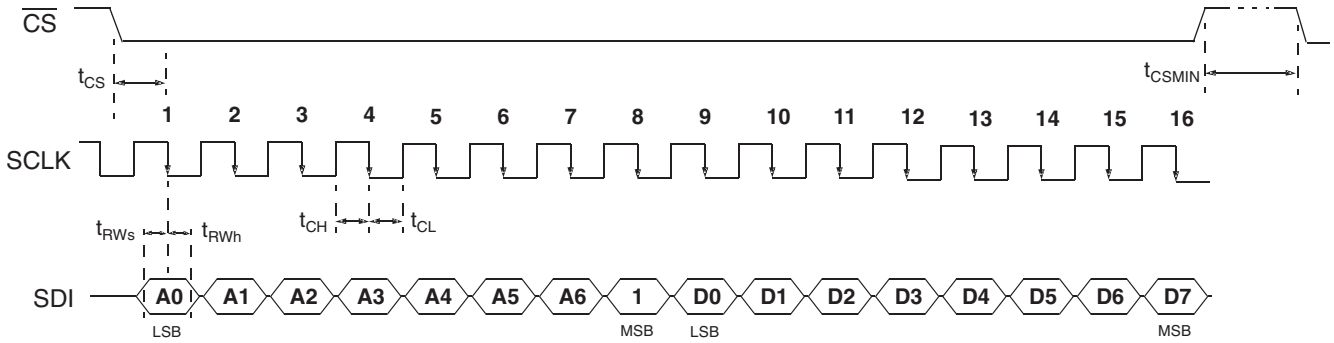
Figure 4



NOTE: SPI_OUT is normally held at logic 0 except when tri-stated during an address read cycle on the SPI_IN pin or when data is being output on the SPI_OUT pin.

Serial Interface Timing, Write Access

Figure 5



Serial Interface Timing

Table 4

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
t_{CS}	~~SPI~~_Enable low to SPI_CLK low	15	-	-	ns	
t_{CH}	SPI_CLK high time	25	-	-	ns	
t_{CL}	SPI_CLK low time	25	-	-	ns	
t_{RWs}	Read/Write setup time	15	-	-	ns	
t_{RWh}	Read/Write hold time	15	-	-	ns	
t_{DRDY}	Data ready	-	-	25	ns	
t_{HLD}	Data Hold	15	-	-	ns	
t_{CSTRI}	Chip Select to data tri-state	5	-	-	ns	
t_{CSMIN}	Minimum delay between successive accesses	300	-	-	ns	

Reference Input Quality Monitoring

Each reference input is monitored for signal presence and frequency offset. Signal presence for the **Ref1-8** inputs is indicated in the **Ref_Activity** register and signal presence for the **M/S REF** is indicated in bit 0 of the **M/S REF_Activity** register. The frequency offset between the **Ref1-8** inputs and the calibrated local oscillator is available in the **Ref_Frq_Offset** registers (8). Register **Ref_Pullin_Sts** indicates, for each of the **Ref1-8** inputs, if the reference is within the maximum pull-in range. The maximum pull-in range is indicated in register **Max_Pullin_Range**, and may be set in 0.1ppm increments. Typically, it would be set according to the values specified by the standards (GR-1244) appropriate for the particular stratum of operation.

The **Ref_Qualified** register contains the "anded" condition of the **Ref_Activity** and **Ref_Pullin_Sts** registers for each of the **Ref1-8** inputs, qualified for 10 seconds. When a reference signal has been present for > 10 seconds and is within the pull-in range, it's bit is set.

The **Ref_Available** register contains the "anded" condition of the **Ref_Qualified** register and the **Ref_Mask** register, and therefore represents the availability of a reference for selection when automatic reference and operational mode selection is enabled.

Reference Input Selection, Frequencies, and Mode Selection

One of eight reference input signals (**Ref 1-8**) are selected for synchronization in Master mode (as below in the **Op_Mode** register description. 0x05). **Ref 1-8** may each be 8 kHz, 1.544 MHz, 2.048 MHz, 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz or 77.76 MHz.

Reference frequencies are auto-detected and the detected frequency can be read from the **Ref_Frq_Priority** registers (See **Register Descriptions and Operation** section).

Active reference and operational mode selection may be manual or automatic, as determined by bit 1 in the **Ctl_Mode** register. In manual mode, register writes to **Op_Mode** select the reference and mode. The reset default is manual mode.

The M/S REF input for slave operation is frequency auto-detected and may be 8kHz, 1.544MHz, 2.048MHz, 12.96MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz or 77.76MHz. Signal presence and frequency for the M/S REF input is indicated in bits 0-3 of the **M/S REF_Activity** register.

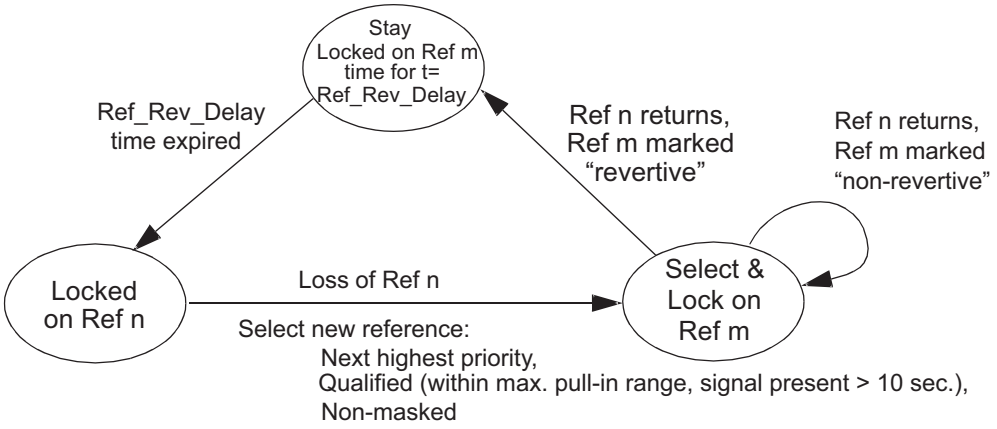
In automatic mode, the reference is selected according to the priorities written to the eight **Ref_Frq_Priority** registers. Individual references may be masked for use/non-use according to the **Ref_Mask** register. A reference may only be selected if it is "available" - that is, it is qualified, as indicated in the **Ref_Qualified** register, and is not masked (See **Reference Input Quality Monitoring and Register Descriptions and Operation** sections).

Furthermore, Bit 3 of each **Ref_Frq_Priority** register will determine if that reference is revertive or non-revertive. When a reference fails, the next highest priority "available" (signal present, non-masked, and acceptable frequency offset) reference will be selected. When a reference returns, it will be switched to only if it is of higher priority and the current active reference is marked "Revertive". Additionally, the reversion is delayed according to the value written to the **Ref_Rev_Delay** register (From 0 to 255 minutes).

The automatic reference selection is shown in the following state diagram:

Automatic Reference Selection

Figure 6

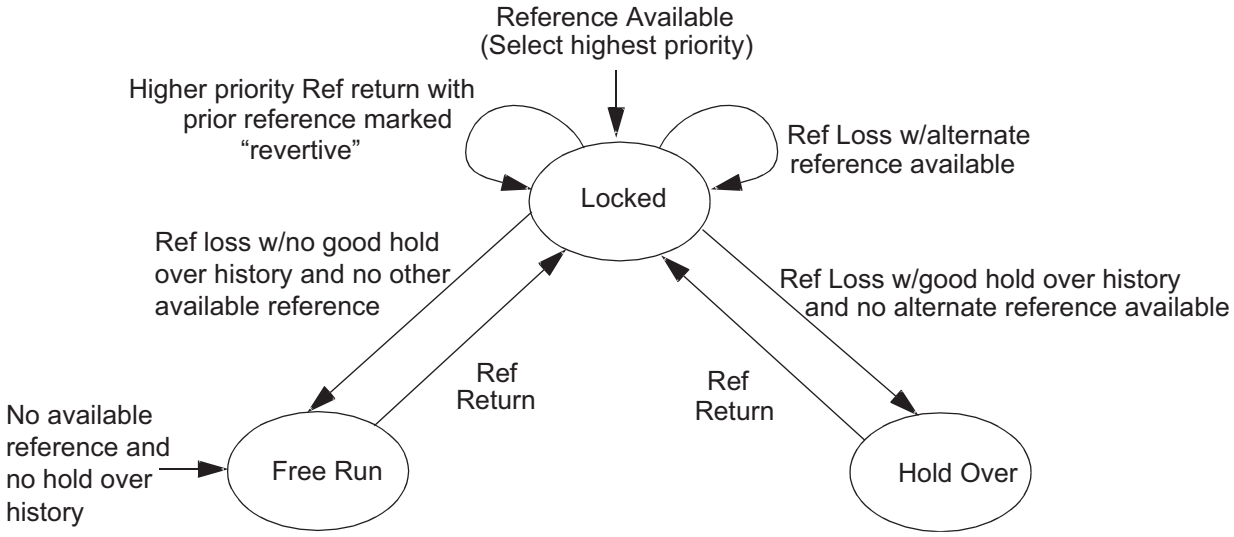


The operational mode is according to the following state diagram:

No available reference and no Hold Over history
Ref loss w/no good Hold Over history and no other available reference

Automatic Operational Mode Selection

Figure 7



Output Signals and Frequency

Output 1 is the primary chip output, and in locked mode is synchronized to the selected reference. **Output 1** may be any of the following frequencies: 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz or 77.76 MHz.

M/S_Out is an 8 kHz output available as a frame reference or synchronization signal for cross-coupled pairs of SM3-8RG5 devices operated in master/slave mode. In master mode, M/S_Out is synchronized to the selected reference. In slave mode, M/S_Out is in phase with the **M/S REF** offset by the value written to the **Phase_offset** register (+31.75 to -32nS, with .25nS resolution). M/S_Out may be a 50% duty cycle signal, or variable high-going pulse width, as determined by the **Ctl_Mode** and **Fr_Pulse_Width** registers. In variable pulse width mode, the width may be from 1 to 15 multiples of the **Output 1** cycle time. See Register Descriptions and Operation section.

BITS_Clk is the BITS clock output at either 1.544 MHz or 2.048 MHz. It is selected by the T1/E1 input and its state may be read in bit 3 of the Ctl_Mode register. When T1/E1 = 1, the BITS frequency is 1.544 MHz, and when T1/E1 = 0, the BITS frequency is 2.048 MHz.

Interrupts

The SM3-8RG5 module supports eight different interrupts and appears in **INTR_EVENT (0x12)** register. Each interrupt can be individually enabled or disabled via the **INTR_ENABLE (0x13**) register. Each bit enables or disables the corresponding interrupt from asserting the **SPI_INT** pin. Interrupt events still appear in the **INTR_EVENT (0x12)** register independent of their enable state. All interrupts are cleared once **INTR_EVENT (0x12)** register is read. The interrupts are:

- Any reference changing from available to not available
- Any reference changing from not available to available
- **M/S REF** changing from activity to no activity
- **M/S REF** changing from no activity to activity
- DPLL Mode status change
- Reference switch in automatic reference selection mode
- Loss of Signal
- Loss of Lock

Interrupts and Reference Change in Autonomous Mode

Interrupts can be used to determine the cause of a reference change in autonomous mode. Let us assume that the module is currently locked to **REF1**. The module switches to **REF2** and ~~**SPI_**~~**INT** pin is asserted. The user reads the **INTR_EVENT (0x12)** register.

If the module is operating in autonomous non-revertive mode, the cause can be determined from bits 4, 5, 6 and 7. Bit 5 is set to indicate Active reference change. If Bit 6 is set then the cause of the reference change is Loss of Active Reference. If Bit 7 is set then the cause of the reference change is a Loss of Lock alarm on the active reference.

If the module is operating in autonomous revertive mode, the cause can be determined from bits 1, 4,5, 6 and 7. Bit 5 is set to indicate Active reference change. If Bit 6 is set then the cause of the reference change is Loss of Active Reference. If Bit 7 is set then the cause of the reference change is a Loss of Lock alarm on the active reference. If Bit 1 is set then the cause of the reference change is the availability of a higher priority reference.

Note: The DPLL Mode Status Change bit (Bit 4) is also set to indicate a change in **DPLL_STATUS (0x11)** register, during an interrupt caused by a reference change. The data in **DPLL_STATUS (0x11)** register however is not useful in determining the cause of a reference change. This is because bits 0-2 of this register always reflects the status of the current active reference and hence cannot be used to determine the status of the last active reference.

Interrupts in Manual Mode

In manual operating mode, when the active reference fails due to a Loss of Signal or Loss of Lock alarm, an interrupt is generated. For example, in case of a Loss of Signal, bits4 and 6 of **INTR_EVENT (0x12)** register would be set to indicate Loss of Signal and DPLL Mode Status Change. The user may choose to read the **DPLL_STATUS (0x11)** register, though in manual mode bit6 of **INTR_EVENT (0x12)** register is a mirror of bit0 of **DPLL_STATUS (0x11)** register. This holds true for a Loss of Lock alarm, where bit7 of **INTR_EVENT (0x12)** register is a mirror of bit1 of **DPLL_STATUS (0x11)** register.

Internal Clock Calibration

The internal clock may be calibrated by writing a frequency offset v.s. nominal frequency into the Calibration register. This calibration is used by the synchronization software to create a frequency corrected from the actual internal clock output by the value written to the Calibration register. See register descriptions.

Register Descriptions and Operation

Chip_ID_low, 0x00 (R)

Bit 7 ~ Bit 0
Low byte of chip ID: 0x11

Chip_ID_High, 0x01 (R)

Bit 7 ~ Bit 0
High byte of chip ID: 0x30

Chip_Revision, 0x02 (R)

Bit 7 ~ Bit 0
Chip revision number: 0x06

Bandwidth_PBO, 0x03 (R/W)

Bit 7 ~ Bit 5	Bit 4	Bit 3 ~ Bit 0
Reserved	Reserved 0: Default	Bandwidth Selection in Hz: 0000: 0.025 0001: 0.025 0010: 0.025 0011: 0.025 0100: 0.025 0101: 0.025 0110: 0.049 0111: 0.098 (Reset Default) 1000: 0.20 1001: 0.39 1010: 0.78 1011 - 1111: 1.6

BITS 3 - 0 select the phase lock loop bandwidth in Hertz.

Ctl_Mode, 0x04 (R/W)

Bit 7 ~ Bit	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Default: 0	M/S Output Pulse width control: 0: 50% 1: Controlled by FR_Pulse_Width register Default: 0	BITS Clock Output Frequency: 1: 1.544 MHz 0: 2.048 MHz (read only)	HM Ref: 0: Register control of op mode/ref (Will always be 0)	Active Reference Selection: 1: Manual 0: Automatic Default: 1	Reserved

When bit 1 is reset (automatic reference and mode selection), Bits 3 - 0 of the Op_Mode register become read-only. The power-up default for Bit 1 = 1 for manual reference selection and default for Bit 4 = 0 for 50% duty cycle on M/S Output.

When the device is in slave mode, it will lock to the M/S REF, independent of the values written to BITS 3 - 0 of the Op_mode register. The operational mode and reference selection written to Bits 3 - 0 while in slave mode will, however, take effect when the device is made the master.

When bit 1 of the Ctl_Mode register is reset (automatic reference and mode selection) and the device is in master mode, BITS 3 - 0 of the Op_Mode register become read-only.

Op_Mode, 0x05 (R/W)

Bit 7 ~ Bit 5	Bit 4	Bit 3 ~ Bit 0
Reserved	Master or Slave Mode 1: Master 0: Slave (Read Only)	Free Run, Locked, or Hold Over: 0000: Free Run mode 0001: Locked on Ref1 0010: Locked on Ref2 0011: Locked on Ref3 0100: Locked on Ref4 0101: Locked on Ref5 0110: Locked on Ref6 0111: Locked on Ref7 1000: Locked on Ref8 1001 - 1111: Hold Over

Max_Pullin_Range, 0x06 (R/W)

Bit 7 ~ Bit 0
Maximum pull-in range in 0.1 ppm unit

This register should be set according to the values specified by the standards (GR-1244) appropriate for the particular stratum of operation. The power-up default value is 10 ppm. (= 4.6ppm aging + 4.6 ppm pullin + margin).

M/S REF_Activity, 0x07 (R)

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Cross reference activity 0000: No signal 0001: 8kHz 0100: 12.96MHz 0101: 19.44MHz 0110: 25.92MHz 0111: 38.88MHz 1000: 51.84MHz 1001: 77.76MHz 1010-1111: Reserved

Indicates signal presence and auto-detected frequency for the M/S REF input.

Ref_Activity, 0x08 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 activity 1: on 0: off	ref7 activity 1: on 0: off	ref6 activity 1: on 0: off	ref5 activity 1: on 0: off	ref4 activity 1: on 0: off	ref3 activity 1: on 0: off	ref2 activity 1: on 0: off	ref1 activity 1: on 0: off

Each bit indicates the presence of a signal for that reference.

Ref_Pullin_Sts, 0x09 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 sts 1: in range 0: out range	ref7 sts 1: in range 0: out range	ref6 sts 1: in range 0: out range	ref5 sts 1: in range 0: out range	ref4 sts 1: in range 0: out range	ref3 sts 1: in range 0: out range	ref2 sts 1: in range 0: out range	ref1 sts 1: in range 0: out range

Each bit indicates if the reference is within the frequency range specified by the value in the Max_Pullin register.

Ref_Qualified, 0x0a (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 qual: 1: avail. 0: not avail.	ref7 qual: 1: avail. 0: not avail.	ref6 qual: 1: avail. 0: not avail.	ref5 qual: 1: avail. 0: not avail.	ref4 qual: 1: avail. 0: not avail.	ref3 qual: 1: avail. 0: not avail.	ref2 qual: 1: avail. 0: not avail.	ref1 qual: 1: avail. 0: not avail.

This register contains the “anded” condition of the Ref_Activity and Ref_Pullin_Sts registers for each of the Ref1-8 inputs, qualified for 10 seconds. When a reference signal has been present for > 10 seconds and is within the pull-in range, its bit is set.

Ref_Mask, 0x0b (R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 mask: 1: avail. 0: not avail. Default: 0	ref7 mask: 1: avail. 0: not avail. Default: 0	ref6 mask: 1: avail. 0: not avail. Default: 0	ref5 mask: 1: avail. 0: not avail. Default: 0	ref4 mask: 1: avail. 0: not avail. Default: 0	ref3 mask: 1: avail. 0: not avail. Default: 0	ref2 mask: 1: avail. 0: not avail. Default: 0	ref1 mask: 1: avail. 0: not avail. Default: 0

Individual references may be marked as “available” or “not available” for selection in the automatic reference selection mode
(bit 1 = 0 in the Ctl_Mode register). The reset default value is 0, “not available”. In manual reference selection, either hardware or register controlled, the reference masks have no effect, but do remain valid and are applied upon a transition to automatic mode.

Ref_Available, 0x0c (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ref8 avail: 1: avail. 0: not avail.	ref7 avail: 1: avail. 0: not avail.	ref6 avail: 1: avail. 0: not avail.	ref5 avail: 1: avail. 0: not avail.	ref4 avail: 1: avail. 0: not avail.	ref3 avail: 1: avail. 0: not avail.	ref2 avail: 1: avail. 0: not avail.	ref1 avail: 1: avail. 0: not

This register contains the “anded” condition of the Ref_Qualified and Ref_Mask registers.

Ref_Rev_Delay, 0x0d (R/W)

Bit 7 ~ Bit 0
Reference reversion delay time, 0 - 255 minutes. default = 0000 0101, 5 minutes

In automatic reference selection mode, when a reference fails and later returns, it must be available for the time specified in the Ref_Rev_Delay register before it can be switched back to as the active reference (if the new reference was marked as “revertive”).

Phase_Offset, 0x0e (R/W)

Bit 7 ~ Bit 0
The 2's complement value of phase offset between Master Output module and Slave Output module, ranges from -32 nS to +31.75 nS Positive Value: Master Output rising edge leads Slave Output Negative Value: Master Output rising edge lags Slave Output

In slave mode, the slave's outputs may be phase shifted -32nS to +31.75nS in .25nS increments, relative to M/S according to the contents of the Phase_Offset register, to compensate for the path length of the M/S to M/S connection.

If a phase offset is used, then the two SM3-8RG5 devices would typically be written to the appropriate phase offset values for the respective path lengths of each Master to Slave connection, to ensure that the same relative output signal phases will persist through master/slave switches.

Calibration, 0x0f (R/W)

Bit 7 ~ Bit 0
2's complement value of local oscillator digital calibration in 0.05 ppm resolution

To digitally calibrate the free running clock synthesized from the internal clock, this register is written with a value corresponding to the known frequency offset of the oscillator from the nominal center frequency.

Fr_Pulse_Width, 0x10 (R/W)

Bit 7 ~ Bit4	Bit 3 ~ Bit 0
Reserved	Pulse width for M/S clock output, 1-15 multiples of the Sync_Clk clock period.

BITS 4 and 5 of the Ctl_Mode register determine if the M/S 8 kHz output is 50% duty cycle or pulsed (high going) outputs. When they are pulsed, the Fr_Pulse_Width register determines the width. Width is the register value multiple of the Sync_Clk clock period. Valid values are 1 - 15.

Reset default is 0001. Writing to 0000 maps to 0001.

DPLL_Status, 0x11 (R)

Bit 7 ~Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Hold Over Build Complete 1: Complete 0: Incomplete	Hold Over Available 1: Avail. 0: Not avail.	Locked 1: Locked 0: Not locked	Loss of Lock 1: Loss of Lock 0: No loss of lock	Loss of Signal 1: No activity on active reference 0: Active reference signal present

Bit 0 indicates the presence of a signal on the selected reference.

Bit 1 indicates a loss of lock (LOL). Loss of lock will be asserted if lock is not achieved within the specified time for the stratum level of operation, or lock is lost after being established previously. LOL will not be asserted for automatic reference switches.

Bit 2 indicates successful phase lock. It will typically be set in <700 seconds for Stratum 3 with a good reference. It will indicate "not locked" if lock is lost.

Bit 3 indicates if a Hold Over history is available.

Bit 4 indicates when a new Hold Over history has been sucessfully built and transferred to the active Hold Over history. See Detailed Description section under Interrupts and Reference Change in Autonomous Mode and Interrupts in Manual Mode

Intr_Event, 0x12 (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Loss of Lock	Loss of Signal	Active reference change	DPLL Mode status change	M/S Ref Change from no activity to activity	M/S Ref Change from activity to no activity	Any reference change from not available to available	Any reference change from available able to not available

Interrupt state = 1. When an enabled interrupt occurs, the SPI_INT pin is asserted, active low. All interrupts are cleared and the SPI_INT pin pulled high when the register is read. Reset default is 0. See Detailed Description section under Interrupts and Reference Change in Autonomous Mode and Interrupts in Manual Mode

Intr_Enable, 0x13 (R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable Interrupt event 7: 1: Enable 0: Disable Default: 0	Enable Interrupt event 6: 1: Enable 0: Disable Default: 0	Enable Interrupt event 5: 1: Enable 0: Disable Default: 0	Enable Interrupt event 4: 1: Enable 0: Disable Default: 0	Enable Interrupt event 3: 1: Enable 0: Disable Default: 0	Enable Interrupt event 2: 1: Enable 0: Disable Default: 0	Enable Interrupt event 1: 1: Enable 0: Disable Default: 0	Enable Interrupt event 0: 1: Enable 0: Disable Default: 0

Enables or disables the corresponding interrupts from asserting the SPI_INT pin. Interrupt events still appear in the Intr_Event register independent of their “enable” state. Reset default is interrupts disabled.

Ref(1-8)_Frq_Offset, 0x14 ~ 0x1b (R)

Bit 7 ~ Bit 0
2’s complement value of frequency offset between reference and calibrated local oscillator, 0.2ppm resolution

These registers indicate the frequency offset, in 0.2ppm resolution, between each reference and the local calibrated oscillator.

0x14 - 0x1b correspond to Ref1 - Ref8.

Ref(1-8)_Frq_Priority, 0x1c ~ 0x23 (R/W)

Bit 7 ~ Bit 4	Bit 3	Bit 2 ~ Bit 0
Frequency 0000: None 0001: 8 kHz 0010: 1.544 MHz 0011: 2.048 MHz 0100: 12.96 MHz 0101: 19.44 MHz 0110: 25.92 MHz 0111: 38.88 MHz 1000: 51.84 MHz 1001: 77.76 MHz 1010-1111: Reserved	Revertivity 1: revertive 0: non-revertive Default: 0, non revertive	Priority 000: Highest 111: Lowest Default: 0

BITS 2 - 0 indicate the priority of each reference for use in automatic reference selection mode (bit 1 of the Ctl_Mode register =0). In manual reference selection mode (bit 1 of the Ctl_Mode register = 1), these BITS are read-only and will contain either the reset default or values written when last in automatic reference selection mode. For equal priority values, lower reference numbers have higher priority.

Bit 3 specifies if the reference is revertive or non-revertive in automatic reference selection mode. When a reference fails, the next highest priority “available” (signal present, non-masked, and acceptable frequency offset) reference will be selected. When a reference returns, it will be switched to only if it is of higher priority and the current active reference is marked “Revertive”.

BITS 7 - 4 indicate the auto-detected frequency for each reference. Invalid frequencies may result in erroneous device operation. If there is no activity on a reference, bits 7-4will be = 0000. Bits 7-4 are read only. 0x1c - 0x23 correspond to Ref1 - Ref8.

FreeRun_Priority, 0x24 (R/W)

Bit 7 - Bit 5	Bit 4	Bit 3	Bit 2 - Bit 0
Reserved	Enable/ Disable 1: Enable 0: Disable Default: 0	Revertivity 1: Enable 0: Disable Default: 0 non-revertive	Priority 000: Highest 111: Lowest Default: 0

Free Run may be treated like a reference. When it is enabled, Free Run will be entered when all references of higher priority are lost or masked. If or when a higher priority reference returns, it is switched to if Free Run is set as "revertive". When disabled, Free Run will be entered only if manually selected or all references fail without an available Hold Over history. For equal priority value, Free Run will be treated as lower priority.

History_Policy, 0x25 (R/W)

Bit 7 - Bit 1	Bit 0
Reserved	Reference Switch Hold Over Hisory Policy 0: Rebuild 1: Continue

Bit 0 determines if Hold Over is retained or rebuilt when a reference switch occurs. See Application Notes, Holdover History Accumulation and Management section.

History_Cmd, 0x26 (R/W)

Bit 7 - Bit 2	Bit 1-0
Reserved	Hold Over Histroy Commands 01: Save active history to backup history 10: Restore active history from backup 11: Flush the active history and accumulation register 00: No command - use to write Bit4 to change policy

Bits 0-1 are written to save a holdover history to the backup history, restore the active holdover history from the backup, or flush the active history. The default value of the register is 00. The last command is latched and may be read by the application. A flush does not affect the backup history. See Application Notes, Holdover History Accumulation and Management section.

HoldOver_Time, 0x27 (R)

Bit 7 - Bit 0
Indicates the time since entering the Hold Over state. from 0-255, one bit per hour. Zero in non-Hold Over state and stops at 255.

Cfgdata, 0x30 (R/W)

Bit 7 - Bit 0
Configuration data write register.

Configuration data is written to this register. Internal use only.

Cfgctr_Lo, 0x31 (R)

Bit 7 - Bit 0
Configuration data write counter low byte.

Low order byte of configuration data write counter. Internal use only.

Cfgctr_Hi, 0x32 (R)

Bit 7 - Bit 0
Configuration data write counter high byte.

High order byte of configuration data write counter. Internal use only.

Chksum, 0x33 (R/W)

Bit 7 - Bit 1	Bit 0
Reserved	Configuration Data Checksum pass/fail indicator 0: Fail 1: Pass

Checksum verification register for configuration data. Internal use only.

EE_Mode, 0x36 (R/W)

Bit 7 - Bit 1	Bit 0
Reserved	EEPROM Write Enable 0: Disable 1: Enable

EEPROM write enable register.

EE_Cmd, 0x37 (R/W)

Bit 7	Bit 6 - Bit 2	Bit 1 - Bit 0
EEPROM read/write ready bit: 0 = Not Ready 1 = Ready	Reserved	EEPROM read/write command bits: 00 = Reset FIFO 01 = Write Command 10 = Read Command

EEPROM read/write command register.

EE_Page_Num, 0x38 (R/W)

Bit 7 - Bit 0
EEPROM read/write page number, 0x00 to 0x9f (0 - 159)

EEPROM read/write page number register. EEPROM consist of 160 pages.

EE_FIFO_Port, 0x39 (R/W)

Bit 7 - Bit 0
EEPROM read/write FIFO data.

EEPROM read/write FIFO port register. EEPROM data is written to/read from this location.

Performance Specifications

Performance Definitions

Jitter and Wander – Jitter and wander are defined respectively as "the short-term and long-term variations of the significant instants of a digital signal from their ideal positions in time". They are therefore the phase or position in time modulations of a digital signal relative to their ideal positions. These phase modulations can in turn be characterized in terms of their amplitude and frequency. Jitter is defined as those phase variations at rates above 10Hz, and wander as those variations at rates below 10Hz.

Fractional frequency offset and drift – The fractional frequency offset of a clock is the ratio of the frequency error (from the nominal or desired frequency) to the desired frequency. It is typically expressed as (n parts in 10^X), or (n x 10^{-X}). Drift is the measure of a clock's frequency offset over time. It is expressed the same way as offset.

Time Interval Error (TIE) – TIE is a measure of wander and is defined as the variation in the time delay of a given signal relative to an ideal signal over a particular time period. It is typically measured in ns. TIE is set to zero at the start of a measurement, and thus represents the phase change since the beginning of the measurement.

Maximum Time Interval Error (MTIE) – MTIE is a measurement of wander that finds the peak-to-peak variations in the time delay of a signal for a given window of time, called the observation interval (*t*). Therefore it is the largest peak-to-peak TIE in any observation interval of length *t* within the entire measurement window of TIE data. MTIE is therefore a useful measure of phase transients, maximum wander and frequency offsets. MTIE increases monotonically with increasing observation interval.

Time Deviation (TDEV) – TDEV is a measurement of wander that characterizes the spectral content of phase noise. TDEV(*t* is the RMS of filtered TIE, where the bandpass filter is centered on a frequency of 0.42/*t*.

SM3-8RG5 Performance

Input Jitter Tolerance – Input jitter tolerance is the amount of jitter at its input a clock can tolerate before generating an indication of improper operation. GR-1244 and ITU-813 requirements specify jitter amplitude v.s. jitter frequency for jitter tolerance. The SM3-8RG5 device provides jitter tolerance that meets the specified requirements.

Input Wander Tolerance – Input wander tolerance is the amount of wander at its input a clock can tolerate before generating an indication of improper operation. GR-1244 and ITU-813 requirements specify input wander TDEV v.s. integration time as shown below.

Integration Time, (seconds)	TDEV (ns)
$0.05 \leq \tau < 10$	100
$10 < \tau < 1000$	$31.6 \times \tau^{0.5}$
$1000 \leq \tau$	N/A

The SM3-8RG5 device provides wander tolerance that meets these requirements.

Phase Transient Tolerance – GR-1244 specifies maximum reference input phase transients that a clock system must tolerate without generating an indication of improper operation. The phase transient tolerance is specified in MTIE(nS) v.s. observation time from .001 to 100 seconds, as shown below.

Observation time S (Seconds)	MTIE (ns)
$0.001326 \leq S < 0.0164$	61,000 x S
$0.0164 < S < 1.97$	925 + 4600 x S
$1.97 \leq S$	10,000

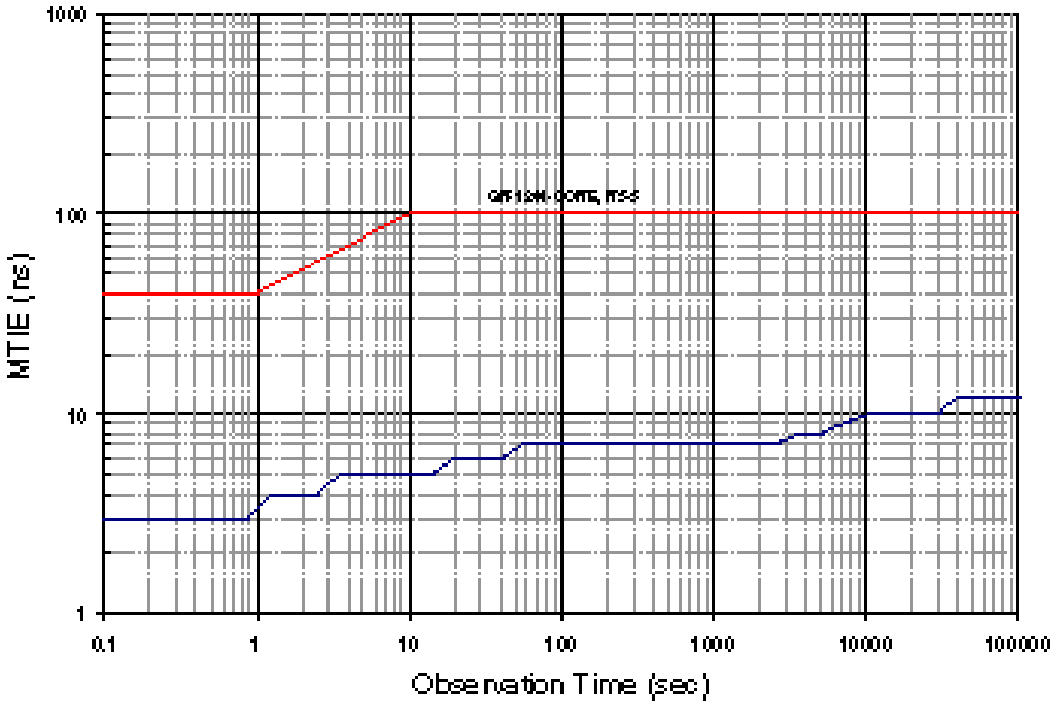
The SM3-8RG5 will tolerate all reference input transients within the GR-1244 specification.

Free-run Frequency Accuracy – The ability of a clock to produce a frequency as close as possible to the nominal frequency in the absence of a reference.

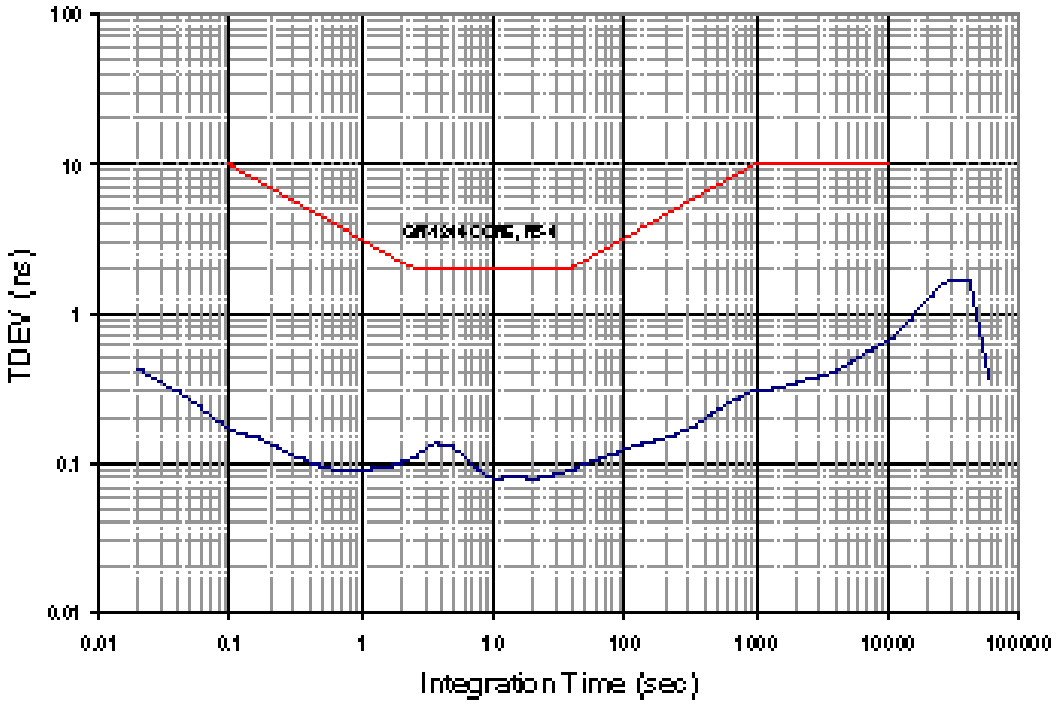
Hold Over Frequency Stability – A measure of a clock's performance while in Hold Over mode over 24 hours, subjected to the specified temperature variations.

Wander Generation – Wander generation is the process whereby wander appears at the output of a clock in the absence of input wander. The SM3-8RG5 wander generation characteristics, MTIE and TDEV, are shown below, along with the requirements masks (bandwidth = 0.098 Hz):

Wander Generation Characteristics – MTIE



Wander Generation Characteristics – TDEV



Wander Transfer – Wander transfer is the degree to which input wander is attenuated (or amplified) from input to output of a clock. The GR-1244 requirements for wander transfer limits are shown below.

Integration time, τ (seconds)	Stratum 3 TDEV (nanoseconds)
$\tau < 0.05$	N/A
$0.05 \leq \tau < 0.1$	$1020 \times \tau$
$0.1 \leq \tau < 1.44$	102
$1.44 \leq \tau < 10$	102
$10 \leq \tau < 300$	$32.2 \times \tau^{0.5}$
$300 \leq \tau \leq 1000$	$32.2 \times \tau^{0.5}$
$1000 < \tau$	N/A

The SM3-8RG5, when configured for the appropriate Stratum 3 bandwidth frequency, meets the Stratum 3 requirements,

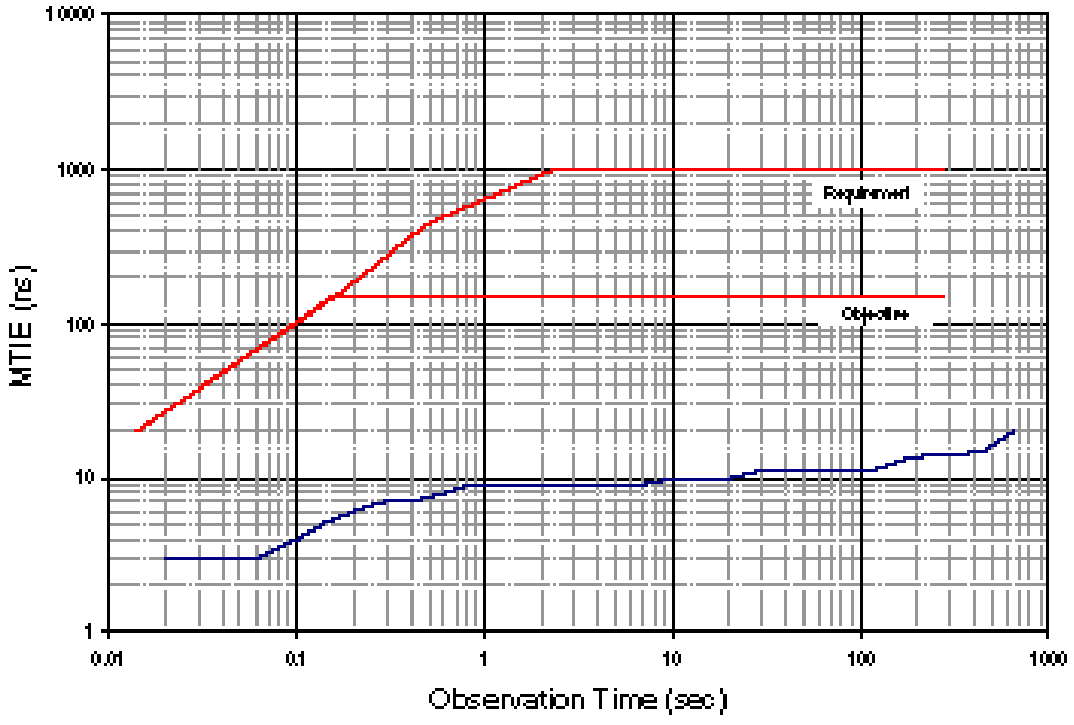
Jitter Generation – Jitter generation is the process whereby jitter appears at the output of a clock in the absence of input jitter. The device jitter generation performance is as shown below:

Jitter	19.44 MHz	77.76 MHz
Broadband (10 Hz - 2 MHz)	8 ps Typical	8 ps Typical
SONET Band	(12 kHz -2MHz) 1 ps Typical	(12 kHz -20MHz) <1 ps Typical

Jitter Transfer – Jitter transfer is the degree to which input jitter is attenuated (or amplified) from input to output of a clock. It is a function of the selected bandwidth. The SM3-8RG5 jitter transfer characteristics are shown below:

Phase Transients – A phase transient is an unusual step or change in the phase-time of a signal over a relatively short time period. This may be due to switching between equipment, reference switching, diagnostics, entry or exit to/from Hold Over, or input reference transients. The SM3-8RG5 performance for reference switches is shown below:

Phase Transients – MITE



Capture range and Lock range – Capture range and lock range are the maximum frequency errors on the reference input within which the phase locked loop is able to achieve lock and hold lock, respectively. The SM3-8RG5 Stratum 3 performance is shown below:

Characteristic	SM3-8RG5	Requirement
Capture range	± 25.5 ppm maximum	GR-1244-CORE, Sec 3.4
Hold range	± 25.5 ppm maximum	GR-1244-CORE, Sec 3.4

This is the minimum capability, and guarantees the ability to capture and lock with a reference that is offset the maximum allowed in one direction in the presence of a clock that is offset the maximum in the opposite direction (4.6 ppm + 4.6 ppm = 9.2 ppm).

Master/Slave Skew and Reference switch settling time– Master/Slave Skew and Reference switch settling time performance are shown below:

Characteristic	SM3-8RG5	Requirement
Master/Slave phase skew	< 2 nS	N/A
Reference switch settling time	Stratum 3: < 100 sec. up to 20 ppm frequency offset	Stratum 3: < 100 sec. up to +/- 4.6 ppm frequency offset

SM3-8RG5 Initialization:

Power-up:

1. If possible, always start up in master mode. After the module is powered up, hold the reset pin low for 10ms. Wait 1200ms and read the contents of register 0x33. If it reads1 then the module came up properly. If it reads 0 then reset the module and re-read register 0x33 after 1200ms. The contents of 0x33 must read 1 before continuing.

2. Remain in the default free-run mode for 10 seconds then read the value of bit 1 of register 0x11 or pin 2, the LOL alarm output. If the LOL alarm is set, the reset pin must be pulled low as in 1 above. In the free-run mode the LOL alarm should never be set. This indicates the module is in an invalid state. If there is no LOL alarm in free-run the module is ready.

Operation:

On power up or after a reset all the registers are loaded with their default values. The default values of some important registers are given below assuming the module operates as a Master

Address(Hex)	Register Name	Value(Binary MSB first)	Notes
0x03	Bandwidth_PBO	00000111	Bandwidth = 0.098Hz
0x04	Ctl_Mode	0000r010	r - Read Only
0x05	Op_Mode	00010000	Indicates Free Run mode
0x06	Max_Pullin_Range	01100100	
0x0b	Ref_Mask	00000000	
0x0d	Ref_Rev_Delay	00000101	
0x0e	Phase_Offset	00000000	
0x0f	Calibration	00000000	
0x11	DPLL_Status	00000000	Indicates No Active Reference
0x13	Intr_Enable	00000000	Indicates Interrupts are disabled
0x1c-0x23	Ref(1-8)_Frq_Priority	xxxx0000	Frequencies are auto detected
0x33	Chksum	xxxxxxx1	Bit0 should be high to indicate that data has been loaded correctly from the EEPROM.

SM3G Initialization continued

I. The unit starts up in Free Run and operates in Manual mode. Here are the steps that need to be taken to lock the unit to a reference in Manual mode.

1. Apply signal to the reference inputs.
2. Set the appropriate pull in range by writing to address 0x06.
3. A value of 0001xxxx, depending on which (Ref 1-8) reference to lock to, should be written to address 0x05.
4. Enable Reference mask for appropriate references by writing a 1 to the reference bit in address 0x0b.
5. Enable all Interrupts by writing 11111111 to address 0x13.

II. To lock the unit to a reference in autonomous (automatic) mode after power up or reset, the following steps should be taken. You can also switch from Manual to Autonomous mode directly. When doing so, please ensure that the appropriate references are available by checking REF_AVAILABLE register (address: 0x0c).

1. Clear bit1 of CTL_MODE register (address: 0x04). This puts the module in autonomous mode.
2. Apply signal to the reference inputs
3. Set the appropriate pull in range by writing to address 0x06
4. Enable Reference mask for appropriate references by writing a 1 to the reference bit in address 0x0b.
5. Set priority and revertivity for the input references by writing to the appropriate Ref_Frq_Priority registers (bits 3-0).
6. Enable all Interrupts by writing 11111111 to address 0x13.
7. Set the unit to operate in autonomous mode by clearing bit1 of address 0x04

III. Slave Mode Operation:

1. As a Slave, the module operates in Autonomous mode.
2. The Bandwidth is set, by default, to 1.6Hz (Bandwidth_PBO register (Address 0x03): 00001011).
3. Note that Bit 4 of the OP_MODE register (Address 0x05) is cleared.
4. The values in Bits 3-0 of this register have no effect on the operation of the Slave module.
5. For the Slave module to track the Master accurately, an appropriate Phase Offset value should be written to PHASE_OFFSET register (Address 0x0e) is used to compensate for the path delay.
6. The module will lock to the Cross Reference Input (XREF) from the master.

IV RESET Parameters:

1. The reset pin should be held low for a minimum of 10 milliseconds to ensure a complete reset occurs.
2. The SPI interface should not be accessed for a minimum of 1200ms after the reset pin is de-asserted.

Switching Master/Slave designations:

The following steps need to be taken before making Master module a Slave and vice versa.

1. Copy the value in the PHASE_OFFSET register (Address 0x0e) of the Slave to the Master module's PHASE_OFFSET regsiter (Address 0x0e).
2. Read the contents of Bits 3-0 of the Master's OP_MODE register (Address 0x05) and copy it into Bits 3-0 of the Slave's OP_MODE register (Address 0x05).
3. It is recommended that the contents of REF(1-8)_FRQ_PRIORITY registers (Address 0x1c-0x23) and REF_MASK register (Address 0x0b) from Master be copied to Slave to ensure seamless Master/Slave switches. Master/Slave switches should be performed with minimal delay between switching the states of each of the two devices.

Acceptable output frequencies are: 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz or 77.76MHz. The device will autodetect the output frequency.

Reference Inputs – The application may supply up to 8 reference inputs, applied at input pins **Ref1 - 8**. They may each be 8 kHz, 1.544 MHz, 2.048 MHz, 12.96 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz or 77.76 MHz. The device auto-detects the reference frequencies, and they may be read from the Ref(1-8)_Frq_Priority registers in register control mode, as described in the control mode sections that follow.

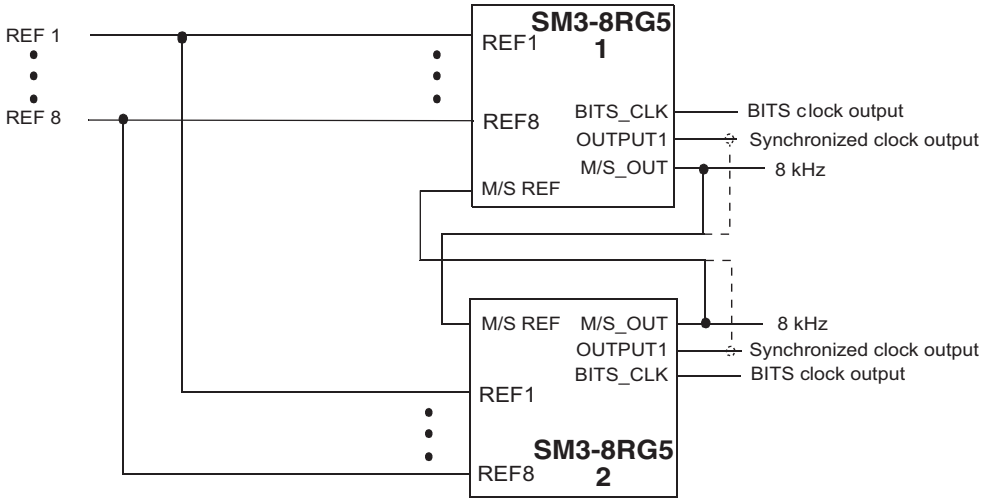
Reference switches are performed in a hitless manner. However, if the application externally changes the frequency of a particular reference, the device requires 20ms to auto-detect the new frequency. Manual switches to a frequency changed reference should not be made during this interval. Automatic reference selection mode accounts for the auto-detection in the reference qualification.

References would typically (but need not be) connected in decreasing order of usage priority. For example if redundant BITS clocks are available, they would typically be assigned to **Ref1** and **Ref2**, with other transmission derived signals following thereafter.

Master/Slave operation – For some applications, reliability requirements may demand that the clock system be duplicated. The SM3-8RG5 device will support the master/slave duplicated configuration for such applications. To facilitate it's use, the device includes the necessary signal cross coupling and control functions. Redundancy for reliability implies two major considerations: 1) Maintaining separate failure groups such that a failure in one group does not affect it's mate, and 2) Physical and logical partitioning for repair, such that a failed component can be replaced while the mate remains in service, if so desired. System design needs to account to meet system level goals.

Master / Slave Configuration

Figure 8



Master/Slave Configuration – A pair of devices are interconnected by cross-coupling their respective **M/S Outputs** or **Output1** to the other device's **M/S REF** input (See Figure 8). Additionally, the reference inputs for each device would typically be correspondingly the same, so that when a Master/Slave switch occurs, synchronization would continue with the same reference. The references may be driven by the same signal directly or via separate drivers, as the redundancy of that part of the system requires. Distribution path lengths are not critical here, as a phase build-out will occur when a device switches from slave to master.

The path lengths of the two M/S Output to **M/S REF** signals is of interest, however. They need not be the same. However, to accommodate path length delays, the SM3-8RG5 provides a programmable phase skew feature, which allows the application to offset the output clock from the cross-reference signal by -32ns to +31.75ns. This offset may therefore be programmed to exactly compensate for the actual path length delay associated with the particular application's cross-reference traces. The offset may be further adjusted to accommodate any output clock distribution path delay differences. Phase offset is programmed by writing to the Phase_Offset register, and is typically a one-time device initialization function. (See register description and Register Access Control sections). Thus, master/slave switches with the SM3-8RG5 devices may be accomplished with near-zero phase hits.

For applications that use Hardware Control only (i.e. phase offset programming is not available), it is desirable to keep the cross couple path lengths at a minimum and relatively equal in length, as the path length will appear as a phase hit in the slave clock output when a master/slave switch occurs in a Hardware Control configuration.

Master/Slave Operation and Control – The Master/Slave state is always manually controlled by the application. Master or slave state of a device is determined by the **MASTER SELECT** pin. Choosing the master/slave states is a function of the application, based on the configuration of the rest of the system and potential detected fault conditions.

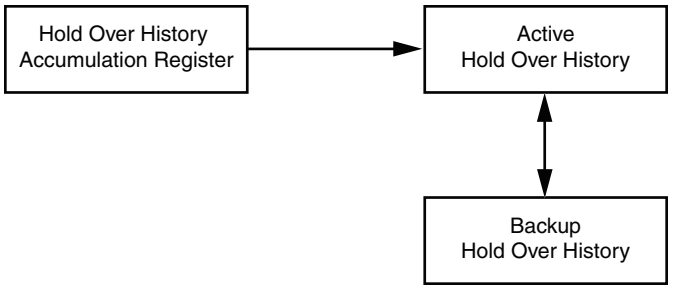
When operating in Hardware Control or Register Access Manual Control mode, it is important to set the slave reference selection the same as the master to ensure use of the same reference when/if the slave becomes master. In Register Access Manual Control mode, the **Ref_Mask** register should also be written to the same value for both devices.

Master/slave switches should be performed with minimal delay between switching the states of each of the two devices. This can be easily accomplished, for example, by controlling the master/slave state with a single signal, coupled to one of the devices through an inverter.

In the case of Register Access Automatic Control mode, where reference selection is automatic, it is necessary to read the operational mode BITS 3-0) from the master's **Op_Mode** register and write it to the slave's **Op_Mode** register. The master's reference selection will then be used by the slave when it becomes master. In addition to having the references populated the same, and in the same order for both devices, it is desireable to write the reference frequency and priority registers **Ref(1-8)_Frq_Priority** and the **Ref_Mask** registers to the same values for both devices to ensure seamless master/slave switches.

Reset – Device reset is an initialization time function, which resets internal logic and register values. A reset is performed automatically when the device is powered up. Registers return to their default values, as noted in the register descriptions. Device mode and functionality following a reset are determined by the state of the various hardware control pins.

Holdover History Accumulation and Maintenance -- Holdover history accumulation and maintenance may be controlled in greater detail if register bus access to the device is provided. Holdover history accumulation and control encompasses three device internal registers, three bus access registers for control and access, and two status bits in the DPLL_Status register.



Once lock has been achieved, holdover history is compiled in the accumulation register. It is transferred to the Active holdover history when it is ready (typically in about 15 minutes). The "Holdover Available" bit and output pin are set to "1". From then on, the Active holdover history is continually updated and kept in sync with the holdover history accumulation register. (See Figure 11).

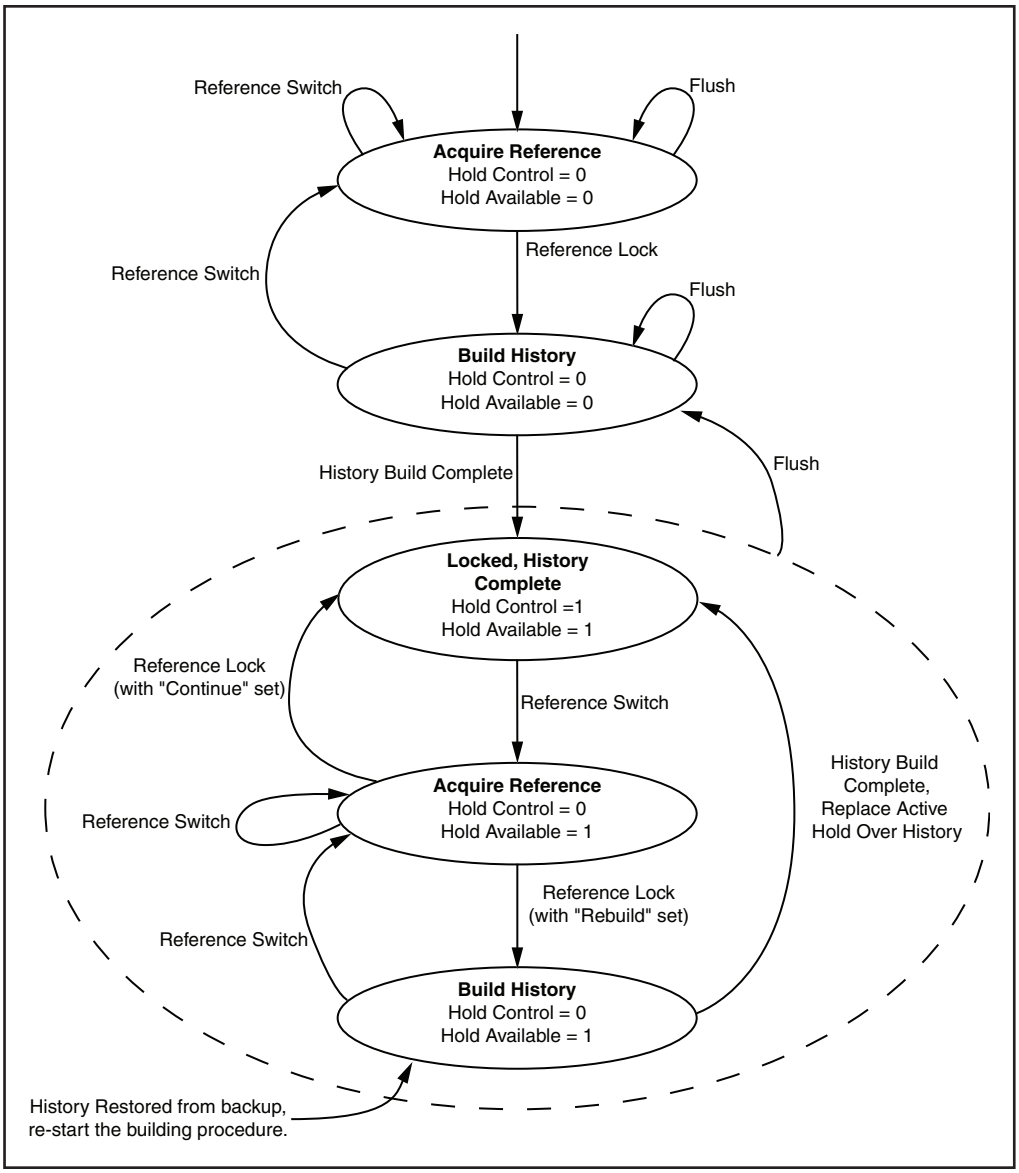
Hold Over History access and Control Registers

Table 5

Register	Register Name	Description
0x25	History_Policy	Sets policy for Hold Over history accumulation: “Rebuild” or “Continue”
0x26	History_Cmd	Save, restore, and flush commands for Hold Over history
0x27	Holdover_Time	Indicates the time since entering the Hold Over state
0x11	DPLL_Status	Bits 3 and 4: Hold Over Available” and “Hold Over Build Complete”

Hold Over History and Status States

Figure 9



Holdover History Accumulation and Maintenance continued – Whenever holdover is entered, it is the Active Holdover History that is used to determine the holdover frequency. The History_Cmd register allows the application to issue three holdover history control commands:

1) Save the Active Holdover History to the Backup History.
2) Restore a Backup History to the Active.
3) Flush the active History as well as the accumulation register. The Backup history remains intact.

Both the Active and the Backup holdover histories are loaded with the calibrated freerun synthesizer control data on reset/power-up.

The application might use the "save to backup" in a situation where, for example, the primary reference is known to be of higher quality than any secondary references, in which case it may be desirable to save and then restore the holdover history accumulated on the primary reference if the primary reference is lost and holdover is entered upon loss of a secondary reference. Users can restore the history from backup any time, even while operating in Holdover mode. The frequency transient will be smooth and continuous.

It is the responsibility of application software to keep track of the age and viability of the holdover backup history. Given time and temperature effects on oscillator aging, the application may wish to periodically perform a "Save" of the Active history to keep the backup current.

When switching to a new reference, the active holdover history will remain intact and marked as "Holdover Available" (if it was available before the reference switch) until a new history is accumulated on the new reference (Typically 15 minutes after lock has been achieved). During the new history accumulation, the "Holdover Build Complete" bit is reset. Once the new history accumulation is complete, it is transferred to the Active History and the "Holdover Build Complete" bit is set. The active history will then continue to be updated to track the reference.

The History_Policy register allows the application to control how a new history is built. When set to "Rebuild":

1) History accumulation begins when lock is achieved on the new reference.
2) The holdover history is rebuilt (taking about 15 minutes). The Active History remains untouched until it is replaced when the build is complete.

When the policy is set to "Continue":

1) If there is no "Available" Active History, a new build occurs, as under the "Rebuild" policy.
2) If there is an "Available" Active History, it will continue, the accumulation register will be loaded from the Active History, and the "Build" process is essentially completed immediately following lock on the new reference.

The "Continue" policy may be used by the application if, for example, it is known that the reference switched to may be traced to the same source and therefore likely has no frequency offset from the prior reference. In that case, the "Continue" policy avoids the delay of rebuilding the holdover history. If the switch is likely to be between references with known or unknown frequency offset, then it is preferable to use the "Rebuild" policy.

The time since the holdover state was entered may be read from the Holdover_Time register. Values are from 0 to 255 hours, limited at 255, and reset to 0 when not in the holdover state.

Boundary Scan IEEE1149.1-2001 (Limited Testability Support) - This module exposes a boundary scan chain which contains one or more boundary scan testable IEEE1149.1-2001 complaint devices. The exposed boundary scan chain is IEEE1149.1-2001 compliant, and supports all documented testing modes of devices contained within chain. Integration of this module into an existing boundary scan chain will require the following.

- Substitution of modules footprint with provided testability model schematic.
- Modified net list will need to be loaded into boundary scan test vector generation software.

Testability Model Schematic and BSDL file(s) can be obtained directly from factory.

Control Modes

The device can in turn be operated in a manual control mode, or automatic control and reference selection mode.

Reset may be pulled low for a minimum of 100nS during chip start-up (or any other desired time) to initialize the full device state. However, power-up will also perform a reset, so in a minimal configuration, **Reset** may be tied input high.

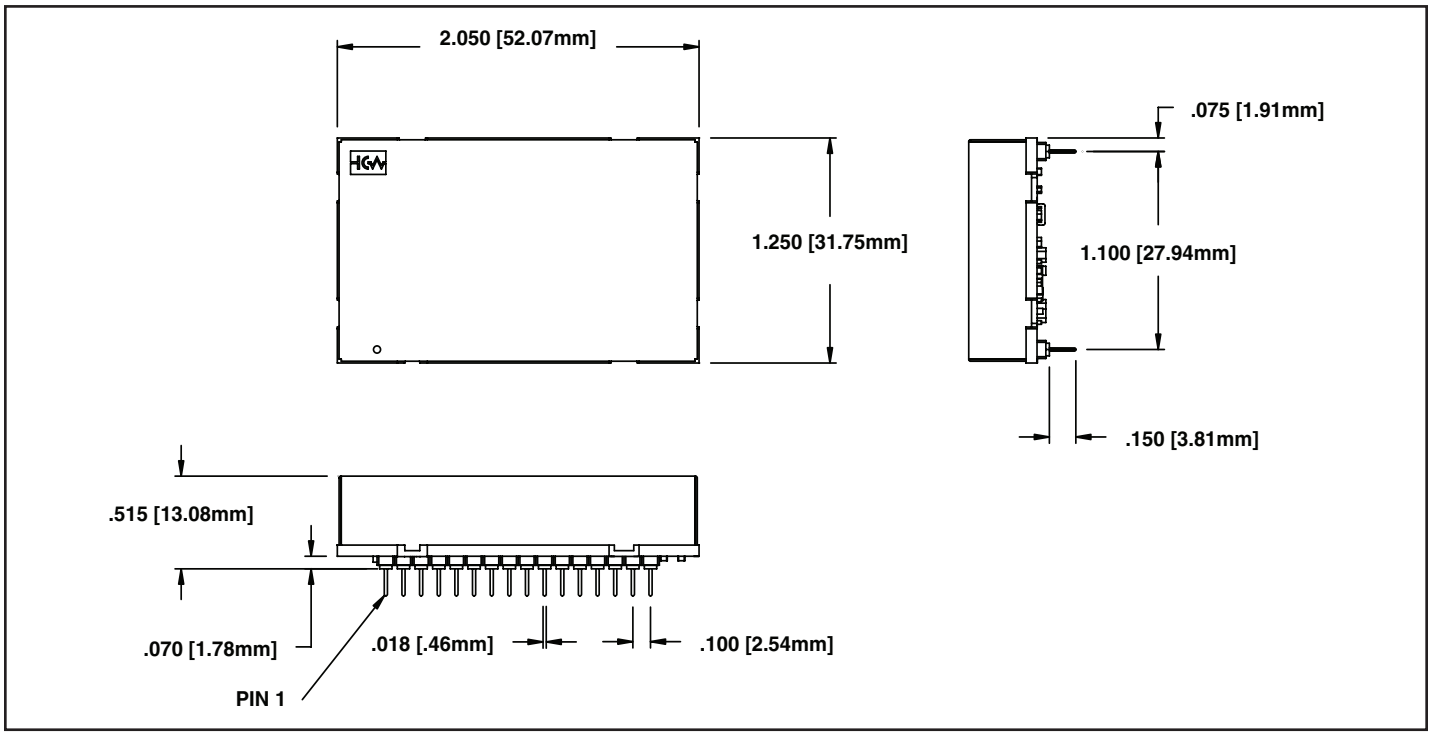
The BITS clock output frequency is selected by the **T1/E1** pin. When **T1/E1** = 1, the BITS frequency is 1.544 MHz, and when **T1/E1** = 0, the BITS frequency is 2.048 MHz.

MASTER SELECT- Determines the master or slave mode. Set to "1" for a master, and "0" for a slave. Master/slave switches should be performed with minimal delay between switching the states of each of the two devices. This can be easily accomplished, for example, by controlling the master/slave state with a single signal, coupled to one of the devices through an inverter.

For simplex operation, the device should be in Master mode - set **MASTER SELECT** to "1".

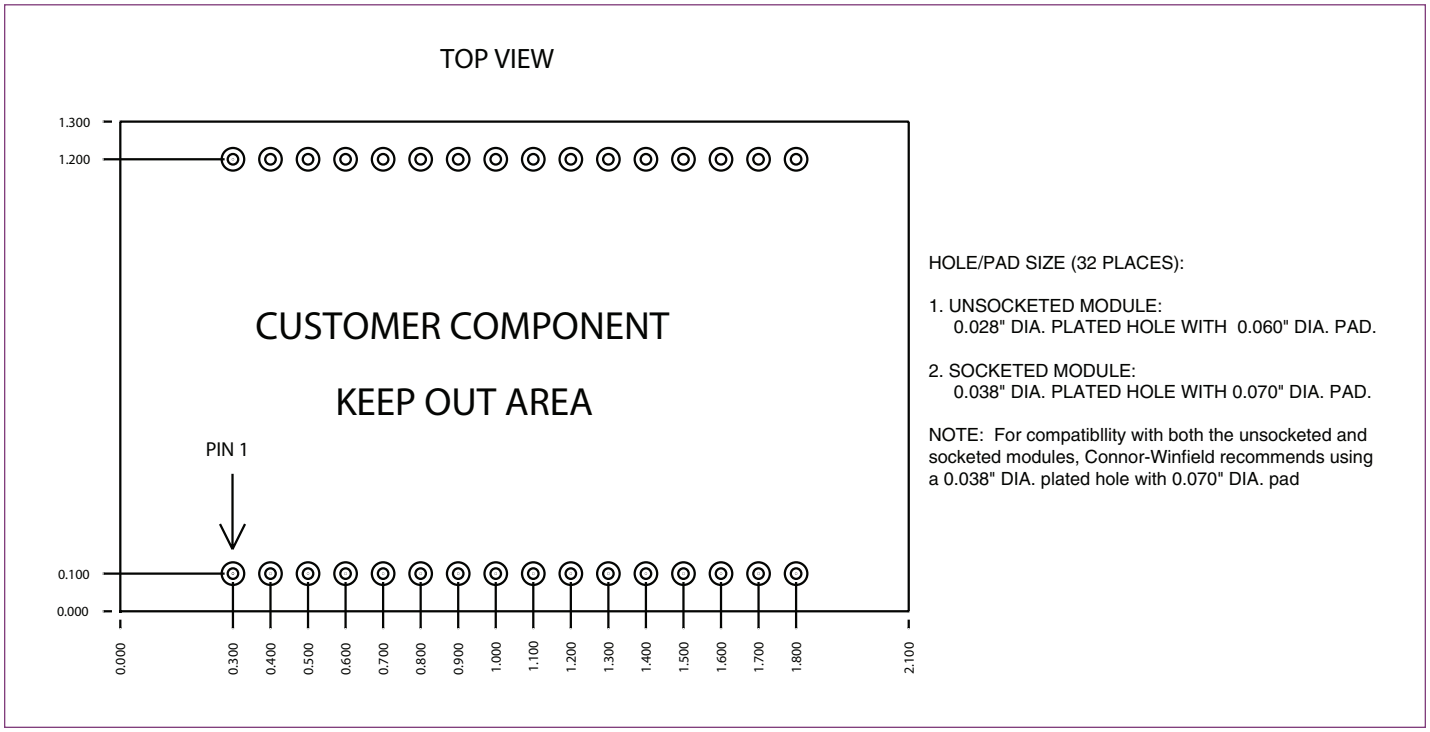
Mechanical Dimensions

Figure 10



Footprint Dimensions

Figure 11



Required External Components

1. Place series resistors (33 ohms) on all reference inputs (Pins 4 - 7 & 15-18).
2. Place series resistors (33 ohms) on SPI_IN and SPI_CLK inputs (Pins 25, 26).
3. Place one .01uF and one 47-100uF capacitor at the input power pin (Pin 27).
4. One 4.7uF (25V) capacitor is required at the VPP pin (Pin 14).
5. One 4.7uF (25V) capacitor is required at the VPN pin (Pin 19).

PCB Layout Recommendations

1. Orient module so airflow is parallel along the header strips (pins).
2. Place de-coupling and/or filter components as close to module pins as possible.
3. Do not place any components directly beneath the module on the topside of the host PCB.
4. Ensure that only clean and well-regulated power is supplied to the module.
5. Isolate power and ground inputs to the module from noisy sources.
6. Provide power and ground connections through a 0.050" wide trace (minimum) using 1-oz. Cu or equivalent copper feature (i.e. internal plane, copper area fill, etc.).
7. Keep module signals away from sensitive or noisy analog and digital circuitry.
8. Avoid split ground planes as high-frequency return currents may be affected.
9. Allow extra spacing between traces of high-frequency inputs and outputs.
10. Keep all traces as short as possible - avoid meandering trace paths.
11. Avoid routing signals directly beneath the module on the topside of the host PCB.
12. If possible, provide a copper area directly beneath the module on the topside of the host PCB. Connect this copper area to ground.
13. It is recommended that the connections of the JTAG, VPP and VPN pins be routed to pads, preferably in a SIL pattern as shown in Figure 13 below. It is recommended to use 0.1" center to center spacing.

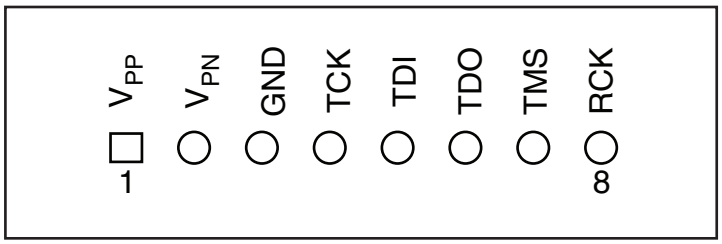


Figure 13

Optional Socket Mounting Recommendations

Mating sockets may be used if permanent installation of the SM3 module is not desired. Two possible sources for these sockets include:

1. Samtec, "Low Profile Socket Strips", SL Series, PN SL-116-G-19. (http://www.samtec.com/)
2. Mill-Max, "Single-In-Line Sockets", 315 Series, PN 315-xx-114-41-001. (http://www.mill-max.com/)

The SM3-8RG5 requires two 16-pin sockets. The optional dual footprint configuration shown in Figure 14 requires one 14-pin and two 16-pin sockets.

Optional SM3/SM3-8RG5 Dual Footprint

A dual footprint configuration may be used when designing a host circuit board containing the Connor Winfield SM3 or SM3-8RG5 modules. The smaller SM3 contains a subset of the signal pins found on the larger SM3-8RG5 in locations which allow for a simple dual footprint arrangement like the one shown in Figure 14.

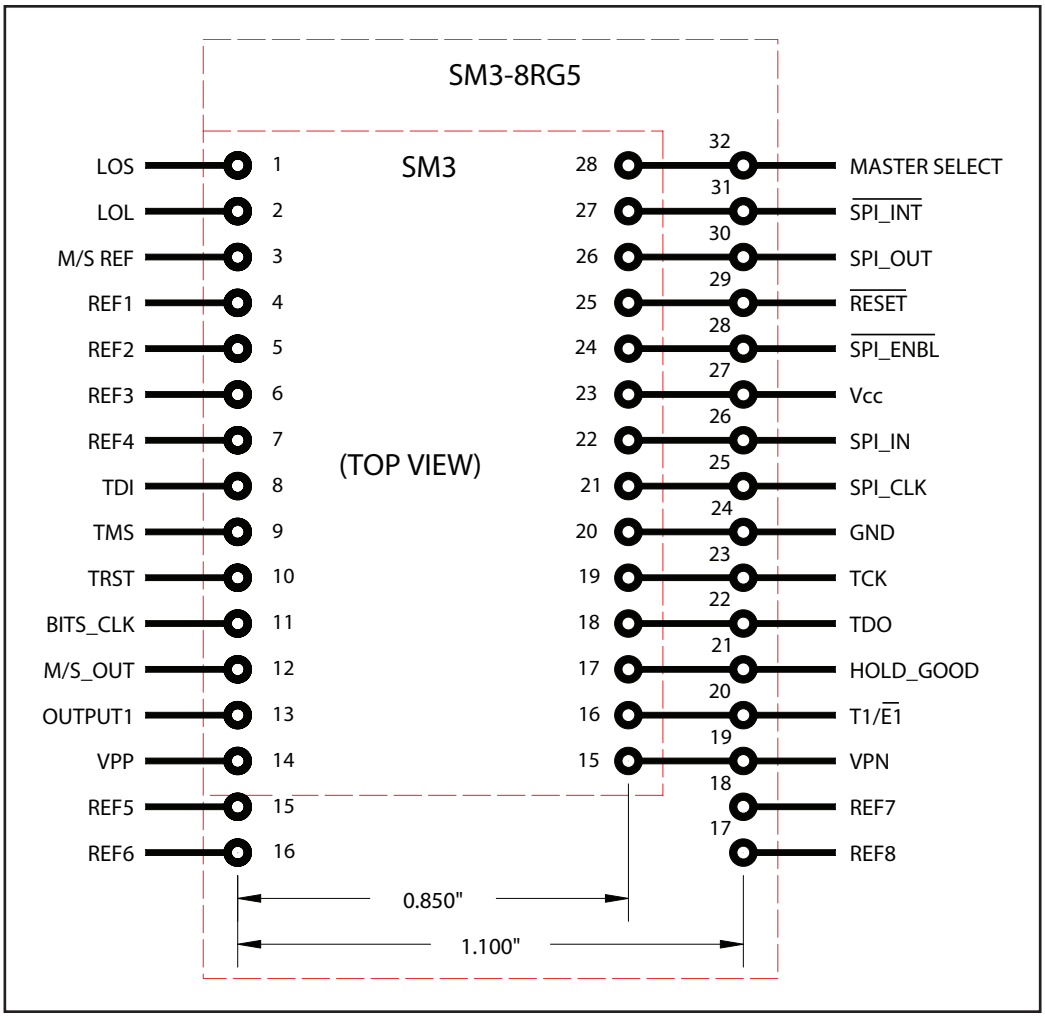


Figure 14

The modules shown in Figure 1 are arranged in a left-justified fashion. Notice that right justified or center justified (with an additional column of SM3 pins) arrangements are also possible, depending on the designer's preference.

Placement of external components

1. Place series resistors (33 ohms) on all reference input (SM3 Pins 4 - 7, SM3-8RG5 Pins 4-7 & 15-18).
2. Place series resistors (33 ohms) on SPI_IN and SPI_CLK inputs (SM3 Pins 21,22, SM3-8RG5 Pins 25 & 26).
3. Place one .01uF and one 47-100uF capacitor at the input power pin (SM3 Pin 23, SM3-8RG5 Pin 27).
4. One 4.7uF (25V) capacitor is required at the VPP pin (SM3 & SM3-8RG5 Pin 14).
5. One 4.7uF (25V) capacitor is required at the VPN pin (SM3 Pin 15, SM3-8RG5 Pin 19).

Be sure to consult Connor Winfield's respective datasheets for additional mechanical, electrical, footprint and keep-out information.

Ordering Information

SM3-8RG5-XXX.XXM
Replace XXX.XX with one of the following available frequencies,
012.96MHz, 019.44MHz, 025.92MHz, 038.88MHz, 051.84MHz or 077.76MHz.

Please contact Connor-Winfield for other frequencies that may be available.

Similar Products from Connor-Winfield

SM3G5-XXX.XXM - Stratum 3 module with 4 input references.
SM3G5-IT-XXX.XXM - Industrial temperature rated Stratum 3 module with 4 input references.
SM3EG5-XXX.XXM - Stratum 3E module with 8 input references.

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Revision	Revision Date	Note
00	10/18/06	Final Release Data Sheet
01	6/14/07	Pg.27, Clarified Boundary Scan
02	10/15/07	Add Initialization info, Pg. 22-23
03	11/06/08	Added Input Pulse Width Spec to Table 1
04	02/11/10	Registration Description Update
05	07/12/10	Pin Description Updates
06	01/26/11	Serial Timing Bus updates to graphics
07	09/06/11	Chip Revision Register updated