Si48xx ATDD Programming Guide

1. Introduction

1.1. Scope

This document provides an overview of the programming requirements for the Si4822/26/27/40/44 analog tune digital display (ATDD) AM/FM/SW receiver. The hardware control interface and software commands are detailed along with several examples of the required steps to configure the device for various modes of operation.

2. Overview

The Si4822/26/27/40/44 family of products is programmed using commands and responses. To perform an action, the system controller writes a command byte and associated arguments, causing the device to execute the given command. The device will, in turn, provide a response depending on the type of command that was sent. Section “6. Commands and Responses” and Section “7. Commands and Properties” describe the procedures for using commands and responses and provide complete lists of commands, properties, and responses.

The device has a slave control interface that allows the system controller to send commands to and receive responses from the device using 2-wire mode (I^2C and SMBUS compatible) serial protocol (or bus modes).

The following sections provide guidelines for programming the ATDD device:

- Section "4. ATDD Device Overview" on page 4 gives an overview of the ATDD device.
- Section "5. ATDD Device Power On/Off and Band Switch Overview" on page 7 gives an overview of the Power on / off and the band switching sequencing for the ATDD device.
- Section "8. Control Interface" on page 55 describes the control interface in details.
- Section "9. Powerup" on page 58 describes the options for the sequencing of VDD and VIO power supplies, provision of the reference clock, RCLK, and sending of the ATDD_POWER_UP command.
- Section "10. Powerdown" on page 59 describes sending of the POWER_DOWN command and removing VDD and VIO power supplies as necessary.
- Section "11. Programming Example" on page 60 provides the flowcharts and step-by-step procedures for programming the device.

Note: The ATDD family has its own power up and getting status commands which are different from previous Si47xx DTDD family. To differentiate, we use “ATDD_POWER_UP” and ATDD_GET_STATUS to denote the ATDD specific commands instead of the general Si47xx “POWER_UP” and “STATUS” commands.

Table 1. Product Family Function

Part Number	General Description	FM Receiver	AM Receiver	SW Receiver	Stereo FM	Wide FM Bands	Wide SW Bands	China TV Channel Audio	EN55020 Compliance	Package Size
Si4822	AM/FM Receiver	✓	✓							SSOP-24
Si4826	AM/SW/FM Receiver	✓	✓	✓						SSOP-24
Si4827	AM/SW/FM Receiver	✓	✓	✓		✓	✓	✓		SOIC-16
Si4840	AM/FM Receiver	✓	✓		✓				✓	SSOP-24
Si4844A*	AM/SW/FM Receiver	✓	✓	✓	✓				✓	SSOP-24
Si4844B*	AM/SW/FM Receiver	✓	✓	✓	✓	✓	✓	✓	✓	SSOP-24
***Note:** New features have been added to Si4844-B20 that are not available in the older Si4844-A10 part.										

3. Terminology

- DTDD— Digital Tune Digital Display
- ATDD— Analog Tune Digital Display
- ATAD— Analog Tune Analog Display
- SDIO— 2-wire bus mode Serial data in/data out pin (Compatible to I^2C SDA pin)
- SCLK— 2-wire bus mode Serial clock pin (Compatible I^2C SCL pin)
- $\overline{RST}$ or RSTb—Reset pin, active low
- IRQ— Interrupt request pin, active high
- RCLK—External reference clock
- CTS—Clear to send
- NVM—Non-volatile internal device memory
- Device—Refers to the AM/FM/SW Receiver
- System Controller—Refers to the system microcontroller
- CMD—Command byte
- COMMANDn—Command register (16-bit) in 3-Wire mode (n = 1 to 4)
- ARGn—Argument byte (n = 1 to 7)
- STATUS—Status byte
- RESPn—Response byte (n = 1 to 15)
- RESPONSEn—Response register (16-bit) in 3-Wire mode (n = 1 to 8)

4. ATDD Device Overview

The Si4822/26/27/40/44 devices are the tuner ICs for the analog tune digital display (ATDD) market. The Si4822/26/27 are the consumer grade FM mono parts and are not EN55020 compliance.

In general, any commands and properties associated with setting FM stereo/mono modes and FM blending sent to the ATDD mono parts will simply be ignored and will not have effects. Also, the commands for getting the FM stereo status of a tuned channel is always "mono" for these parts. This effect will not be specified again in the rest of the document.

The ATDD device has two operating modes of band detection configuration options: either the ATDD device detects the band or the system controller detects and controls the band by its own mechanism. The diagrams below illustrate how the ATDD device works in each mode.

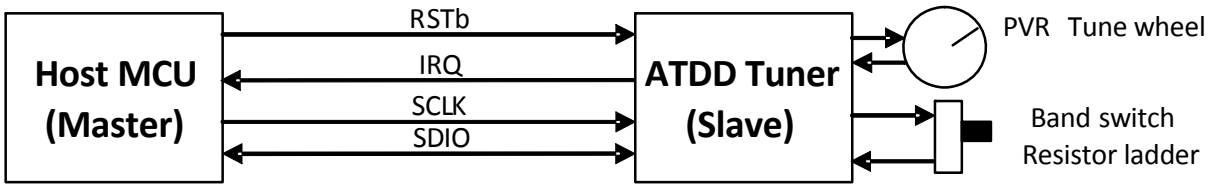


Figure 1. ATDD Device is Responsible for Band Detection

Figure 2. System Controller is Responsible for Band Detection

Each of these two operating modes requires different hardware configuration. For the ATDD device, the BAND pin of the device must be connected to the band switch resistor or to the power supply pin instead, i.e. VDD1 for Si4822/26/40/44 and VDD for Si4827. At power up, the system controller is required to read the band configuration state bits from the ATDD device and determine which configuration option is responsible for the band detection.

The ATDD device is a slave device which requires a host system controller to control it, similar to the Si47xx DTDD family. The communication between the host and the salve devices is via the 2-wire bus mode. Unlike the Si47xx DTDD devices, the ATDD device has its own PVR based tune wheel and resistor ladder based band switch. The ATDD device reads the band switch resistor ladder to determine the frequency band and then reads the PVR tune wheel position for channel tuning. When the ATDD device senses a change in either the PVR tune wheel position or the band switch position, it will send out an interrupt request to the host system controller. The system controller then issues a get status command to read the updated tuned frequency and band status for display on its LCD or LED.

The communication interface between the system controller and the ATDD device is the 2-wire bus mode interface. The hardware interface pins of the ATDD device are described in Table 2:

Table 2. ATDD Device Hardware Interface

Pin Name	Function
RSTb	Device reset input (active low)
IRQ	Host interrupt request output (active high)
SDIO	2-wire bus mode serial data input/output
SCLK	2-wire bus mode serial clock input (Note: ATDD device is slave)

The ATDD device is a slave device and its seven-bit device address is (0010001b). To achieve acceptable or higher tune frequency update performance, the system controller 2-wire bus mode clock speed of 10 kHz* or higher is recommended. The ATDD device requires a 32.768 kHz clock supply of 100 ppm for proper radio operation. The system controller can configure the ATDD device by applying an external reference clock to the device (various frequencies can be selected) or by using a 32.768 kHz crystal instead.

The ATDD device has flexibility in selecting bands and configuring band properties, such as band top, band bottom, and channel spacing. In addition, the Si4822/26/40/44 SSOP24 packaged parts have a pull up resistor option (at pin 1 LNA_EN) to force the ATDD device to use its default band properties rather than the values programmed by the system controller. For example, when the ATDD device pin 1 is pulled up, it will ignore the band properties programmed by the system controller programmed (band top, band bottom, channel space, FM de-emphasis, and FM blend RSSI mono/stereo thresholds). The system controller is able to read this information from the band configuration state bits from the ATDD device. The Si4827 SOIC16 package ATDD part doesn't have the pin pull-up option. However, the host controller can send an extra argument byte in the ATDD_POWER_UP command to specify this band properties priority.

***Note:** The ATDD device requires a slower I^2C clock for proper powerup immediately after a hardware reset; i.e., no higher than 10 kHz is recommended. After the powerup command sequence is succeeded, the host controller can switch to a higher speed.

To power up the ATDD device for higher I2C clock speed, the host controller needs to obey more strict timing requirements as below:

1. After reset, the host controller needs to wait till the first IRQ pulse is finished before sending a command; i.e. send a command after the IRQ falling edge or wait 2.5 ms after the IRQ rising edge.
2. The pulse width of the I^2C clock signal (i.e., high to low level ratio) must be equal or greater than 50%.
3. After sending either the ATDD_GET_STATUS command 0xE0 or the ATDD_POWER_UP command 0xE1, the host controller needs to wait for 2 ms before polling response byte CTS bit or reading the response directly.

Following the above timing requirements, the ATDD device is tested by powering up successfully for I^2C clock speed up to 50 kHz. Clock speed higher than 50 kHz is possible but is not guaranteed. After reset and the first successful powerup, the host controller is free to switch to a higher I^2C speed and shorter CTS polling interval (down to 50 µs is recommended).

Customers using 10 kHz I^2C clock speed or below for powerup are not required to change their existing host controller firmware with respect to the new timing requirements.

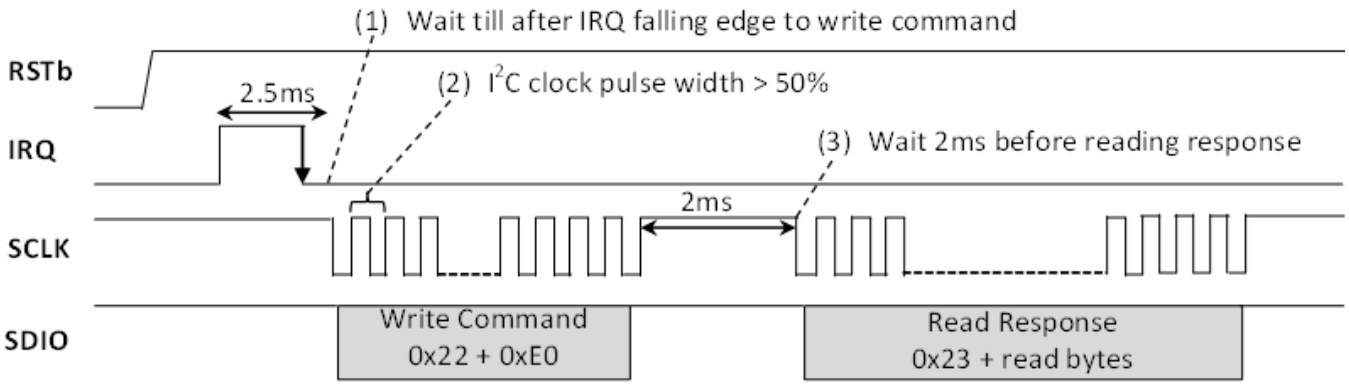


Figure 3. System Controller Powerup Timings for I²C speed > 10 kHz

5. ATDD Device Power On/Off and Band Switch Overview

The power on and band switching sequences of the ATDD device vary based on which band detection configuration is selected.

5.1. Band Detection by ATDD Device

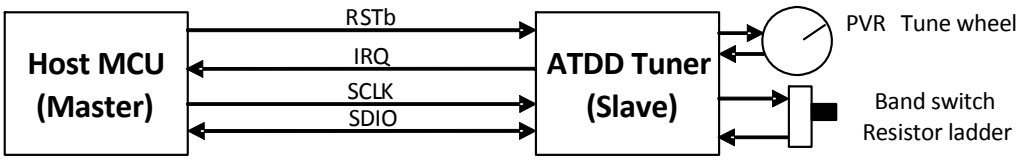


Figure 4. Band Detection by ATDD Device

The ATDD device is responsible for detecting the band via its internal ADC, which is connected to the external resistor ladder band switch. When the device detects the band switch position is changed, it will interrupt the host system controller via the IRQ pin. The system controller issues a get status command to obtain the updated status, which includes the new band position and the required action. The required action depends on whether the band is switched within the same band mode (e.g., FM1→FM5) or switched across different band modes (e.g., FM5→AM1).

For situations when the band is switched within the same band mode, the system controller is requested to re-issue the power up command with the new band number, optionally with band properties other than the predefined ones. For situations when the band is switched across different band modes, the system controller is requested to reset the ATDD device and wait until the device is ready again, then issue the same power up command with the new band number and optional band properties.

5.1.1. Power On Sequence

1. System controller resets the ATDD device and releases the RSTb pin.
2. System controller waits till first IRQ is received (indicates that the ATDD device is ready to receive commands).
3. System controller issues ATDD_GET_STATUS command to obtain the ATDD device status. The system controller is required to check in the reply from the BCFG0 bit to determine if the ATDD device or the system controller is responsible for band detection and selection. In this case, the BCFG0 bit should be 0 (i.e., the ATDD device detects band). Note that the HOSTPWRUP bit is always set, which prompts the system controller to issue the ATDD_POWER_UP command. Band and tune information are not ready in this power up stage.
4. System controller issues ATDD_POWER_UP command with the bulleted arguments below to power up the device:
   - For first power up, set ARG1 bit[5:0] BANDIDX = 0 as host doesn't know the actual band number.
   - Set ARG1 bit[7] XOSEN bit = 1 if a 32.768 kHz crystal is in use. Set ARG1 bit[6] XOWAIT bit =0 if typical 600 ms crystallization time is enough or set the XOWAIT bit = 1 for a longer time of 900 ms.
   - Optionally include ARG2 ARG3* if new band bottom frequency is different from default.
   - Optionally include ARG4 ARG5* if new band top frequency is different from default.
   - Optionally include ARG6* if new band channel space is different from default (AM only).
   - Optionally include ARG7 for new features of Si4827 and Si4844B devices.
5. System controller waits till IRQ is received again when the valid band is detected.
6. System controller issues ATDD_GET_STATUS command to obtain the latest status:
   - If REPLY0 bit[4] INFORDY bit = 1, i.e. band info ready, the host is required to save the band index in REPLY1bit[5:0] BANDIDX for later use.
   - Host checks REPLY0 bit[7] HOSTRST bit and bit[6] HOSTPOWERUP bit for any host required actions and handles it accordingly.
   - If HOSTPOWERUP bit = 1, i.e., band switching is within same band mode, the host is required to issue the

ATDD_POWER_UP command again with the known band index to switch to the correct band.
- If HOSTRST bit = 1, i.e., band switching is across different band modes, the host is required to reset the ATDD device and wait for IRQ received, and then issue the ATDD_POWER_UP command again with the known band index.

7. System controller waits till further IRQ is received for the tune wheel frequency ready.
8. System controller issues ATDD_GET_STATUS command to obtain the latest status for display:
   - If REPLY0 bit[4] INFORDY, bit = 1, i.e., info ready, the host can read and display the status, i.e., the band mode, the station and stereo states.
   - The tune frequency is ready when combined frequency of REPLY2, REPLY3 is a non-zero (4-digit BCD number).
   - Host should always save the REPLY1 bit[5:0] BANDIDX band index byte for later use.
9. Optionally system controller can issue the ATDD_AUDIO_MODE command to specify number of audio options (FM example):
   - AUDIO_MODE bits selects one of the audio output modes: (0) digital volume mode, (1) bass/treble mode, (2) bass/treble with volume control mix mode 1, (3) bass/treble with volume control mix mode 2
   - ADJPT_ATTN bit specifies if the 100 kHz adjacent points have audio output attenuated by 2 dB or not.
   - ADJPT_STEO bit specifies if the 100 kHz adjacent points have stereo indicator and stereo separation.
   - FM_MONO bit specifies if FM audio output is forced mono or stereo.
10. Optionally, the system controller can issue the SET_PROPERTY command to change the receive volume, bass/treble level, FM de-emphasis, soft-mute, and banding properties to override the default settings.

***Note:** If pin 1 of Si4822/26/40/44 SSOP24 packaged ATDD devices has been pulled up by the resistor, it is forced to use the default band properties. The band properties specified by the system controller, such as band top, band bottom, channel space, FM de-emphasis, and FM blend RSSI mono thresholds, will be ignored and have no effects.

5.1.2. Band Switch Sequence

1. The ATDD device detects band is changed and then interrupts the system controller when band is switched by user.
2. System controller waits for any IRQ is received:
3. System controller issues ATDD_GET_STATUS command to obtain the latest status:
   - If REPLY0 bit[4] INFORDY bit = 1, i.e. band info ready, the host is required to save the band index in REPLY1 bit[5:0] BANDIDX for later use.
   - Host checks REPLY0 bit[7] HOSTRST bit and bit[6] HOSTPOWERUP bit for any host required actions and handles it accordingly.
   - If HOSTPOWERUP bit = 1, i.e.,band switching is within same band mode, the host is required to issue the ATDD_POWER_UP command again with the known band index to switch to the correct band.
   - If HOSTRST bit = 1, i.e., band switching is across different band modes, the host is required to reset the ATDD device and wait for IRQ received, and then issue the ATDD_POWER_UP command again with the known band index.
4. System controller waits till further IRQ is received for the tune wheel frequency ready.
5. System controller issues ATDD_GET_STATUS command to obtain the latest status for display:
   - If REPLY0 bit[4] INFORDY bit = 1, i.e. info ready, the host can read and display the status, i.e. the band mode, the station, and stereo states.
   - The tune frequency is ready when combined frequency of REPLY2, REPLY3 is non-zero (4-digit BCD number).
   - Host should always save theREPLY1 bit[5:0] BANDIDX band index byte for later use.
6. Optionally, the system controller can issue the ATDD_AUDIO_MODE command to select one of the audio output modes: (0) digital volume mode, (1) bass/treble mode, (2) bass/treble with volume control mix mode 1, (3) bass/treble with volume control mix mode 2 (FM example).
7. Optionally, the system controller can issue the SET_PROPERTY command to change the receive volume, bass/treble level, FM de-emphasis, soft-mute, and banding properties to override the default settings (FM example).

5.1.3. Power Off Sequence

1. System controller can optionally issue the POWER_DOWN command first to stop device current operations.
2. System controller holds the ATDD device RSTb pin in low state in power off. The current consumption of the ATDD device will be at about 10 µA at 3.3 V supply. (Note that the Si47xx DTDD device POWER_UP commands is not supported in the ATDD device; the system controller needs to reset device and issue ATDD_POWER_UP command to power up.)

5.2. Band Detection by System Controller

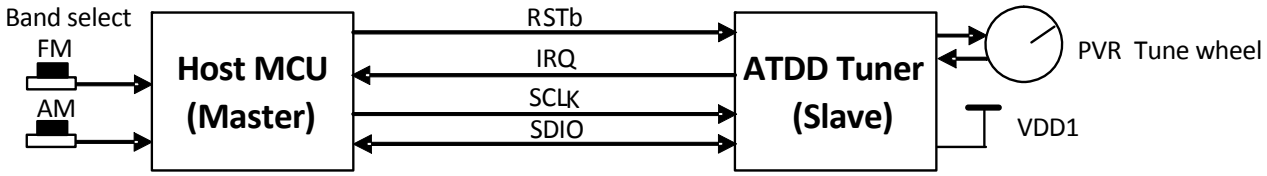


Figure 5. Band Detection and Control by System Controller

The system controller is responsible for detecting the band with its own mechanism. The method used to handle band switching on the ATDD device depends on whether the system controller wants to switch to the new band within the same band mode (e.g., FM1→FM5) or switch it across different band modes (e.g. FM5→AM1).For example, to switch to a new band within the same band mode, the system controller should re-issue the power up command with the new band number, optionally with band properties other than the predefined ones. Alternatively, to switch across different band modes, the system controller should reset the ATDD device and wait till it is ready again, then issue the same power up command with the new band number with optional band properties.

5.2.1. Power On Sequence

1. System controller resets the ATDD device and releases the RSTb pin.
2. System controller waits till first IRQ is received (indicates that the ATDD device is ready to receive commands).
3. System controller issues ATDD_GET_STATUS command to obtain the ATDD device status. The system controller is required to check in the reply from the BCFG0 bit to determine if the ATDD device or the system controller is responsible for band detection and selection. In this case, the BCFG0 bit should be 1 (i.e., host detects band). Note that the HOSTPWRUP bit is always set, which prompts the system controller to issue the ATDD_POWER_UP command. Band and tune information are not ready in this power up stage.
4. System controller issues ATDD_POWER_UP command with the bulleted arguments below to power up the device:
   - Set ARG1 bit[5:0] BANDIDX band index to the desired band number.
   - Set ARG1 bit[7] XOSEN bit = 1 if a 32.768 kHz crystal is in use. Set ARG1 bit[6] XOWAIT bit =0 if typical 600 ms crystallization time is enough or set the XOWAIT bit = 1 for a longer time of 900 ms.
   - Optionally include ARG2 ARG3* if new band bottom frequency is different from default.
   - Optionally include ARG4 ARG5* if new band top frequency is different from default.
   - Optionally include ARG6* if new band channel space is different from default (AM only).
   - Optionally include ARG7 for new features of Si4827 and Si4844B devices.
5. System controller waits till IRQ is received for the tune wheel frequency ready.
6. System controller issues ATDD_GET_STATUS command to obtain the latest status for display:
   - If REPLY0 bit[4] INFORDY bit = 1, i.e., info ready, the host can read and display the status, such as the band mode, the station, and stereo states.
   - The tune frequency is ready when combined frequency of REPLY2, REPLY3 is non-zero (4-digit BCD number).
7. Optionally, the system controller can issue the ATDD_AUDIO_MODE command to specify the number of

audio options (FM example):

- AUDIO_MODE bits selects one of the audio output modes: (0) digital volume mode, (1) bass/treble mode, (2) bass/treble with volume control mix mode 1, (3) bass/treble with volume control mix mode 2.
- ADJPT_ ATTN bit specifies if the 100 kHz adjacent points have audio output attenuated by 2 dB or not.
- ADJPT_STEO bit specifies if the 100 kHz adjacent points have stereo indicator and stereo separation.
- FM_MONO bit specifies if FM audio output is forced mono or stereo.

8. Optionally, the system controller can issue the SET_PROPERTY command to change the receive volume, bass/treble level, FM de-emphasis, soft-mute, and banding properties to override the default settings.

***Note:** If pin 1 of the Si4822/26/40/44 SSOP24 packaged ATDD devices has been pulled up by the resistor, it is forced to use default band properties. The system controller-specified band properties (i.e., band top, band bottom, channel space, FM de-emphasis, FM blend RSSI mono thresholds) will be ignored and have no effects.

5.2.2. Band Switch Sequence

1. Depends on system controller wants to switch to the new band within the same band mode across different band modes.
2. If system controller wants to switch band within same band mode, it can directly issue the power up command as in step 3. Otherwise, it needs to reset ATDD device first and wait till IRQ is received to power up the ATDD device again.
3. System controller issues ATDD_POWER_UP command with the bulleted arguments below to power up the device:
   - Set ARG1 bit[5:0] BANDIDX band index to the desired band number.
   - Set ARG1 bit[7] XOSEN bit = 1 if a 32.768 kHz crystal is in use. Set ARG1 bit[6] XOWAIT bit =0 if typical 600 ms crystallization time is enough or set the XOWAIT bit = 1 for a longer time of 900 ms.
   - Optionally include ARG2 ARG3* if new band bottom frequency is different from default.
   - Optionally include ARG4 ARG5* if new band top frequency is different from default.
   - Optionally include ARG6* if new band channel space is different from default (AM).
   - Optionally include ARG7 for new features of Si4827 and Si4844B devices.
4. System controller waits till IRQ is received for the tune wheel frequency ready.
5. System controller issues ATDD_GET_STATUS command to obtain the latest status for display:
   - If REPLY0 bit[4] INFORDY bit = 1, i.e. info ready, the host can read and display the status, such as the band mode, station, and stereo states.
   - The tune frequency is ready when combined frequency of REPLY2, REPLY3 is non-zero (4-digit BCD number).
6. Optionally, the system controller can issue the ATDD_AUDIO_MODE command to select one of the audio output modes: (0) digital volume mode, (1) bass/treble mode, (2) bass/treble with volume control mix mode 1, (3) bass/treble with volume control mix mode 2 (FM example).
7. Optionally, the system controller can issue the SET_PROPERTY command to change the receive volume, bass/treble level, FM de-emphasis, soft-mute, and banding properties to override the default settings (FM example).

***Note:** If pin 1 of the Si4822/26/40/44 SSOP24 packaged ATDD devices has been pulled up by resistor, it is forced to use default band properties. The system controller optionally specified band properties (i.e., band top, band bottom, channel space, FM de-emphasis, FM blend RSSI mono thresholds) will be ignored and have no effects.

5.2.3. Power Off Sequence

1. System controller can optionally issue the POWER_DOWN command first to stop device current operations.
2. System controller holds the ATDD device RSTb pin in low state in power off. The current consumption of the ATDD device will be at about 10 µA at 3.3 V supply. (Note that the Si47xx DTDD device POWER_UP commands is not supported in the ATDD device. The system controller needs to reset the device and issue ATDD_POWER_UP command to power up.)

6. Commands and Responses

Commands control actions, such as ATDD_GET_STATUS. Arguments are specific to a given command and are used to modify the command. For example, after the ATDD_POWER_UP command, arguments are required to set the band number, band top/bottom frequencies, channel spacing and optional features like China TV channel audio, universal AM band and more. Arguments are one byte in size, and each command may require up to seven argument bytes.

Responses provide the system controller with status information and are returned after a command and its associated arguments are issued. All commands return a one byte status containing minimum the 1 bit clear-to-send the next command and 1 bit error status. Commands may return up to 15 additional response bytes. A complete list of commands is available in Section “7. Commands and Properties” .

Table 2 shows an example of the ATDD_POWER_UP command. This command requires that a command and optionally 7 argument bytes to be sent and that one status byte be returned. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS), or response (RESP). The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Table 3. Using the ATDD_POWER_UP Command

Action	Data	Description
CMD	0xE1	ATDD_POWER_UP
ARG1	0x80	Band index = 0 (i.e., FM1), Enable crystal, typical crystal waiting time
ARG2	0x22	Set band bottom frequency to 88 MHz
ARG3	0x60	e.g., 0x2260→ 8800 (in 10 kHz unit)
ARG4	0x2A	Set band top frequency to 108 MHz
ARG5	0x30	e.g., 0x2A30→10800 (in 10 kHz unit)
ARG6	0x0A	Set channel spacing to 100 kHz (10 kHz unit)
ARG7	0x00	Disable Si4827/44B features
STATUS	→0x80	Reply Status. Clear-to-send high

Properties are special command arguments used to modify the default device operation and are generally configured immediately after powerup. An example of a property is FM_MODE_DE_EMPHASIS. A complete list of properties is available in “7. Commands and Properties” .

Table 3 shows an example of setting the digital volume level using the RX_VOLUME property by sending the SET_PROPERTY command and 1 argument bytes. ARG1 of the SET_PROPERTY command is always 0x00. ARG2 and ARG3 are used to select the property number, PROP (0x04000 in this example).,ARG4 and ARG5 are used to set the property value, PROPD (0x003F max digital volume level in the example).

Table 4. Using the SET_PROPERTY Command

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_VOLUME
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Set digital volume to max volume level (63)
ARG5 (PROPD)	0x3F	
STATUS	→0x80	Reply Status. Clear-to-send high

Section “8. Control Interface” details the required bit transactions on the 2-wire bus mode.

7. Commands and Properties

There are two different components for these ATDD product families:

1. FM Receiver component
2. AM/SW component

The following two subsections list all the commands and properties used by each component.

7.1. Commands and Properties for the FM Receiver

Tables 4 and 5 summarize the commands and properties for the FM Receiver component applicable to Si4822/26/40/44.

Table 5. FM Receiver Command Summary

CMD	Name	Description
0xE0	ATDD_GET_STATUS	Get tune freq, band, and etc., status of the device
0xE1	ATDD_POWER_UP	Power up device, band selection, and band properties setup
0xE2	ATDD_AUDIO_MODE	Audio output mode: get/set audio mode and settings
0x10	GET_REV	Returns the revision information of the device
0x11	POWER_DOWN	Power down device
0x12	SET_PROPERTY	Sets the value of a property
0x13	GET_PROPERTY	Retrieves a property's value
***Note:** The ATDD family has its own power up and get status commands, which is different from previous Si47xx DTDD family. To differentiate, we use “ATDD_POWER_UP” and “ATDD_GET_STATUS” to denote the ATDD specific commands instead of the general Si47xx “POWER_UP” and “STATUS” commands.		

Table 6. FM Receiver Property Summary

Prop	Name	Description	Default
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0201	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x1100	FM_DEEMPHASIS	Sets de-emphasis time constant. Default is 75 µs.	0x0002
0x1300	FM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040
0x1301	FM_SOFT_MUTE_SLOPE	Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Default value is 2.	0x0002
0x1302	FM_SOFT_MUTE_ MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x1303	FM_SOFT_MUTE_ SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004
0x1207	FM_STEREO_IND _BLEND_THRESHOLD	Sets the blend threshold for stereo indicator. Default value is band-dependent (either 0x9F or 0xB2). **Note:** Applicable to Si4840/44 parts only.	0x9F 0xB2
0x1800	FM_BLEND_RSSI_ STEREO_THRESHOLD	Sets RSSI threshold for stereo blend. (Full stereo above threshold, blend below threshold.) To force stereo, set this to 0. To force mono, set this to 127. Default value is 49 dBµV. **Note:** Applicable to Si4840/44 parts only.	0x0031
0x1801	FM_BLEND_RSSI_ MONO_THRESHOLD	Sets RSSI threshold for mono blend. (Full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. Default value is band dependent (either 8 or 7). **Note:** Applicable to Si4840/44 parts only.	0x0008 0x0007
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently.	0x0000
0x4002	RX_BASS_TREBLE	Sets the output bass/treble level.	0x0004
0x4003	RX_ACTUAL_VOLUME	Read the actual output volume.	0x003F

7.1.1. FM Receiver Commands

Command 0xE0. ATDD_GET_STATUS

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	HOSTRST	HOSTPWRUP	INFORDY	STATION	STEREO*	BCFG1	BCFG0
RESP1	BANDMODE		BANDIDX					
RESP2	CHFREQ[15:8]							
RESP3	CHFREQ[7:0]							

RESP	Bit	Name	Function
STATUS	7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command
STATUS	6	HOSTRST	**Host Reset.**[1] 0 = None 1= Host reset action requested
STATUS	5	HOSTPWRUP	**Host Power Up.**[1] 0 = None 1= Host sending ATDD_POWER_UP command action requested

Notes:

1. For band detection by the ATDD device case, the system controller is always required to check the host actions bits and handle them correctly first. (i.e., HOSTRST and HOSTPWRUP bits.)
   - HOSTRST bit = 1, reset the ATDD device.
   - HOSTPWRUP bit = 1, issue the ATDD_POWER_UP command with the valid band index detected.
2. During power up case, the system controller should not display any of the channel frequency, band mode, band index, station, or stereo statuses until the INFORDY bit is set. The host controller should not display the channel frequency when CHFREQ remains zero even when INFORDY=1. Furthermore, the system controller is advised to save the band index for later use whenever the INFORDY bit is set.For example, when the band switches from FM to AM, the system controller is required to reset the ATDD device and then issue the ATDD_POWER_UP command with the new band index, which is the saved valid band index value, before resetting the device.
   After power up, whenever the ATDD device detects changes in any of the statuses, it will generate a high pulse on its IRQ pin to interrupt the system controller. The system controller is then required to issue the ATDD_GET_STATUS command to get the latest tune status and update its display contents accordingly.
3. For FM band, if the China TV channel audio sub-carrier display feature is enabled, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 50 kHz for the channel frequency.
4. For SW band, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 5 kHz for the channel frequency.

RESP	Bit	Name	Function
STATUS	4	INFORDY	**Information Ready.**[2] 0 = Tune info not ready yet 1 = Tune info ready (i.e., Band mode, band index, channel frequency, station, and stereo indicators)
STATUS	3	STATION	**Station Indicator.** 0 = Station invalid 1 = Station valid
STATUS	2	STEREO	**Stereo indicator.** 0 = Stereo off 1 = Stereo on ***Note:** Applicable to Si4840/44 parts FM function only.
STATUS	1	BCFG1	**Band CFG1 (Band Properties Priority).** 0 = ATDD device accepts host customized band properties 1 = ATDD device ignores host customized band properties
STATUS	0	BCFG0	**Band CFG0 (Band Detection Configuration).** 0 = ATDD device detects band 1 = Host detects band
RESP1	7:6	BANDMODE	**Band Mode Detected.** 0 = FM mode 1 = AM mode 2 = SW mode
RESP1	5:0	BANDIDX	**Band Index Detected.** 0~19: FM band 20~24: AM band 25~40: SW band
RESP2:3	15:0	CHFREQ	**Channel Frequency.** The channel frequency is a 16-bit word of 4 digits in BCD format: FM[3] 0640..1090 (64.0–109.0 MHz) AM 0504..1750 (504–1750 kHz) SW[4] *0230..2850 (2.3– 28.5 MHz)

Notes:

1. For band detection by the ATDD device case, the system controller is always required to check the host actions bits and handle them correctly first. (i.e., HOSTRST and HOSTPWRUP bits.)
   - HOSTRST bit = 1, reset the ATDD device.
   - HOSTPWRUP bit = 1, issue the ATDD_POWER_UP command with the valid band index detected.
2. During power up case, the system controller should not display any of the channel frequency, band mode, band index, station, or stereo statuses until the INFORDY bit is set. The host controller should not display the channel frequency when CHFREQ remains zero even when INFORDY=1. Furthermore, the system controller is advised to save the band index for later use whenever the INFORDY bit is set.For example, when the band switches from FM to AM, the system controller is required to reset the ATDD device and then issue the ATDD_POWER_UP command with the new band index, which is the saved valid band index value, before resetting the device.
   After power up, whenever the ATDD device detects changes in any of the statuses, it will generate a high pulse on its IRQ pin to interrupt the system controller. The system controller is then required to issue the ATDD_GET_STATUS command to get the latest tune status and update its display contents accordingly.
3. For FM band, if the China TV channel audio sub-carrier display feature is enabled, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 50 kHz for the channel frequency.
4. For SW band, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 5 kHz for the channel frequency.

Command 0xE1. ATDD_POWER_UP

The power up process of this ATDD device is different from the Si47xx DTDD devices. The ATDD device provides only the FM/AM functions. The device doesn't provide patch and op-mode capabilities such that it is force-configured to analog audio outputs (LOUT/ROUT) only.

When the system controller resets the ATDD device and releases the RSTb pin from low to high, the ATDD device boots autonomously and comes to an active waiting state instead of staying at power down mode and waiting for the system controller commands. Only two commands are accepted in this active waiting state:

1. ATDD_POWER_UP command 0xE1
2. ATDD_GET_STATUS command 0xE0

The ATDD_POWER_UP command should be issued after the system controller has reset the device successfully. A high pulse is then output from the device's IRQ, indicating the device is reset successfully. The command initiates the boot process to move the device from active waiting state to normal operating state.

Instead of specifying the FM and AM function directly, a band index is required to specify both the function and one of the predefined bands. The ATDD device uses the PVR as the tune wheel to mimic the traditional mechanical tuning. However, the tune wheel position of the PVR can be represented only in finite resolutions per band. Therefore, multiple bands are necessary to cover the FM and SW bands' full ranges. A total of 41 bands (20 for FM, 5 for AM and 16 for SW bands) are pre-defined for the ATDD device to address different country and customer requirements.

Table 7. ATDD Device Band Index Corresponding Function

Band index	Function	Band Range	Si4822/40	Si4826/27/44
0~19	FM	FM 64~109 MHz	✓	✓
20~24	AM*	AM 504~1750 kHz	✓	✓
25~40	AM*	SW 2.3~28.5 MHz	×	✓
***Note:** The AM and SW bands share a single firmware function.				

The ATDD_POWER_UP command configures the state of ROUT and LOUT for analog audio mode and IRQ for interrupt operation. The IRQ pin is driven low during normal operation and high for a minimum of 1 ms during the interrupt. The CTS function is always enabled by default and cannot be disabled by the system controller.

For Si4822/26/40/44A ATDD parts, due to finite resolution of the ATDD device internal ADC for tune wheel position sensing, very wide frequency range bands should be broken into smaller range sub-bands such that a sub-band should not contain more than 230 channels. For example, the 64–109 MHz band range should be broken into two smaller bands, one from 64–88 MHz and another from 88–109 MHz. Similarly for SW, the entire 5.6–22 MHz range must be broken into 8 smaller bands. Furthermore, there are two band groups for SW, one is for standard or narrow band frequency while another is for wide band frequency range. Thus, we have a total of 16 SW bands. The extended SW band frequency ranges from 2.3–5.6 MHz and 22–28.5 MHz are not covered in pre-defined bands.Theyare supported only via API and the system controller programming the extended band range.

For Si4827/44B ATDD parts with new firmware that supports the wide FM bands and the wide SW bands, the host controller is allowed to re-configure a wider band range without the 230 channel resolution restriction.

For FM, there are five different band frequency ranges and for each there are two different de-emphasis and stereo separation and RSSI thresholds options. Therefore, there is a total 20 FM bands. For AM, there are 5 different band frequency ranges which support 9 kHz and 10 kHz channel spaces respectively. For SW, we have a total of16 bands, 8 of which are standard narrow ranges while another 8 bands are wider ranges.

Note: To change function (e.g. FM RX to AM RX or vice versa), the system controller needs to reset the ATDD device first and then issue ATDD_POWER_UP with the detected band number and optional band properties.

Table 8. Pre-defined Band Table

Band Index	Band Name	Band Freq Range	De-emphasis (FM) Channel Space (AM)	Stereo Separation* & RSSI Thresholds
0	FM1	87–108 MHz	75 µs	6 dB separation, RSSI = 20
1	FM1	87–108 MHz	75 µs	12 dB separation, RSSI = 28
2	FM1	87–108 MHz	50 µs	6 dB separation, RSSI = 20
3	FM1	87–108 MHz	50 µs	12 dB separation, RSSI = 28
4	FM2	86.5–109 MHz	75 µs	6 dB separation, RSSI = 20
5	FM2	86.5–109 MHz	75 µs	12 dB separation, RSSI = 28
6	FM2	86.5–109 MHz	50 µs	6 dB separation, RSSI = 20
7	FM2	86.5–109 MHz	50 µs	12 dB separation, RSSI = 28
8	FM3	87.3–108.25 MHz	75 µs	6 dB separation, RSSI = 20
9	FM3	87.3–108.25 MHz	75 µs	12 dB separation, RSSI = 28
10	FM3	87.3–108.25 MHz	50 µs	6 dB separation, RSSI = 20
11	FM3	87.3–108.25 MHz	50 µs	12 dB separation, RSSI = 28
12	FM4	76–90 MHz	75 µs	6 dB separation, RSSI = 20
13	FM4	76–90 MHz	75 µs	12 dB separation, RSSI = 28
14	FM4	76–90 MHz	50 µs	6 dB separation, RSSI = 20
15	FM4	76–90 MHz	50 µs	12 dB separation, RSSI = 28
16	FM5	64–87 MHz	75µs	6 dB separation, RSSI = 20
17	FM5	64–87 MHz	75 µs	12 dB separation, RSSI = 28
18	FM5	64–87 MHz	50 µs	6 dB separation, RSSI = 20
19	FM5	64–87 MHz	50 µs	12 dB separation, RSSI = 28
20	AM1	520–1710 kHz	10 kHz	
21	AM2	522–1620 kHz	9 kHz	
22	AM3	504–1665 kHz	9 kHz	
23	AM4	520–1730 kHz	10 kHz	
24	AM5	510–1750 kHz	10 kHz	
25	SW1	5.6–6.4 MHz		
26	SW2	5.9–56.2 MHz		

***Note:** The Stereo Separation specification is applicable to Si4840/44 FM stereo parts only.

Table 8. Pre-defined Band Table (Continued)

Band Index	Band Name	Band Freq Range	De-emphasis (FM) Channel Space (AM)	Stereo Separation* & RSSI Thresholds
27	SW3	6.8–7.6 MHz		
28	SW4	7.1–7.6 MHz		
29	SW5	9.2–10 MHz		
30	SW6	9.2–9.9 MHz		
31	SW7	11.45–12.25 MHz		
32	SW8	11.6–12.2 MHz		
33	SW9	13.4–14.2 MHz		
34	SW10	13.57–13.87 MHz		
35	SW11	15–15.9 MHz		
36	SW12	15.1–15.8 MHz		
37	SW13	17.1–18 MHz		
38	SW14	17.48–17.9 MHz		
39	SW15	21.2–22 MHz		
40	SW16	21.45–21.85 MHz		
***Note:** The Stereo Separation specification is applicable to Si4840/44 FM stereo parts only.				

Command arguments: Minimum one and optionally seven

Response bytes: One

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	0	1
ARG1	XOSCEN	XOWAIT	BANDIDX					
ARG2	BANDBOT[15:8]							
ARG3	BANDBOT[7:0]							
ARG4	BANDTOP[15:8]							
ARG5	BANDTOP[7:0]							
ARG6	CHSPC							
ARG7*	TVFREQ	UNI_AM	DFBAND	0	0	0	0	0
***Note:** Additional command argument ARG7 is supported by Si4827/44B parts only.								

ARG	Bit	Name	Function
1	7	XOSCEN	**Crystal Oscillator Enable.** 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (XTALI and XTALO with external 32.768 kHz crystal). See the Si484x Data Sheet Application Schematic for external BOM details.
1	6	XOWAIT	**Crystal Oscillator Stabilization Wait Time After Reset.** 0 = 600 ms (for typical crystal) 1 = 900 ms (for crystal requiring extra stabilization time) **Note:** Applicable to Si4822/26/40/44A parts only. Later Si4827/44B parts don't care this bit and will wait till crystal oscillation is stable unconditionally.
1	5:0	BANDIDX	**Band Index to Set.**[1] 0~19: FM band number range 20~24: AM band number range 25~40: SW band number range
2:3	15:0	BANDBOT[2,4]	**Band Bottom Frequency Limit.** FM 6400..10900 (64.0–109.0 MHz) AM 510..1750 (510–1750 kHz) SW 2300..28500 (2.3–28.5 MHz)
4:5	15:0	BANDTOP[2,4]	**Band Top Frequency Limit.** FM 6400..10900 (64.0–109.0 MHz) AM 510..1750 (510–1750 kHz) SW 2300..28500 (2.3–28.5 MHz)
6	7:0	CHSPC[2,3]	**Channel Spacing.** FM 10 (e.g.,100 kHz) AM 9 or 10 (e.g., 9 kHz or 10 kHz) SW 5 (e.g., 5 kHz)
7	7	TVFREQ[5]	**TV Audio Channel Frequency Display.** 0 = Disable TV audio channel frequency display format 1 = Enable TV audio channel frequency display format **Note:** Applicable to Si4827 and Si4844B parts and FMRX mode only
7	6	UNI_AM[5]	**Universal AM Band.** 0 = Disable universal AM band (default AFC range of 1.1 kHz) 1 = Enable universal AM band (wider AFC range in tuning) **Note:** Applicable to Si4827 and Si4844B parts and AMRX mode only
7	5	DFBAND[5]	Default Band Settings. 0 = Allow host controller to override the band property settings 1 = Force to use tuner default band property settings **Note:** Applicable to Si4827 part only

Notes:

1. The band index to set for the ATDD device band detection case needs to be consistent with the band index detected by the device (e.g., band index reads from ATDD_GET_STATUS command when INFORDY bit is set.)
2. The band bottom, top, and channel spacing arguments are optional and can be omitted if the system controller doesn't need to override the corresponding default band properties. However, if pin 1 of the Si4822/26/40/44 ATDD parts has been pulled up by the resistor, it is forced to use default band properties. The system controller optionally specified band properties will be ignored and have no effects.
3. The channel spacing is configurable for the AM band mode only. System controller can select between 9 (9 kHz) and 10 (10 kHz) channel space. For FM and SW, it should be set to 10 (100 kHz) and 5 (5 kHz) respectively.
4. System controller can re-program the band frequency limits, i.e., BANDBOT and BANDTOP, of a band to override the default values.
   For Si4822/26/40/44A ATDD parts, the programmed values must satisfy the following requirements for proper tuning operation:
   - BANDBOT needs to be multiple of CHSPC; i.e., exact dividable by the channel spacing.
   - (BANDTOP – BANDBOT)/(CHSPC) must be in 50…230 range
   - When programming the BANDTOP value, the system controller is required to add extra margin to guarantee the band top frequency can be reached.
     FM: 70 kHz (value of 7) margin is required
     AM: 6 kHz (value of 6) margin is required
     SW: 4 kHz (value of 4) margin is required
   - For example, to program the customized FM band from 80–103 MHz of the total 230 channels, the values set for BANDBOT is 8000 and BANDTOP is (10300+7) which is 10307.

   For later Si4827/44B ATDD parts which support wide FM and wide SW bands, system controller is allowed to set BANDBOT and BANDTOP for the maximum band range without restrictions. System controller is no longer required to reserve extra margin when programming the BANDTOP.
   - BANDBOT and BANDBOT need to be multiple of CHSPC; i.e., exact dividable by the channel spacing.
5. ARG7 is supported by Si4827/44B parts only. System controller is optional to send this argument in the ATDD_POWER_UP command if advanced features are needed.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR			ERRCODE			

Command 0xE2. ATDD_AUDIO_MODE

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	1	0
ARG1	OPCODE	Reserved		ADJPT_STEO	ADJPT_ATTN	FM_MONO*	AUDIOMODE	

ARG	Bit	Name	Function
1	7	OPCODE	**Operation Code.** 0 = Set audio mode and settings 1 = Get current audio mode and settings without setting
1	4	ADJPT_STEO	**Station Adjacent Tune Wheel Positions Stereo Option.** 0 = Adjacent points allow stereo separation and stereo indicator on (default) 1 = Adjacent points disable stereo separation and stereo indicator are off
1	3	ADJPT_ATTN	**Station Adjacent Tune Wheel Positions Audio Attenuation Option.** Audio attention of adjacent tune wheel positions of a station: 0 = {–2 dB, -0dB, –2 dB} i.e., adjacent points volume levels –2 dB (default) 1 = {–0 dB, -0dB, –0 dB} i.e., adjacent points same volume levels
1	2	FM_MONO	**FM Mono/Stereo.** 0 = Stereo audio output (default) 1 = Mono audio output ***Note:** Applicable to Si4840/44 FM stereo parts only. Setting this bit for FM mono parts will have no effect.
1	1:0	AUDIOMODE	**Audio Mode.** 0 = Digital volume mode (no bass/treble effect, volume levels from 0 to 63) 1 = Bass/treble mode (no digital volume control, fixed volume level at 59) 2 = Mixed mode 1 (bass/treble and digital volume coexist, max volume = 59) 3 = Mixed mode 2 (bass/treble and digital volume coexist, max volume = 63) Default is 3 (Mixed mode 2)

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved	ADJPT_STEO	ADJPT_ATTN	FM_MONO	AUDIOMODE	

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision, and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in power up mode.

Command arguments: None

Response bytes: Eight

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	Reserved							
RESP5	Reserved							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							

RESP	Bit	Name	Function
1	7:0	PN	Final 2 digits of Part Number (HEX).
2	7:0	FWMAJOR	Firmware Major Revision (ASCII).
3	7:0	FWMINOR	Firmware Minor Revision (ASCII).
6	7:0	CMPMAJOR	Component Major Revision (ASCII).
7	7:0	CMPMINOR	Component Minor Revision (ASCII).
8	7:0	CHIPREV	Chip Revision (ASCII).

Command 0x11. POWER_DOWN

Moves the device from power up to power down mode. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode. Note that only the ATDD_POWER_UP and ATDD_GET_STATUS commands are accepted in power down mode. If the system controller writes a command other than the two commands when in power down mode, the device does not respond. The device will only respond when an ATDD_POWER_UP command is written. GPO pins are powered down and not active during this state.

Note: The following describes the state of all the pins when in powerdown mode: ROUT, LOUT = HiZ

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					

Command 0x12. SET_PROPERTY

Sets a property shown in Table 5, “FM Receiver Command Summary,” on page 12. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode.

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify
3	7:0	$PROP_L$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify
4	7:0	$PROPD_H$	**Property Value High Byte.** This byte in combination with $PROPD_L$ is used to specify the property to modify
5	7:0	$PROPD_L$	**Property Value Low Byte.** This byte in combination with $PROPD_H$ is used to specify the property to modify

Command 0x13. GET_PROPERTY

Gets a property as shown in Table 5, “FM Receiver Command Summary,” on page 12. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode.

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get
3	7:0	$PROP_L$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPD_H$[7:0]							
RESP3	$PROPD_L$[7:0]							

RESP	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROPD_H$	**Property Value High Byte.** This byte in combination with $PROPD_L$ represents the requested property value
3	7:0	$PROPD_L$	**Property Value Low Byte.** This byte in combination with $PROPD_H$ represents the requested property value

7.1.2. FM Receiver Properties

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 ±5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an reference clock at XTALI pin of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. Reference clock frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these reference clock gaps.

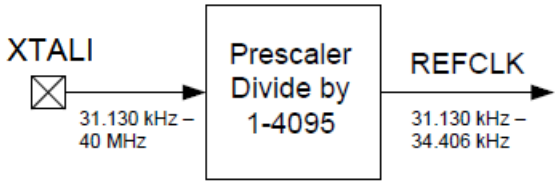


Figure 6. REFCLK Prescaler

Table 9. XTLI Reference Clock Frequency Gaps

Prescaler	XTALI Low (Hz)	XTALI High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before resetting and valid at all times for proper tuning and AFC operations. XTALI reference clock input frequency could be changed but is not recommended and REFCLK properties values need to be reconfigured accordingly. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 32768 Hz.

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130-34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:2	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768±5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external reference clock frequency down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an XTALI reference clock of 13 MHz would require a prescaler value of 400 to divide it to 3250 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The reference clock must be valid 10 ns before the chip reset signal. In addition, the reference clock must be valid at all times for proper tuning and AFC operations. XTALI reference clock input frequency could be changed but is not recommended and REFCLK properties values need to be reconfigured accordingly. The CTS bit (and optional interrupt) is set when it is safe to send the next command.

This property may only be set or read when in powerup mode. The default is 1.

Default: 0x0001

Step: 1

Range: 1-4095.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK SEL	REFCLK[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = Reserved
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide clock frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x4000. RX_VOLUME

Sets the audio output volume. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 63.

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	VOL	**Output Volume.** Sets the output volume level. The max level is dependent on the audio mode selected. 0 - Digital volume mode: Actual volume level ranges from 0~63 1 - Bass/Treble mode: Actual volume level ranges from 0~59 2 - Mixed mode 1: Actual volume level ranges from 0~59 3 - Mixed mode 2: Actual volume level ranges from 0~63

Property 0x4001. RX_HARD_MUTE

Mutes the audio output. L and R audio outputs may be muted independently. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is un-mute (0x0000).

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LMUTE	RMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LMUTE	**Left Mute.** Mutes L Audio Output.
0	RMUTE	**Right Mute.** Mutes R Audio Output.

Property 0x4002. RX_BASS_TREBLE

Sets the audio output bass/treble effect. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 4.

The bass effect is achieved by boosting the audio low frequency components and attenuating the audio frequency components. The treble effect is achieved vice versa. As additional dynamic range is required to process the bass/treble effects, the maximum digital volume output level for maximum bass/treble effect is reduced by 5dB compared with no bass/treble effects. For the same reason, the audio SNR under the bass/treble audio mode is a few dB worst than that under the digital volume audio mode.

Default: 0x0004

Step: 1

Range: 0–8

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	BASSTREBLE[4:0]				

Bit	Name	Function
15:5	Reserved	Always write to 0.
4:0	BASSTREBLE	**Bass/Treble level.** Sets the output bass/treble effect level: 0 -Bass boost +4 (max) 1- Bass boost +3 2- Bass boost +2 3- Bass boost +1 (min) 4- Normal (No Bass/Treble effect) (Default) 5- Treble boost +1 (min) 6- Treble boost +2 7- Treble boost +3 8- Treble boost +4 (max)

Property 0x4003. RX_ACTUAL_VOLUME

Read only reflects the actual digital audio output volume in use. When bass/treble effect is enabled at high volume level, the actual volume read can be different from what the property 0x4000 RX_VOLUME set due to the extra dynamic range required for making the bass/treble effect. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 63.

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	ACT_VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	ACT_VOL	**Actual Volume.** Actual volume level ranges from 0~63

Property 0x1100. FM_DEEMPHASIS

Sets the FM Receive de-emphasis to 50 or 75 µs. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 75 µs.

Default: 0x0002

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEEMPH[1:0]	

Bit	Name	Function
15:2	Reserved	Always write to 0.
1:0	DEEMPH	**FM De-emphasis.** 10 = 75 µs. Used in USA 01 = 50 µs. Used in Europe, Australia, Japan, China 00 = Reserved 11 = Reserved

Property 0x1300. FM_SOFT_MUTE_RATE

Sets the attack and decay rates when entering and leaving soft mute. Later values increase rates, and lower values decrease rates. The CTS is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 64.

Default: 64

Step: 1

Range: 1—255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	SMRATE[7:0]							

Property 0x1301. FM_SOFT_MUTE_SLOPE

Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Soft mute attenuation is the minimum of SMSLOPE x (SMTHR – SNR) and SMATTN. The recommended SMSLOPE value is CEILING(SMATTN/SMTHR). SMATTN and SMTHR are set via the FM_SOFT_MUTE_MAX_ATTENUATION and FM_SOFT_MUTE_SNR_THRESHOLD properties. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode.

Default: 0x0002

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	SMSLOPE[7:0]							

Property 0x1302. FM_SOFT_MUTE_MAX_ATTENUATION

Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 16 dB.

Default: 0x0010

Units: dB

Step: 1

Range: 0–31

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	SMATTN[4:0]				

Bit	Name	Function
15:5	Reserved	Always write to 0.
4:0	SMATTN	**FM Soft Mute Maximum Attenuation.** Set maximum attenuation during soft mute. If set to 0, then soft mute is disabled. Specified in units of dB in 1 dB steps (0–31). Default is 16 dB.

Property 0x1303. FM_SOFT_MUTE_SNR_THRESHOLD

Sets SNR threshold to engage soft mute. Whenever the SNR for a tuned frequency drops below this threshold, the FM reception will go in soft mute, provided soft mute max attenuation property is non-zero. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 4 dB.

Default: 0x0004

Units: dB

Step: 1

Range: 0–15

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	SMTHR[3:0]			

Bit	Name	Function
15:2	Reserved	Always write to 0.
3:0	SMTHR	**FM Soft Mute SNR Threshold.** Threshold which will engage soft mute if the SNR falls below this. Specified in units of dB in 1 dB steps (0–15). Default is 4 dB.

Property 0x1207. FM_STEREO_IND_BLEND_THRESHOLD (Si4840/44 only)

Sets the blend threshold for stereo indicator. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default value is band dependent (either 0x9F or 0xB2)

Default: 0x009F or 0x00B2 (Band dependent)

Range: 0–0xFF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	BLEND[7:0]							

Property 0x1800. FM_BLEND_RSSI_STEREO_THRESHOLD (Si4840/44 only)

Sets RSSI threshold for stereo blend (full stereo above threshold, blend below threshold). To force stereo, set to 0. To force mono, set to 127. The CTS bit is set when it is safe to send the next command.

This property may only be set or read when in powerup mode. The default is 49 dBµV.

Default: 0x0031

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	STRTHRESH[6:0]						

Property 0x1801. FM_BLEND_RSSI_MONO_THRESHOLD (Si4840/44 only)

Sets RSSI threshold for mono blend (full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. The CTS is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is band dependent (0x0008 or 0x0007)

Default: 0x0008 or 0x0007 (Band dependent)

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MONOTHRESH[6:0]						

7.2. Commands and Properties for the AM/SW Receiver

AM (Medium Wave) and SW (Short Wave) use the same AM_SW component, thus the commands and properties for these functions are the same. For simplicity, the commands and properties only have a prefix AM instead of AM_SW. The main difference among AM and SW is on the frequency range.

The common frequency range and spacing for AM/SW are:

- AM in US 520 kHz–1.71 MHz in 10 kHz frequency spacing
- AM in Asia 522 kHz–1.71 MHz in 9 kHz frequency spacing
- SW 2.3–28.5 MHz in 5 kHz frequency spacing

Tables 8 and 10 summarize the commands and properties for the AM/SW Receiver components applicable to the ATDD family.

Table 10. AM/SW Receiver Command Summary

Cmd	Name	Description
0xE0	ATDD_GET_STATUS	Gets tune freq, band, and etc., status of the device.
0xE1	ATDD_POWER_UP	Power up device, band selection, and band properties setup.
0xE2	ATDD_AUDIO_MODE	Audio output mode: get/set audio mode settings.
0x10	GET_REV	Returns the revision information of the device.
0x11	POWER_DOWN	Power down device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
Notes: The ATDD family has its own power up and get status commands, which is different from previous Si47xx DTDD family. To differentiate, we use “ATDD_POWER_UP” and “ATDD_GET_STATUS” to denote the ATDD specific commands instead of the general Si47xx “POWER_UP” and “STATUS” commands.		

Table 11. AM/SW Receiver Property Summary

Prop	Name	Description	Default
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently.	0x0000
0x4002	RX_BASS_TREBLE	Sets the output bass/treble level.	0x0003
0x4003	RX_ACTUAL_VOLUME	Reads the actual output volume.	0x003F
0x3300	AM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040
0x3301	AM_SOFT_MUTE_SLOPE	Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold.	0x0002
0x3302	AM_SOFT_MUTE_ MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute.	0x0010
0x3303	AM_SOFT_MUTE_ SNR_THRESHOLD	Sets SNR threshold to engage soft mute.	0x0008

7.2.1. AM/SW Receiver Commands

Command 0xE0. ATDD_GET_STATUS

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	HOSTRST	HOSTPWRUP	INFORDY	STATION	STEREO*	BCFG1	BCFG0
RESP1	BANDMODE		BANDIDX					
RESP2	CHFREQ[15:8]							
RESP3	CHFREQ[7:0]							

RESP	Bit	Name	Function
STATUS	7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
STATUS	6	HOSTRST	**Host Reset.**[1] 0 = None 1= Host reset action requested
STATUS	5	HOSTPWRUP	**Host Powerup.**[1] 0 = None 1= Host sending ATDD_POWER_UP command action requested

Notes:

1. For band detection by ATDD device case, the system controller is always required to check the host actions bits and handle them correctly first (i.e., HOSTRST and HOSTPWRUP bits.)
   - HOSTRST bit = 1, reset the ATDD device.
   - HOSTPWRUP bit = 1, issue the ATDD_POWER_UP command with the valid band index detected.
2. During power up case, the system controller should not display any of the channel frequency, band mode, band index, station and stereo status until the INFORDY bit is set. Host controller should not display the channel frequency when CHFREQ remains zero even when INFORDY=1. Furthermore, the system controller is advised to save the band index for later use whenever the INFORDY bit is set.For example, when the band switches from FM to AM, the system controller is required to reset the ATDD device and then issue the ATDD_POWER_UP command with the new band index, which is the saved valid band index value, before resetting the device.
   After power up, whenever the ATDD device detects changes in either status, it will generate a high pulse on its IRQ pin to interrupt the system controller. Then the system controller is required to issue the ATDD_GET_STATUS command to get the latest tune status and update its display contents accordingly.
3. For FM band, if the China TV channel audio sub-carrier display feature is enabled, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 50 kHz for the channel frequency.
4. For SW band, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 5 kHz for the channel frequency.

RESP	Bit	Name	Function
STATUS	4	INFORDY	**Information Ready.**[2] 0 = Tune info not ready yet 1 = Tune info ready (i.e., Band mode, band index, channel frequency, station and stereo indicators)
STATUS	3	STATION	**Station Indicator.** 0 = Station invalid 1 = Station valid
STATUS	2	STEREO	**Stereo Indicator.** 0 = Stereo off 1 = Stereo on ***Note:** Applicable to Si4840/44 parts FM function only.
STATUS	1	BCFG1	**Band CFG1 (Band Properties Priority).** 0 = ATDD device accepts host customized band properties 1 = ATDD device ignores host customized band properties
STATUS	0	BCFG0	**Band CFG0 (Band Detection Configuration).** 0 = ATDD device detects band 1 = Host detects band
RESP1	7:6	BANDMODE	**Band Mode Detected.** 0 = FM mode 1 = AM mode 2 = SW mode
RESP1	5:0	BANDIDX	**Band Index Detected.** 0~19: FM band 20~24: AM band 25~40: SW band
RESP2:3	15:0	CHFREQ	**Channel Frequency.** The channel frequency is a 16-bit word of 4 digits in BCD format: FM[3] 0640..1090 (64.0–109.0 MHz) AM 0504..1750 (504–1750 kHz) SW[4] *0230..2850 (2.3–28.5 MHz)

Notes:

1. For band detection by ATDD device case, the system controller is always required to check the host actions bits and handle them correctly first (i.e., HOSTRST and HOSTPWRUP bits.)
   - HOSTRST bit = 1, reset the ATDD device.
   - HOSTPWRUP bit = 1, issue the ATDD_POWER_UP command with the valid band index detected.
2. During power up case, the system controller should not display any of the channel frequency, band mode, band index, station and stereo status until the INFORDY bit is set. Host controller should not display the channel frequency when CHFREQ remains zero even when INFORDY=1. Furthermore, the system controller is advised to save the band index for later use whenever the INFORDY bit is set.For example, when the band switches from FM to AM, the system controller is required to reset the ATDD device and then issue the ATDD_POWER_UP command with the new band index, which is the saved valid band index value, before resetting the device.
   After power up, whenever the ATDD device detects changes in either status, it will generate a high pulse on its IRQ pin to interrupt the system controller. Then the system controller is required to issue the ATDD_GET_STATUS command to get the latest tune status and update its display contents accordingly.
3. For FM band, if the China TV channel audio sub-carrier display feature is enabled, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 50 kHz for the channel frequency.
4. For SW band, the CHFREQ bit[15] MSB = 1 means the host controller needs to add an additional 5 kHz for the channel frequency.

Command 0xE1. ATDD_POWER_UP

The power up process of this ATDD device is different from the Si47xx DTDD devices. The ATDD device provides only the FM/AM functions. The device doesn't provide patch and op-mode capabilities such that it is force-configured to analog audio outputs (LOUT/ROUT) only.

When the system controller resets the ATDD device and releases the RSTb pin from low to high, the ATDD device boots autonomously and comes to an active waiting state instead staying at power down mode and waiting for the system controller commands. Only two commands are accepted in this active waiting state:

1. ATDD_POWER_UP command 0xE1
2. ATDD_GET_STATUS command 0xE0

The ATDD_POWER_UP command should be issued after the system controller has reset the device successfully. A high pulse is output from the device's IRQ indicating the device is reset successfully. The command initiates the boot process to move the device from active waiting state to normal operating state.

Instead of specifying the FM and AM functions directly, a band index is required to specify both the function and one of the predefined bands. The ATDD device uses the PVR as the tune wheel to mimic the traditional mechanical tuning. However, the tune wheel position of the PVR can be represented only in finite resolutions per band. Therefore, multiple bands are necessary to cover the FM and SW bands full ranges. A total of 41 bands (20 for FM, 5 for AM, and 16 for SW bands) are pre-defined for the ATDD device to address different country and customer requirements:

Table 12. ATDD Device Band Index Corresponding Function

Band index	Function	Band Range	Si4822/40	Si4826/27/44
0~19	FM	FM 64–109 MHz	✓	✓
20~24	AM*	AM 504–1750 kHz	✓	✓
25~40	AM*	SW 2.3–28.5 MHz	×	✓
***Note:** The AM and SW bands share a single firmware function.				

The ATDD_POWER_UP command configures the state of ROUT and LOUT for analog audio mode and IRQ for interrupt operation. The IRQ pin is driven low during normal operation and high for a minimum of 1 ms during the interrupt. The CTS function is always enabled by default and cannot be disabled by the system controller.

For Si4822/26/40/44A ATDD parts, due to finite resolution of the ATDD device internal ADC for tune wheel position sensing, very wide frequency range bands should be broken into smaller range sub-bands such that a sub-band should not contain more than 230 channels. For example, the 64–109 MHz band range should be broken into two smaller bands, one from 64–88 MHz and another from 88–109 MHz. Similarly for SW, the entire 5.6– 22 MHz range must be broken into 8 smaller bands. Furthermore, there two band groups for SW, one is for standard or narrow band frequency while another is for wide band frequency range. Thus, we have a total of 16 SW bands. The extended SW band frequency ranges from 2.3–5.6 MHz and 22–28.5 MHz are not covered in pre-defined bands.Theyare supported only via API and the system controller programming the extended band range.

For Si4827/44B ATDD parts with new firmware that supports the wide FM bands and the wide SW bands, the host controller is allowed to re-configure a wider band range without the 230 channel resolution restriction.

For FM, there are five different band frequency ranges and for each there are two different de-emphasis and stereo separation and RSSI thresholds options. Therefore, there is a total 20 FM bands. For AM, there are 5 different band frequency ranges which support 9 kHz and 10 kHz channel spaces respectively. For SW, we have a total of16 bands, 8 of which are standard narrow ranges while another 8 bands are wider ranges.

Note: To change function (e.g. FM RX to AM RX or vice versa), the system controller needs to reset the ATDD device first and then issue ATDD_POWER_UP with the detected band number and optional band properties.

Table 13. Pre-defined Band Table

Band Index	Band Name	Band Freq Range	De-emphasis (FM) Channel Space (AM)	Stereo Separation* & RSSI Thresholds
0	FM1	87–108 MHz	75 µs	6 dB separation, RSSI = 20
1	FM1	87–108 MHz	75 µs	12 dB separation, RSSI = 28
2	FM1	87–108 MHz	50 µs	6 dB separation, RSSI = 20
3	FM1	87–108 MHz	75 µs	12 dB separation, RSSI = 28
4	FM2	86.5–109 MHz	75 µs	6 dB separation, RSSI = 20
5	FM2	86.5–109 MHz	75 µs	12 dB separation, RSSI = 28
6	FM2	86.5–109 MHz	50 µs	6 dB separation, RSSI = 20
7	FM2	86.5–109 MHz	50 µs	12 dB separation, RSSI = 28
8	FM3	87.3–108.25 MHz	75 µs	6 dB separation, RSSI = 20
9	FM3	87.3–108.25 MHz	75 µs	12 dB separation, RSSI = 28
10	FM3	87.3–108.25 MHz	50 µs	6 dB separation, RSSI = 20
11	FM3	87.3–108.25 MHz	50 µs	12 dB separation, RSSI = 28
12	FM4	76–90 MHz	75 µs	6 dB separation, RSSI = 20
13	FM4	76–90 MHz	75 µs	12 dB separation, RSSI = 28
14	FM4	76–90 MHz	50 µs	6 dB separation, RSSI = 20
15	FM4	76–90 MHz	50 µs	12 dB separation, RSSI = 28
16	FM5	64–87 MHz	75 µs	6 dB separation, RSSI = 20
17	FM5	64–87 MHz	75 µs	12 dB separation, RSSI = 28
18	FM5	64–87 MHz	50 µs	6 dB separation, RSSI = 20
19	FM5	64–87 MHz	50 µs	12 dB separation, RSSI = 28
20	AM1	520–1710 kHz	10 kHz	
21	AM2	522–1620 kHz	9 kHz	
22	AM3	504–1665 kHz	9 kHz	
23	AM4	520–1730 kHz	10 kHz	
24	AM5	510–1750 kHz	10 kHz	
25	SW1	5.6–6.4 MHz		
26	SW2	5.95–6.2 MHz		
***Note:** The Stereo Separation specification is applicable to Si4840/44 FM stereo parts only.				

Table 13. Pre-defined Band Table

Band Index	Band Name	Band Freq Range	De-emphasis (FM) Channel Space (AM)	Stereo Separation* & RSSI Thresholds
27	SW3	6.8–7.6 MHz		
28	SW4	7.1–7.6 MHz		
29	SW5	9.2–10 MHz		
30	SW6	9.2–9.9 MHz		
31	SW7	11.45–12.25 MHz		
32	SW8	11.6–12.2 MHz		
33	SW9	13.4–14.2 MHz		
34	SW10	13.57–13.87 MHz		
35	SW11	15–15.9 MHz		
36	SW12	15.1–15.8 MHz		
37	SW13	17.1–18 MHz		
38	SW14	17.48–17.9 MHz		
39	SW15	21.2–22 MHz		
40	SW16	21.45–21.85 MHz		
***Note:** The Stereo Separation specification is applicable to Si4840/44 FM stereo parts only.				

Command arguments: Minimum one and optionally seven

Response bytes: One

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	0	1
ARG1	XOSCEN	XOWAIT	BANDIDX					
ARG2	BANDBOT[15:8]							
ARG3	BANDBOT[7:0]							
ARG4	BANDTOP[15:8]							
ARG5	BANDTOP[7:0]							
ARG6	CHSPC							
ARG7*	TVFREQ	UNI_AM	DFBAND	0	0	0	0	0
***Note:** Additional command argument ARG7 is supported by Si4827/44B parts only.								

ARG	Bit	Name	Function
1	7	XOSCEN	**Crystal Oscillator Enable.** 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (XTALI and XTALO with external 32.768 kHz crystal). See Si484x Data Sheet Application Schematic for external BOM details.
1	6	XOWAIT	**Crystal Oscillator Stabilization Wait Time after Reset.** 0 = 600 ms (for typical crystal) 1 = 900 ms (for crystal requires extra stabilization time) ***Note:** Applicable to Si4822/26/40/44A parts only. Later Si4827/44B parts don't care this bit and will wait till crystal oscillation is stable unconditionally.
1	5:0	BANDIDX	**Band Index to Set.**[1] 0~19: FM band number range 20~24: AM band number range 25~40: SW band number range
2:3	15:0	BANDBOT[2,4]	**Band Bottom Frequency Limit.** FM 6400..10900 (64.0–109.0 MHz) AM 510..1750 (510–1750 kHz) SW 2300..28500 (2.3–28.5 MHz)
4:5	15:0	BANDTOP[2,4]	**Band Top Frequency Limit.** FM 6400..10900 (64.0–109.0 MHz) AM 510..1750 (510–1750 kHz) SW 2300..28500 (2.3–28.5 MHz)
6	7:0	CHSPC[2,3]	**Channel Spacing.** FM 10 (i.e.,100 kHz) AM 9 or 10 (i.e., 9 kHz or 10 kHz) SW 5 (i.e., 5 kHz)
7	7	TVFREQ[4]	**TV Audio Channel Frequency Display.** 0 = Disable TV audio channel frequency display format 1 = Enable TV audio channel frequency display format ***Note:** Applicable to Si4827 and Si4844B parts and FMRX mode only
7	6	UNI_AM[4]	**Universal AM Band.** 0 = Disable universal AM band (default AFC range of 1.1kHz) 1 = Enable universal AM band (wider AFC range in tuning) ***Note:** Applicable to Si4827 and Si4844B parts and AMRX mode only
7	5	DFBAND[4]	**Default Band Settings.** 0 = Allow host controller to override the band property settings 1 = Force to use tuner default band property settings ***Note:** Applicable to Si4827 part only

Notes:

1. The band index to set for the ATDD Device band detection case needs to be consistent with the band index detected by the device (i.e., band index read from ATDD_GET_STATUS command when INFORDY bit is set).
2. The band bottom, top, and channel spacing arguments are optional and can be omitted if the system controller doesn't need to override the corresponding default band properties. However, if the ATDD Device pin 1 has been pulled up by the resistor, it is forced to use default band properties. The system controller optionally specified band properties will be ignored and have no effects.
3. The channel spacing is configurable for the AM band mode only. The system controller can select between 9 (9 kHz) and 10 (10 kHz) channel space. For FM and SW band modes, the value should be set to 10 (100 kHz) and 5 (5 kHz) respectively.
4. The system controller can re-program the band frequency limits, i.e. BANDBOT and BANDTOP, of a band to override the default values.
   For Si4822/26/40/44A ATDD parts, the programmed values must satisfy the following requirements for proper tuning operation:
   - BANDBOT needs to be a multiple of CHSPC; i.e., exactly dividable by the channel spacing.
   - (BANDTOP – BANDBOT)/(CHSPC) must be in 50…230 range
   - When programming the BANDTOP value, the system controller is required to add extra margin to guarantee the band top frequency can be reached.
     FM: 70 kHz (value of 7) margin is required
     AM: 6 kHz (value of 6) margin is required
     SW: 4 kHz (value of 4) margin is required
   - For example, to program the customized AM band from 510–1750 kHz of the total 125 channels, the values set for BANDBOT is 510 and BANDTOP is (1750+6) which is 1756.

   For later Si4827/44B ATDD parts that support wide FM and wide SW bands, the system controller is allowed to set BANDBOT and BANDTOP for the maximum band range without restrictions. The system controller is no longer required to reserve an extra margin when programming the BANDTOP, etc.
   - BANDBOT and BANDBOT need to be multiple of CHSPC; i.e., exact dividable by the channel spacing.
5. ARG7 is supported by Si4827/44B parts only. System controller is optional to send this argument in the ATDD_POWER_UP command if advanced features are needed.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR			ERRCODE			

Command 0xE2. ATDD_AUDIO_MODE

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	0	0	0	1	0
ARG1	OPCODE	Reserved			SWADJ_ATTN	Reserved		

ARG	Bit	Name	Function
1	7	OPCODE	**Operation Code.** 0 = Set audio mode settings 1 = Get current audio mode settings without setting
1	3	ADJPT_ATTN	**Shortwave (SW) Adjacent Tune Wheel Positions Audio Attenuation Option.** Audio attention of adjacent tune wheel positions of a station: 0 = (–2 dB, –0 dB, –2 dB) i.e., adjacent points volume levels –2 dB (default) 1 = (–0 dB, –0 dB, –0 dB) i.e., adjacent points same volume levels ***Note:** This bit is not applicable to wide SW bands (i.e., SW band range > 1.5 MHz), which are supported by Si4827/44B parts. For wide SW bands, all adjacent points will have the same volume level.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR			SWADJ_ATTN			

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision, and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in power up mode.

Command arguments: None

Response bytes: Eight

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	Reserved							
RESP5	Reserved							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	Final 2 digits of Part Number (HEX).
2	7:0	FWMAJOR	Firmware Major Revision (ASCII).
3	7:0	FWMINOR	Firmware Minor Revision (ASCII).
6	7:0	CMPMAJOR	Component Major Revision (ASCII).
7	7:0	CMPMINOR	Component Minor Revision (ASCII).
8	7:0	CHIPREV	Chip Revision (ASCII).

Command 0x11. POWER_DOWN

Moves the device from power up to power down mode. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode. Note that only the ATDD_POWER_UP and ATDD_GET_STATUS commands are accepted in power down mode. If the system controller writes a command other than the two commands when in power down mode, the device does not respond. The device will only respond when an ATDD_POWER_UP command is written. GPO pins are powered down and not active during this state.

Note: The following describes the state of all the pins when in powerdown mode: ROUT, LOUT = HiZ

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					

Command 0x12. SET_PROPERTY

Sets a property shown in Table 10, “AM/SW Receiver Command Summary,” on page 34. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode.

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify
3	7:0	$PROP_L$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify
4	7:0	$PROPD_H$	**Property Value High Byte.** This byte in combination with $PROPD_L$ is used to specify the property to modify
5	7:0	$PROPD_L$	**Property Value Low Byte.** This byte in combination with $PROPD_H$ is used to specify the property to modify

Command 0x13. GET_PROPERTY

Gets a property as shown in Table 10, “AM/SW Receiver Command Summary,” on page 34. The CTS bit is set when it is safe to send the next command. This command may only be sent when in power up mode.

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get
3	7:0	$PROP_L$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	Reserved					
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPD_H$[7:0]							
RESP3	$PROPD_L$[7:0]							

RESP	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROPD_H$	**Property Value High Byte.** This byte in combination with $PROPD_L$ represents the requested property value.
3	7:0	$PROPD_L$	**Property Value Low Byte.** This byte in combination with $PROPD_H$ represents the requested property value.

7.2.2. AM/SW Receiver Properties

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 ±5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an reference clock at XTALI pin of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. Reference clock frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these reference clock gaps.

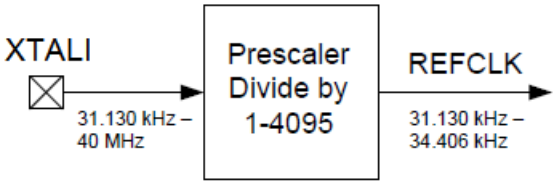


Figure 7. REFCLK Prescaler

Table 14. XTLI Reference Clock Frequency Gaps

Prescaler	XTALI Low (Hz)	XTALI High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before resetting and be valid at all times for proper tuning and AFC operations. XTALI reference clock input frequency could be changed but is not recommended and REFCLK properties values need to be reconfigured accordingly. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 32768 Hz.

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130-34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:2	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768±5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external reference clock frequency down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an XTALI reference clock of 13 MHz would require a prescaler value of 400 to divide it to 3250 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The reference clock must be valid 10 ns before the chip reset signal. In addition, the reference clock must be valid at all times for proper tuning and AFC operations. XTALI reference clock input frequency could be changed but is not recommended and REFCLK properties values need to be reconfigured accordingly. The CTS bit (and optional interrupt) is set when it is safe to send the next command.

This property may only be set or read when in powerup mode. The default is 1.

Default: 0x0001

Step: 1

Range: 1-4095.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK SEL	REFCLK[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = Reserved
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide clock frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x4000. RX_VOLUME

Sets the audio output volume. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 63.

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	VOL	**Output Volume.** Sets the output volume level

Property 0x4001. RX_HARD_MUTE

Mutes the audio output. L and R audio outputs may be muted independently. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is unmute (0x0000).

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LMUTE	RMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LMUTE	**Left Mute.** Mutes L Audio Output.
0	RMUTE	**Right Mute.** Mutes R Audio Output.

Property 0x4002. RX_BASS_TREBLE

Sets the audio output bass/treble effect. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 3.

Unlike the FM bass/treble effect, the AM/SW bass/treble effect is achieved by setting different channel filters, i.e., narrow or wide, to allow less or more high frequency audio components to the user. Thus the actual maximum volume level is unaffected by the bass/treble level set.

Default: 0x0003

Step: 1

Range: 1–7

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	BASSTREBLE[4:0]				

Bit	Name	Function
15:5	Reserved	Always write to 0.
4:0	BASSTREBLE	**Bass/Treble level** Sets the output bass/treble effect level: 1- 1.0 kHz channel filter 2- 1.8 kHz channel filter 3- 2.0 kHz z channel filter (default) 4- 2.5 kHz Channel filter 5- 2.828 kHz Channel filter 6- 4.0 kHz Channel filter 7- 6.0 kHz Channel filter
***Note:** : Unlike FM, there are a total of seven different channel filters for AM/SW mode and thus there are only seven bass/ treble effects for AM and SW.		

Property 0x4003. RX_ACTUAL_VOLUME

Reads only what reflects the actual digital audio output volume in use. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 63.

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	ACT_VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	ACT_VOL	**Actual Volume.** Actual volume ranges from 0~63

Property 0x3300. AM_SOFT_MUTE_RATE

Sets the attack and decay rates when entering or leaving soft mute. The value specified is multiplied by 4.35 dB/s to come up with the actual attack rate. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default rate is 278 dB/s.

Default: 0x0040

Actual Rate: SMRATE x 4.35

Units: dB/s

Step: 1

Range: 1–255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SMRATE[15:0]															

Bit	Name	Function
15:0	SMRATE	**AM Soft Mute Rate.** Determines how quickly the AM goes into soft mute when soft mute is enabled. The actual rate is calculated by taking the value written to the field and multiplying it with 4.35 dB/s. The default rate is 278 dB/s (SMRATE[15:0] = 0x0040).

Property 0x3301. AM_SOFT_MUTE_SLOPE

Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Soft mute attenuation is the minimum of SMSLOPE x (SMTHR – SNR) and SMATTN. The recommended SMSLOPE value is CEILING(SMATTN/SMTHR). SMATTN and SMTHR are set via the AM_SOFT_MUTE_MAX_ATTENUATION and AM_SOFT_MUTE_SNR_THRESHOLD properties. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default slope is 2 dB/dB.

Default: 0x0001

Units: dB/dB

Range: 1–5

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	SMSLOPE[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	SMSLOPE	**AM Slope Mute Attenuation Slope.** Set soft mute attenuation slope in dB attenuation per dB SNR below the soft mute SNR threshold.

Property 0x3302. AM_SOFT_MUTE_MAX_ATTENUATION

Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default attenuation is 16 dB.

Default: 0x0010

Units: dB

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	SMATTN[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	SMATTN	**AM Soft Mute Max Attenuation.** Maximum attenuation to apply when in soft mute. Specified in units of dB. Default maximum attenuation is 16 dB.

Property 0x3303. AM_SOFT_MUTE_SNR_THRESHOLD

Sets the SNR threshold to engage soft mute. Whenever the SNR for a tuned frequency drops below this threshold the AM reception will go in soft mute, provided soft mute max attenuation property is non-zero. The CTS bit is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default SNR threshold is 8.

Default: 0x0008

Units: dB

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	SMTHR[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	SMTHR	**AM Soft Mute SNR Threshold.** The SNR threshold for a tuned frequency below which soft mute is engaged provided the value written to the AM_SOFT_MUTE_MAX_ATTENUATION property is not zero. Default SNR threshold is 8 dB.

8. Control Interface

Unlike the Si47xx DTDD devices, the ATDD devices support only the 2-wire bus mode interface. To enable the 2-wire bus mode interface, the IRQ pin must keep low during reset and keep at least 500 µs after the rising edge of reset. The IRQ pin includes a 45 kΩ internal pull-down resistor; therefore, leaving this pin floating is acceptable, but do NOT pull-up this pin externally. (Neither with external pull-up resistor nor pull-up option of the system controller pin connecting to IRQ).

When the radio function is not required, the system controller is advised to set the RSTb pin low to place the device in reset mode. In reset mode, all circuitry is disabled including the device control interface; registers are set to their default settings, and the control bus is disabled.

To enable the radio function, the system controller is required to release the RSTb pin from low to high. Unlike the Si47xx DTDD device, the ATDD device boots autonomously and comes to an active waiting state instead staying at power down mode and waiting for POWER_UP command from the system controller. Only two commands are accepted in this active waiting state:

1. ATDD_POWER_UP command 0xE1
2. ATDD_GET_STATE command 0xE0

The device comes out of the active waiting state when the ATDD_POWER_UP command is written to the command register. Once in power up mode, the device accepts additional commands, such as getting status to update the tune frequency display and the setting of properties, such as bass/treble level. The device will not accept other commands while in the active waiting state

8.1. 2-Wire Bus Mode Control Interface

Figures 8 and 9 show the 2-wire Bus Mode Control Interface Read and Write Timing Parameters and Diagrams, respectively. Refer to the Si484x data sheet for timing parameter values.

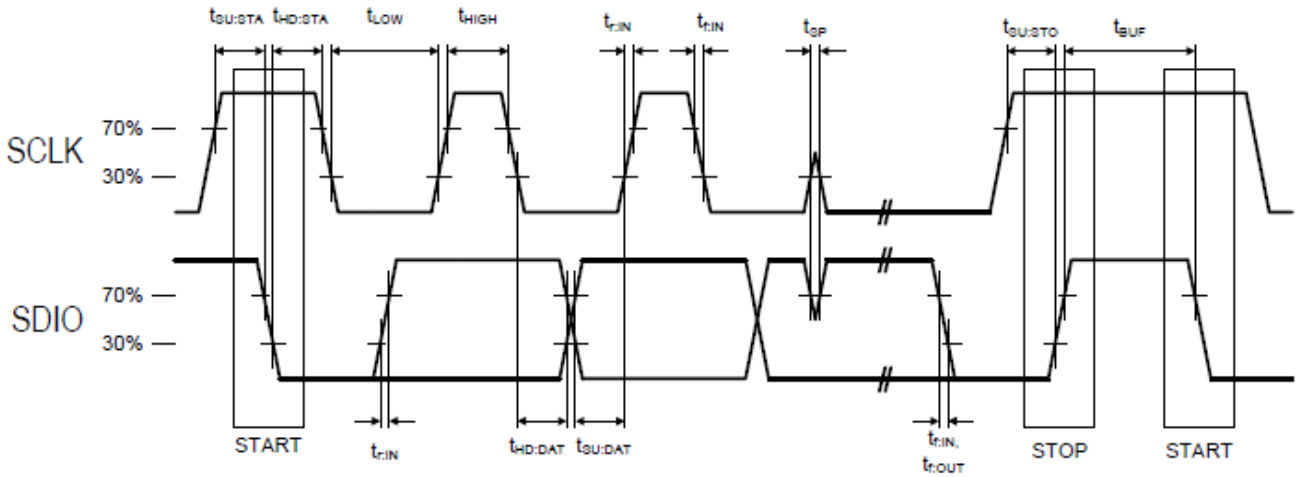


Figure 8. 2-wire Control Interface Read and Write Timing Parameters

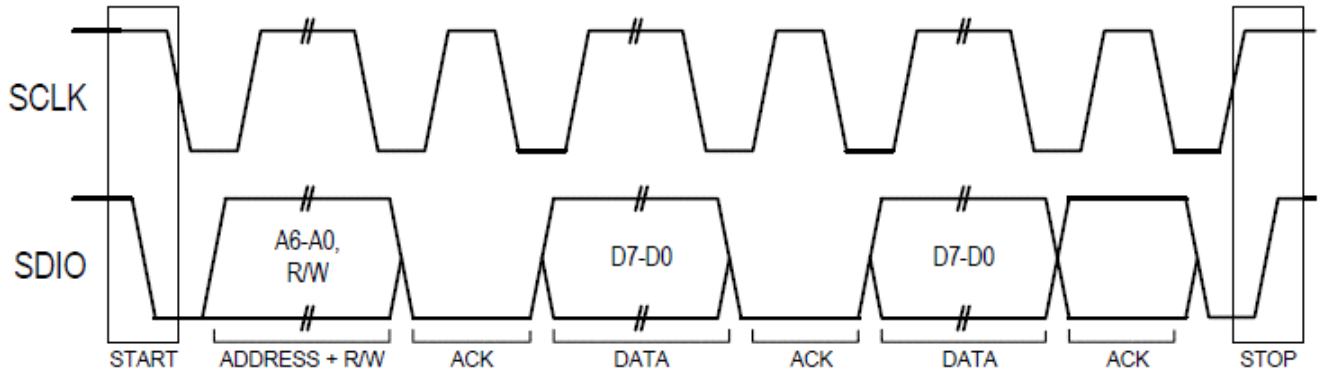


Figure 9. 2-wire Control Interface Read and Write Timing Diagram

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the system controller drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven-bit device address followed by a read/write bit (read = 1, write = 0). The device acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

The seven-bit device address of the ATDD device is fixed to 0010001b. Unlike the Si47xx DTDD devices, the device address is non-configurable.

For write operations, the system controller next sends a data byte on SDIO, which is captured by the device on rising edges of SCLK. The device acknowledges each data byte by driving SDIO low for one cycle on the next falling edge of SCLK. The system controller may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments. Writing more than 8 bytes results in unpredictable device behavior.

For read operations, after the device has acknowledged the control byte, it will drive an eight-bit data byte on SDIO, changing the state of SDIO on the falling edges of SCLK. The system controller acknowledges each data byte by driving SDIO low for one cycle on the next falling edge of SCLK. If a data byte is not acknowledged by the system controller, the transaction will end. The system controller may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the status byte and response data from the device.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

Table 15 demonstrates the command and response procedure implemented in the system controller to use the 2-wire bus mode. In this example the ATDD_POWER_UP command is demonstrated.

Table 15. Command and Response Procedure 2-Wire Bus Mode

Action	Data	Description
CMD	0xE1	ATDD_POWER_UP
ARG1	0x80	Band index = 0 (i.e., FM1), Enable crystal, typical crystal waiting time
ARG2	0x22	Set band bottom frequency to 88 MHz
ARG3	0x60	e.g. 0x2260 → 8800 (in 10 kHz unit)
ARG4	0x2A	Set band top frequency to 108 MHz
ARG5	0x30	e.g. 0x2A30 → 10800 (in 10 kHz unit)
ARG6	0x0A	Set channel spacing to 100 kHz (10 kHz unit)
STATUS	→0x80	Reply Status. Clear-to-send high

To send the ATDD_POWER_UP command and arguments, the system controller sends the START condition, followed by the 8-bit control word, which consists of a seven-bit device address (0010001b) and the write bit (0b) indicated by ADDR+W = 00100010b = 0x22. The device acknowledges the control word by setting SDIO = 0, indicated by ACK = 0. The system controller then sends the CMD byte, 0xE1, and again the device acknowledges by setting ACK = 0. The system controller and device repeat this process for the ARG1, ARG2, ARG3, ARG4, ARG5, and ARG6 bytes. Commands may take up to seven argument bytes, and this flexibility should be designed into the 2-wire bus mode implementation. Alternatively, all seven argument bytes may be sent for all commands, but unusual arguments must be 0x00. Unpredictable device behavior will result if more than seven arguments are sent.

START	ADDR+W	ACK	CMD	ACK	ARG1	ACK	…	ARG6	ACK	STOP
START	0x22	0	0xE1	0	0x080	0	…	0x0A	0	STOP

To read the status and response from the device, the system controller sends the START condition, followed by the eight-bit control word, which consists of the seven bit device address and the read bit (1b) (i.e., the write control word is ADDR+R = 00100011b = 0x23). The device acknowledges the control word by setting ACK = 0. Next the system controller reads the STATUS byte. In this example, the STATUS byte is 0x00, indicating that the CTS bit, bit 8, has not been set. The response bytes are not ready for reading and that the device is not ready to accept another command. The system controller sets SDIO = 1, indicated by NACK = 1, to signal to the device the 2-wire transfer will end. The system controller should set the STOP condition. This process is repeated until the STATUS byte indicates that CTS bit is set, 0x80 in this example.

START	ADDR+R	ACK	STATUS	NACK	STOP
START	0x23	0	0x00	1	STOP

When the STATUS byte returns CTS bit set, 0x80 in this example, the system controller may read the response bytes from the device. The controller sets ACK = 0 to indicate to the device that additional bytes will be read. The RESP1 byte is read by the system controller, followed by the system controller setting ACK = 0. This is repeated for RESP2. RESP3 is read by the system controller followed by the system controller setting NACK = 1, indicating that RESP3 is the last byte to be read. The system controller then sets the STOP condition. Responses may be up to 15 bytes in length (RESP1–RESP15) depending on the command. It is acceptable to read all 15 response bytes. However, unused response bytes return random data and must be ignored. Note that the ATDD_POWER_UP command returns only the STATUS byte and response bytes are shown only for completeness.

START	ADDR+R	STATUS	ACK	RESP1	ACK	RESP2	ACK	RESP3	NACK	STOP
START	0x23	0x80	0	0x00	0	0x00	0	0x00	1	STOP

9. Powerup

This section describes the procedure for booting the ATDD device to move it from power off mode (reset state) to the power up mode. The first and most common procedure is a boot from internal device memory.

To power up the device:

1. Supply VDD and VIO while keeping the RSTb = 0.
   The minimum VDD and VIO rise time is 25 µs, and VDD and VIO must be stable 250 µs before setting RSTb = 1.
   Power supplies may be sequenced in any order.
   RSTb is in the VIO supply domain and therefore RSTb = 0 must be maintained before VIO is supplied.
2. Set RSTb = 1.
3. Wait till IRQ pin goes high and write ATDD_POWER_UP command to the command register.
4. The ATDD_POWER_UP command instructs the device to boot from internal memory and load the corresponding FM or AM/SW function to the given band index specified in the command argument. After CTS = 1, the device is ready to commence normal operation and accept additional commands.
5. Provide RCLK. Note that the RCLK buffer is in the VIO supply domain and may therefore be supplied at any time after VIO is supplied.

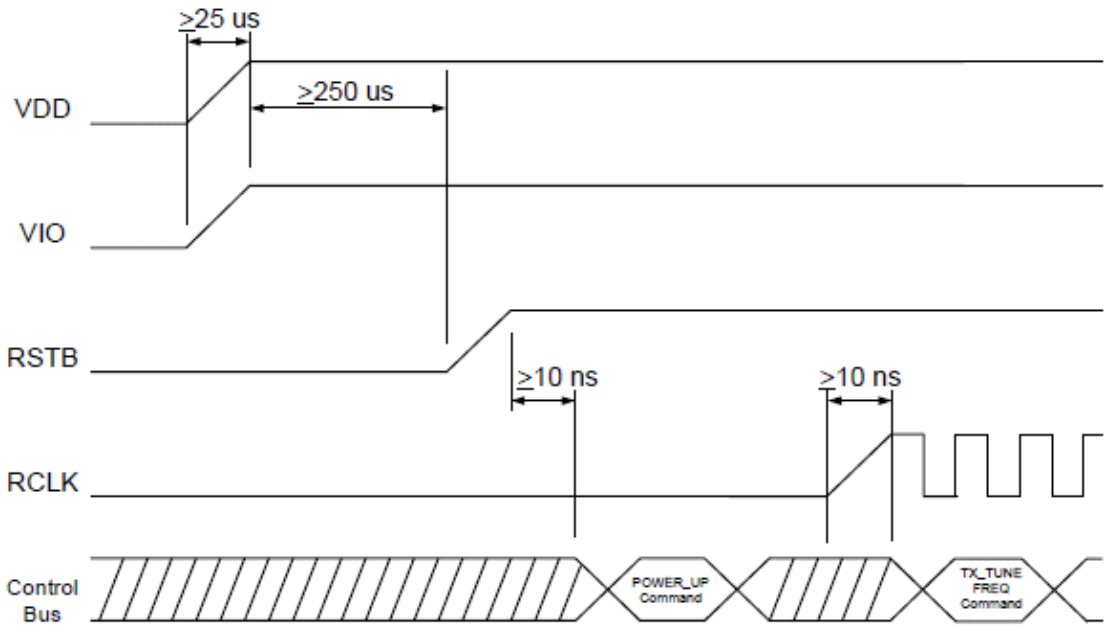


Figure 10. Device Powerup Timing

10. Powerdown

The procedure for moving the ATDD device from power up to power down (reset state) modes requires writing the POWER_DOWN command.

Table 16. Using the POWER_DOWN Command

Action	Data	Description
CMD	0x11	POWER_DOWN
STATUS	→0x80	Reply Status. Clear-to-send high

To power down the device and remove VDD and VIO (optional):

1. Set RCLK = 0 (optional).
2. Write POWER_DOWN to the command register. Note that all register contents will be lost.
3. Set RSTb = 0. Note that RSTb must be held high for 10 ns after the completion of the POWER_DOWN command.
4. Remove VDD (optional).
5. Remove VIO (optional). Note that VIO must not be removed without removing VDD. **Unexpected device operation may result.**

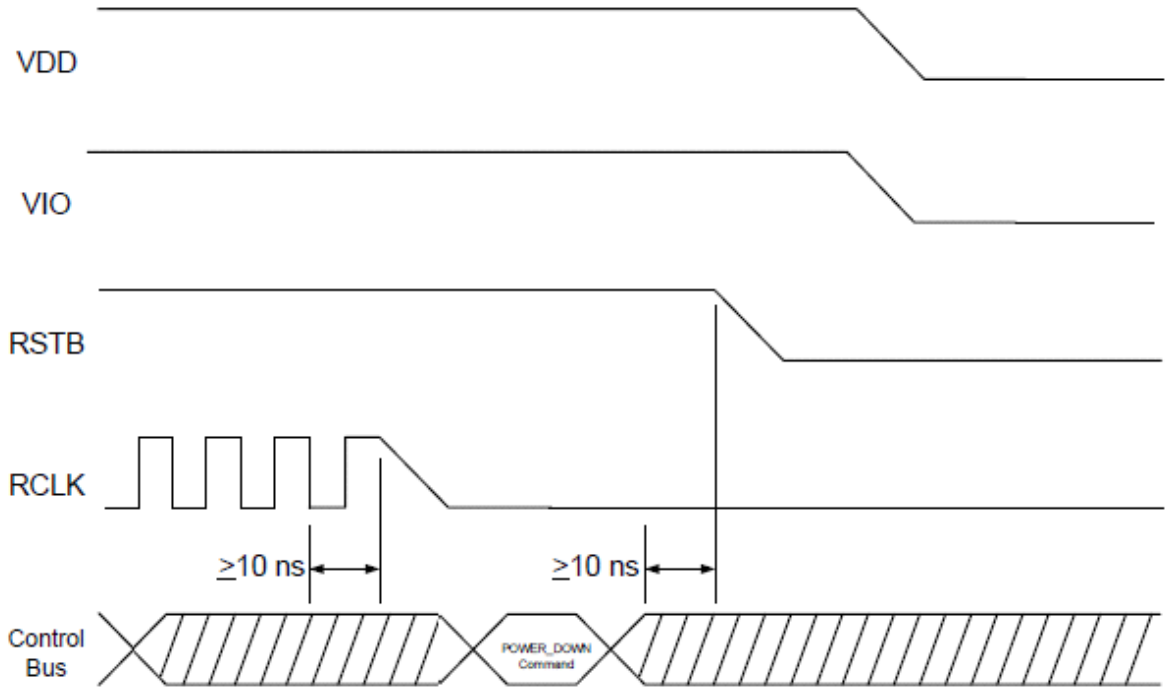


Figure 11. Powerdown Timing

11. Programming Example

This section contains the programming examples for each of the functions, FM Receive and AM/SW Receive. Before each example, an overview of how to program the device is shown as a flowchart. Silicon Labs also provides the actual software (example code), which can be downloaded from mysilabs.com.

The following flowchart is an overview of how to program the FM and AM/SW Receivers:

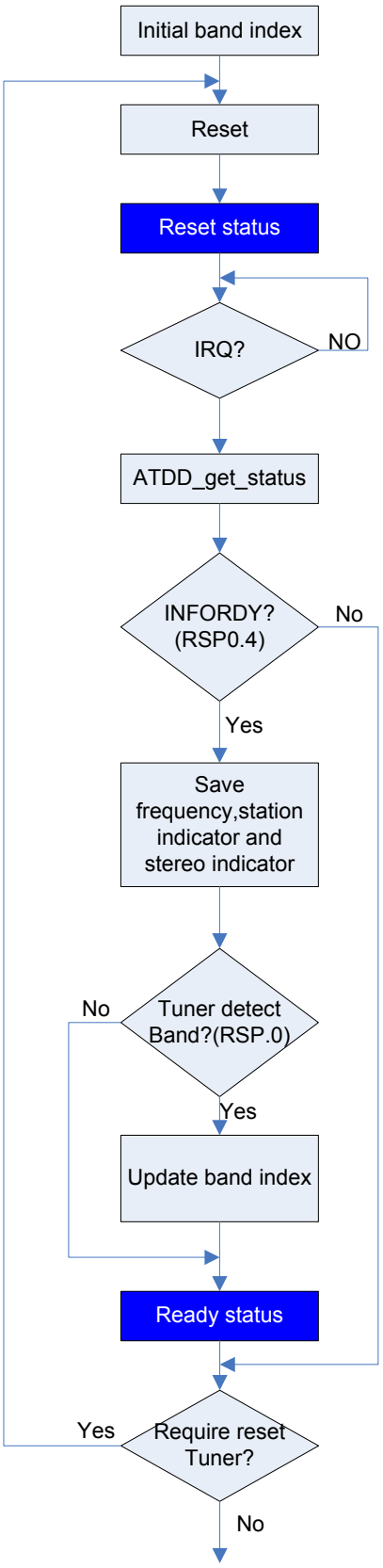


Figure 12a. FM and AM/SW Receiver Programming Example Flowchart

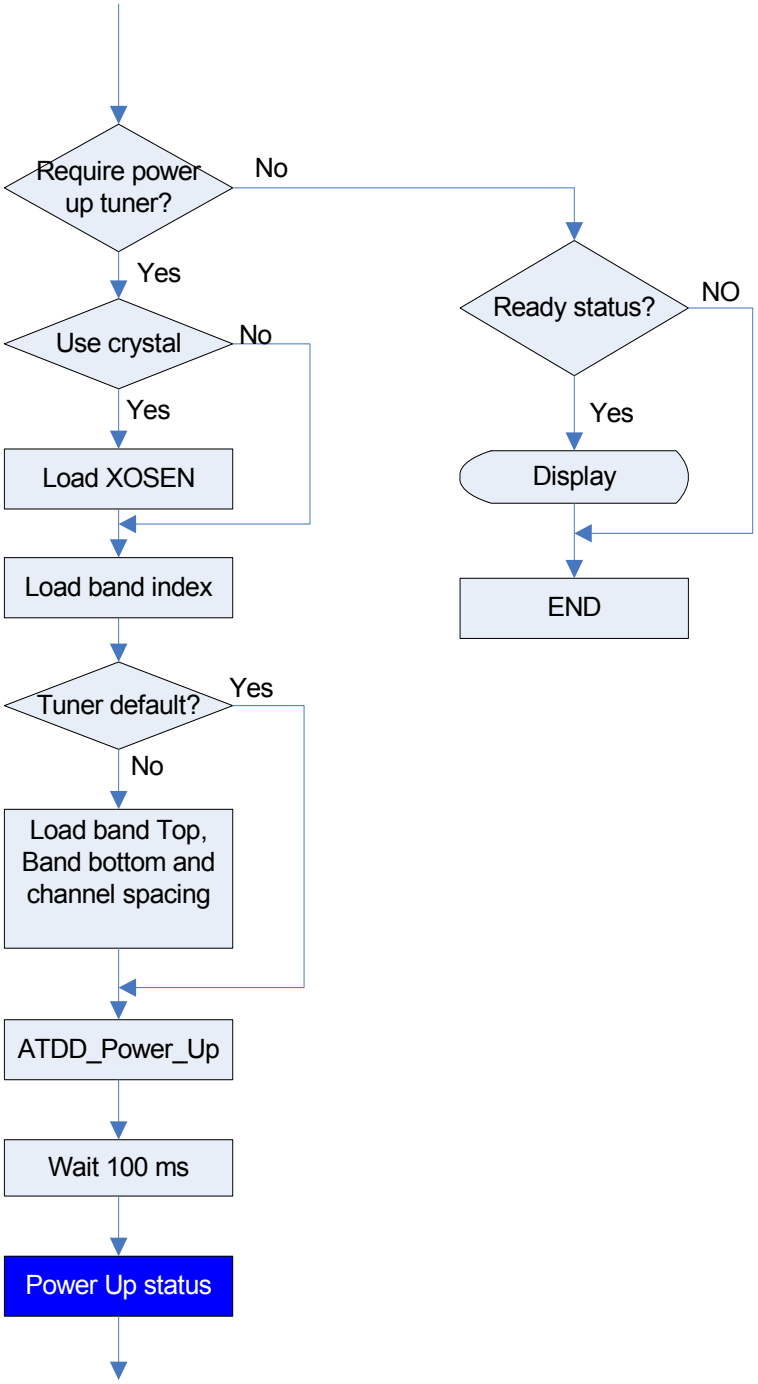


Figure 12b. FM and AM/SW Receiver Programming Example Flowchart

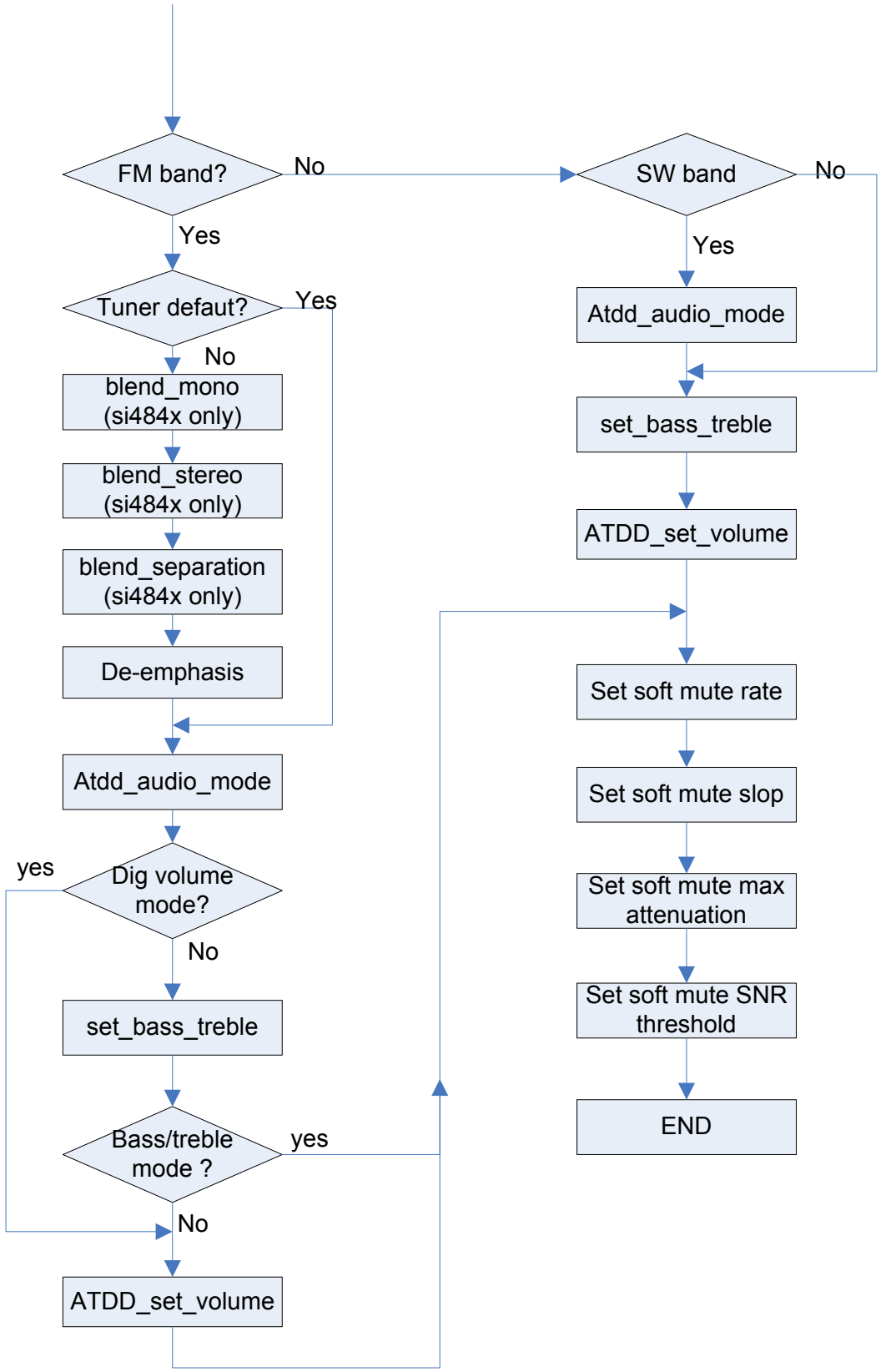


Figure 9c. FM and AM/SW Receiver Programming Example Flowchart

11.1. Programming Example for the FM Receiver

Table 17 provides an example for the FM Receiver. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

In some cases the default properties may be acceptable and no modification is necessary. Refer to Section “7. Commands and Properties” for the full description of each command and property.

Table 17. Programming Example for the FM Receiver

Action	Data	Description
Power up in Analog Mode		
CMD	0xE1	ATDD_POWER_UP
ARG1	0xC0	Band index = 0 (i.e., FM1), Enable crystal, typical crystal waiting time
ARG2	0x22	Set band bottom frequency to 88 MHz
ARG3	0x60	e.g. 0x2260 → 8800 (in 10 kHz unit)
ARG4	0x2A	Set band top frequency to 108 MHz
ARG5	0x30	e.g. 0x2A30 → 10800 (in 10 kHz unit)
ARG6	0x0A	Set channel spacing to 100 kHz (10 kHz unit)
STATUS	→0x80	Reply Status. Clear-to-send high
Configurations		
CMD	0xE2	ATDD_AUDIO_MODE
ARG1	0x00	Set audio mode to digital volume mode ADJPT_STEO: Adj. points enable stereo ADJPT_ATTN: Adj. points audio attenuated
STATUS	→0x80	FM_MONO: Set stereo audio output (Si484x only) Reply Status. CTS: Clear-to-send high AUDIOMODE: current mode is 0 ADJPT_STEO: Adj. points enable stereo ADJPT_ATTN: Adj. points audio attenuated FM_MONO: Stereo audio output (Si484x only)
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_VOLUME
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Output Volume = 63
ARG5 (PROPD)	0x3F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x11	FM_DEEMPHASIS
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	50 µs
ARG5 (PROPD)	0x01	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 17. Programming Example for the FM Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_BASS_TREBLE
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Bass/treble level = 4 (normal)
ARG5 (PROPD)	0x04	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY (Si484x only)
ARG1	0x00	
ARG2 (PROP)	0x18	FM_BLEND_RSSI_STEREO_THRESHOLD
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Threshold = 49 dBµV = 0x0031
ARG5 (PROPD)	0x31	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY (Si484x only)
ARG1	0x00	
ARG2 (PROP)	0x18	FM_BLEND_RSSI_MONO_THRESHOLD
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Threshold = 30 dBµV = 0x001E
ARG5 (PROPD)	0x1E	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x13	FM_SOFT_MUTE_MAX_ATTENUATION
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Attenuation = 10 dB = 0x000A
ARG5 (PROPD)	0x0A	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x13	FM_SOFT_MUTE_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Threshold = 6 dB = 0x0006
ARG5 (PROPD)	0x06	
STATUS	→0x80	Reply Status. Clear-to-send high.
Status Display (wait for ATDD device IRQ)		

Table 17. Programming Example for the FM Receiver (Continued)

Action	Data	Description
CMD	0xE0	ATDD_GET_STATUS
STATUS	→0xAC	Reply Status: CTS: Clear-to-send high HOSTREST: Host reset not needed HOSTPWRUP: Host power up not needed INFORDY: Information ready STATION: Station qualified STEREO: Stereo on (Si484x only) BCFG: ATDD device detects band
RESP1	→0x00	BANDMODE: FM band mode detected BANDIDX: Band index detected = FM1(0)
RESP2	→0x09	CHFREQ: Channel frequency = 98.1 MHz
RESP3	→0x81	
Power Down		
CMD	0x11	POWER_DOWN
STATUS	→0x81	Reply Status. Clear-to-send high.

The device sets the CTS bit to indicate that it is ready to accept the next command. The CTS bit also indicates that the ATDD_POWER_UP, GET_REV, POWER_DOWN, and GET_PROPERTY commands have completed execution.

11.2. Programming Example for the AM/SW Receiver

Table 18 provides a programming example for the AM/SW Receiver. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

In some cases, the default properties may be acceptable and no modification is necessary. Refer to “7. Commands and Properties” for a full description of each command and property.

Table 18. Programming Example for the AM/SW Receiver

Action	Data	Description
Power up in Analog Mode		
CMD ARG1 ARG2 ARG3 ARG4 ARG5 ARG6 STATUS	0xE1 0x94 0x00 0x00 0x00 0x00 0x0A →0x80	ATDD_POWER_UP Band index = 20 (i.e., AM1), Enable crystal, typical crystal waiting time Keep default band bottom frequency Keep default band top frequency Set channel spacing to 10 kHz Reply Status. Clear-to-send high
Configurations		
CMD ARG1 STATUS	0xE2 0x08 →0x88	ATDD_AUDIO_MODE Set SWADJ_ATTN=1 {-0, -0, -0} dB for SW audio profile Reply Status CTS: Clear-to-send high SWADJ_ATTN=1
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x40 0x02 0x00 0x06 →0x80	SET_PROPERTY RX_BASS_TREBLE Bass/treble level = 6 (4 kHz channel filter) Reply Status. Clear-to-send high.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x40 0x00 0x00 0x3F →0x80	SET_PROPERTY RX_VOLUME Output Volume = 63 Reply Status. Clear-to-send high.

Table 18. Programming Example for the AM/SW Receiver (Continued)

Action	Data	Description
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x33 0x02 0x00 0x0A →0x80	SET_PROPERTY AM_SOFT_MUTE_MAX_ATTENU-ATION 10 dB attenuation = 0x0A Reply Status. Clear-to-send high.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x33 0x03 0x00 0x09 →0x80	SET_PROPERTY AM_SOFT_MUTE_SNR_THRESH-OLD 9 dB = 0x09 Reply Status. Clear-to-send high.
Status Display (wait for ATDD device IRQ)		
CMD STATUS RESP1 RESP2 RESP3	0xE0 →0xA9 →0x54 →0x10 →0x00	ATDD_GET_STATUS Reply Status: CTS: Clear-to-send high HOSTREST: Host reset not needed HOSTPWRUP: Host power up not needed INFORDY: Information ready STATION: Station qualified STEREO: (Not applicable for AM) BCFG: ATDD device detects band BANDMODE: AM band mode detected BANDIDX: Band index detected = AM1(20) CHFREQ: Channel frequency = 1000 kHz
Power Down		
CMD STATUS	0x11 →0x81	POWER_DOWN Reply Status. Clear-to-send high.

The device sets the CTS bit to indicate that it is ready to accept the next command. The CTS bit also indicates that the ATDD_POWER_UP, GET_REV, POWER_DOWN, and GET_PROPERTY commands have completed execution.

11.3. Band Switching Between Two AM Bands with Different Channel Spacing

For order Si48422/26/40/44A ATDD parts, when band switching between two AM bands with similar band bottom/top frequencies but with different channel spacing, the frequency display may not be updated after the band is switched. However, the display will be updated with any subsequent tuning after the band switching. This inconsistency can be completely eliminated with the host MCU firmware.

The ATDD device has four possible application circuit configurations depending on whether (1) the host MCU or tuner selects the band and (2) whether the MCU sets the band properties or the default band properties are used. The following describes the ways for the host MCU firmware to handle the band switching case between two or more AM bands for each of the circuit configurations:

1. Host MCU Selects Radio Band and Sets Band Properties
   For customers using this configuration, the host MCU is required to specify the AM channel spacing associated with the ATDD_POWER_UP command sent.
2. Host MCU Selects Default Band and Uses Default Band Properties
   For customers using this configuration, the host MCU is required to reset the tuner IC first, wait for it to be ready, and then re-power up the tuner IC when switching from one AM band to another.
3. Tuner Slide Switch Selects Band and MCU Re-defines Band Properties
   For customers using this configuration, when the host MCU receives an IRQ from tuner and the reply from the ATDD_GET_STATUS command is requesting to power up another AM band (i.e., STATUS byte HOSTPWRUP bit is set, RSP1 byte BANDMODE is still AM, and BANDIDX is another AM band), the host MCU is required to specify the AM channel spacing associated with the ATDD_POWER_UP command sent.
4. Tuner Slide Switch Selects Band and Uses Default Band Properties
   For customers using this configuration, when the host MCU receives an IRQ from tuner and the reply from the ATDD_GET_STATUS command is requesting to power up another AM band (i.e., STATUS byte HOSTPWRUP bit is set, RSP1 byte BANDMODE is still AM, and BANDIDX is another AM band), the host MCU is required to reset the tuner IC first, wait for it to be ready, and then re-power up the tuner IC.

***Note:** Refer to “AN602: Si4822/26/27/40/44 Antenna, Schematic, Layout, and Design Guidelines” for details on Si4822/26/27/40/44 application circuit configurations.

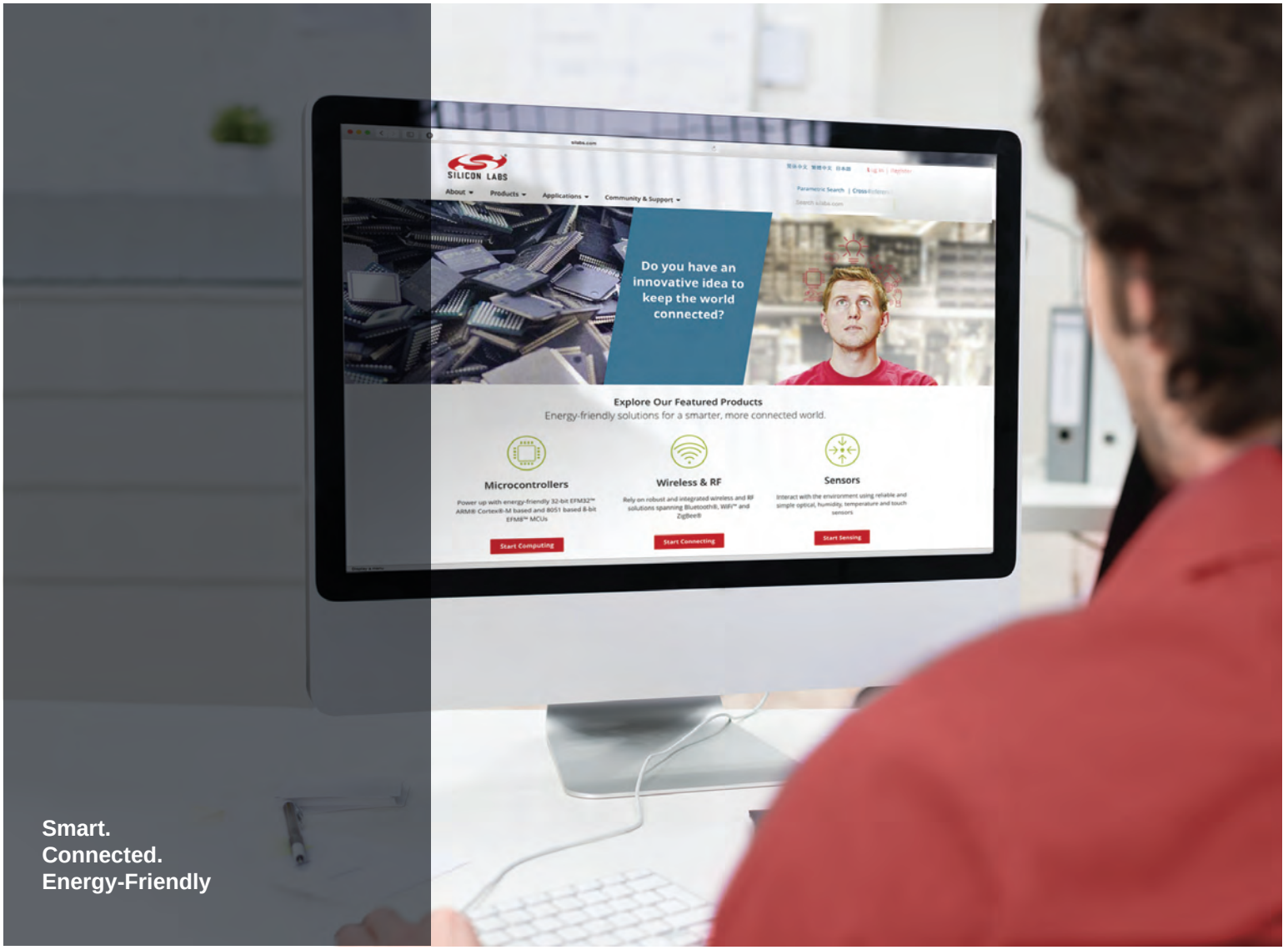
Document Change List

Revision 0.1 to Revision 0.2

- Added Si4822/26 FM/AM/SW Mono Receiver support.
- Added note for proper host power up I^2C speed requirement.

Revision 0.2 to Revision 0.3

- Added Si4827/44B FM/AM/SW Receiver support.
- Pre-defined band table 50 µs/75 µs FM de-emphasis definition correction.
- Updated note for host power up I^2C clock speed > 10 kHz.
- Add support of new properties 0x0201 and 0x0202 Reference Clock Frequency settings.
- Added notes for wide FM bands, wide SW bands, universal AM band and China TV audio channel new features.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com