CLEAR LOGIC

LIBERATOR
CL1K30

Key Features

- Fully Compatible to the Altera® ACEX® 1K Family
- Prototype Your System With Altera FPGAs
- Seamlessly Migrate Production To Clear Logic
- No ASIC Engineering, No NRE, And No Test Vector Development
- Very Fast, Dense Signal Routing Using Vertical Link Interconnect
- "Gate Array" Option Eliminates Configuration EPROMs
- Fabricated Using 0.35 Micron CMOS Process
- Very Low Power Consumption (Active And Standby)
- High Density
  - 30,000 Usable Gates
  - 1,728 Logic Elements
  - 24,576 RAM Bits
  - 171 Maximum User I/O Pins

CL1K Product Family Overview

Parameter	CL1K30	CL1K50	CL1K100
Typical Gates (Logic and RAM)	30,000	50,000	100,000
Maximum System Gates	119,000	199,000	257,000
Logic Elements	1,728	2,880	4,992
Embedded Array Blocks	6	10	12
Total RAM Bits	24,576	40,960	49,152
Max User I/O pins	171	249	333
Speed Grades	-1, -2, -3	-1, -2, -3	-1, -2, -3
Packages	144-pin TQFP 208-pin PQFP 256-pin FBGA	144-pin TQFP 208-pin PQFP 256-pin FBGA 484-pin FBGA	208-pin PQFP 256-pin FBGA 484-pin FBGA

1K tbl 01

Description

The LIBERATOR™ CL1K family offers you all of the time-to-market benefits of designing with programmable logic. Simply use Altera ACEX® 1K FPGAs to prototype and verify the design. Then, take five minutes to submit the bitstream using Clear Logic's web site! Within eight weeks, your system can be in volume production using compatible Clear Logic devices.

LIBERATOR technology frees you to completely design, prototype, and verify your custom logic using Altera ACEX 1K products. Clear Logic's innovative technology eliminates NRE costs, test vector development, ordering minimums, and long lead times. No re-simulation or re-layout is required, because Clear Logic offers an architecture that is exactly compatible to the functionality of the FPGA prototype. Clear Logic's NoFault® test technology ensures complete test coverage through the use of special scan test registers.

The LIBERATOR family is based upon an array of logic elements. Each logic element contains a configurable look-up table for combinatorial functions and a register for sequential operations. Eight logic elements in a group form a block. Logic functions and signal routing are defined by Clear Logic's proprietary vertical metal links.

Laser-based configuration allows quick-turn prototyping and eliminates NRE costs for photomasks. Inherent CL1K family performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

Configuration

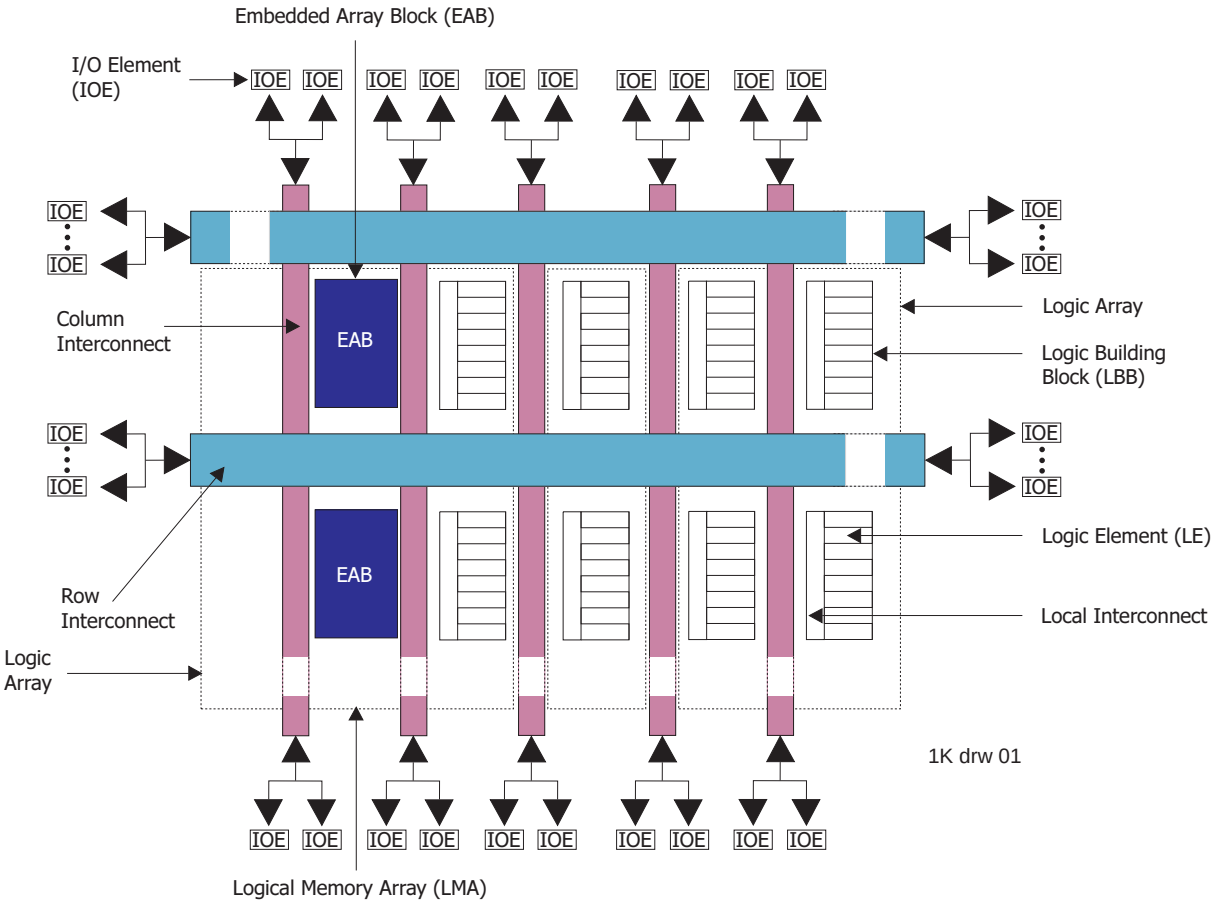
The "Gate Array" configuration mode eliminates the need for external EPROMs or software configuration. The LIBERATOR device is already factory-configured when it is shipped. When using the device in the "Gate Array" mode, it powers up fully configured. In this mode, if the customer selects INIT_DONE option, this pin will always be high.

Additional Information

For further information on designing with the CL1K LPLD® family, please refer to the following documents (all CL10K documents also pertain to the CL1K devices):

- AN-01: Requesting a First Article. This document provides instructions on how to request first articles by submitting a bitstream file to Clear Logic's web site.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL10K family and other Clear Logic devices.
- AN-13: LIBERATOR -- A New Way To Design. This document describes the most efficient path for custom logic designs up to 200K gates using FPGA design techniques and going to production with Clear Logic.
- AN-14: CL10K Technology White Paper. This document outlines the technologies employed by the LIBERATOR family.
- AN-15: LIBERATOR System Configuration. This document contains a detailed discussion of all aspects of configuring CL10K-based systems.
- AN-16: Introduction to the Clear Logic Verilog Model Generator. Clear Logic now has Verilog models of your FPGA converted design. Learn what it is and how it can help you.
- AN-17: Clear Logic LIBERATOR Design Models. This document outlines the capabilities and freedom available in the Clear Logic Verilog and VHDL design models.
- AN-18: Debugging Designs Using Clear Logic Models. This document shows the enhanced troubleshooting capabilities that the Clear Logic LIBERATOR Verilog/VHDL design models bring to the system debugging process.

Block Diagram



CLEARLOGIC

Pin Configuration

Pin Name	144-Pin TQFP	208-Pin PQFP	256-Pin FBGA
MSEL0	77	108	P1
MSEL1	76	107	R1
nSTATUS	35	52	T16
nCONFIG	74	105	N4
DCLK	107	155	B2
CONF_DONE	2	2	C15
INIT_DONE	14	19	G16
nCE	106	154	B1
nCEO	3	3	B16
nWS	142	206	B14
nRS	141	204	C14
nCS	144	208	A16
CS	143	207	A15
RDYnBSY	11	16	G14
CLKUSR	7	10	D15
DATA7	116	166	B5
DATA6	114	164	D4
DATA5	113	162	A4
DATA4	112	161	B4
DATA3	111	159	C3
DATA2	110	158	A2

1K30 tbl 01A

Pin Configuration

Pin Name	144-Pin TQFP	208-Pin PQFP	256-Pin FBGA
DATA1	109	157	B3
DATA0	108	156	A1
TDI	105	153	C2
TDO	4	4	C16
TCK	1	1	B15
TMS	34	50	P15
TRST		51	R16
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	B9, E8, M9, R9
Dedicated Clock Pins	55, 125	79, 183	A9, L8
DEV_CLRn	122	180	D8
DEV_OE	128	186	C9
VCCINT	16, 50, 75, 85, 103, 127	21, 33, 48, 72, 91, 106, 124, 130, 152, 185, 201	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5,L7, L12, M11, R2
VCCIO	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12
VCC_CKLK	53	77	L9
GNDINT	6, 15, 25, 40, 52, 58, 66, 84, 93, 104, 123, 129, 139	6, 20, 23, 32, 35, 43, 49, 59, 76, 82, 109, 117, 123, 129, 137, 145, 151, 171, 181, 188	A3, A14, C7, E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K5, K7, K10, L1, L6, L11, M5, M12
GND_CKLK	57	81	T8
No Connect	-	-	D1, E3, E16, G3, H1, H16, J1, K3, K14, K16, L2, L4, M14, M16, N15
Total user I/O Pins	**102**	**147**	**171**

1K30 tbl 01B

DC Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.5	3.6	V
V_I	DC Input Voltage[1]		-2.0	5.75	V
I_{OUT}	DC Output Current, per Pin		-25	25	mA
T_{STG}	Storage Temperature	No Bias	-65	150	°C
T_{AMB}	Ambient Temperature	Under Bias	-65	135	°C
T_J	Junction Temperature	Under Bias		135	°C

1K tbl 02

Recommended Operating Conditions [2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply Voltage, Internal Logic and Input Buffers				
	Commercial Grade Devices		2.375	2.625	V
	Industrial Grade Devices		2.375	2.625	V
V_{CCIO}	DC Input Voltage for 3.3V Operation				
	Commercial Grade Devices		3.00	3.60	V
	Industrial Grade Devices		3.00	3.60	V
V_{CCIO}	DC Input Voltage for 2.5V Operation				
	Commercial Grade Devices		2.375	2.625	V
	Industrial Grade Devices		2.375	2.625	V
V_I	Input Voltage		-0.5	5.75	V
V_O	Output Voltage		0	V_{CCIO}	V
T_A	Operating Temperature				
	Commercial Temperature Range		0	70	°C
	Industrial Temperature Range		-40	85	°C
t_R	Input Signal Rise Time			40	ns
t_F	Input Signal Fall Time			40	ns

1K tbl 03

DC Electrical Specifications cont.

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ[3]	Max	Unit
V_{IH}	Input HIGH Voltage		Lower of 1.7 or 0.5 x V_{CCINT}		5.75	V
V_{IL}	Input LOW Voltage		-0.5		0.3 x V_{CCIO}	V
V_{OH}	3.3-V High-Level TTL Output Voltage	I_{OH} = -8 mA DC, V_{CCIO} = 3.00 V	2.4			V
	3.3-V High-Level CMOS Output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 3.00 V	V_{CCIO}-0.2			V
	3.3-V High-Level PCI Output Voltage	I_{OH} = -0.5 mA DC, V_{CCIO} = 3 to 3.60 V	0.9 x V_{CCIO}			V
	2.5-V High-Level Output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 2.30 V	2.1			V
		I_{OH} = -1 mA DC, V_{CCIO} = 2.30 V	2.0			V
		I_{OH} = -2 mA DC, V_{CCIO} = 2.30 V	1.7			V
V_{OL}	3.3-V Low-Level TTL Output Voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V			0.45	V
	3.3-V Low-Level CMOS Output Voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V			0.2	V
	3.3-V Low-Level PCI Output Voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3 to 3.60 V			0.1 x V_{CCIO}	V
	2.5-V Low-Level Output Voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V			0.7	V
I_{IN}	Input Leakage Current	V_I = 5.3V to -0.3V	-10		10	µA
I_{OZ}	Output Leakage Current	V_O = 5.3V to -0.3V	-10		10	µA
I_{CC0}	Standby Current	V_I = GND, No Load		5		mA

1K tbl 04

Capacitance[4]

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

1K tbl 05

AC Electrical Specifications

I/O Element Timing Parameters [5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}	IOE Register Data Delay		2.4		2.8		3.8	ns
t_{IOC}	IOE Register Control Signal Delay		0.3		0.3		0.5	ns
t_{IOCO}	IOE Register Clock to Output Delay		0.2		0.2		0.3	ns
t_{IOCOMB}	IOE Combinatorial Delay		0.5		0.6		0.8	ns
t_{IOSU}	IOE Register Setup Time Before Clock	2.2		2.6		3.5		ns
t_{IOH}	IOE Register Hold Time After Clock	0.5		0.6		0.8		ns
t_{IOCLR}	IOE Register Clear Delay		0.2		0.2		0.3	ns
t_{OD1}	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = V_{CCINT}		1.1		1.3		1.8	ns
t_{OD2}	Output Buffer and Pad Delay Slow Slew Rate = off, VCCIO = Low Voltage		0.6		0.9		1.6	ns
t_{OD3}	Output Buffer and Pad Delay Slow Slew Rate = on		3.0		3.5		4.8	ns
t_{ZX}	Output Buffer Disable Delay[6]		1.1		1.3		1.8	ns
t_{ZX1}	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = V_{CCINT}[6]		1.1		1.3		1.6	ns
t_{ZX2}	Output Buffer Disable Delay Slow Slew Rate = off, VCCIO = Low Voltage[6]		0.6		0.9		1.6	ns
t_{ZX3}	Output Buffer Disable Delay Slow Slew Rate = on[6]		3.0		3.5		4.8	ns
t_{INREG}	IOE Input Pad and Buffer to IOE Register Delay		5.0		5.9		8.0	ns
t_{IOFD}	IOE Register Feedback Delay		3.0		3.6		4.8	ns
t_{INCOMB}	IOE Input Pad and Buffer to Interconnect Delay		3.0		3.6		4.8	ns

1K tbl 06

AC Electrical Specifications cont.

External Timing Parameters[4]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}	Register to Register Delay via Four LEs, Three Row Interconnects, and Four Local Interconnects		8.0		9.5		12.5	ns
t_{INSU}	Setup Time with Global Clock at IOE Register	3.0		3.6		4.8		ns
t_{INH}	Hold time with Global Clock at IOE Register	0.0		0.0		0.0		ns
t_{OUTCO}	Output Data Hold Time After Clock	2.0	3.5	2.0	4.5	2.0	7.1	ns

1K tbl 07A

Logic Element Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}	Look-up Table Delay for Data-in		0.6		0.8		1.1	ns
t_{CLUT}	Look-up Table Delay for Carry-in		0.5		0.6		0.8	ns
t_{RLUT}	Look-up Table Delay for LE Register Feedback		0.7		0.8		1.1	ns
t_{PACKED}	Data-in to Packed Register Delay		0.5		0.6		0.8	ns
t_{EN}	LE Register Enable Delay		0.6		0.7		0.9	ns
t_{CICO}	Carry-in to Carry-out Delay		0.2		0.2		0.3	ns
t_{CGEN}	Data-in to Carry-out Delay		0.5		0.5		0.8	ns
t_{CGENR}	LE Register Feedback to Carry-out Delay		0.2		0.2		0.3	ns
t_{CASC}	Cascade Chain Routing Ddelay		0.8		0.9		1.2	ns
t_{C}	LE Register Control Signal Delay		0.5		0.6		0.8	ns
t_{CO}	LE Register Clock-to-output Delay		0.5		0.6		0.7	ns
t_{COMB}	Combinatorial Delay		0.5		0.6		0.7	ns
t_{SU}	LE Register Setup Time Before Clock	0.5		0.6		0.8		ns
t_{H}	LE Register Hold Time After Clock	0.9		1.1		1.5		ns
t_{PRE}	LE Register Preset Delay		0.5		0.6		0.8	ns
t_{CLR}	LE Register Clear Delay		0.5		0.6		0.8	ns
t_{CH}	Clock High Time	2.0		2.5		3.0		ns
t_{CL}	Clock Low Time	2.0		2.5		3.0		ns

1K tbl 08

AC Electrical Specifications cont.

Interconnect Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{DIN2IOE}$	Delay from Dedicated Input Pin to IOE Control Input		4.1		4.6		5.9	ns
t_{DIN2LE}	Delay from Dedicated Input Pin to LE or EAB Control Input		0.9		1.0		1.3	ns
$t_{DIN2DATA}$	Delay from Dedicated Input or Clock Pin to LE or EAB Data		1.8		1.9		2.3	ns
$t_{DCLK2IOE}$	Delay from Dedicated Clock Pin to IOE Clock		3.9		4.6		6.2	ns
$t_{DCLK2LE}$	Delay from Dedicated Clock Pin to LE or EAB Clock		0.9		1.0		1.3	ns
$t_{SAMELAB}$	Delay from an LE to LE in Same LAB		0.1		0.1		0.2	ns
$t_{SAMEROW}$	Delay for Driving a Row IOE, LE or EAB to a Row IOE, LE or EAB in the Same Row		1.3		1.3		1.8	ns
$t_{SAMECOLUMN}$	Delay from an LE to IOE in the Same Column		0.7		0.8		1.5	ns
$t_{DIFFROW}$	Delay for Driving a Column IOE, LE or EAB to an LE or EAB in a Different Row		2.0		2.1		3.3	ns
$t_{TWOROWS}$	Delay for Driving a Row IOE or EAB to an LE or EAB in a Different Row		3.3		3.4		5.1	ns
$t_{LEPERIPH}$	Delay from an LE to IOE Control Signal via the Peripheral Dontol Bus		3.8		4.1		5.3	ns
$t_{LABCARRY}$	Delay from an LE Carry-out Signal to an LE Carry-in Signal in a Different LAB		0.1		0.1		0.2	ns
$t_{LABCASC}$	Delay from an LE Cascade-out Signal to an LE Cascade-in Signal in a Different LAB		0.3		0.3		0.5	ns

1K tbl 09A

AC Electrical Specifications cont.

EAB Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{EABDATA1}$	Delay from Data or Address to EAB for Combinatorial Input		1.7		2.0		2.7	ns
$t_{EABDATA2}$	Delay from Data or Address to EAB for Registered Input		0.6		0.7		0.9	ns
t_{EABWE1}	WE Delay to EAB for Combinatorial Input		1.1		1.3		1.8	ns
t_{EABWE2}	WE Delay to EAB for Registered Input		0.4		0.4		0.6	ns
t_{EABCLK}	EAB Register Clock Delay		0.0		0.0		0.0	ns
t_{EABCO}	EAB Register Clock-to-output Delay		0.3		0.3		0.5	ns
$t_{EABBYPASS}$	Bypass Register Delay		0.5		0.6		0.8	ns
t_{EABSU}	EAB Register Setup Time	0.9		1.0		1.4		ns
t_{EABH}	EAB Register Hold Time	0.4		0.4		0.6		ns
t_{AA}	Address Access Delay		3.2		3.8		5.1	ns
t_{WP}	Write Pulse Width	2.5		2.9		3.9		ns
t_{WDSU}	Data Setup Time Before Falling Edge of Write Pulse	0.9		1.0		1.4		ns
t_{WDH}	Data Hold Time After Falling Edge of Write Pulse	0.1		0.1		0.2		ns
t_{WASU}	Address Setup Time Before Rising Edge of Write Pulse	1.7		2.0		2.7		ns
t_{WAH}	Address Hold After Falling Edge of Write Pulse	1.8		2.1		2.9		ns
t_{WO}	Write Enable to Date Output Delay		2.5		2.9		3.9	ns
t_{DD}	Data-in to Date-out Delay		2.5		2.9		3.9	ns
t_{EABOUT}	Data-out Delay		0.5		0.6		0.8	ns
t_{EABCH}	Clock High Time	1.5		2.0		2.5		ns
t_{EABCL}	Clock Low Time	1.5		2.0		2.5		ns

1K tbl 10

AC Electrical Specifications cont.

EAB Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{EABAA}	EAB Address Access Delay		6.4		7.6		10.2	ns
$t_{EABRCCOMB}$	EAB Asynchronous Read Cycle Time	6.4		7.6		10.2		ns
$t_{EABRCREG}$	EAB Synchronous Read Cycle Time	4.4		5.1		7.0		ns
t_{EABWP}	EAB Write Pulse Width	2.5		2.9		3.9		ns
$t_{EABWCCOMB}$	EAB Asynchronous Write Cycle Time	6.0		7.0		9.5		ns
$t_{EABWCREG}$	EAB Synchronous Write Cycle Time	6.8		7.8		10.6		ns
t_{EABDD}	EAB Data-in to Data-out Delay		5.7		6.7		9.0	ns
$t_{EABDATACO}$	EAB Clock-to-output Delay Using Output Registers		0.8		0.9		1.3	ns
$t_{EABDATASU}$	EAB Data/Address Setup Time Using Input Register	1.5		1.7		2.3		ns
$t_{EABDATAH}$	EAB Data/Address Hold Time Using Input Register	0.0		0.0		0.0		ns
$t_{EABWESU}$	EAB WE Setup When Using Input Register	1.3		1.4		2.0		ns
$t_{EABWESH}$	EAB WE Hold Time When Using Input Register	0.0		0.0		0.0		ns
$t_{EABWDSU}$	EAB Data Setup Time to Falling Edge of Write Pulse When Not Using Input Registers	1.5		1.7		2.3		ns
t_{EABWDH}	EAB Data Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0.0		0.0		0.0		ns
$t_{EABWASU}$	EAB Address Setup Time to Rising Edge of Write Pulse When Not Using Input Registers	3.0		3.6		4.8		ns
t_{EABWAH}	EAB Address Hold Time After Falling Edge of Write Pulse When Not Using Input Registers	0.5		0.5		0.8		ns
t_{EABWO}	EAB WE to Data Output Delay		5.1		6.0		8.1	ns

1K tbl 11

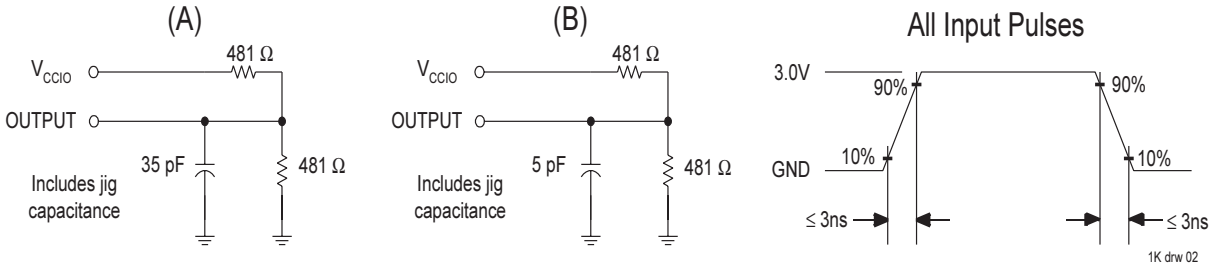
AC Electrical Specifications cont.

External Bidirectional Timing Parameters[5]

		Speed: -1		Speed: -2		Speed: -3		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{INSUBIDIR}$	Setup for Bi-directional Pins with Global Clock at Adjacent LE Registers	1.5		2.2		3.6		ns
$t_{INHBIDIR}$	Hold Time for Bi-directional Pins with Global Glock at Adjacent LE Registers	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	Clock-to-output Delay for Bi-directional Pins with Global Clock at IOE Register	2.0	3.5	2.0	4.5	2.0	7.1	ns
$t_{XZBIDIR}$	Synchronous IOE Output Buffer Disable Delay	2.0	5.8	2.0	6.3	2.0	8.0	ns
$t_{ZXBIDIR}$	Synchronous IOE Output Buffer Disable Delay, Slow Slew Rate = off	2.0	4.7	2.0	5.3	2.0	7.2	ns

1K tbl 12A

AC Test Conditions



A: Test fixture set-up A is for general testing.
B: Test fixture set-up B is for high Z testing ($t_{ZX\#}$).

Notes to Tables

1. During transitions, inputs may undershoot to -2.0V or overshoot to 5.75V for periods shorter than 20ns. Otherwise, minimum DC input voltage is -0.5V.

2. Device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.

3. Typical values are at V_{CC} of 3.3 volts and ambient temperature of 25 ºC.

4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

6. Use AC Test Conditions set-up B for these parameters.

Revision History

02 Dec. 2000: Created new document

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL1K30TC144-3	Commercial	144-pin TQFP	-3	EPF1K30TC144-3
CL1K30TC144-2			-2	EPF1K30TC144-2
CL1K30TC144-1			-1	EPF1K30TC144-1
CL1K30QC208-3	Commercial	208-pin Plastic QFP	-3	EPF1K30QC208-3
CL1K30QC208-2			-2	EPF1K30QC208-2
CL1K30QC208-1			-1	EPF1K30QC208-1
CL1K30FC256-3	Commercial	256-pin FBGA	-3	EPF1K30FC256-3
CL1K30FC256-2			-2	EPF1K30FC256-2
CL1K30FC256-1			-1	EPF1K30FC256-1

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