

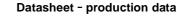
Pin2

1610 package

Pin1

ESDA7P60-1U1M

High power transient voltage suppressor

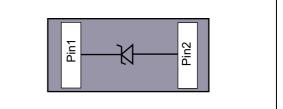




The ESDA7P60-1U1M is a unidirectional single line TVS diode designed to protect the power line against IOS and ESD transients.

The device is ideal for applications where high power TVS and board space saving are required.

Figure 1. Pin configuration



Features

- Low clamping voltage
- Typical peak pulse power:
 700 W (8/20µs)
- Stand off voltage 5 V
- Unidirectional diode
- Low leakage current:
 0.2 μA at 25 °C
- RoHS compliant

Complies with the following standards:

- IEC 61000-4-2 level 4
 - ±30 kV (air discharge)
 - ±30 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Portable multimedia, tablets, mobile phone, smart phone
- USB V_{BUS} protection
- Power supply protection
- Battery protection

November 2014

DocID027044 Rev 1

This is information on a product in full production.

1 Characteristics

Symbol	Parameter	Value	Unit				
V _{PP}	Peak pulse voltage: V _{PP} IEC 61000-4-2 contact discharge EC 61000-4-2 air discharge		kV				
P _{PP}	Peak pulse current (8/20 µs)	700	W				
I _{PP}	Peak pulse current (8/20 µs)	60	A				
T _{stg}	T _{stg} Storage temperature range		°C				
Т _{ор}	Operating junction temperature range	-55 to +150	°C				

Table 1. Absolu	ite maximum	ratings	$(T_{amb} = 25 \ ^{\circ}C)$

Figure 2. Electrical characteristics (definitions)

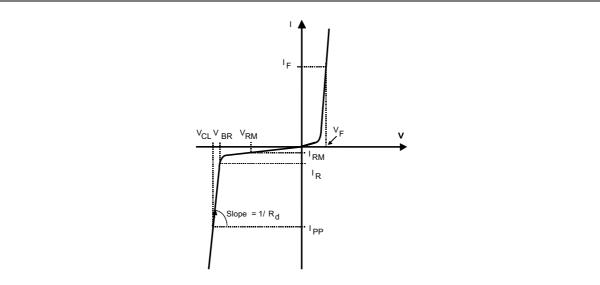


Table 2. Electrical characteristics	(values, $T_{omb} = 25 ^{\circ}C$)
	(1000, 100) = 200

Symbol	Test conditions	Min.	Тур.	Max.	Unit
V _{BR}	I _R = 1 mA	6.4	6.8	7.2	V
I _{RM}	V _{RM} = 5 V			200	nA
V _{CL} I _{PP} = 60 A 8/20 μs			10.2	11.6	V
R _d	R _d 8/20 μs		0.06		Ω



initial junction temperature (typical values)

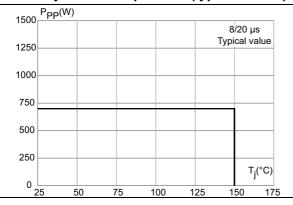


Figure 5. Peak pulse current versus clamping voltage (maximum values)

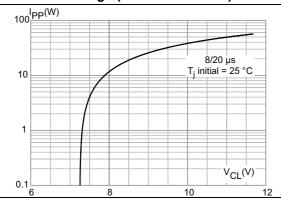


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

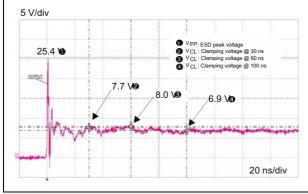
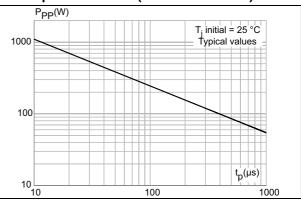
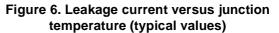


Figure 3. Peak pulse power dissipation versus Figure 4. Peak pulse power versus exponential pulse duration (maximum values)





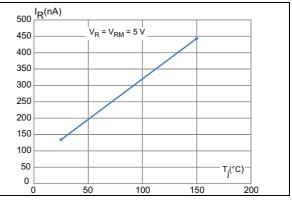
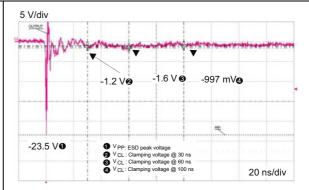


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)





2 Package information

- Epoxy meets UL94, V0
- Dot indicates pin 1

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

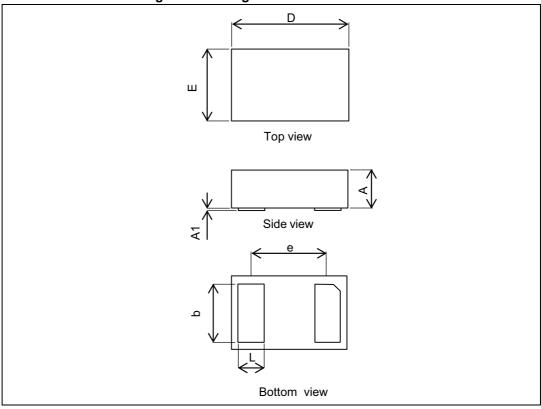
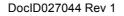


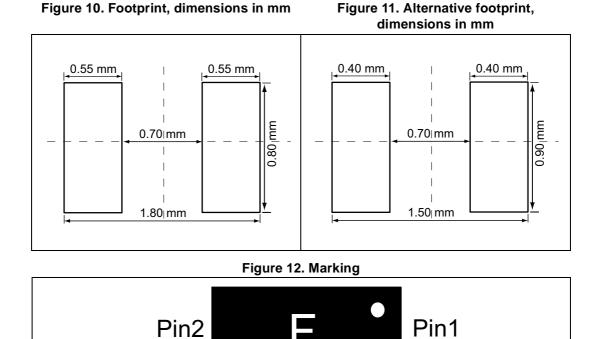
Figure 9. Package dimension definitions

Table 3. 1610 package dimension values

	Dimensions						
Ref. Millimeters				Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
А	0.51	0.55	0.60	0.020	0.021	0.023	
A1	0.00	0.02	0.05			0.002	
b	0.75	0.80	0.85	0.029	0.031	0.033	
D	1.50	1.60	1.70	0.059	0.063	0.067	
E	0.90	1.00	1.10	0.035	0.039	0.043	
е		1.05			0.041		
L	0.30	0.35	0.40	0.011	0.013	0.016	







Note:

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

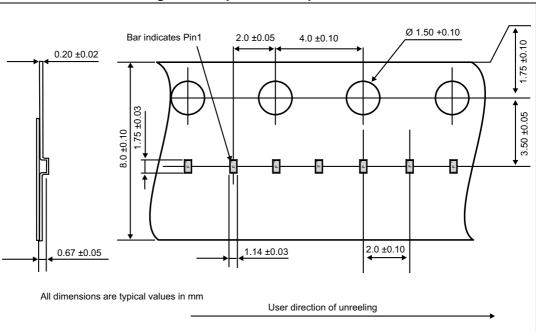


Figure 13. Tape and reel specifications

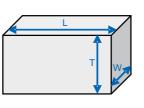


3 Recommendation on PCB assembly

3.1 Stencil opening design

- 1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 14. Stencil opening dimensions



b) General design rule

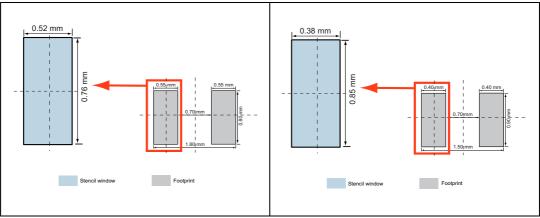
Stencil thickness (T) = 75 ~ 125 μ m

Aspect Ratio =
$$\frac{W}{T} \ge 1.5$$

Aspect Area =
$$\frac{L \times W}{2T(L + W)} \ge 0.66$$

- 2. Reference design
 - a) Stencil opening thickness: 100 µm
 - b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 15. Recommended stencil window Figure 16. Alternative stencil window position position





3.2 Solder paste

- 1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste recommended.
- 3. Offers a high tack force to resist component displacement during PCB movement.
- 4. Use solder paste with fine particles: powder particle size 20-45 $\mu m.$

3.3 Placement

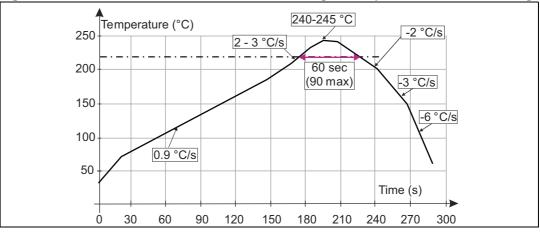
- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- 3. Standard tolerance of \pm 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



3.5 Reflow profile





Note:

Minimize air convection currents in the reflow oven to avoid component movement.



4 Ordering information

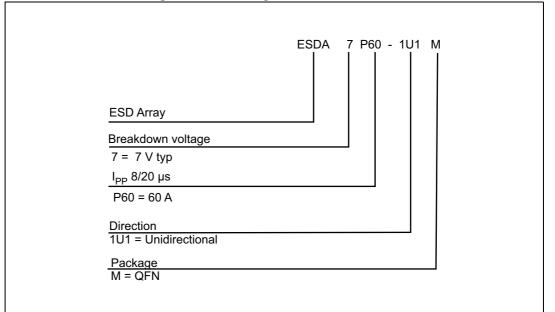


Figure 18. Ordering information scheme

Table 4. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDA7P60	F ⁽¹⁾	2.4 mg	8000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
14-Nov-2014	1	Initial release.



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