



# FDB024N08BL7

## N-Channel PowerTrench® MOSFET

80V, 229A, 2.4mΩ

### Features

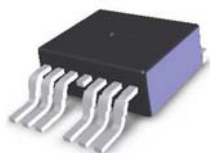
- $R_{DS(on)} = 1.7m\Omega$  (Typ.) @  $V_{GS} = 10V, I_D = 100A$
- Low FOM  $R_{DS(on)} \cdot Q_G$
- Low reverse recovery charge,  $Q_{rr}$
- Soft reverse recovery body diode
- Enables highly efficiency in synchronous rectification
- Fast Switching Speed
- RoHS Compliant
- Qualified according to JEDEC Standards JESD22-A113F and IPC/JEDEC J-STD-020D.1

### Description

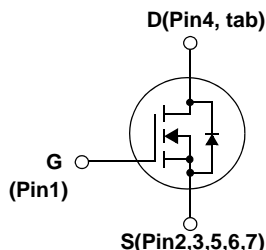
This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- Synchronous Rectification for Server / Telecom PSU
- Battery Charger and Battery Protection circuit
- DC motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



**D<sup>2</sup>-PAK-7L**  
FDB Series with suffix - L7



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	80	V
$V_{GSS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ C$ , Silicon Limited)	229*
		-Continuous ( $T_C = 100^\circ C$ , Silicon Limited)	162*
		-Continuous ( $T_C = 25^\circ C$ , Package Limited)	120
$I_{DM}$	Drain Current	- Pulsed (Note 1)	916
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	917
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	246
		- Derate above $25^\circ C$	1.64
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A

### Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.61	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB020N08B	FDB020N08BL7	D2-PAK-7L	330 mm	24 mm	800

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.05	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 64\text{V}, T_C = 150^\circ\text{C}$	-	-	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 100\text{A}$	-	1.7	2.4	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 100\text{A}$ (Note 4)	-	227	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	10170	13530	pF
$C_{oss}$	Output Capacitance		-	1670	2220	pF
$C_{riss}$	Reverse Transfer Capacitance		-	35	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	3025	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40\text{V}, V_{GS} = 10\text{V}$ $I_D = 100\text{A}$	-	137	178	nC
$Q_{gs}$	Gate to Source Gate Charge		-	56	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	25	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4, 5)	-	28	-
ESR	Equivalent Series Resistance (G-S)	Drain Open, $f = 1\text{MHz}$	-	2.4	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{V}, I_D = 100\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	47	104	ns
$t_r$	Turn-On Rise Time		-	66	142	ns
$t_{d(off)}$	Turn-Off Delay Time		-	87	184	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	-	41	92

### Drain-Source Diode Characteristics

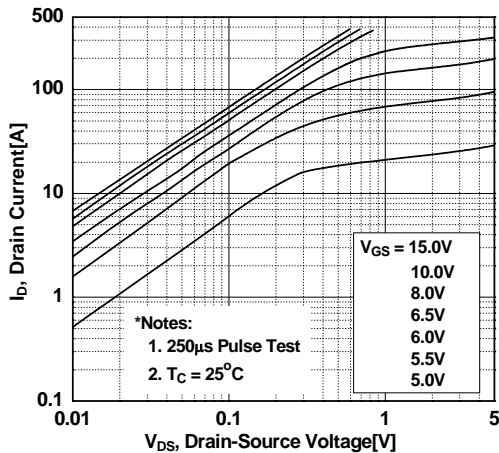
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	229*	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	916	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 100\text{A}$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, V_{DD} = 40\text{V}, I_{SD} = 100\text{A}$	-	80	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	112	-	nC

#### Notes:

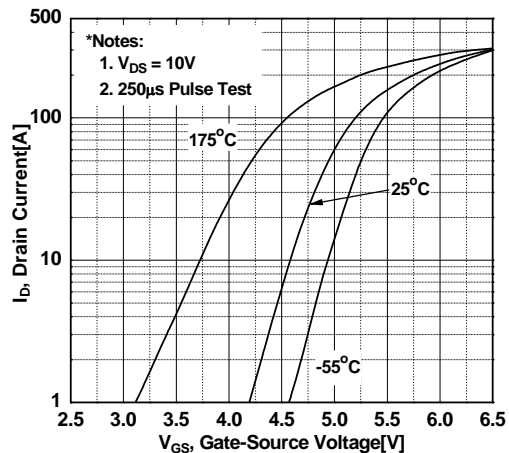
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 3\text{mH}, I_{AS} = 24.72\text{A}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 100\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Dual Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

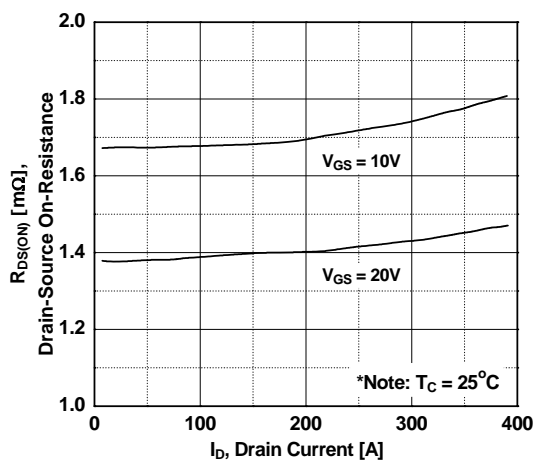
**Figure 1. On-Region Characteristics**



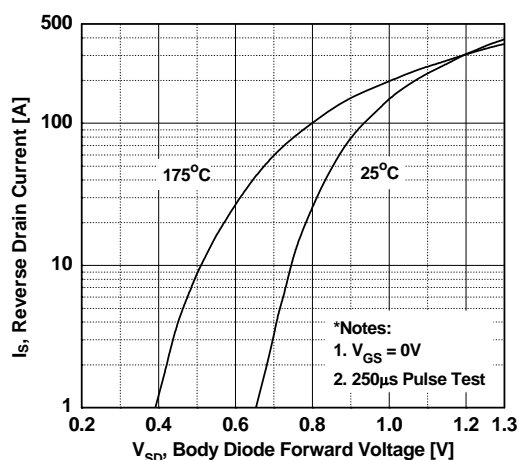
**Figure 2. Transfer Characteristics**



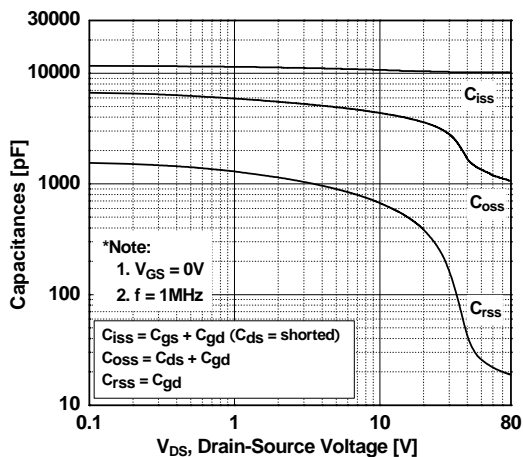
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



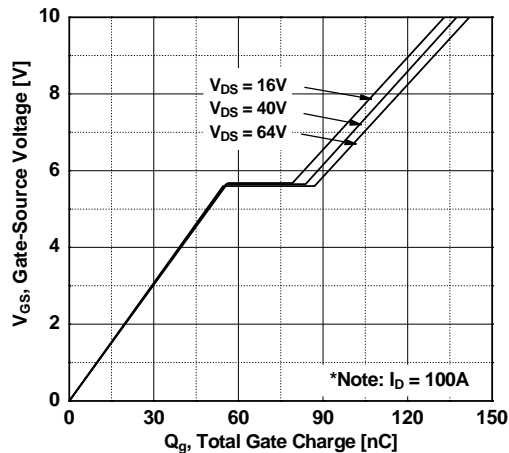
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

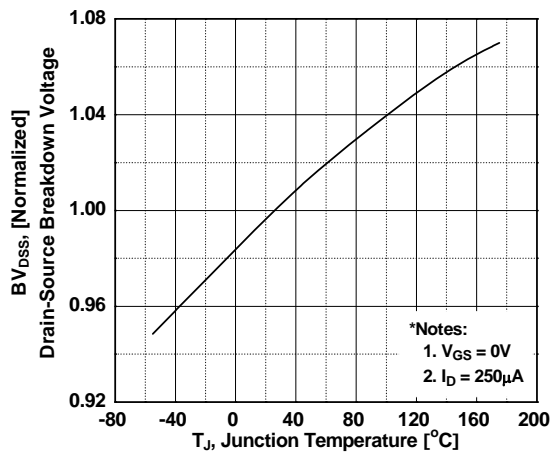


**Figure 6. Gate Charge Characteristics**

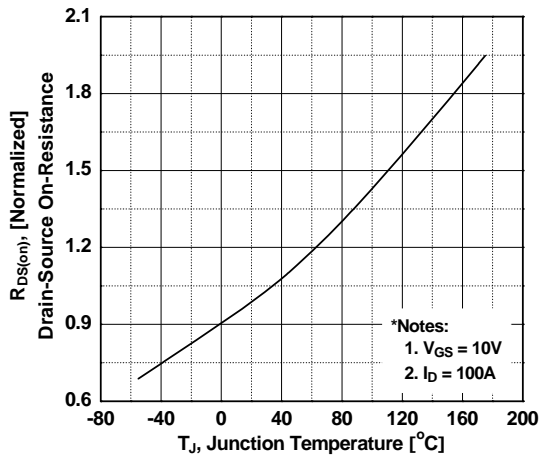


## Typical Performance Characteristics (Continued)

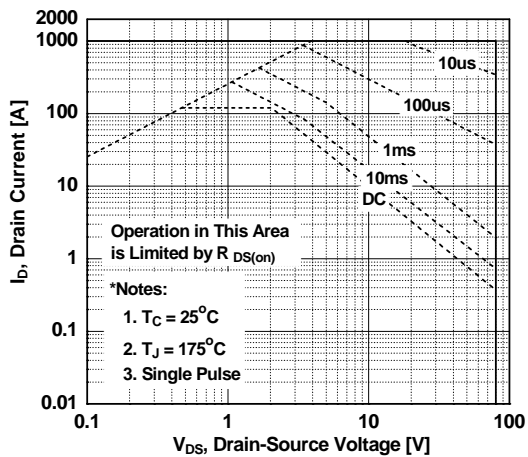
**Figure 7. Breakdown Voltage Variation vs. Temperature**



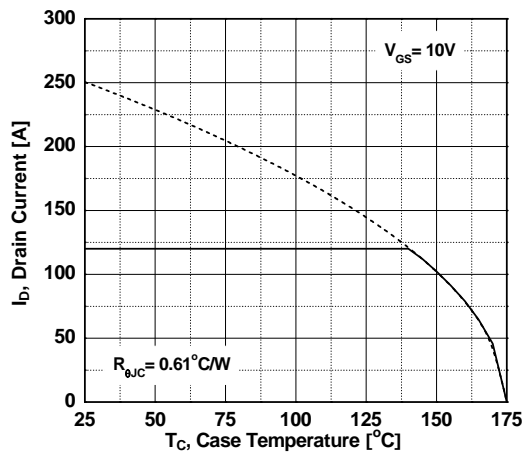
**Figure 8. On-Resistance Variation vs. Temperature**



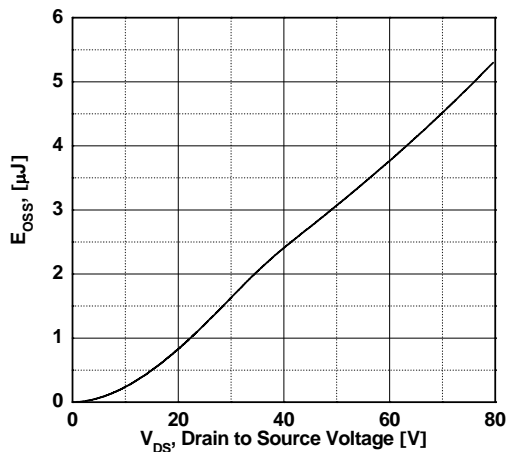
**Figure 9. Maximum Safe Operating Area vs. Case Temperature**



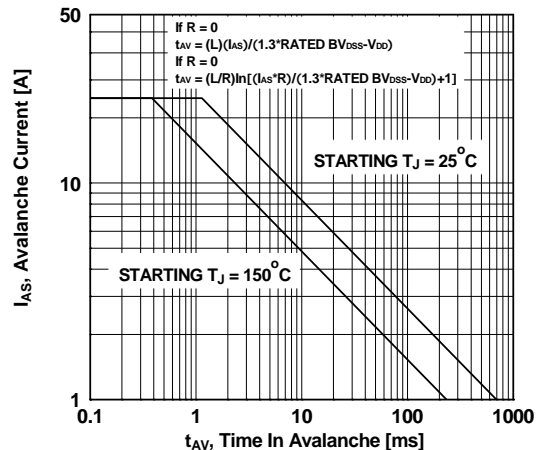
**Figure 10. Maximum Drain Current**



**Figure 11. E<sub>oss</sub> vs. Drain to Source Voltage**

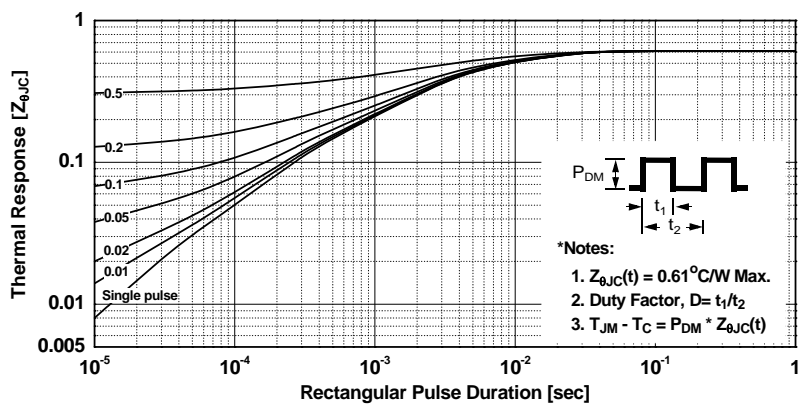


**Figure 12. Unclamped Inductive Switching Capability**

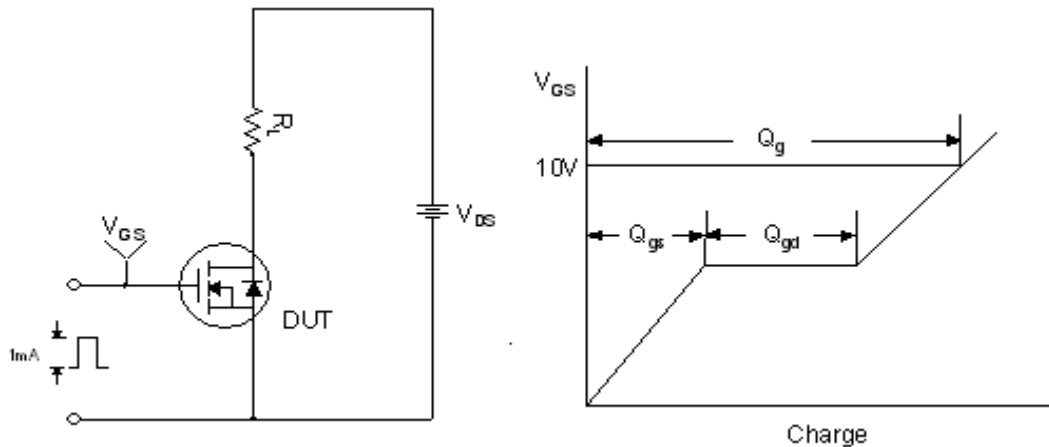


Typical Performance Characteristics (Continued)

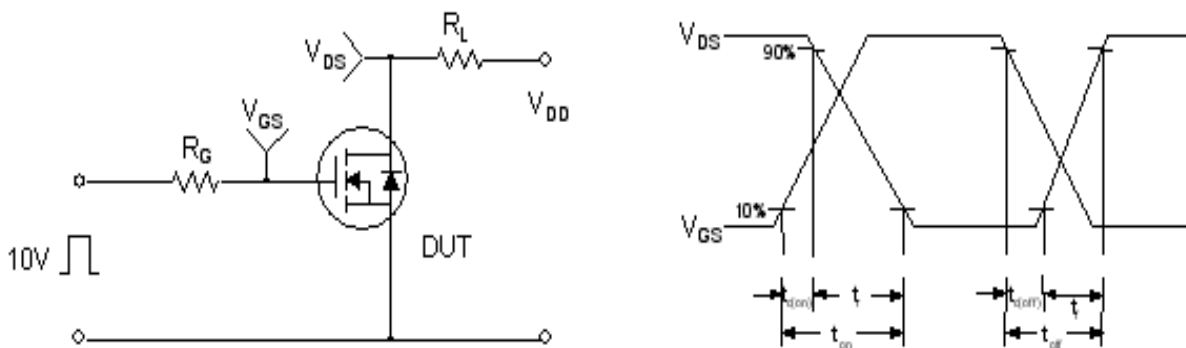
Figure 12. Transient Thermal Response Curve



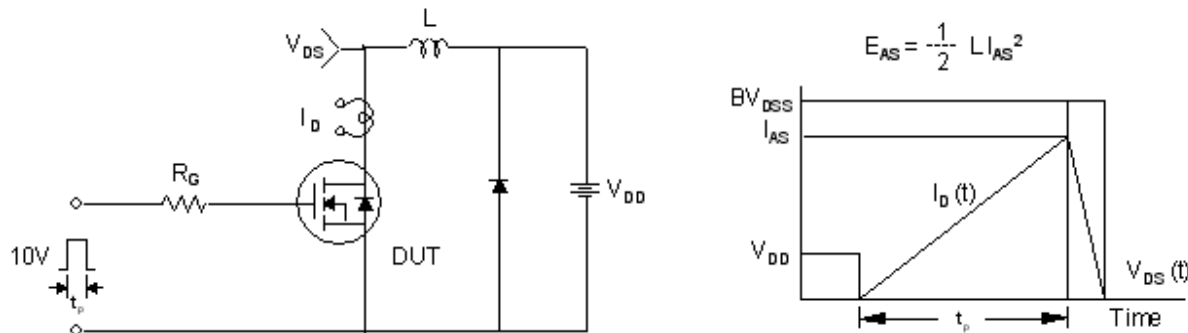
**Gate Charge Test Circuit & Waveform**



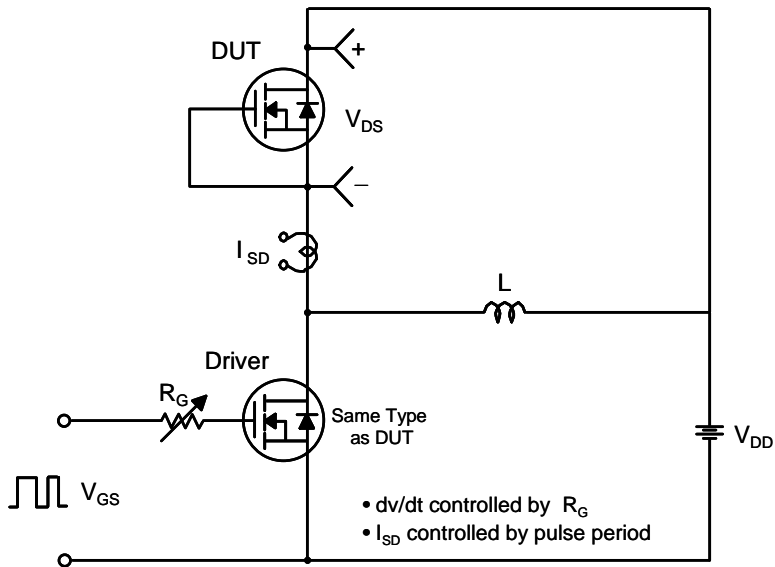
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

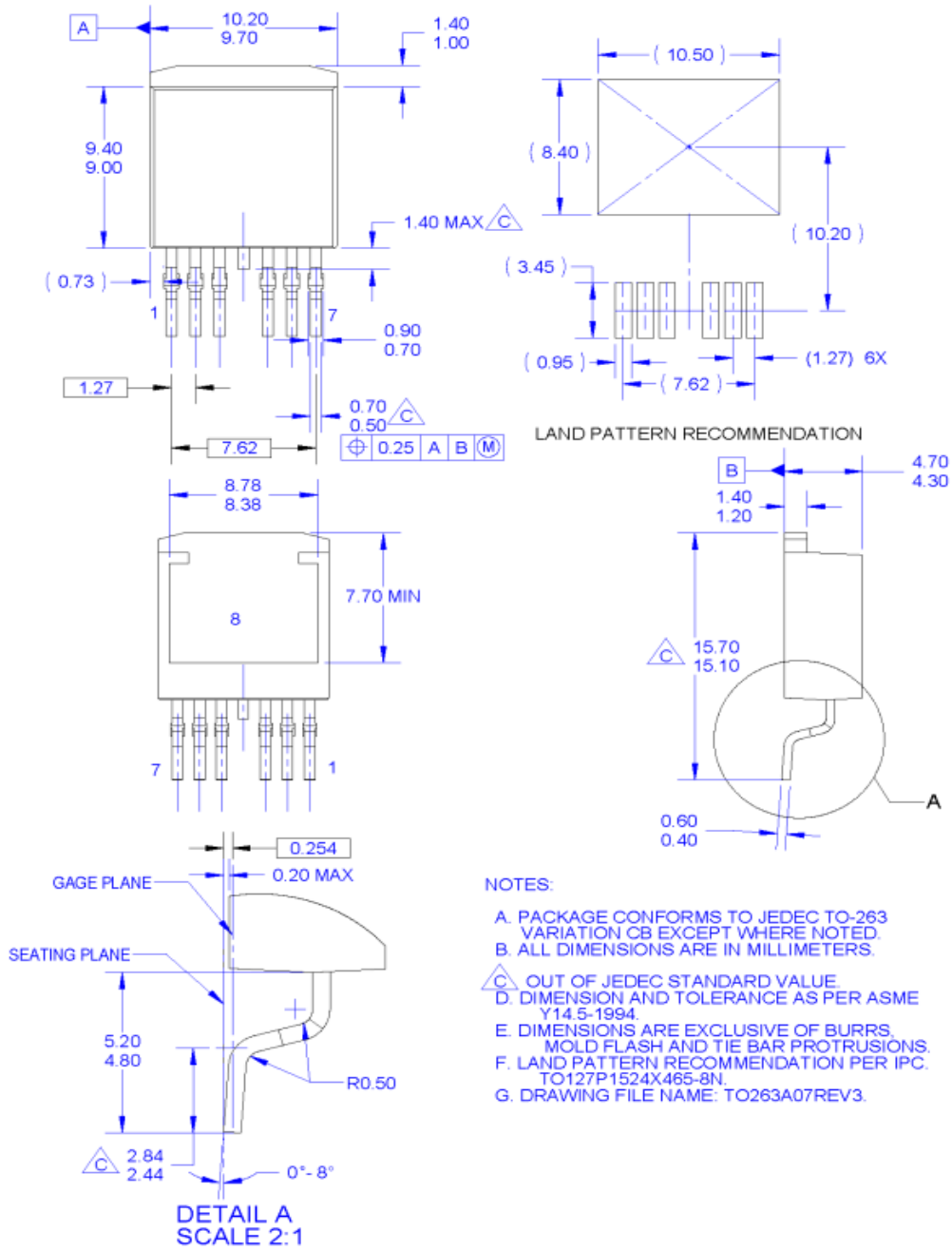


Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Dimensional Outline and Pad Layout

### D2-PAK-7L











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