MA17501

Radiation Hard MIL-STD-1750A Execution unit

Replaces March 1997 version, DS4548 - 2.3

DS4548 - 3.2 January 2000

The MA17501 Execution Unit is a component of the Dynex Semiconductor MAS281 chip set. Other chips in the set include the MA17502 Control Unit and the MA17503 Interrupt Unit. Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit. These chips in conjunction implement the full MIL-STD-1750A Instruction Set.

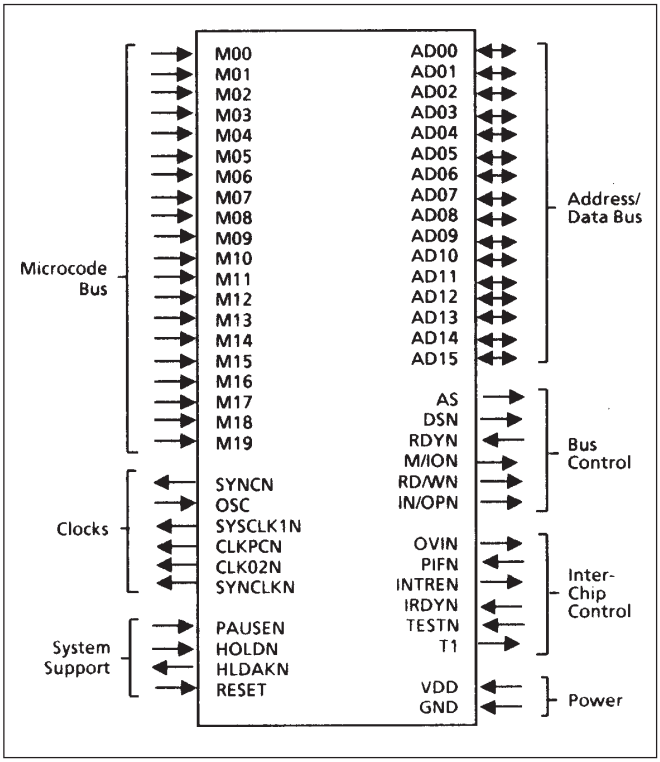
The MA17501 - consisting of a full function 16-bit ALU, 24 x 16-bit dual-port RAM register file, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, synchronisation clock generation logic, and microcode decode logic - provides all computational, logical, and synchronisation functions for the chip set. Table 1 provides brief signal definitions.

The MA17501 is offered in several package styles including; dual-in-line, flatpack and leadless chip carrier. Full packaging information is given at the end of the document.

FEATURES

- MIL-STD-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range (-55°C to +125°C)
- Radiation Hard CMOS/SOS Technology
- 16-Bit Bidirectional Address/Data Bus
- 16-Bit Full Function Registered ALU
- 32-Bit Barrel Shifter
- 24 x 16-Bit Dual-Port RAM File
  - 16 User Accessible General Purpose Registers
  - 8 Microcode Accessible Registers
- 4 x 24-Bit Parallel Multiplier
  - 48-Bit Accumulator
  - 16-Bit x 16-Bit Multiply in 4 Machine Cycles
- Instruction Pre-Fetch
- MAS281 Integrated Built-in Self Test
- TTL Compatible System Interface

BLOCK DIAGRAM



1.0 SYSTEM CONSIDERATIONS

The MA17501 Execution Unit (EU) is a component of the Dynex Semiconductor MAS281 chip set. This chip set implements the full MIL-STD-1750A instruction set architecture. The other chips in the set are the MA17502 Control Unit (CU) and the MA17503 Interrupt Unit (IU). Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit (MMU(BPU)).

Figure 1 depicts the relationship between the chip set components. The EU provides the arithmetic and logical computation resources for the chip set. The EU also provides program sequencing logic in support of branching and subroutine functions. The IU provides interrupt and fault handling resources, DMA interface control signals, and the three MIL-STD-1750A timers. The EU and IU are each controlled by microcode from the CU. The MMU(BPU) may be configured to provide 1M-word memory management (MMU) and/or 1K-word memory block write protection (BPU) functions.

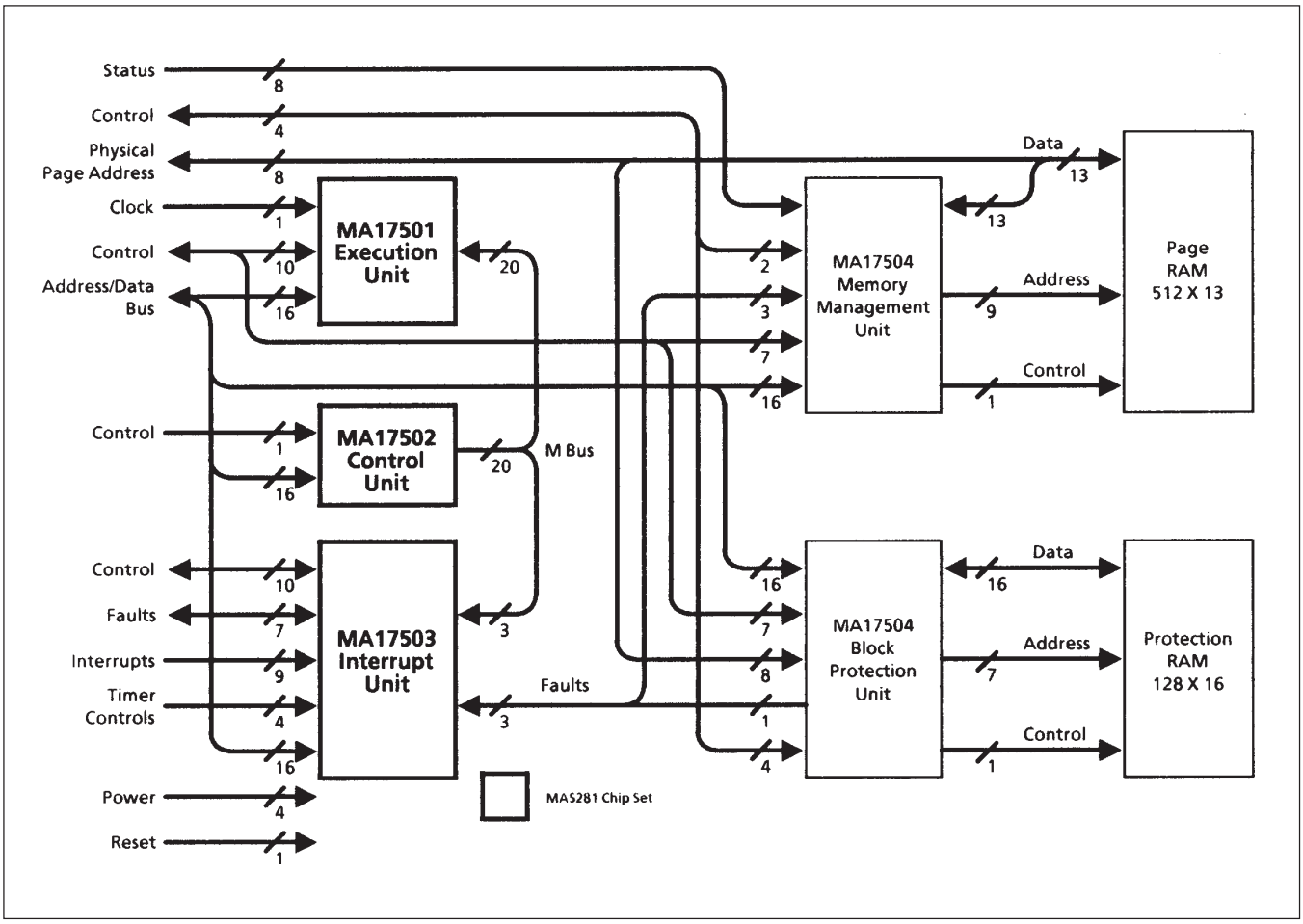


Figure 1: MAS281 Chip Set with Optional MA17504 and Support RAMs

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of a MA31751 allows access to a 1M-word address space and/or provides hardware support for 1K-word memory block write protection.

The EU, as with all components of the MAS281 chip set, is fabricated with GEC Plessey Semiconductors CMOS/SOS process technology. Input and output buffers associated with signals external to the MAS281 are TTL compatible.

Detailed descriptions of the EU's companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and DAIS mix benchmarking analysis are provided in separate applications notes.

The Execution Unit consists of a full function 16-bit ALU, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, 24 x 16bit dual-port RAM register file, processor status word register, three operand transfer registers, three instruction fetch registers, various interconnect buses, synchronization clock generation logic, and microcode decode logic. Details of these components are depicted in Figure 2 and are discussed below:

2.0 ARCHITECTURE

2.1 ALU

The ALU is a full function 16-bit arithmetic/logic unit capable of performing arithmetic and logic operations on either one or two 16-bit operands in a single machine cycle. In addition to operand manipulation, the ALU is used to compute memory addresses.

The ALU supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit floating-point extended-precision data in two's complement representation. Double-precision and extended-precision operands are passed through the ALU 16 bits at a time on consecutive machine cycles. Machine flags provide an indication of ALU results and are used to set condition status (CS) bits C, P, Z, and N in the Status Word Register. Condition status bits and the Status Word register are discussed below.

Signal	I/O	Definition
AD00 - AD15	I/O	External 16-Bit Address/Data Bus
AS	O/Z	Address Strobe Indicates Address lnformation on A/D Bus
$\overline{\text{CLKPC}}$	O	Precharge Clock
$\overline{\text{CLK02}}$	O	Phase 2 Clock
$\overline{\text{PAUSE}}$	I	DMA Acknowledge (A/D Bus to be used for DMA)
$\overline{\text{DS}}$	O/Z	Data Strobe lndicates Data lnformation on A/D Bus
$\overline{\text{HLDAK}}$	O	Hold Acknowledge
$\overline{\text{HOLD}}$	I	Hold Request Suspends lnternal Processor Functions
IN/$\overline{\text{OP}}$	O/Z	lnstruction/Operand lndicates Type of Memory Access
$\overline{\text{INTRE}}$	O	lnterrupt Enable
$\overline{\text{IRDY}}$	I	lnterrupt Unit Ready Signal
M/$\overline{\text{IO}}$	O/Z	Memory or lnput/Output lndicates Transaction on A/D Bus
M00 - M19	I	20-Bit Microcode Bus
OSC	I	External Oscillator Clock
$\overline{\text{OVI}}$	O	Overflow lndicator
$\overline{\text{PIF}}$	I	Privileged Instruction Fault
RD/$\overline{\text{W}}$	O/Z	Read/Write IndicatesData Direction on A/D Bus
$\overline{\text{RDY}}$	I	Ready lnforms CPU of the Conclusion of External Bus Cycle
RESET	I	Reset Indicates Device Initialization
$\overline{\text{SYNCLK}}$	O	Interrupt Unit's Sync Clock
$\overline{\text{SYNC}}$	O	System Clock - CPU Sync Clock (External)
$\overline{\text{SYSCLK1}}$	O	System Clock (Internal)
$\overline{\text{TEST}}$	I	Test Enable
T1	O	Branch or Jump Control
VDD		Power (External), 5 Volts
GND		Ground

Table 1: Signal Definitions

2.2 BARREL SHIFTER

The Barrel Shifter is a 32-bit input, 16-bit output right shift network. A 32-bit operand may be shifted right arithmetically, logically, or cyclically up to 31 bit positions in a single machine cycle. While not directly accessible or visible to user programs, the Barrel Shifter is utilized by microcode to effect all shift, rotate, and normalize instructions with minimum execution time.

2.3 PARALLEL MULTIPLIER

The Parallel Multiplier performs a 4-bit multiplier by 24-bit multiplicand multiplication plus accumulation in a single machine cycle. Only four machine cycles are required to complete a 16-bit by 16-bit multiplication. Contained within the multiplier is a 48-bit product accumulation register with the lower 24 bits serving as a source operand register.

On each multiply machine cycle, the lower four bits of the accumulator are multiplied by 24 bits from the two ALU operand source buses (R and S). The lower 24 bits of this 28-bit product are then added to the upper 24 bits of the accumulator and the whole accumulator is shifted right four bits. This right shift makes room for the upper four bits of the product. The four bits shifted out are used in the next multiply iteration.

2.4 DUAL-PORT REGISTER FILE

The Register File is a dual port RAM structure containing 24, 16-bit registers. Sixteen of these registers are general purpose and user accessible. These user accessible registers - referred to as R0 through R15 - may be used as accumulators, index registers, base registers temporary operand registers, or stack pointers. The remaining eight registers are only accessible by microcode.

Adjacent registers are concatenated to effectively form 32-bit and 48-bit registers for storage of double precision and extended-precision operands, respectively. Instructions access these operands by specifying the register containing the most significant part of the operand, and the register set wraps around automatically under microcode control, e.g., R15 concatenates with R0 for 32-bit operands and R15 concatenates with R0 and R1 for 48-bit operands.

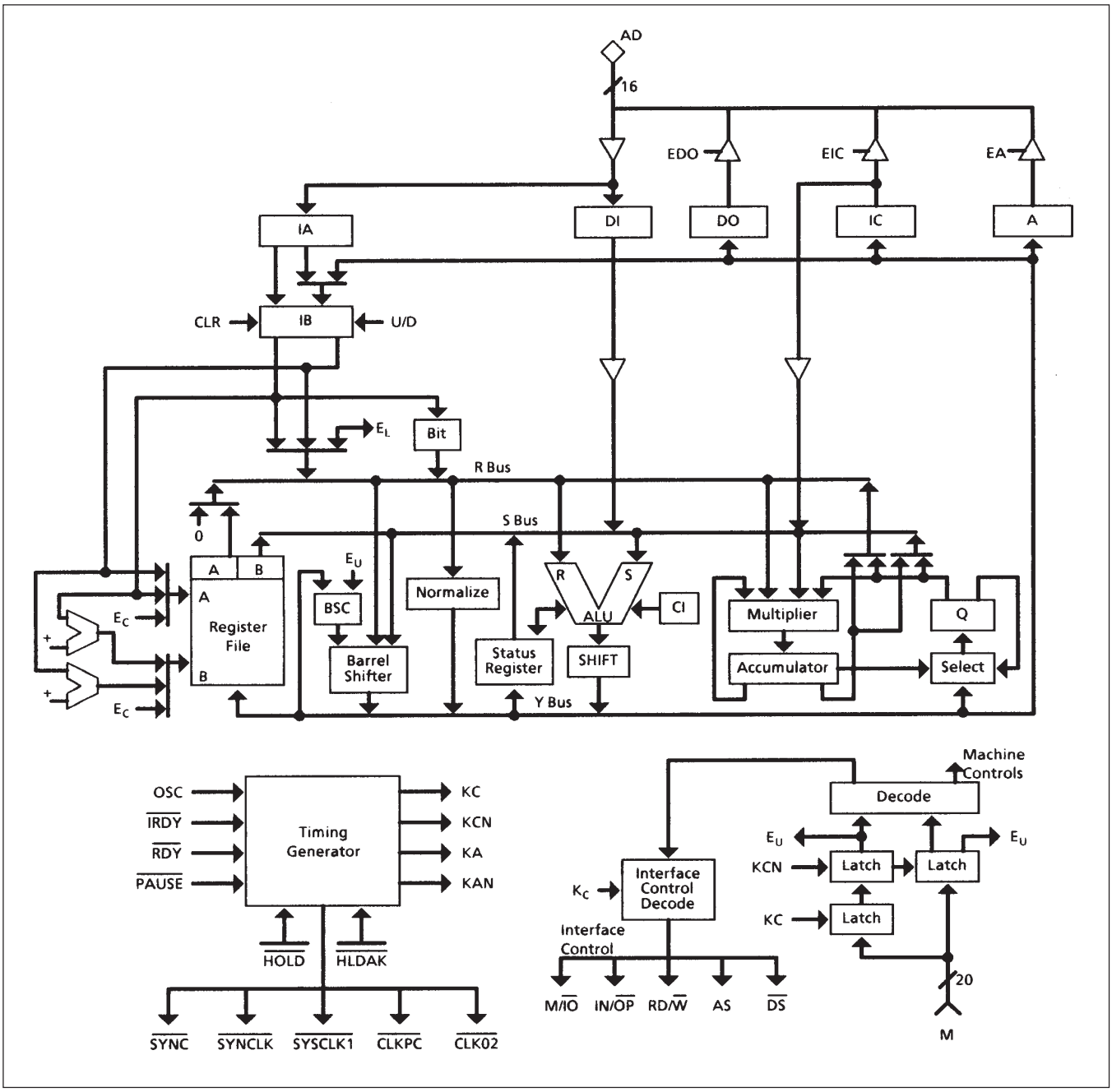


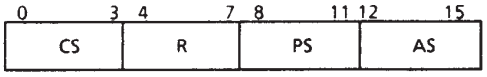
Figure 2: MA17501 Execution Unit Architecture

2.5 STATUS WORD REGISTER

The Status Word Register (SW) holds the condition status (CS) bits C, P, Z, and N generated by ALU operations. The SW also stores the address state (AS) and processor state (PS) fields. Figure 3 defines the Status Word Register storage format. The CS bits are stored with each logical, shift, and arithmetic operation performed by the ALU as required by MIL-STD-1750A and remain valid until changed by subsequent operations. The CS bits are interrogated during "jump on condition" and "instruction counter relative" MIL-STD-1750A branch instructions.

2.6 OPERAND TRANSFER REGISTERS

The Address (A), Data Output (DO), and Data Input (DI) registers are referred to as Operand Transfer Registers. These registers serve as storage buffers between internal EU buses and the EU's externally accessible address/data (AD) Bus. The DO register buffers data transferred from the EU to the AD Bus. The A register buffers operand addresses and XIO commands onto the AD Bus. The DI register buffers data transferred from the AD Bus to the EU .



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result<0
R	4 - 7	RESERVED
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

2.7 INSTRUCTION FETCH REGISTERS

The Instruction Counter (IC), Instruction A (IA), and Instruction B (IB) registers allow sequential instruction fetches to be performed without assistance from the ALU. The lC register, which holds the 16-bit address of the next instruction to be fetched from memory, is loaded automatically by reset, jump, or branch operations. Once loaded, it functions as a dedicated counter to sequence from one instruction to the next. The current IC contents may be stored in registers R0 through R15 or in memory (pushed onto a stack) to provide return linkages for subroutine calls. As part of the microcoded interrupt handling routine the IC is saved in memory via the interrupt linkage pointer.

Registers lA and IB provide an instruction look-ahead capability. In the case of 16-bit instructions, lB holds the instruction currently executing while lA holds the next instruction to be executed. In the case of 32-bit instructions, IB and lA each hold half of the instruction. IA and Dl (Dl stores the immediate operands) are loaded as the instruction in lA is transferred to lB for execution; if the instruction in lB uses an immediate operand, lA is reloaded with the next instruction while Dl maintains the immediate data. This overlapping of operations allows higher performance levels to be achieved.

2.8 BUSES

Three 16-bit wide buses (R, S, and Y) interconnect the EU data storage and computational elements. The R and S buses accept operands from selected EU data storage elements and route them to inputs of selected EU computational elements. The Y, or destination, bus serves to route computational results either back to EU data storage and computational elements or to the various operand transfer registers.

A 16-bit multiplexed Address/Data (AD) Bus provides a communications path between the EU, other components of the MAS281 chip set, and any other devices mapped into the chip set's address space. Data transfers between the AD Bus and the R, S, and Y buses are buffered by the operand transfer registers.

A 20-bit multiplexed microcode (M) bus provides a pathway between the Control Unit (CU) and the Execution Register (E) buffered microcode decode logic on the EU chip. Microcode placed on this bus by the CU controls all actions of the EU.

2.9 SYNCHRONISATION CLOCK GENERATION LOGIC

The Execution Unit generates all of the synchronisation clocks required by the chip set and CPU system. The EU converts an externally supplied oscillator signal into five synchronisation signals: SYNCN, SYSCLK1N,SYNCLKN, CLKPCN, CLK02N. The EU generates SYNCN for elements external to the chip set whereas SYNCLKN and SYSCLK1N are generated for the Interrupt Unit and internal EU synchronisation, respectively. SYSCLK1N is also brought out on a pin for use by external monitoring systems. The EU generates CLKPCN and CLK02N for use in the Control Unit. The CU uses CLKPCN to precharge the M Bus and transmit the first microword while CLK02N is used to transmit microword two.

The EU also contains the wait state generation interface. Failure of memory or I/O subsystems to drive RDYN low at the proper time during the DSN pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS and DSN, in the low state; and RD/WN, IN/OPN and M/ION in their current states for one or more oscillator cycles beyond the end of the normal five OSC cycle machine cycle. When RDYN is asserted low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

Additionally, IRDYN is used to signal completion of internal I/O command control of the Interrupt Unit (IU). The IU thus can extend the duration of the above mentioned bus signals. Failure of the IU to drive lRDYN low at the proper time during the DSN low pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS, and DSN in the low state; and lN/OPN, M/lON, and RD/WN in the state for the normal five OSC cycle machine cycle. When the IU asserts IRDYN low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

[NOTE: Whenever the EU is executing a machine cycle which requires IRDYN to drop low for completion, the machine cycle will be a minimum of six OSC cycles long. The maximum duration of this machine cycle depends on the length of time that the IU holds IRDYN high.]

3.0 INTERFACE SIGNALS

All signals comply with the voltage levels of Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND. A 500-ohm pull-up at the OSC input pin is recommended to damp line reflections.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix, e.g., HOLDN. Referenced signals that are not found on the MA17501 are preceded by the originating chip's functional acronym in parentheses, e.g., (IU)DMARN.

A description of each pin function, grouped according to functional interface, follows. The function acronym is presented first, followed by its definition, its type, and its detailed description. Function type is either input, output, high impedance (Hi-z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 5.0.

3.1 POWER INTERFACE

The power interface consists of one 5V VDD connection and three common GND pins.

3.2 CLOCKS

The Execution Unit provides the synchronisation clocks for the MAS281 chip set. Together these clocks form the basic operation cycle.

3.2.1 Oscillator (OSC)

Input. The MA17501 requires a single external oscillator input for operation. The EU converts the oscillator into the five other clocks listed in this section. To minimise skew between OSC edges and signals derived from OSC, the OSC rise and fall times should be minimised. It is recommended that a clock driver with high drive capability, such as a 54AS244, 54ALS244 or 54HST240, be used to drive the OSC input.

In order to avoid double clocking due to line reflections, a 500-ohm pull-up resistor, placed close to the EU, is recommended.

3.2.2 Synchronisation Clock (SYNCN)

Output. The MA17501 provides the MAS281 Synchronisation Clock output to synchronise external circuitry to the MAS281 machine cycle. The high-to-low transition of this signal indicates the start of a new machine cycle.

SYNCN cycles associated with external memory or I/O bus transactions are a minimum of five OSC cycles in duration and may be extended by inserting wait states via the RDYN input. SYNCN low indicates that either an address or XIO command is on the AD Bus; a high indicates data is on the bus. Wait states extend the high state of SYNCN.

SYNCN cycles associated with internal CPU operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a SYNCN cycle of seven OSC cycles duration. Though unlikely, this condition must be taken into account in implementing a RDYN generation circuit. Refer to the description of the RDYN signal for further details].

3.2.3 IU Synchronisation Clock (SYNCLKN)

Output. The SYNCLKN signal is a logical equivalent of the SYNCN signal provided for Interrupt Unit synchronisation.

3.2.4 System Clock (SYSCLK1N)

Output. SYSCLK1N is the MA17501's synchronization clock. It is the logical equivalent of SYNCN and SYNCLKN with the exception that during PAUSEN low or during HLDAKN low, SYSCLK1N is held in its low state. SYSCLK1N, like SYNCLKN, has a VSS to VDD logic level swing.

3.2.5 Precharge Clock (CLKPCN)

Output. CLKPCN is used by the MA17502 Control Unit (CU) to synchronize the precharging of the internal M Bus and most other CU operations to the MAS281 machine cycle.

CLKPCN cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input. CLKPCN low indicates that the internal CU M Bus is being precharged to the high state; the low-to-high transition places the lower 20 bits of a microinstruction on the external M Bus. Wait states extend the high state of CLKPCN. When PAUSEN or HLDAKN is low, CLKPCN is held low.

CLKPCN cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLKPCN cycle of seven OSC cycles duration.]

3.2.6 Phase 2 Clock (CLK02N)

Output. CLK02N is used by the MA17502 Control Unit (CU) in conjunction with CLKPCN to synchronize microinstruction transmission on the M Bus to the MAS281 machine cycle.

CLK02N cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input.

The high-to-low transition of CLK02N places the upper 20 bits of a microinstruction on the external M Bus. Wait states extend the trailing (based on SYNCN high-to-low beginning the machine cycle) low state of CLK02N. When PAUSEN or HLDAKN is low, CLK02N is held high.

CLK02N cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLK02N cycle of seven OSC cycles duration.]

3.3 BUS CONTROL

This group of signals is provided to control Address/Data (AD) bus transmissions (See Figure 4). The signals indicate when address or data information is on the AD Bus and what type of transaction is taking place during a particular machine cycle.

3.3.1 Address Strobe (AS)

Output/Hi-z. AS high indicates that the Address/Data (AD) Bus contains address information. The address information is assured stable at the high-to-low transition of this signal. In this way, AS provides the necessary control for a system Address Bus transparent latch system interface.

The Interrupt Unit uses AS to extract the XIO command information off the AD Bus for internally decoded XIO commands, and the Memory Management Unit/Block Protection Unit (MMU(BPU)) uses AS to extract address information for memory management and block protection functions, and to extract XIO command information for MMU(BPU) decoded XIO commands.

AS is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. During internal non-AD Bus related CPU operations, AS is held low for the entire machine cycle via microcode control.

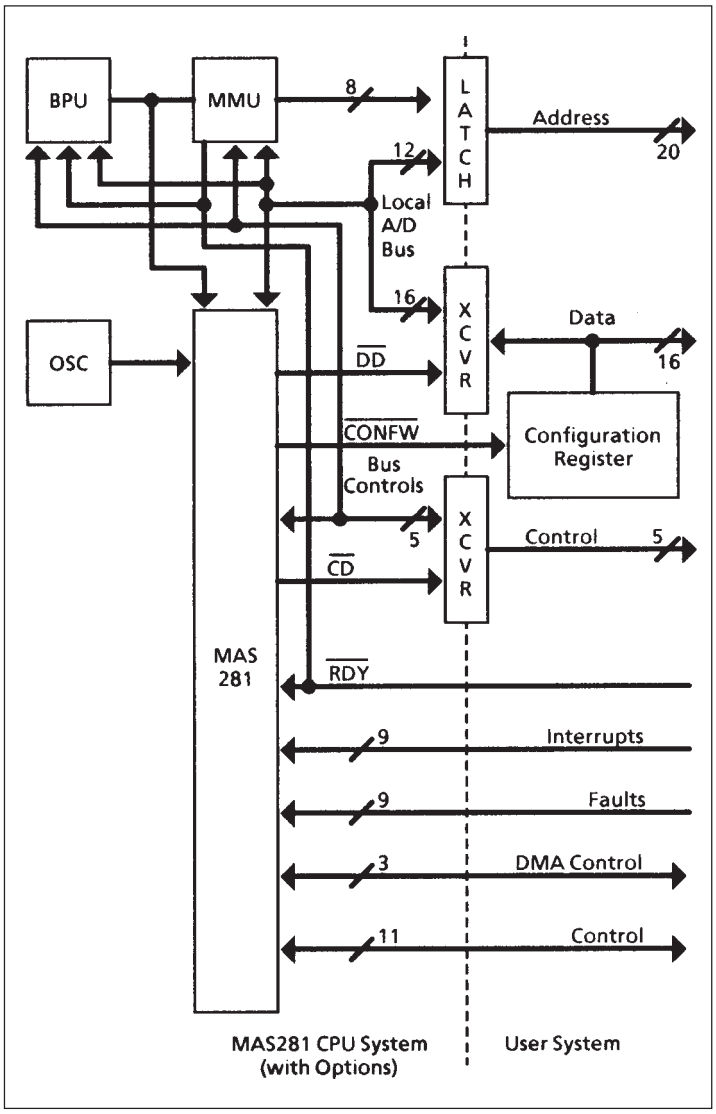


Figure 4: Typical MAS281/MA17504 System Interface

3.3.2 Data Strobe (DSN)

Output/Hi-z. DSN low indicates that data is on the AD Bus (write/output cycles) or that the MAS281 AD Bus drivers are in the high-impedance state (read/input cycles). For write/output cycles, the data is guaranteed stable at the low-to-high transition of DSN. For read/input cycles, the DSN low-to-high transition indicates the acceptance of data by the MAS281 (SYSCLK1N high-to-low transition latches AD Bus data into the lA and Dl registers).

DSN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. DSN is held high, for the entire machine cycle, during internal non-AD Bus operations via microcode.

3.3.3 Read/Write (RD/WN)

Output/Hi-z. RD/WN defines the direction of data flow on the bidirectional AD Bus and provides read/write cycle information to the MMU(BPU) for write protection control. RD/WN high indicates a read/input bus cycle and data transfer to the MAS281. RD/WN low indicates a write/output bus cycle and data transfer from the MAS281.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. RD/WN is placed in the high impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.4 Memory/lnput-Output (M/ION)

Output/Hi-z. M/lON defines the type of device involved in the data transfer occurring on the AD Bus and provides functional control for the lnterrupt Unit (lU) and the Memory Management Unit/Block Protection Unit (MMU(BPU)). The lU ignores memory transfer AD Bus activity and the MMU(BPU) uses M/lON to decide whether to decode the address information on the AD Bus as an MMU(BPU) XlO command or a memory address. M/lON high indicates a memory access, and M/lON low indicates an input-output operation.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. M/lON is placed in the high impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. M/lON is raised high, for the entire machine cycle, during internal non AD Bus operations via microcode.

3.3.5 Instruction/Operand (IN/OPN)

Output/Hi-z. lN/OPN high indicates an instruction is to be read from memory during the current AD Bus cycle. IN/OPN is low for all other MAS281 directed AD Bus transfers. The Memory Management Unit/Block Protection Unit (MMU(BPU)), when configured as a MMU, uses lN/OPN to select the proper page register set within the specified page register group.

IN/OPN is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. lN/OPN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.6 Ready (RDYN)

Input. During external AD Bus transfers (those dealing with devices external to the MAS281 chip set), a low is required on this input to allow the MAS281 machine cycle to complete (high-to-low transition of SYNCN). RDYN high is used to prolong the data portion of the machine cycle (SYNCN high) to accommodate slow memory and l/O devices. The MAS281 assumes memory or l/O devices are NOT ready to provide (accept) data to (from) the AD Bus, and requires these devices to signal their readiness via the RDYN input.

A low on RDYN, enveloping the current machine cycle's fifth (or later) OSC cycle high-to-low transition, allows the current machine cycle to complete (SYNCN high-to-low transition) at the following low-to-high transition of the OSC input.

3.4 BUSES

The following is a discussion of the communication buses connecting the MA17501 to the other chips of the MAS281 set. The AD Bus transfers all data and instructions and the M Bus provides the microcode instructions from the MA17502.

3.4.1 Address/Data Bus (AD Bus)

Input/Output/Hi-z. These signals comprise a 16-bit bidirectional multiplexed address and data bus. During external bus transfers, the AD Bus accommodates the transfer of address and data information between the MA17501 and memory, or l/O ports. During internal bus operations, the AD Bus provides additional communication among the Execution, Control, Interrupt and Memory Management/Block Protection Units. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic one and a low corresponds to a logic zero.

Address information is valid on the bus at the AS high to-low transition. The RD/WN signal indicates the MA17501 AD Bus drivers state during the data portion of the bus cycle (DSN low) and the M/lON function defines the type of device the transfer is with. The AD Bus drivers are placed in the high impedance state during Read operations (DSN low), during DMA cycles by PAUSEN low, and during the Hold state by HLDAKN low.

3.4.2 Microcontrol Bus (M Bus)

Input. The M Bus is a 20-bit multiplexed microcontrol bus which provides microcoded control to the EU. The Control Unit multiplexes the 40-bit microcode instructions into two 20-bit words. The upper 20 bits are placed on the M Bus by the CLKPCN low-to-high transition and the lower 20 bits are placed on the M Bus by the trailing high-to-low transition of CLK02N. The microinstruction is reassembled in the EU's Execution (E) register and used to control EU functions during the next machine cycle. M19 is the most significant bit position and M00 is the least significant bit position for both microwords. The high order 20 bits are transmitted first, followed by the low order 20 bits of the microinstruction. A high on this bus corresponds to a logic one and low corresponds to a logic zero.

3.5 SYSTEM SUPPORT INTERFACE

The system support interface signals have control over functions that affect the chip set as a whole.

3.5.1 Processor Pause (PAUSEN)

lnput. PAUSEN is driven low by the lnterrupt Unit upon acknowledgement of a DMA transfer request. A low on PAUSEN causes the EU to place all the bus control signals (AS, DSN, M/lON, RD/WN, IN/OPN) and the AD Bus in the high impedance state, and to disable all clock outputs, except for SYNCLKN and SYNCN. The requesting device maintains control of the AD Bus and bus control lines until (lU)DMARN is raised high, thus causing PAUSEN to raise high.

lt is recommended that the MAS281 chip set be buffered to the memory/input-output system. lf an MMU(BPU) peripheral chip is used for memory expansion/protection it must reside on the MAS281 side of these buffer transceivers (see Figure 4). Thus, for a DMA device to access the MMU(BPU), the MAS281 AD Bus and bus control signal drivers must be in the high impedance state to allow the DMA device to drive these signals. The interrupt Unit also provides the CDN signal for the directional control of the bus control transceivers.

3.5.2 Processor Hold Request (HOLDN)

lnput. A low on this input suspends all chip set functions (except SYNCN and SYNCLKN) at the end of the current MIL-STD-1750A instruction. The AD Bus and bus control functions (AS, DSN, M/ION, lN/OPN, RD/WN) are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. The internal synchronisation clocks are placed in an inactive state, which halts further instruction sequencing until HOLDN is released. As with DMA cycles, the reason for this is to allow access to the MMU(BPU) if an expanded memory system is used. The (lU)CDN output is provided for control bus transceiver directional control during the Hold state. This input should be synchronised to AS falling.

3.5.3 Processor Hold Acknowledge (HLDAKN)

Output. HLDAKN drops low after reaching the end of the MIL-STD-1750A instruction during which HOLDN was pulled low, or after encountering a BPT software instruction. The Hold state is terminated by raising HOLDN high (if HOLDN low initiated the Hold state), or by pulsing HOLDN low (if the Hold state was initiated by a BPT instruction). During the Hold state, software execution is suspended and the MAS281 interface functions are placed in the high impedance state to allow a monitor system to take control of the memory/input-output system.

3.6 INTER-CHIP CONTROL

The following signals perform control functions internal to the MAS281 chip set. These functions include microcode execution branching control and arithmetic error indication.

3.6.1 Internal Ready (IRDYN)

Input. The IRDYN signal is the means by which Interrupt Unit (IU) command cycles, involving the AD Bus, are completed. The lU drops lRDYN low when the XlO command has been decoded and allows the six OSC period machine cycle to complete. The IRDYN and RDYN signals are effectively ORed together to control the EU clock generation circuitry; therefore, RDYN should be high during lU decoded XlO commands.

3.6.2 Interrupt Unit Microinstruction Enable (INTREN)

Output. The Execution Unit controls the lnterrupt Unit (lU) 3-bit microcode interface through the use of the INTREN signal. lNTREN low enables the lU microcode decoding logic. lU functions handled through microcode are; enable/disable DMA interface XlO command control, set Normal Power-Up discrete, load fault register, and read encoded 4-bit vector identifying the highest priority pending interrupt.

Machine cycles during lNTREN low are a special case of internal non-AD Bus operations. These cycles are denoted by a six OSC period machine cycle.

3.6.3 Overflow Indicator (OVIN)

Output. OVlN is an indication that a fixed-point overflow condition, as specified in MIL-STD-1750A, has occurred during an operation. The Interrupt Unit accepts this as an input to the pending interrupt register level four interrupt bit.

3.6.4 Privileged Instruction Fault (PIFN)

lnput. PIFN low is an indication to the Execution Unit that a fault, requiring the current MIL-STD-1750A instruction to be aborted, has occurred. The faults that cause the instruction abort are 0, 5, and 8 which are, respectively, memory protect error ((IU)MPROEN low), an out-of-bounds memory/input-output address ((lU)EXADE low), or a bus fault timeout. ln response to PIFN low, the EU maintains AS low, DSN high, and forces the M/lON signal high for two machine cycles. ln addition, the EU will internally complete the current SYNCN cycle and resume operation. This allows the Control Unit to sequence to the interrupt handling routine without affecting the bus status.

3.6.5 Branch or Jump Control (T1)

Output. The Execution Unit raises the T1 signal high to indicate a microcode conditional branch condition is true. The Control Unit accepts T1 and feeds it into the microcode address multiplexer where microinstruction branches are effected.

3.6.6 Test Microword (TESTN)

lnput. The TESTN signal is used during chip test to load 40-bit microinstructions into the EU execution register. TESTN low loads E39 (MSB) to E20, and TESTN high loads E19 to E00 (LSB). TESTN should be pulled-up to VDD in customer applications.

4.0 OPERATING MODES

The following discussions detail the MAS281 chip set operating modes from the perspective of the Execution Unit. MAS281 operating modes involving the MA17501 include: (1) Initialisation, (2) lnstruction Execution, (3) Interrupt Servicing, (4) Fault Servicing, (5) DMA Support, and (6) Software Development Support.

4.1 INITIALISATION

RESET starts the chip set microcoded initialisation sequence, but also affects the Execution Unit Circuitry directly. When RESET is raised high, the Hold state acknowledge signal (HLDAKN) is forced high thus releasing the MAS281 from the Hold state (if changing HOLDN is unable to release the Hold state). RESET also forces the clock generation circuitry to create a five OSC period machine cycle by disabling state machine inputs that vary the machine cycle length.

Upon releasing RESET, the EU Hold State circuitry is enabled and the clock generation circuitry is allowed to function normally. HOLDN will not have an effect on chip set operation until the initialisation routine has completed because the microcode branch to the Hold routine is disabled.

The microcoded initialisation routine clears the lnstruction Counter (lC), Status Word Register (SW), and Register File (R00-R15) and performs the BIT. The successful completion of the BIT is necessary to guarantee the register file is cleared at the end of the initialisation routine.

The microcoded BIT exercises all legal microinstruction bit combinations and tests all internally accessible structures of the MAS281. For the Execution Unit this includes the full Register Set, ALU, Multiplier, Barrel Shifter, and Macroflag logic. Table 2 details the tests performed by each of the five BIT subroutines.

lf any part of BIT fails, an error code identifying the failed subroutine is loaded into the lnterrupt Unit Fault Register (via the AD Bus), BIT is aborted, and NPU is left in the low state. Table 2 defines the coding of the BIT results. (lNTREN enables microcode control of the lnterrupt Unit (lU) to raise NPU high (if BIT passes) and load BIT error codes (if BIT fails) into the lU Fault Register).

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero (page zero) from the Start-Up ROM (if implemented). Whether or not BIT passes, the processor will begin instruction execution at this point.

[NOTE: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, the Timers A and B must be clocked for BIT success.]

BIT	Test Coverage	BIT Fail Codes ($FT_{13,14,15}$)	Cycles
1	Mlcrocode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, Pl, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15	110	154
5	Timer A Timer B	111	763
-	BIT Pass/Fail Overhead	-	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15.

Table 2: MAS281 BIT Summary

4.2 INSTRUCTION EXECUTION

Instruction execution is characterised by a variety of operations composed of various types of machine cycles. The Execution Unit contains the clock generation circuitry that creates the different machine cycles depending on the particular operation being performed at the time. These operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by the PAUSEN (denoting DMA operations) clock generation circuitry input, and at the beginning of any given MIL-STD-1750A instruction by an (IU)IRN or HOLDN low input to the Control Unit.

4.2.1 Internal CPU Cycles

All CPU data manipulation and housekeeping operations are performed using internal CPU cycles. Internal CPU cycles are either five or six OSC periods long and are characterised by AS low and DSN, (IU)DDN, and M/ION high. Section 5.0 provides timing characteristics for internal CPU cycles.

The majority of Internal CPU Cycles are five OSC period machine cycles. Six OSC period machine cycles occur when executing conditional jump or branch microinstructions; the EU is calculating the branch condition to determine the state of the T1 output signal.

4.2.2 Instruction Fetches

Instruction fetches are used to keep the instruction pipeline full. This ensures that the next instruction is ready for execution when the preceding instruction is completed.

During jump and branch instruction execution the pipeline is flushed, then refilled via two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of the interrupt and Hold processing.

Instruction fetches are five (minimum) OSC period machine cycles characterised by IN/OPN, M/lON, and RD/WN high. Instruction fetches use pipeline registers lA and IB, the instruction counter (IC), and the data input register (Dl). Assuming an empty instruction pipeline (as a result of a reset, jump or branch), the contents of IC are placed on the AD Bus as an address. The returned value (the instruction) is stored in the IA register. The lC register is incremented (dedicated counter mode) and the next fetch is performed.

This second returned value, which may be an instruction or an immediate operand, is stored in both the lA and Dl registers as the previous contents of IA advance to the IB register to be decoded into their microcoded routine. If the second returned value is an immediate operand, a third instruction fetch will occur with the instruction being loaded into lA only; Dl retains the immediate operand.

The data portion (SYNCN high) of instruction fetch cycles can be extended beyond their minimum five OSC periods by use of the RDYN signal. RDYN held high during the high-to-low transition of the machine cycles fifth OSC cycle will extend the data portion of the machine cycle. The machine cycle can be completed at any succeeding OSC cycle high-to-low transition by enveloping this OSC edge with RDYN low.

4.2.3 Operand Transfers

Operand transfers are used to obtain operands to be used by an instruction and to save any results of an instructions execution. Machine cycles associated with operand transfers are a minimum of five OSC periods in duration. The RDYN signal can be used to insert wait states into the data portion of the machine cycle (SYNCN high) to accommodate slow memory.

Operand transfers use the address register (A), data input register (DI), and data output register (DO). Before the operand transfer begins, the Execution Unit calculates the effective operand address and stores this value in A.

For write transfers the EU loads the operand into DO. For operand ready cycles the EU latches the operand from the AD Bus into DI at the SYSCLK1N high-to-low transition.

All operand transfers between the MAS281 and memory are referenced to the AS and DSN bus control signals and are characterised by IN/OPN low, M/ION and CDN high, and RD/WN (high, read; low, write).

The EU first places the contents of A on the AD Bus at the SYSCLK1N high-to-low transition. Shortly following, AS is raised high to enable the system address bus transparent latch. This address is assured valid at the high-to-low transition of AS. At the SYSCLK1N low-to high transition, DSN drops low to indicate the contents of DO have been placed on the AD Bus (write) or the EU AD Bus drivers have been placed in the high impedance state (read).

DSN subsequently raises high when the output data is stable, prior to SYSCLK1N dropping low, or raises high in response to SYSCLK1N dropping low to indicate the EU's acceptance of the input data.

All operand transfer cycles are allowed to complete via the RDYN input. During the data portion of the cycle the EU assumes memory is NOT READY, and requires RDYN low to signal the memory's readiness to complete the cycle. If RDYN is high at the high-to-low transition of the fifth OSC cycle within the operand transfer cycle, a wait state will be injected (one OSC period at a time) for each OSC high-to-low transition that RDYN remains high. Memory readiness, thus cycle completion, is signalled by RDYN low enveloping a subsequent OSC high-to-low transition.

4.2.4 Input/Output Transfers

Input/Output transfers are characterised by M/ION and IN/OPN low, and RD/WN (high, input; low, output). AS and DSN operate as during operand transfers. Two different types of input/output transfers are controlled by the Execution Unit: internal and external.

Internal I/O transfers involve all XIO commands that are decoded by the Interrupt Unit (IU) and use the local AD Bus to transfer response data. These commands are listed in Table 3 (the only exception is RCW; it is an IU decoded, IRDYN completed, External I/O command). Internal XIO commands implemented in the IU (per Table 3) use a six OSC period machine cycle and the IRDYN cycle completion input. Internal XIO commands implemented in the MA31751 MMU/BPU use a minimum five OSC period machine cycle. The system RDYN generator provides the RDYN cycle completion input to the EU.

The term "local AD Bus" in this context refers to the AD Bus on the processor side of the system data bus demultiplexing transceivers. The three chips of the MAS281 and the MA17504 (in either configuration) reside on the local AD Bus and communicate to the user system through the required address and data bus buffers, as depicted in Figure 4.

External I/O transfers involve all XIO and VIO instructions not included under Internal I/O transfers. They execute during a minimum five OSC period machine cycle that is extendible via RDYN, as previously described.

4.3 INTERRUPT SERVICING

Interrupts are latched into the Interrupt Unit (IU) pending interrupt register by the SYNCLKN high-to-low transition. The IU signals the Control Unit (CU) that an interrupt is pending and the CU branches to the microcoded interrupt handling routine at the completion of the currently executing MIL-STD-1750A instruction.

The EU supports the interrupt handling routine by enabling microcode control of the IU at the proper time via the INTREN signal and by calculating the memory addresses of the service and linkage pointers based on the 4-bit interrupt priority code transmitted by the IU. Machine cycles during which INTREN is low are six OSC periods in length. During these INTREN cycles, DSN and M/ION are high, and AS is low.

The EU also provides a hardwired interrupt to the IU. the OVIN interrupt signals a fixed-point arithmetic overflow.

4.4 FAULT SERVICING

The Interrupt Unit (IU) latches fault inputs into the fault register on the high-to-low transition of SYNCLKN. Faults other than 0, 5, and 8 latch a level one pending interrupt in the IU and the interrupt sequencing proceeds as previously explained. Faults 0, 5, and 8 caused during non-DMA AD Bus transactions demand more immediate attention; the MIL-STD-1750A instruction during which the fault occurred must be aborted.

PIFN indicates to the Control Unit that one of these faults has occurred and forces a branch to the "next instruction fetch'' microinstruction so that the interrupt caused by the PIFN fault can be serviced immediately. Under normal instruction execution circumstances, the bus control signals would operate during the machine cycle between the fault and the instruction fetch machine cycle. PIFN causes the bus control signals AS and DSN to stay in their inactive state during this transitional machine cycle to allow the branch to the microcoded interrupt routine without performing any AD Bus transactions.

4.5 DIRECT MEMORY ACCESS

The Interrupt Unit DMA interface logic signals the Execution Unit (EU) that it has acknowledged a DMA request (PAUSEN low). PAUSEN low causes the EU to halt the synchronisation clocks CLK02N (high), CLKPCN (low), and SYSCLK1N (low); disables clock generation circuitry input that could vary the machine cycle length; and places all bus control signals and the AD Bus in the high impedance state. The SYNCN and SYNCLKN clocks continue to operate with a five OSC cycle period. Upon removal of PAUSEN by the Interrupt Unit, the MAS281 resumes microinstruction execution where it was interrupted.

4.6 SOFTWARE DEVELOPMENT SUPPORT

The Execution Unit responds to a HOLDN signal by suspending all internal operations upon completion of the currently executing instruction. Microcode, from the Control Unit, directs HLDAKN low during the third SYNCN cycle after HOLDN has been pulled low and the previous instruction has been completed. M/ION, RD/WN, IN/OPN, AS, DSN, and the AD Bus are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. Raising HOLDN releases the MAS281 from the Hold state and instruction execution begins by refilling the pipeline.

The execution of a BPT instruction also causes HLDAKN to drop low and the bus control signals and AD Bus to be placed in the high impedance state. A low pulse on HOLDN releases the MAS281 from the BPT initiated Hold state.

Operation	Command Code(Hex)	Mnemonic	Cycles*		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt Request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Timer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
Input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	S0XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	S1XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 3: Internal I/O Command Summary

5.0 TIMING CHARACTERISTICS

This section provides the detailed timing specifications for the MA17501. Figure 5 depicts the test loads used to obtain timing data. Figures 6 through 20 depict the timing waveforms associated with various MA17501 signals. Table 5 provides values for parameters specified in the timing waveforms. All timing values provided in Table 5 are valid over the full military temperature range (-55°C to +125°C), and are measured from 50% point to 50% point (50% VDD supply voltage, unless otherwise specified). Crosshatching in Figures 6 through 20 indicates either a "don't care" or indeterminate state.

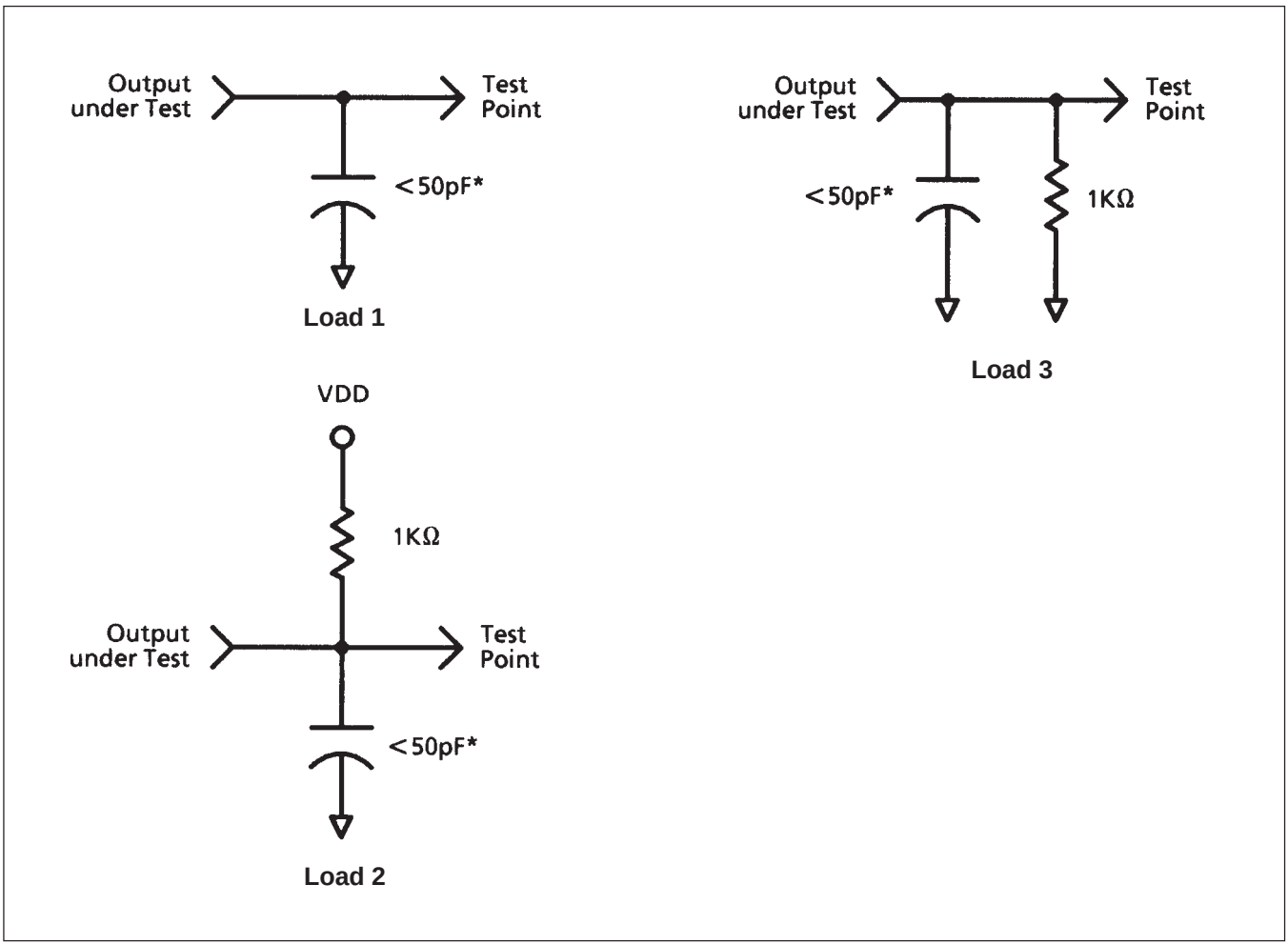


Figure 5: Test Loads

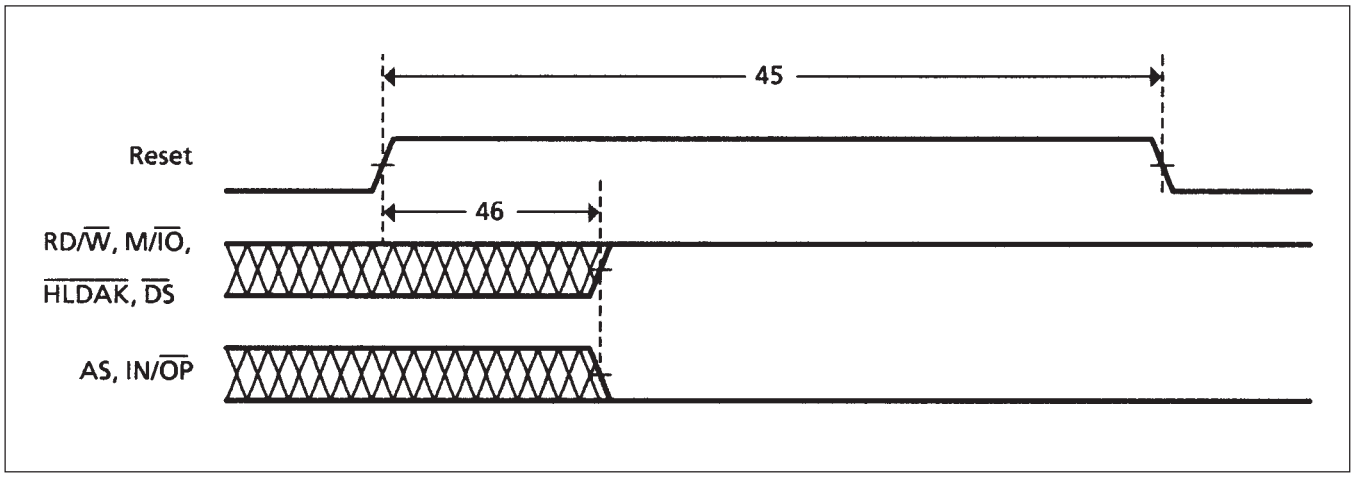


Figure 6: Reset Timing

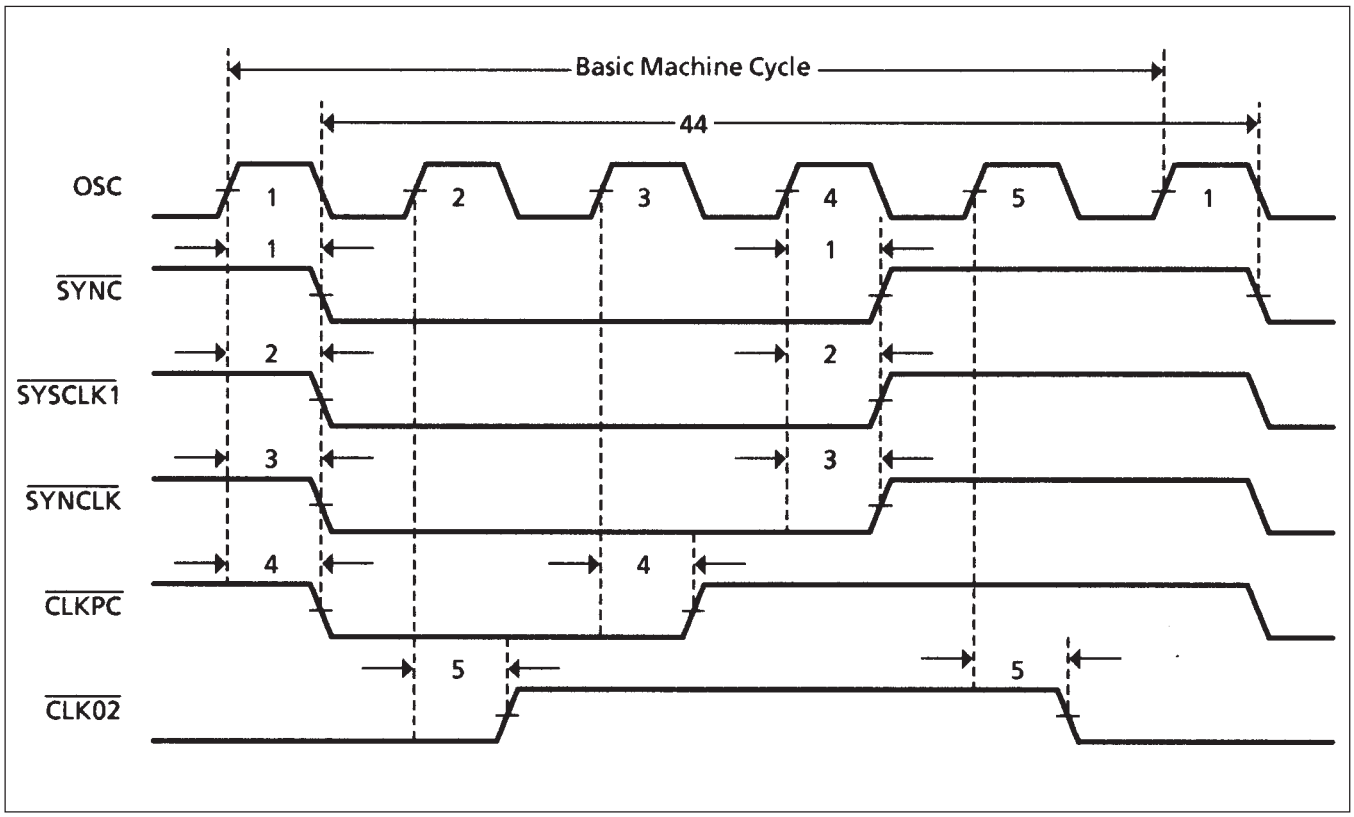


Figure 7: Basic Clock Timing

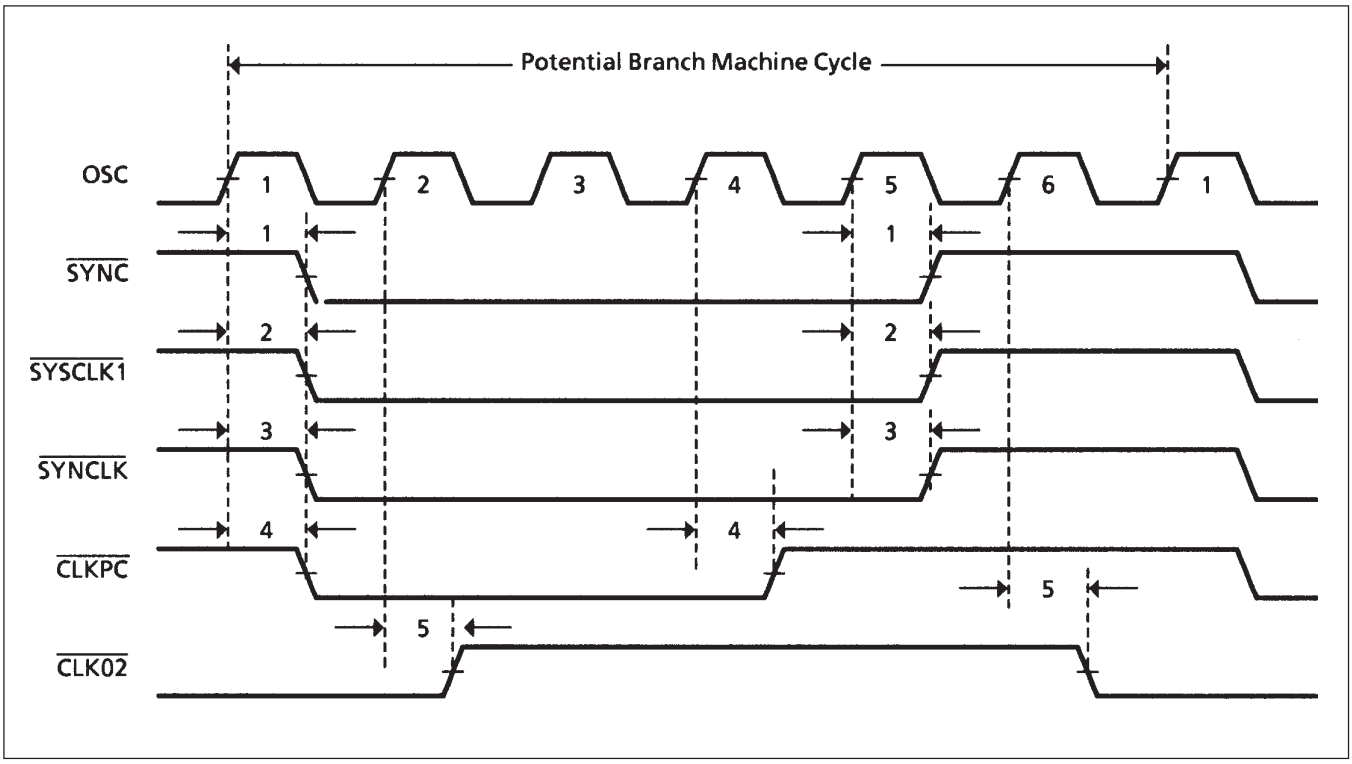


Figure 8: Potential Branch Clock Timing

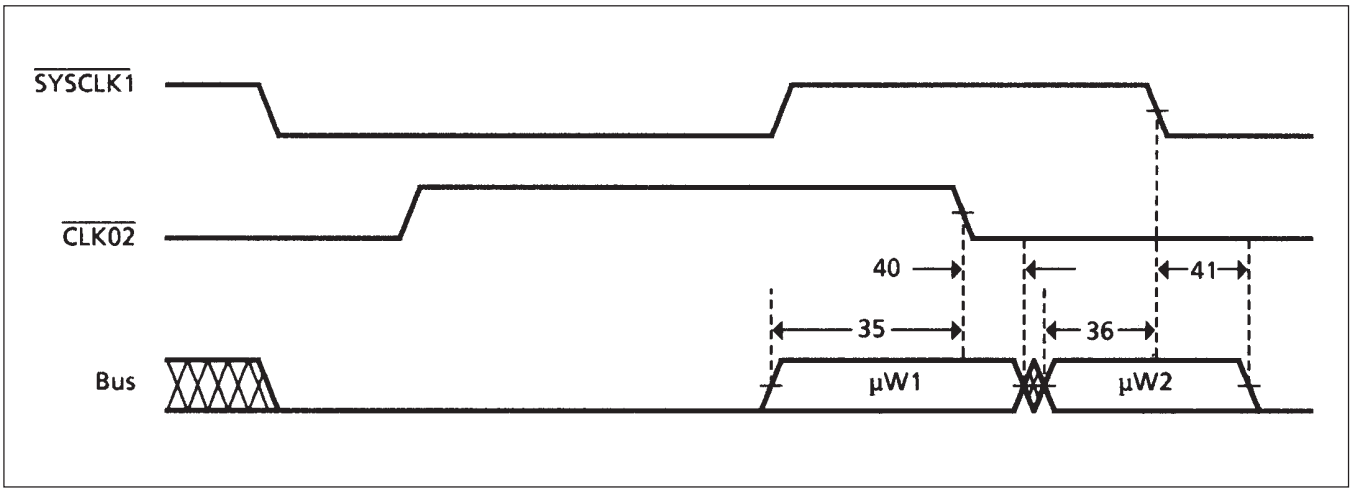


Figure 9: Microcode Bus Timing

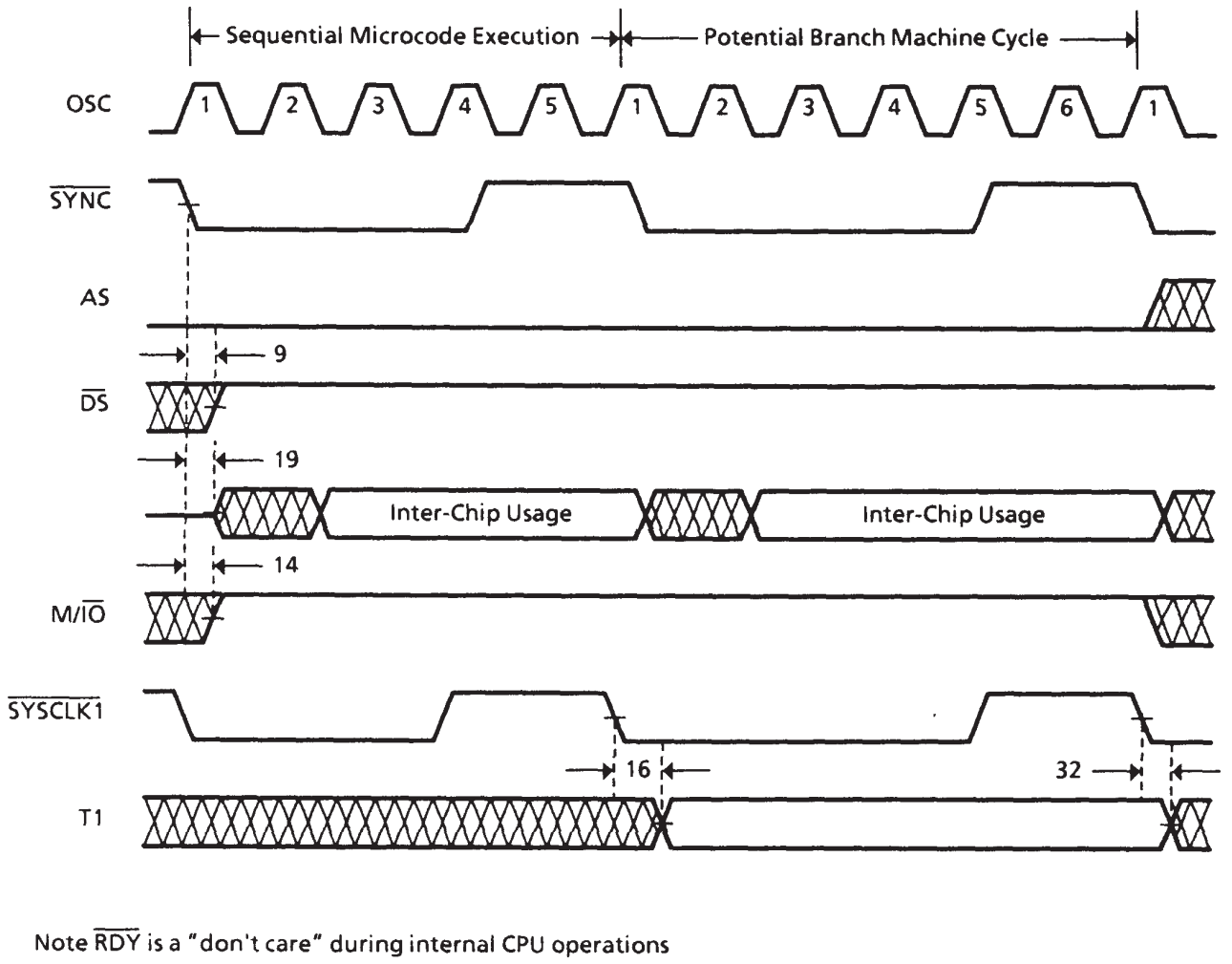


Figure 10: Internal Processor Cycle

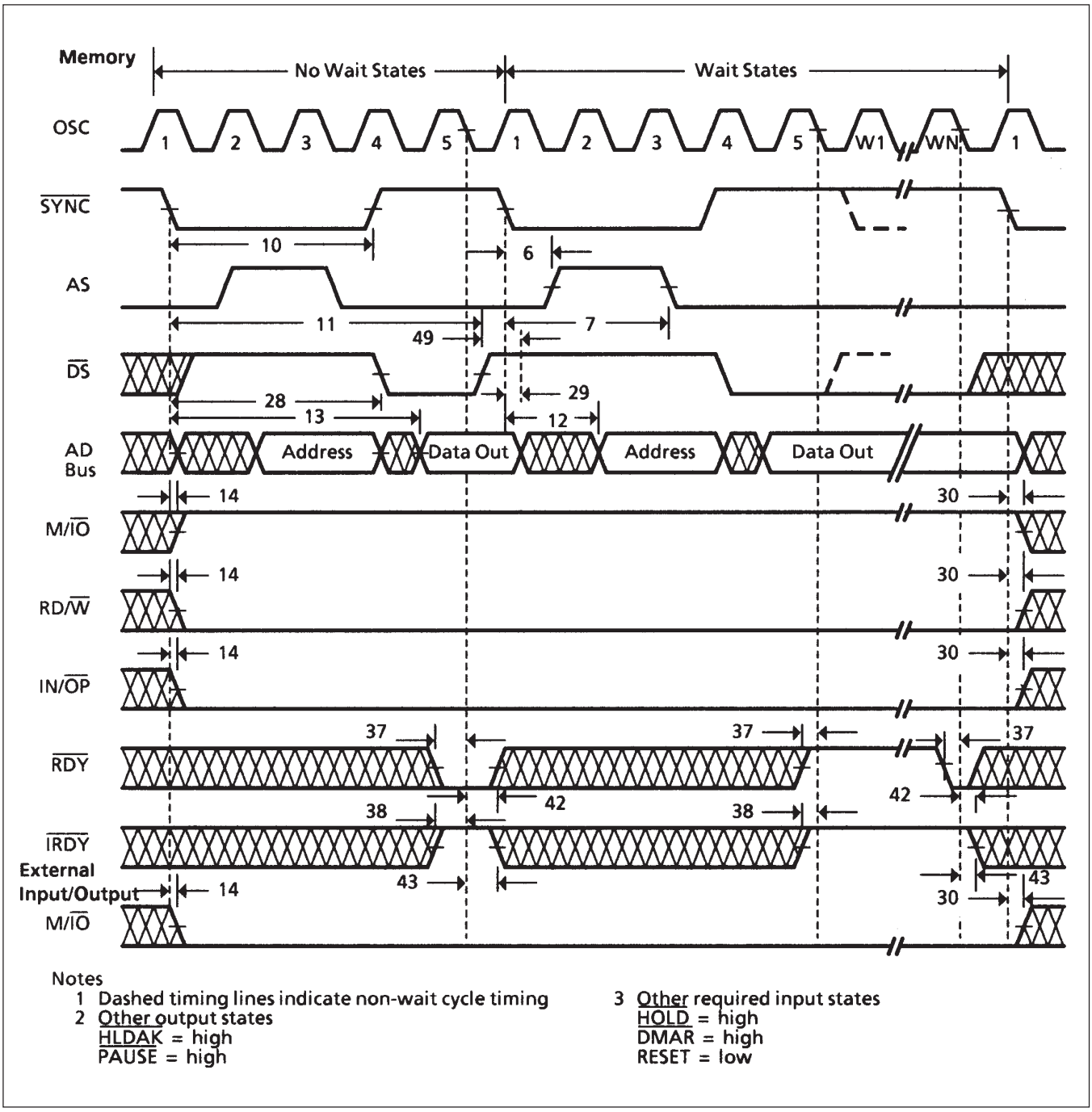


Figure 11: Write Transfer Timing

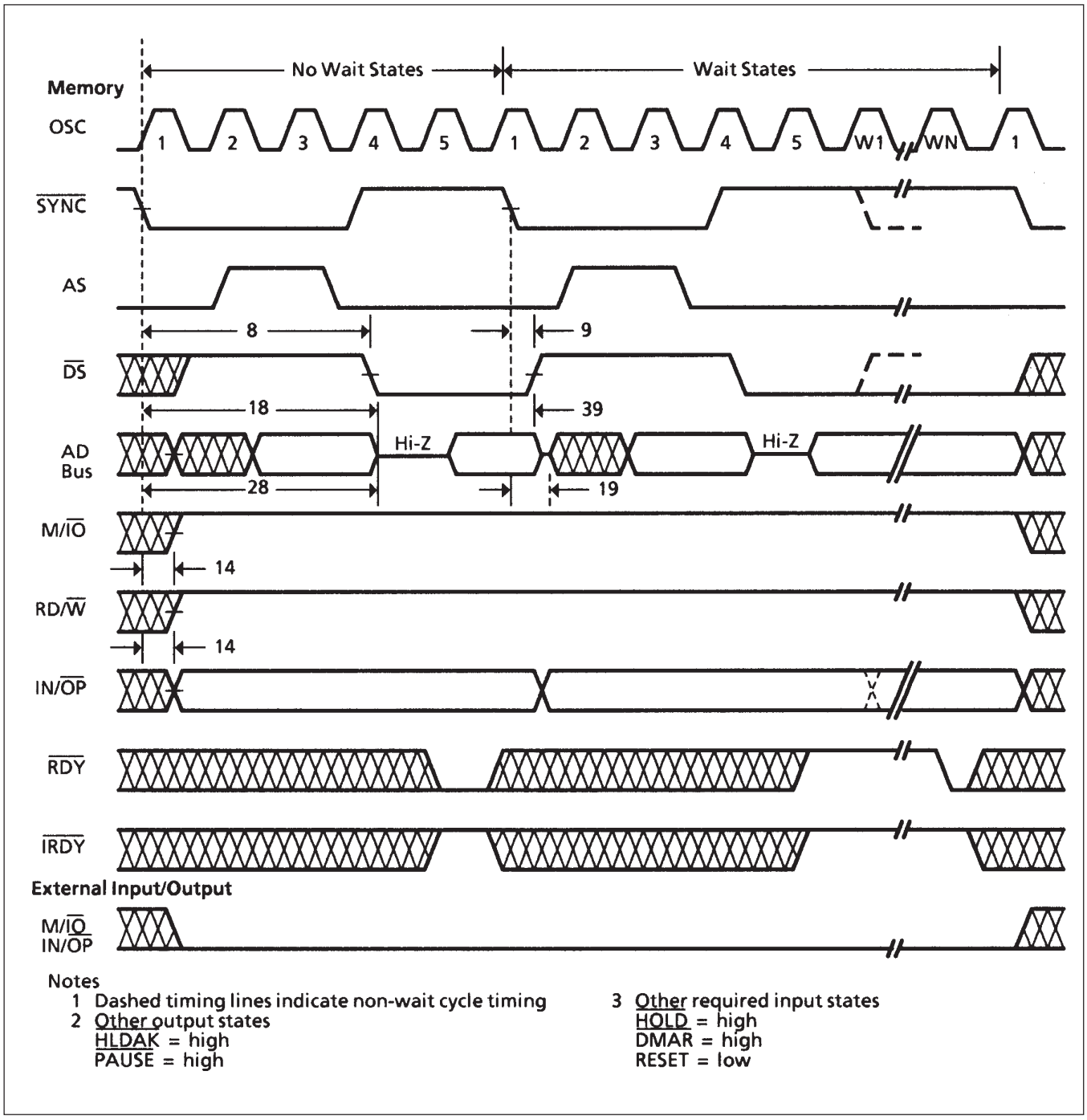


Figure 12: Read Transfer Timing

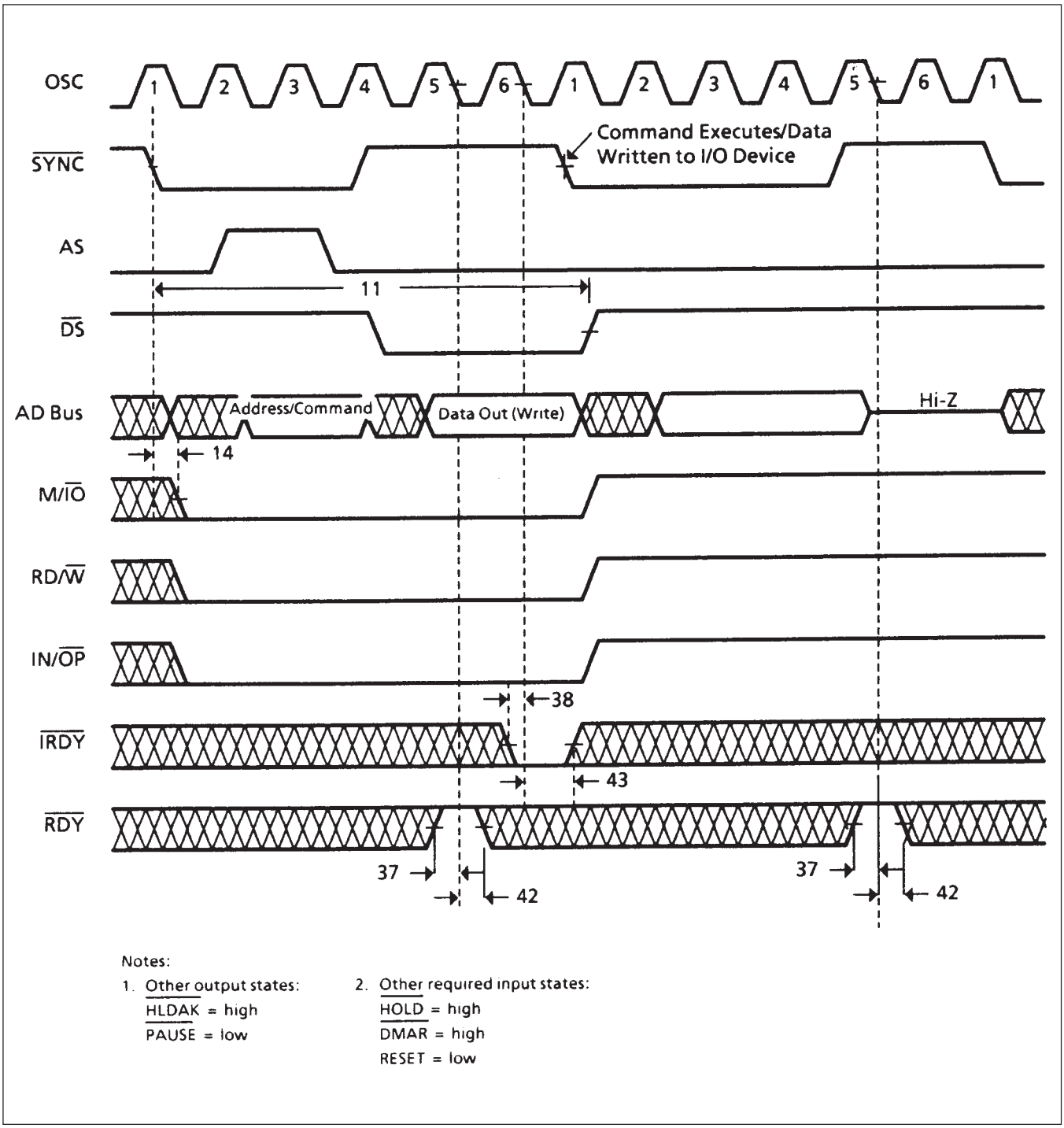
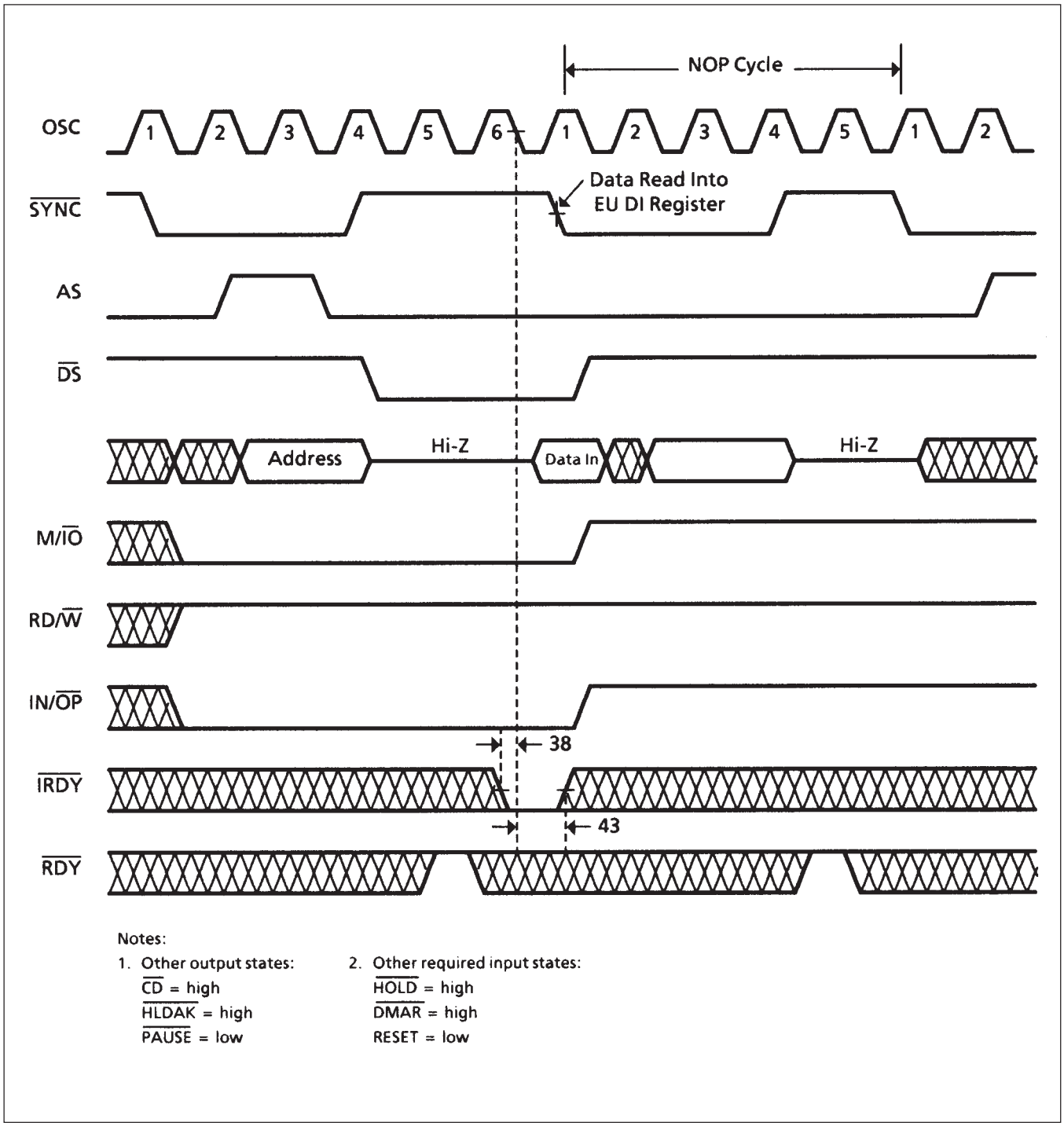


Figure 13: Internal I/O Timing - Write/Command



Notes:

1. Other output states:
   - CD = high
   - HLDAK = high
   - PAUSE = low
2. Other required input states:
   - HOLD = high
   - DMAR = high
   - RESET = low

Figure 14: Internal I/O Timing - Read

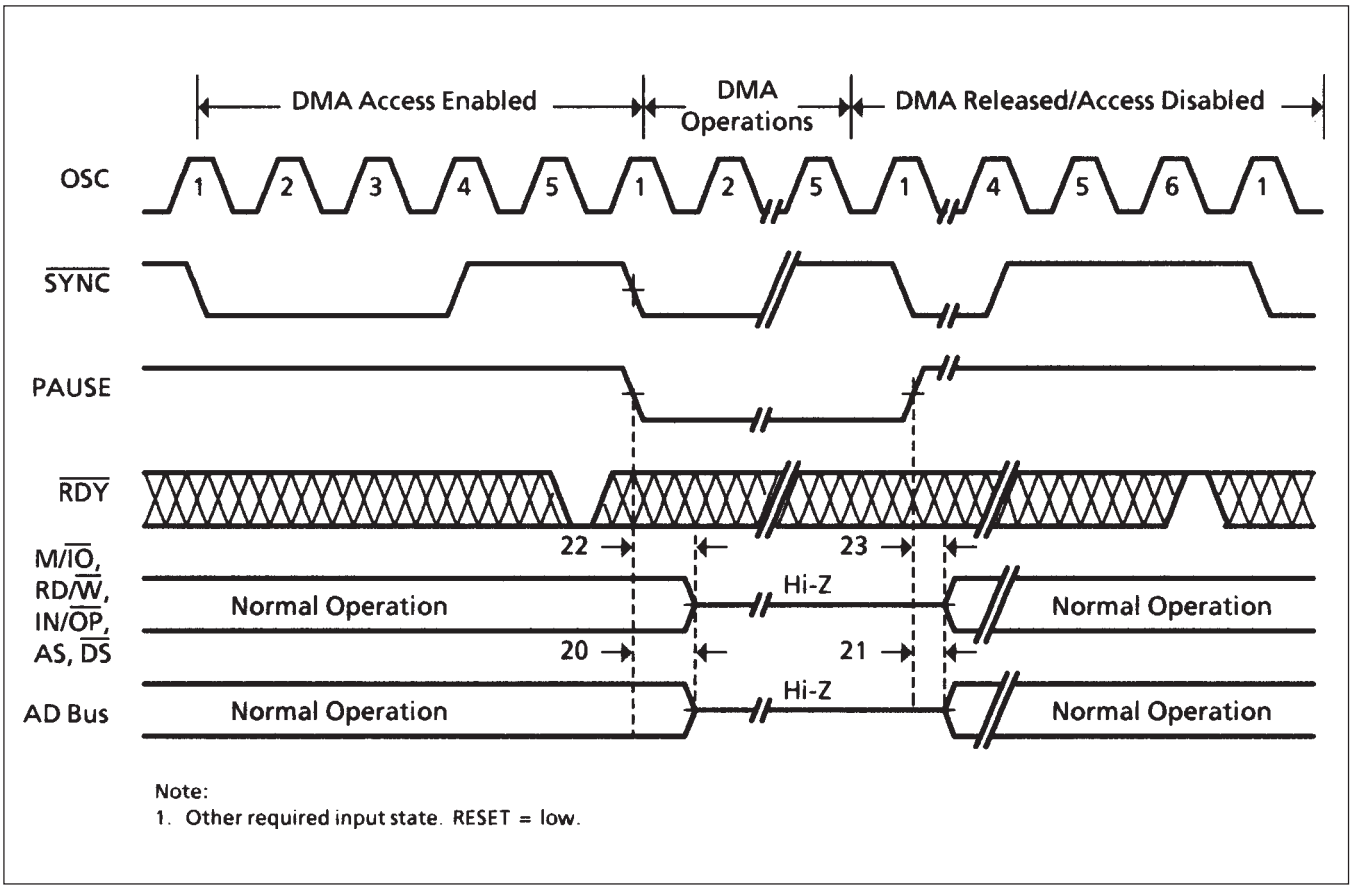


Figure 15: DMA Access/Release Timing

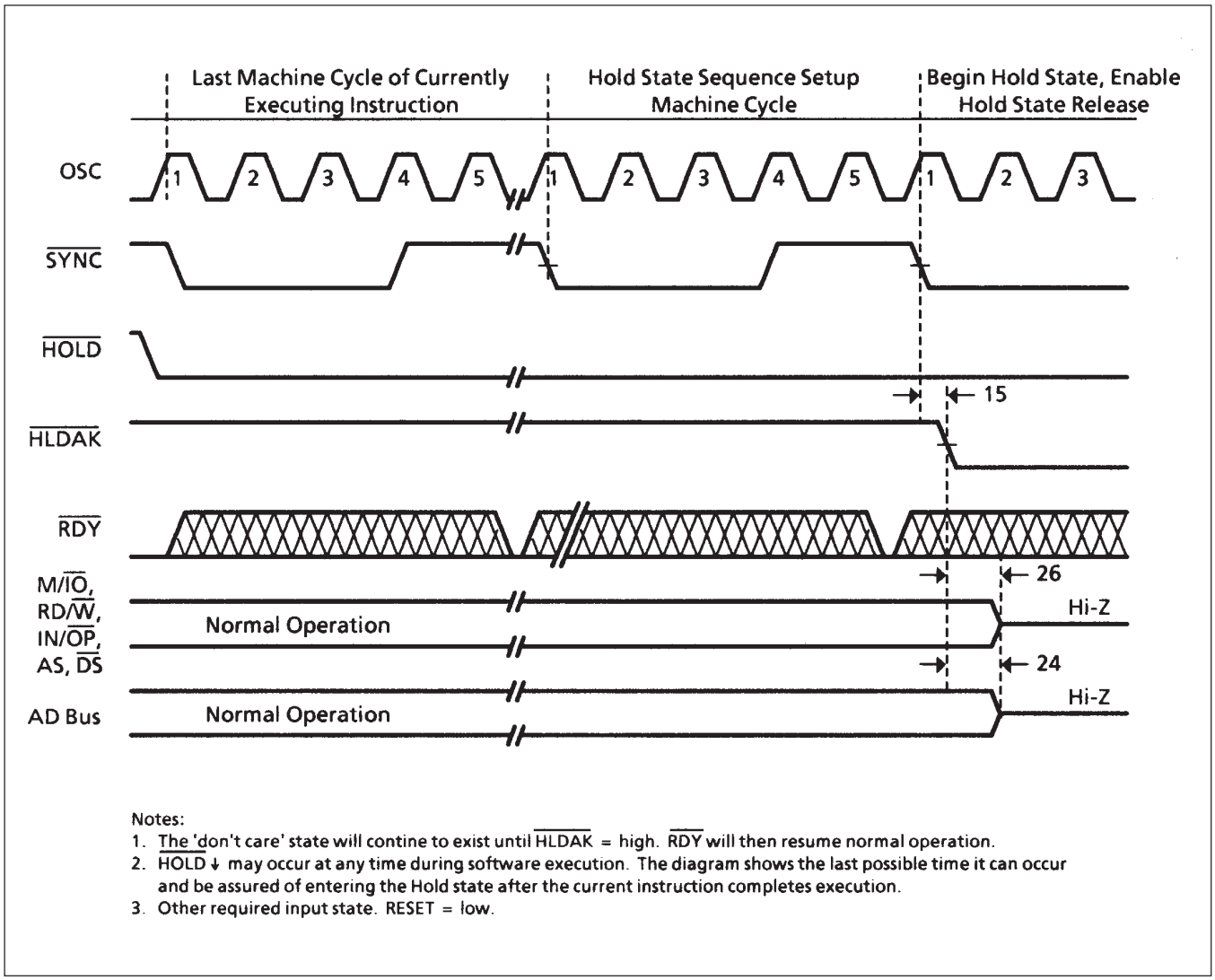


Figure 16: Hold State Generation Timing

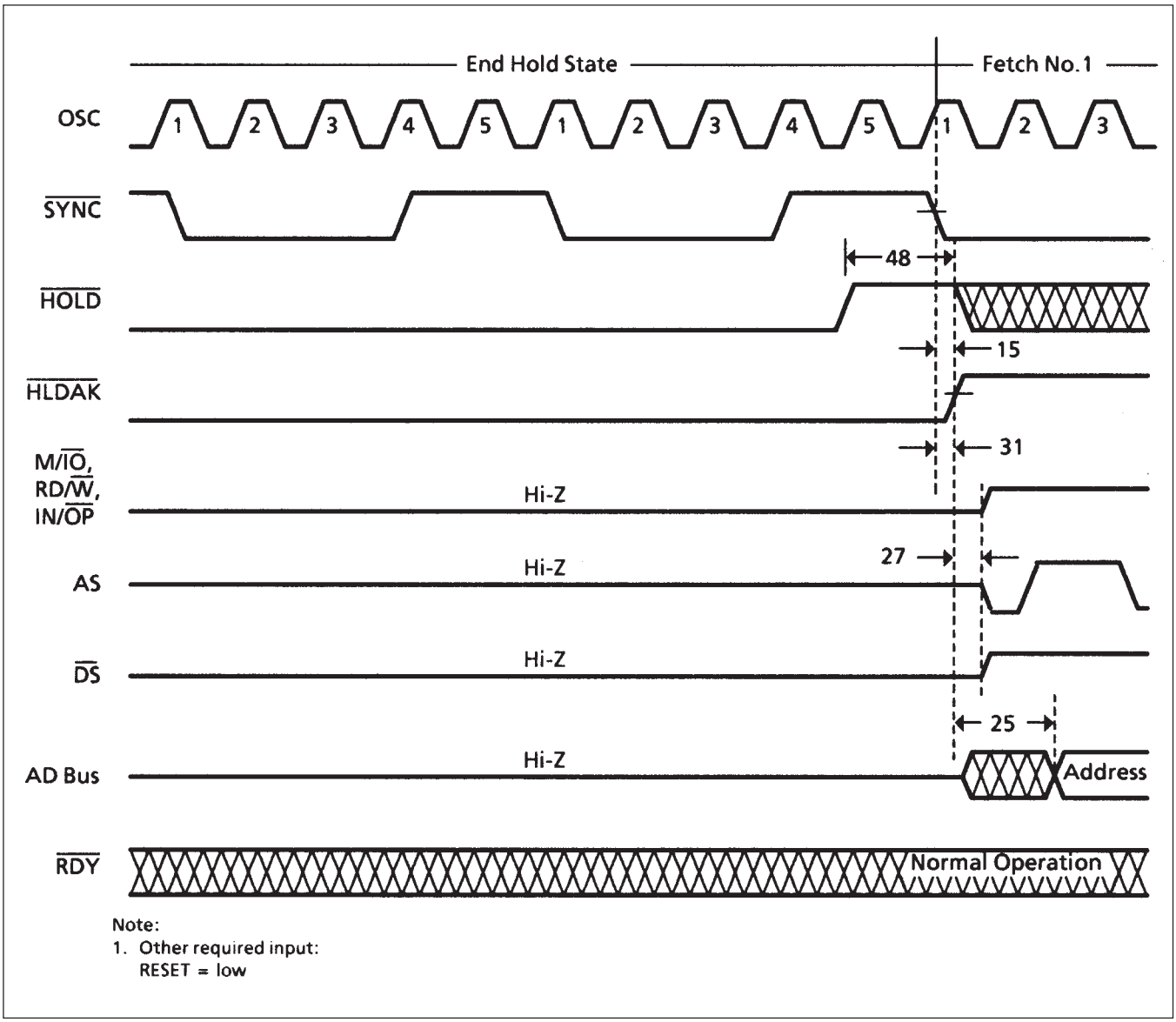


Figure 17: Hold State Termination Timing

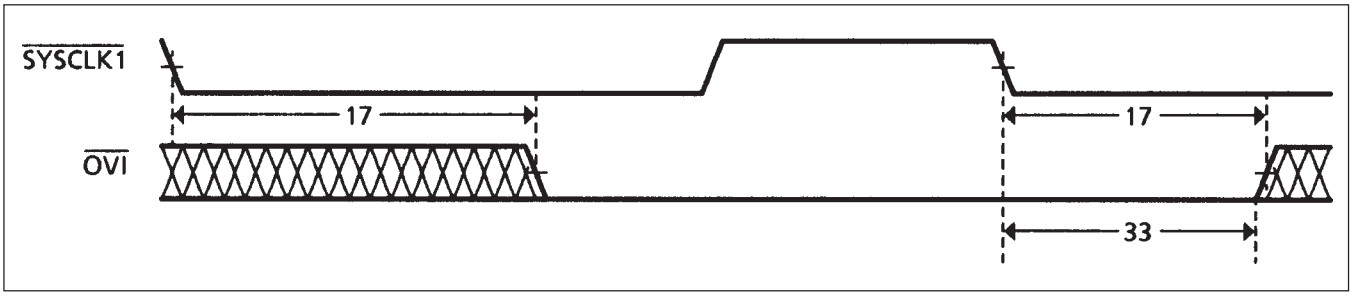


Figure 18: Fixed Point Overflow Timing

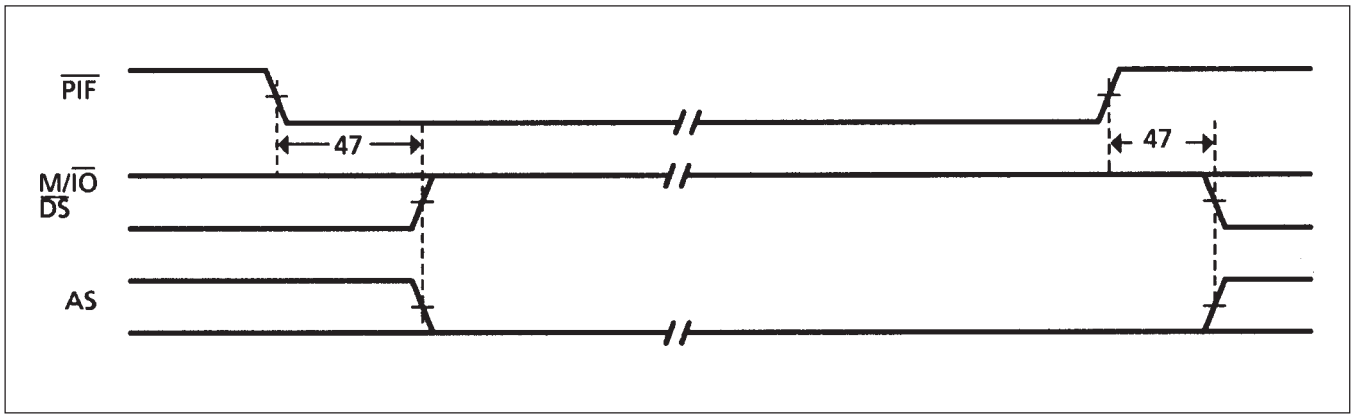


Figure 19: Instruction Abort Fault Timing

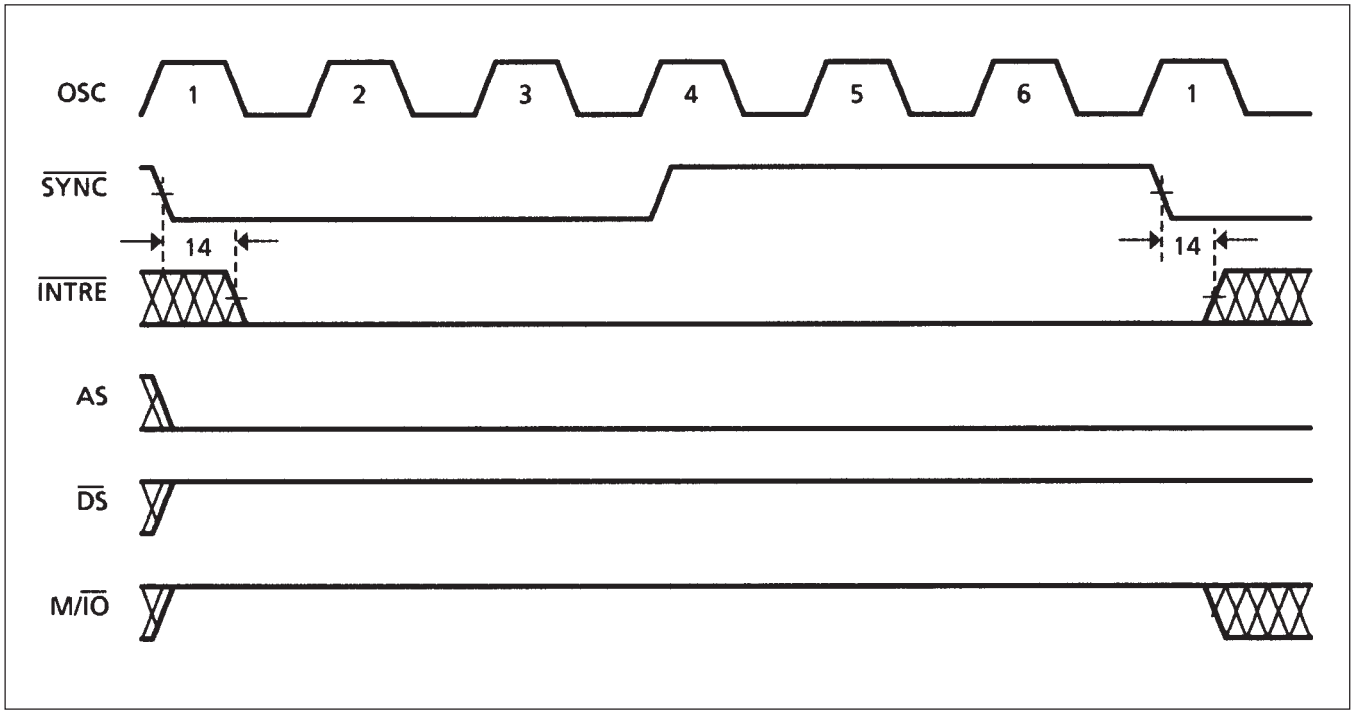


Figure 20: Interrupt Unit Microcode Enable Timing

Subgroup	Definition
1	Static characteristics specified in Table 6 at +25°C
2	Static characteristics specified in Table 6 at +125°C
3	Static characteristics specified in Table 6 at -55°C
7	Functional tests at +25°C
8a	Functional tests at +125°C
8b	Functional tests at -55°C
9	Switching characteristics specified in Table 4b at +25°C
10	Switching characteristics specified in Table 4b at +125°C
11	Switching characteristics specified in Table 4b at -55°C

Table 4a: Definition of Subgroups

No.	Parameter	Test Conditions (1) (2)	Min (2)	Typ (2)	Max (2)	Units
1	OSC ↑ to SYNCN	Load 1	10		40	ns
2	OSC ↑ to SYSCLK1N	Load 1			40	ns
3	OSC ↑ to SYNCLKN	Load 1			40	ns
4	OSC ↑ to CLKPCN	Load 1			40	ns
5	OSC ↑ to CLK02N	Load 1			40	ns
6	SYNCN ↓ to AS ↑	Load 1	1τ-10		1τ+5	ns
7	SYNCN ↓ to AS ↓ (4)	Load 1	2.5τ-10		2.5τ+15	ns
8	SYNCN ↓ to DSN (Read)	Load 1	3τ-5		3τ+20	ns
9	SYNCN ↓ to DSN ↓ (Read) (3)	Load 1	10		30	ns
10	SYNCN ↓ to DSN ↓ (Write)	Load 1	3τ-5		3τ+22	ns
11	SYNCN ↓ to DSN ↑ (Write) (3)	Load 1	4.5τ-5		4.5τ+10	ns
12	SYNCN ↓ to Address Valid	Load 1			68	ns
13	SYNCN ↓ to Data Valid	Load 1			3τ+45	ns
14	SYNCN ↓ to M/ION, RD/WN, IN/OPN, INTREN Valid	Load 1			70	ns
15	SYNCN ↓ to HLDAKN Valid	Load 1			20	ns
16	SYSCLKN1 ↓ to T1 Valid	Load 1			75	ns
17	SYSCLKN1 ↓ to OVIN Valid	Load 1			100	ns
18	SYNCN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			3τ+50	ns
19	SYNCN ↓ to AD Bus Active (Read)	Load 2	15			ns
20	PAUSEN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			70	ns
21	PAUSEN ↑ to AD Bus Valid	Load 2			60	ns
22	PAUSEN ↓ to AS, DSN, M/ION, RD/WN, IN/IOPN Hi-Z (6)	Load 2, 3			50	ns
23	PAUSEN ↑ to AS, DSN, M/ION, RD/WN, IN/IOPN Valid	Load 2, 3			59	ns
24	HLDAKN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			60	ns
25	HLDAKN ↑ to AD Bus Valid	Load 2			50	ns
26	HLDAKN ↓ to AS, DSN, M/ION, RD/WN, IN/IOPN Hi-Z (6)	Load 2, 3			30	ns
27	HLDAKN↑ to AS, DSN, M/ION, RD/WN, IN/IOPN Valid	Load 2, 3			30	ns
28	Address after SYNCN ↓	Load 1	3τ+15			ns
29	Data after SYNCN ↓	Load 1	12			ns
30	M/ION, RD/WN, IN/OPN, INTREN after SYNCN	Load 1	5			ns
31	HLDAKN after SYNCN ↓	Load 1	-7			ns
32	T1N after SYSCLK1N ↓	Load 1	15			ns
33	OVIN after SYSCLK1N ↓	Load 1	20			ns
34	Data to SYNCN ↓		20			ns
35	Microcode to CLK02N ↓		10			ns
36	Microcode to SYSCLK1N ↓		10			ns
37	RDYN to OSC ↓		15			ns
38	IRDYN to OSC ↓		15			ns
39	Data after SYNCN ↓		0			ns
40	Microcode after CLK02N ↓		5			ns
41	Microcode after SYSCLK1N ↓		15			ns
42	RDYN after OSC ↓		5			ns
43	IRDYN after OSC ↓		10			ns
44	SYNCN to SYNCN ↓ (7)		5τ-2		5τ+2	ns
45	RESET ↑ to RESET ↓ (7)		2			ns
46	RESET ↑ to Related Outputs Valid (7)				50	ns
47	PIFN to Related Outputs Valid				50	ns
48	HOLDN to Related Outputs Valid (7)				50	ns
49	DSN to Data Valid (Write) (7)	Load 3 (DSN) Load 2 (Data)	15			ns
50	SYNCN to SYNCLKN (No.1 - No.3)		-5		8	ns
51	CLKPCN to SYNCLKN (No.4 - No.3)		-5		5	ns
52	SYSCLK1 to CLKPC (No.2 - No.4)		-5		10	ns

MIL-STD-883, Method 5005, Subgroup 9, 10, 11

Notes: 1. T_A = +25°C, -55°C and +125°C tested at VDD = 4.5V and 5.5V
2. r = 1OSC period 0.5r implies 50% OSC duty cycle
3. Add 1r for internal XlO; nr for memory wait
4. Excluding DMA and Hold conditions
5. Unless otherwise noted: V_{Il} = ≥ 0.0V, V_{IHTTL} ≤ 4.0V, VIHOSC = 4.0V timing measured from 50% to 50% points
6. High impedance measured by 20% (of VDD) voltage change using 1K-ohm pullup resistor
7. Data obtained by characterisation or analysis, not routinely measured
8. Load 2 applies to bus interface signals AS, RD/W and IN/OP; Load 3 applies to bus interface signals M/ION and DSN

Table 4b: Timing Parameter Values

6.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.0 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Total Dose Radiation Not Exceeding 3x10^5 Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS}+1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{CH}	OSC Input High Voltage (Note 6)	-	4.0	-	-	V
V_{CL}	OSC Input Low Voltage (Note 6)	-	-	-	1.0	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2mA, V_{DD} = 5.5V	-	-	0.5	V
V_{OHT}	TTL Output High Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	3.5	-	-	V
V_{OLT}	TTL Output Low Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	-	-	0.4	V
V_{OHCLK}	Clock Output High Voltage (Note 3)	I_{OH} = -12mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLCLK}	Clock Output Low Voltage (Note 3)	I_{OL} = 12mA, V_{DD} = 5.5V	-	-	0.5	V
I_I	Input Leakage Current (Note 4)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 4)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	µA
I_{IPU}	TESTN Input Pullup Current (Note 5)	V_{DD} = 5.5V, TESTN = 0V	-	-150	-300	µA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, OSC = 20MHz	-	25	35	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, OSC = 0MHz	-	5	10	mA

Mil-Std-883, Method 5005, Subgroup 1, 2, 3.

Notes: 1. The following signals are CMOS compatible:
   a) CMOS inputs: Microcode Bus, (M00-M19), TESTN, IRDYN and PIFN.
   b) CMOS outputs: T1, OVIN, INTREN, SYSCLK1N, CLKPCN and CLK02N.
2. The following signals are TTL compatible:
   a) TTL inputs: HOLDN, RESET, PAUSEN, RDYN and OSC.
   b) TTL outputs: HOLDAKN and SYNCN.
   c) TTL 3 state outputs: AS, DSN, M/ION, RD/WN and IN/OPN.
   d) TTL 3 state I/O signals: Address/Data Bus (AD00-AD15).
3. The clock output pins, SYSCLK1N, SYNCLK, CLKPCN and CLK02N have a higher drive capability than the standard outputs.
4. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
5. The TESTN input signal is used during chip test and has an integral pullup reistor. In normal operation TESTN is at V_{DD}.
6. Guaranteed but not tested.

Table 6: Operating DC Electrical Characteristics

8.0 PACKAGING INFORMATION

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.508	0.014	-	0.020
c	0.229	-	0.36	0.009	-	0.014
D	-	-	82.04	-	-	3.230
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	22.86 Typ.	-	-	0.900 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	23.4	-	-	0.920
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG413

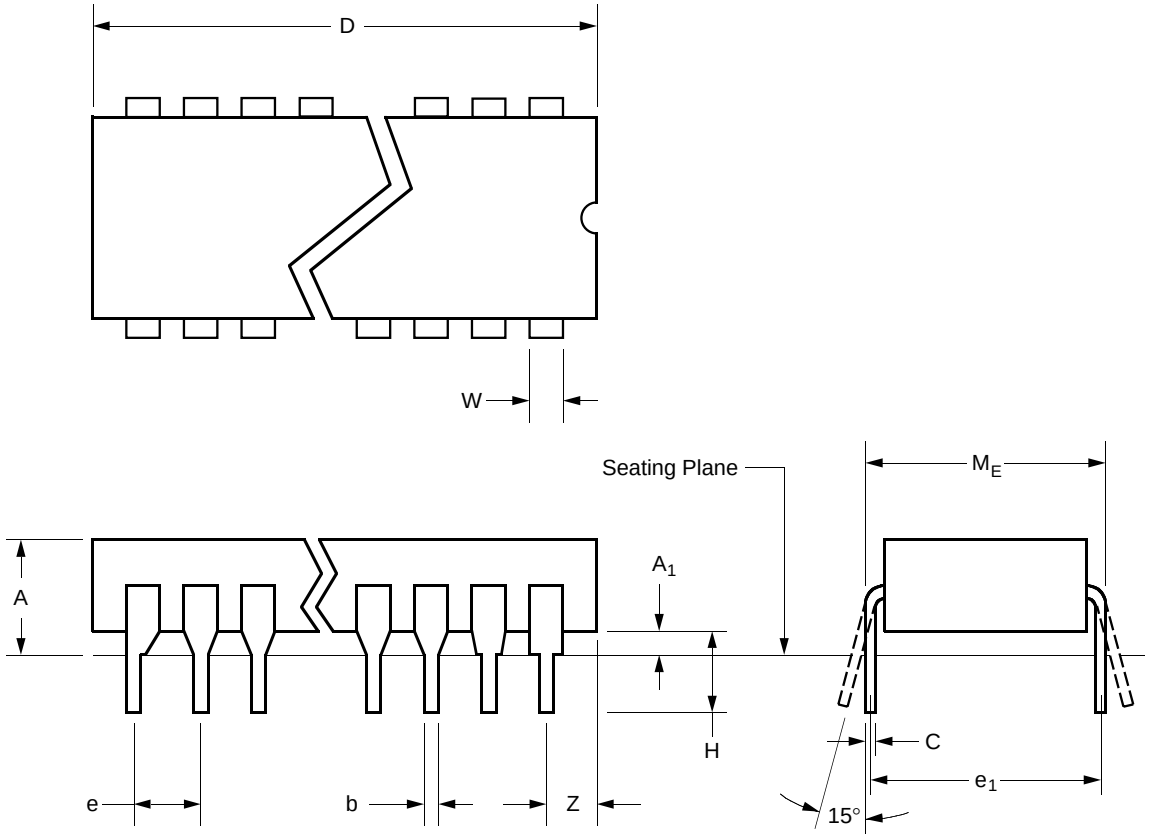


Figure 21a: 64-Lead Ceramic DIL - Package Style C

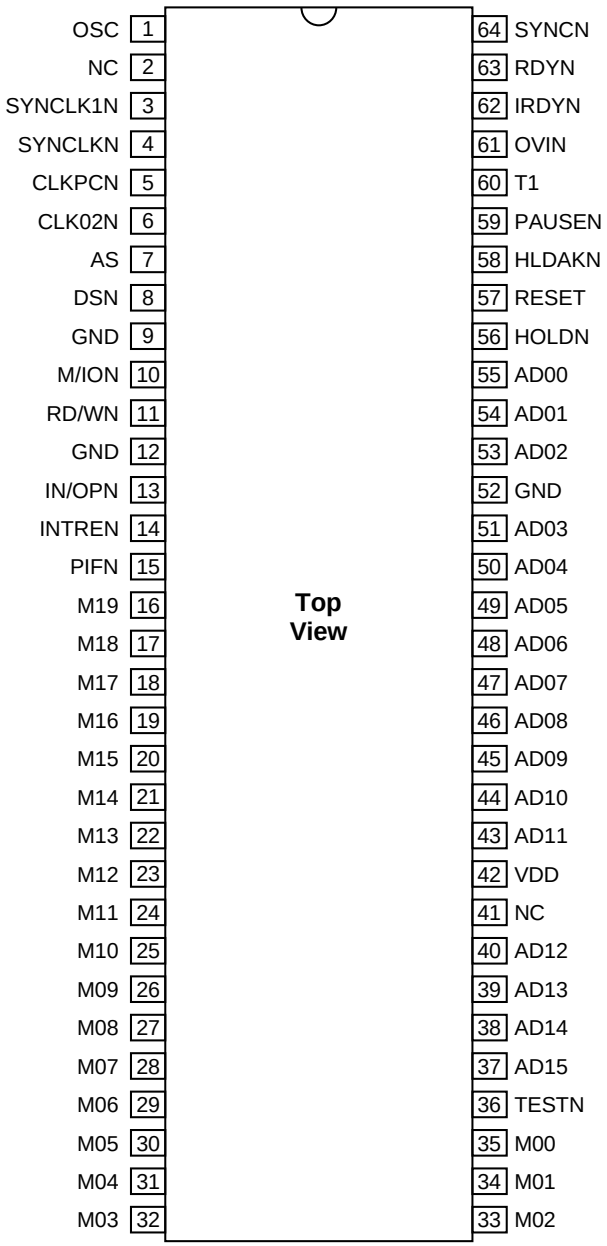


Figure 21b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.905	-	2.21	0.075	-	0.087
b1	-	0.51	-	-	0.020	-
D	18.08	-	18.62	0.712	-	0.733
E	18.08	-	18.62	0.712	-	0.733
e	-	1.02	-	-	0.040	-
Z	1.40	-	1.78	0.055	-	0.070

XG493

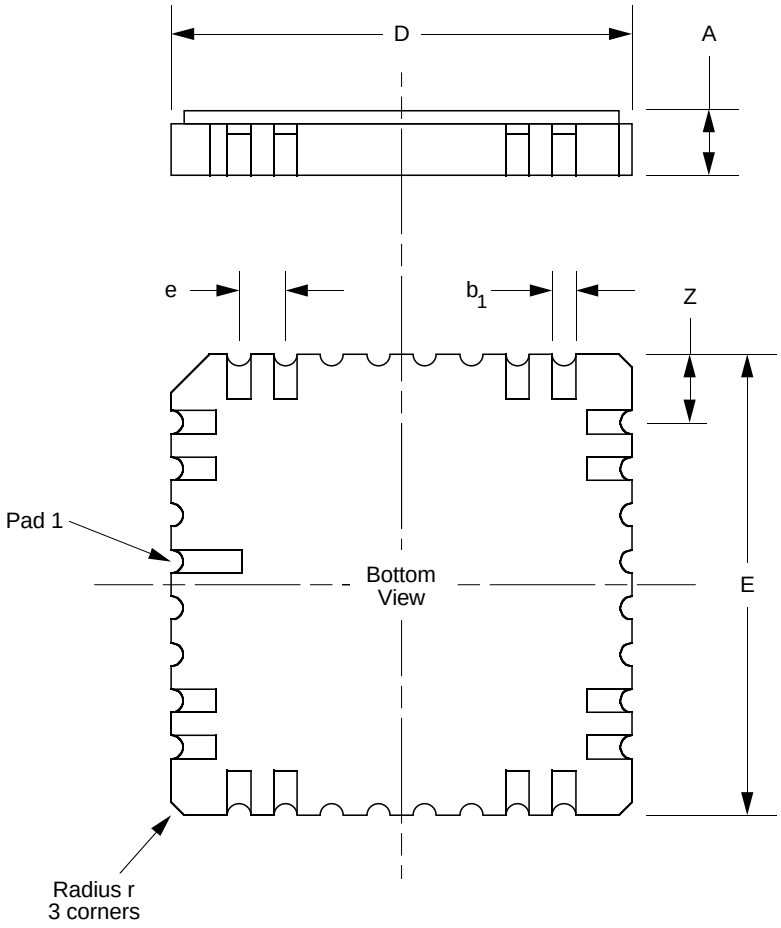


Figure 22a: 64-Lead Leadless Chip Carrier - Package Style L

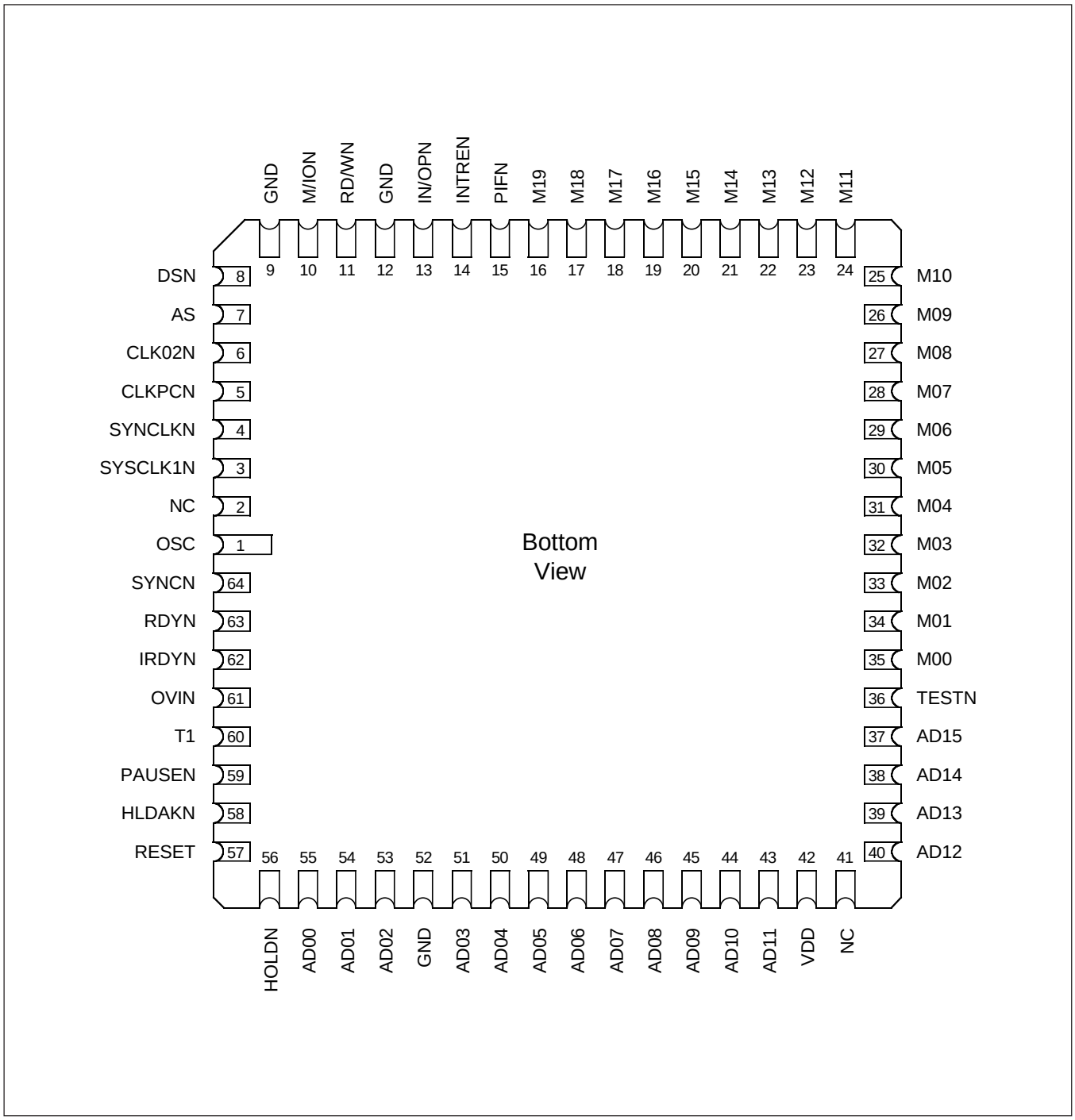


Figure 22b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

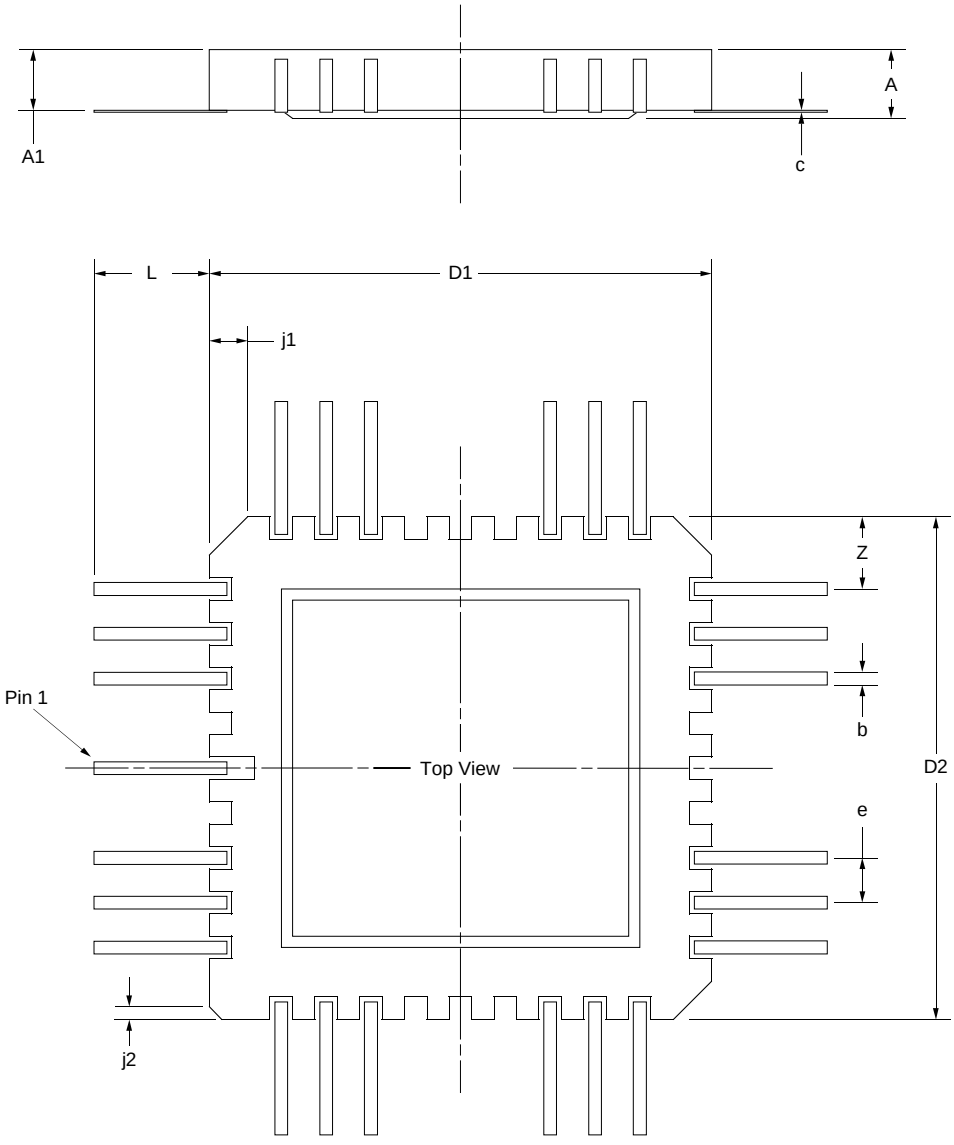


Figure 23a: 68-Lead Topbraze Flatpack - Package Style F

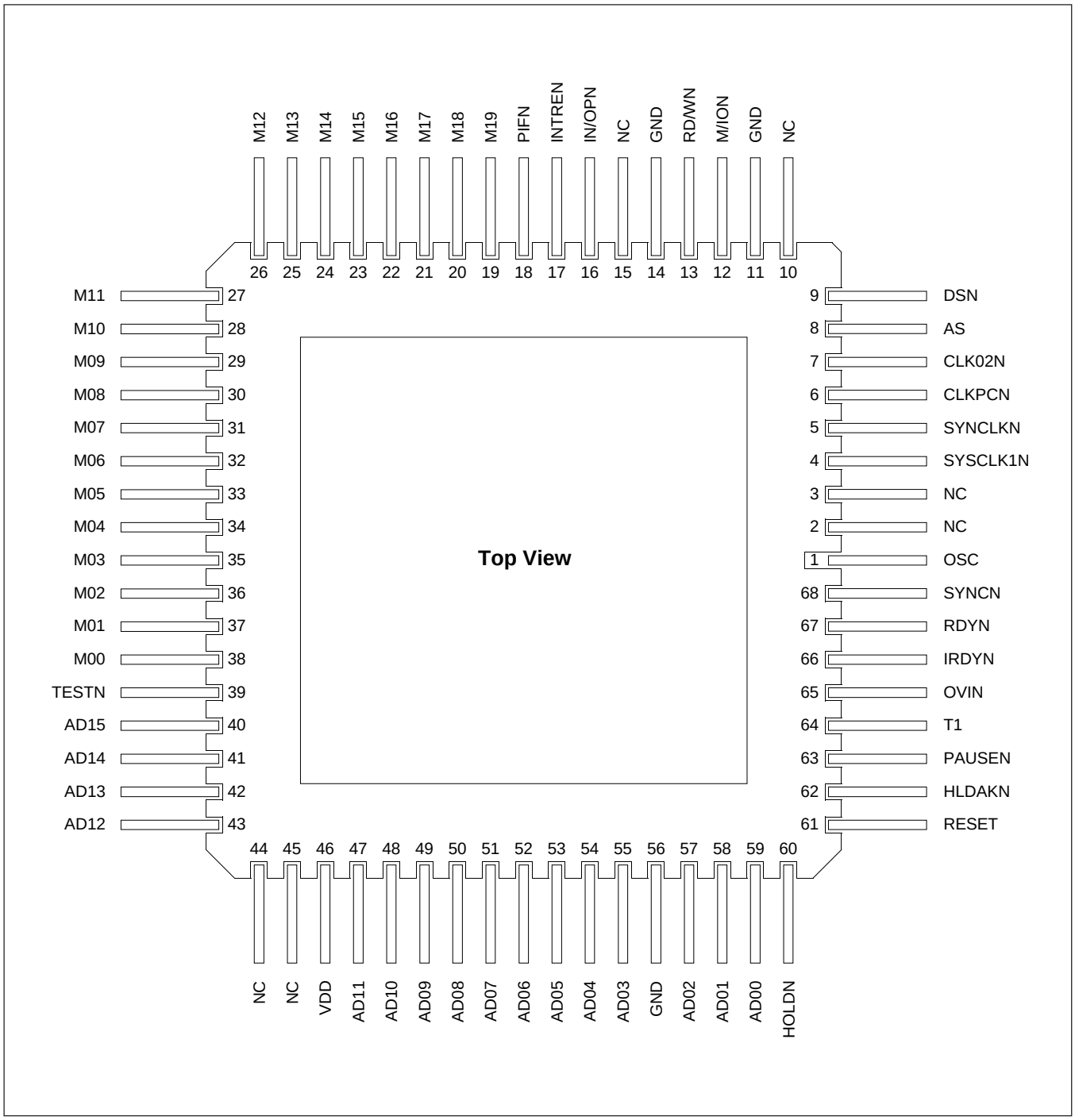


Figure 23b: Pin Assignments

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Dynex Semiconductor can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

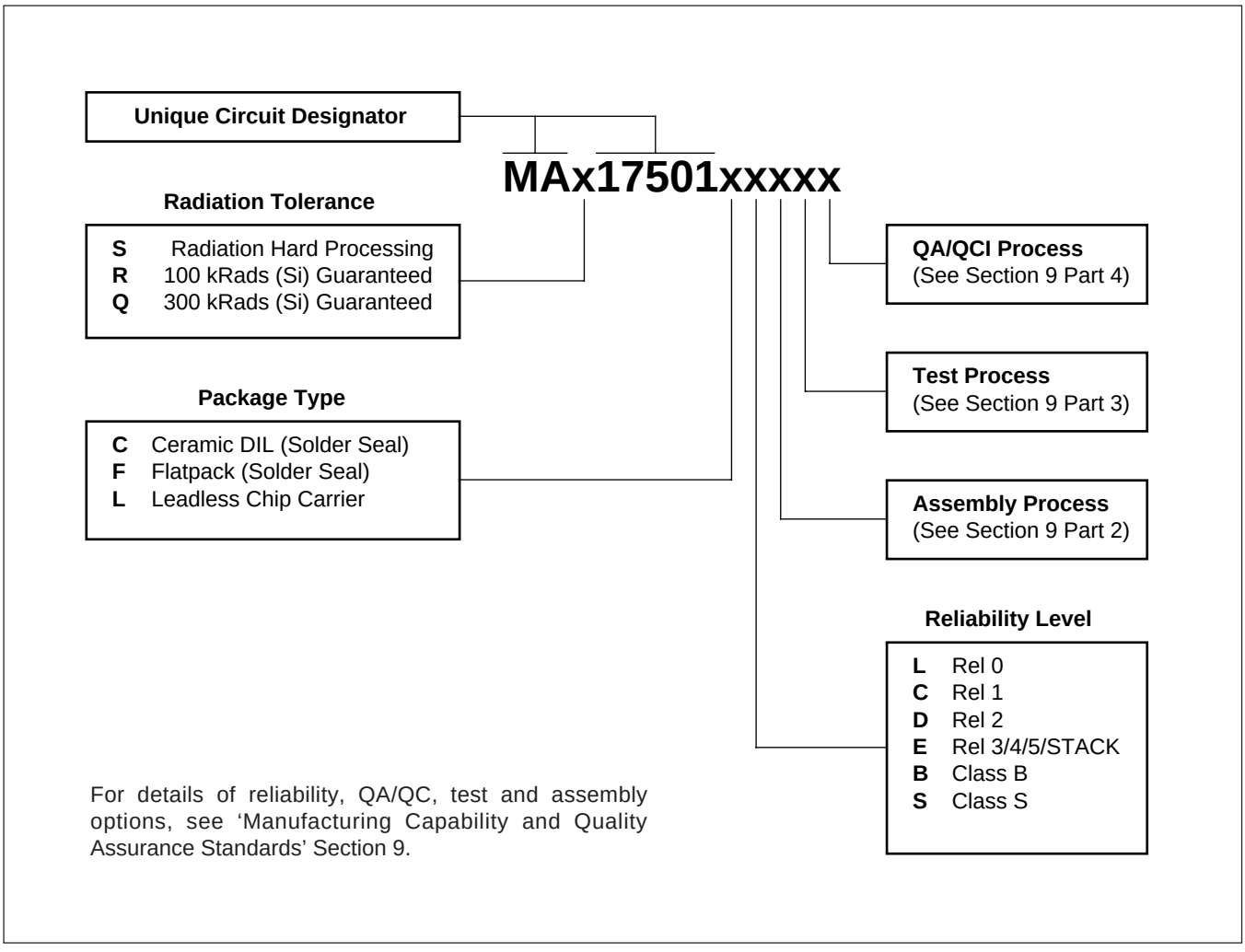
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 10: Radiation Hardness Parameters

10.0 ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

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Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hard corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.