MYSON TECHNOLOGY

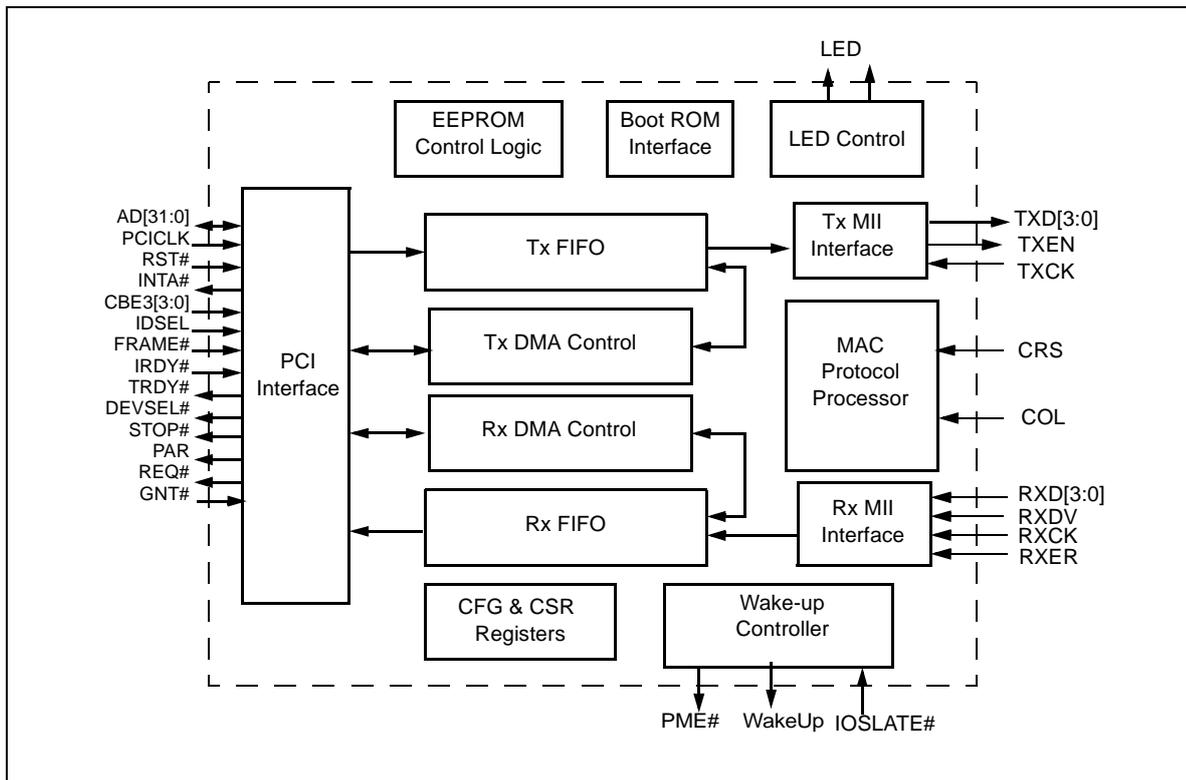# MTD 800 (Preliminary)

Integrated Fast Ethernet Controller

FEATURES

- Compliant to PCI bus interface v2.2.
- IEEE802.3 and 802.3u compliant.
- High performance with PCI bus master structure.
- Programmable PCI burst length for low CPU utilization rate.
- Transmit packet queuing capability for higher performance.
- Supports both full-duplex and half-duplex mode operation.
- Supports both IEEE802.3x and XON/XOFF full duplex flow control method.
- Contains separate transmit and receive FIFOs.
- Supports Magic packet and Microsoft wake-up frame filtering.
- Supports ACPI and PCI power management.
- Supports CardBus STSCHG pin and status changed registers. The CIS can be stored in the EEPROM.
- Supports up to 128K bytes boot ROM or flash memory without external latch.
- Autoload EEPROM contents after power-on.
- Programmable EEPROM interface.
- 128 pin PQFP package.
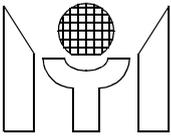- Single 3.3V Power Supply.

GENERAL DESCRIPTION

MTD800 is a highly integrated fast ethernet controller for PCI interface. The chip contains a PCI interface block, two large FIFOs(each is 2KiloBytes) for transmit and receive DMA, IEEE802.3 and 802.3u compliant MAC interface for MII connection. Besides that, the chip has the built-in Wake-Up controller to perform ACPI function, and the capability of sensing IEEE 802.3x frame to support XON/XOFF flow control protocol. The chip also has EEPROM and BootROM interface for no glue logic board implementation. For CardBus application, MTD800 supports four status-changed registers, an interface for accessing CIS which is stored in EEPROM and STSCHG pin to reflect the general wake-up event.
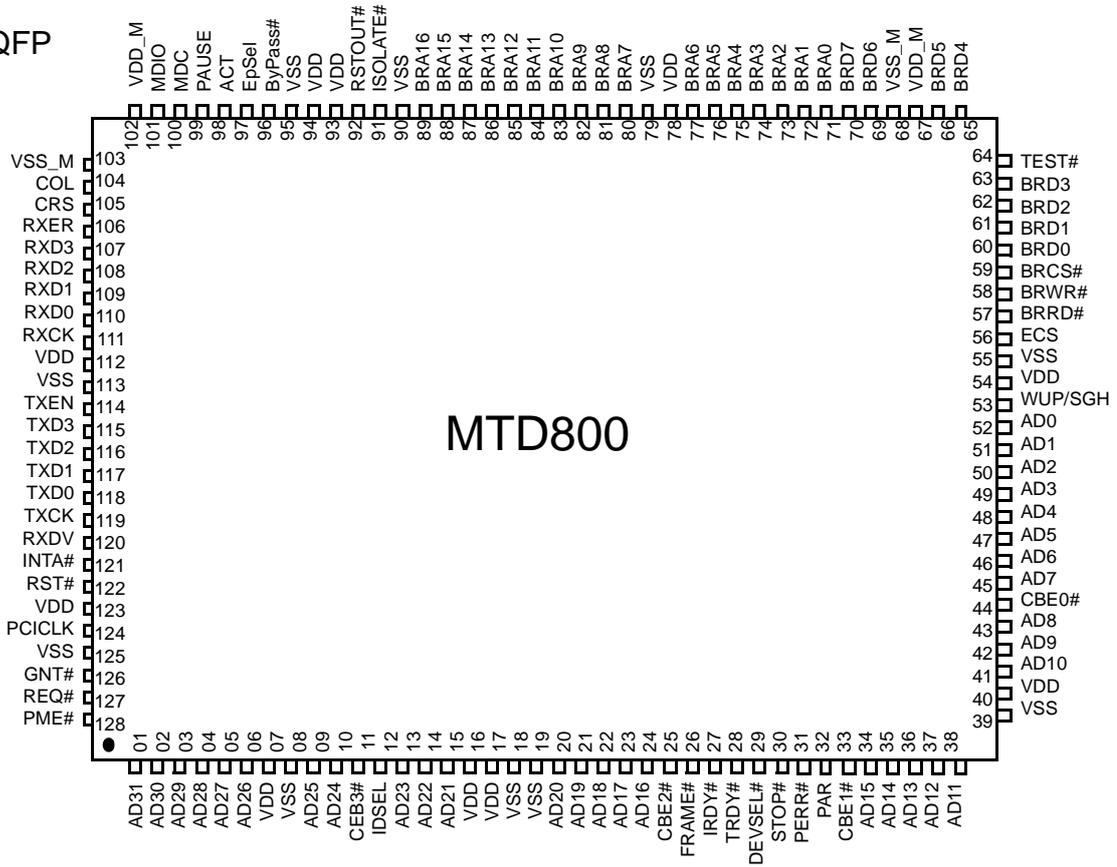
BLOCK DIAGRAM

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MTD 800
(Preliminary)

1.0 PIN CONNECTION

128 pin QFP

MTD800

Top pins (102–65): VDD_M, MDIO, MDC, PAUSE, ACT, EpSel, ByPass#, VSS, VDD, VDD, RSTOUT#, ISOLATE#, VSS, BRA16, BRA15, BRA14, BRA13, BRA12, BRA11, BRA10, BRA9, BRA8, BRA7, VSS, VDD, BRA6, BRA5, BRA4, BRA3, BRA2, BRA1, BRA0, BRD7, BRD6, VSS_M, VDD_M, BRD5, BRD4

Left pins (103–128): VSS_M (103), COL (104), CRS (105), RXER (106), RXD3 (107), RXD2 (108), RXD1 (109), RXD0 (110), RXCK (111), VDD (112), VSS (113), TXEN (114), TXD3 (115), TXD2 (116), TXD1 (117), TXD0 (118), TXCK (119), RXDV (120), INTA# (121), RST# (122), VDD (123), PCICLK (124), VSS (125), GNT# (126), REQ# (127), PME# (128)

Right pins (64–39): TEST# (64), BRD3 (63), BRD2 (62), BRD1 (61), BRD0 (60), BRCS# (59), BRWR# (58), BRRD# (57), ECS (56), VSS (55), VDD (54), WUP/SGH (53), AD0 (52), AD1 (51), AD2 (50), AD3 (49), AD4 (48), AD5 (47), AD6 (46), AD7 (45), CBE0# (44), AD8 (43), AD9 (42), AD10 (41), VDD (40), VSS (39)

Bottom pins (01–38): AD31, AD30, AD29, AD28, AD27, AD26, VDD, VSS, AD25, AD24, CEB3#, IDSEL, AD23, AD22, AD21, VDD, VDD, VSS, VSS, AD20, AD19, AD18, AD17, AD16, CBE2#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PERR#, PAR, CBE1#, AD15, AD14, AD13, AD12, AD11

2.0 PIN DESCRIPTIONS
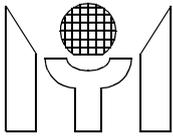
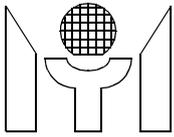| Name	Pin #	I/O	Descriptions
PCI Bus Interface			
PCICLK	124	I	PCICLK provides timing reference for the MTD800 related PCI transactions. All PCI signals except RST#,INTA# and PME# are sampled on the rising edge of this clock.
RST#	122	I	When RST# is asserted, all output signals are put into tristate and all open drain pins are floated. This signal is asynchronous to PCICLK and have to be asserted for at least 10 active PCI clock cycles.
AD[31:0]	1 - 6, 9, 10, 13 -15, 20 - 24, 34 - 38, 41 - 43, 45 -52	I/O	32-bit multiplexed address and data bus. A bus transaction consists of an address phase followed by one or more data phases. During the first cycle in which the FRAME# is asserted, the AD[31:0] represents the address bus while it is considered as a data bus during subsequent cycles.

Name	Pin #	I/O	Descriptions
CBE#[3:0]	11, 25, 33, 44	I/O	4-bit multiplexed bus command and byte enables. During the address phase transaction, CBE is considered as bus command. On the data phase cycles, CBE represents the byte enable signals for PCI data bus.
IDSEL	12	I	Used as a chip select during access to the configuration registers
FRAME#	26	I/O	Driven by MTD800 to Indicate the start and duration of a transaction. The FRAME# is deasserted when the master is ready to complete the final data phase in the transaction.
IRDY#	27	I/O	During a write transaction, the current bus master asserts IRDY# to indicate that valid data is being driven onto the PCI bus. During a read transaction, this signal is asserted to indicate that the master is ready to accept data from the selected target. Wait states are inserted until both IRDY# and TRDY# are asserted.
TRDY#	28	I/O	During a read transaction, the target asserts TRDY# to indicate that valid data is being driven onto the PCI bus. During a write transaction, this signal is asserted to indicate that the target is ready to accept data. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted.
DEVSEL#	29	I/O	Asserted by MTD800 to indicate that the device has decoded the address as the target of current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
STOP#	30	I/O	Asserted by MTD800 to disconnect any further transaction. As an input, DEVSEL# indicates whether any device on the bus or bridge has terminated the transaction.
INTA#	121	O/D	INTA# is an asynchronous signal which is used to request an interrupt.
PAR	32	I/O	Ensures even parity across AD[31:0] and CBE[3:0]. PAR is stable and valid for one clock after the address phase. During the data phase, PAR is stable and valid for one clock after either IRDY#(write transaction) or TRDY#(read transaction) is asserted.
GNT#	126	I	Asserted by the PCI bus arbiter to indicate that MTD800 has granted the bus control authority.
REQ#	127	O/Z	Asserted by MTD800 to signal bus arbiter that it needs the dedicated access to the PCI bus.
PERR#	31	I/O	PERR# is asserted when a data parity error is detected.
PME#	128	O/D	An interrupt signal for the occurrence power management event. Asserted by MTD800 to request a change in the device or system power state.
Network Interface			
COL	104	I	Collision signal. COL is asserted high when PHY detects a collision on the medium. This signal is asynchronous to TXCK or RXCK.
RXDV	120	I	Receive data valid. RXDV is asserted high by PHY to indicate the incoming receive data RXD[3:0] is valid. This signal is synchronous to RXCK.
TXCK	119	I	Transmit Clock. TXCK is a continuous clock that provides the timing reference for the transfer of the TXD[3:0] and TXEN signals.
TXD[3:0]	115 - 118	O	Transmit Data signals. TXD are driven by MTD800 and transits synchronously with respect to the TXCK.
TXEN	114	O	Transmit Data Enable. TXEN is driven by MTD800 and transits synchronously with respect to the TXCK.
RXCK	111	I	Receive Clock. RXCK is a continuous clock that provides the timing reference for the transfer of the RXD[3:0], RXDV and RXER.

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Name	Pin #	I/O	Descriptions
RXD[3:0]	107 - 110	I	Receive Data signals. RXD are driven by PHY and transit synchronously with respect to the RXCK.
RXER	106	I	Receive Error signal. RXER is asserted high to indicate a coding error is detected by PHY. This signal is synchronous to RXCK.
CRS	105	I	Carrier Sense signal. CRS is asserted by PHY when either the transmit or receive medium is non-idle. This signal is asynchronous to TXCK or RXCK.
MDC	100	O	Management Data Clock. MDC is sourced by the MTD800 to control the transfer of the MDIO data. A 1.5K pull up resistor is required to connect to this pin.
MDIO	101	I/O	Management Data Input/Output. A bi-directional data interface connected to PHY. A 1.5K pull up resistor is required to connect to this pin.
LED Status Output			
LED_ACT#	98	O	Activity LED. This signal will drive the led light on when detecting activity on MII interface. A 510 ohm pull up resistor is required to connect to this pin.
LED_PAUSE#	99	O	Pause LED. This signal will drive the led light on when detecting transmission is paused under the condition of receiving a XON frame.
BootROM/ EEPROM Interface			
ECS	56	O	A chip select signal for the external EEPROM. EEPROM is used to provide the configuration data and Ethernet Address. A 100K pull-up resister is connected to this pin.
BRRD#	57	O	BootROM read signal. Read out the content of BootROM onto the memory support data bus.
BRWR#	58	O	BootROM write signal. When flash memory is used, BRWR# is asserted low to enable the write action.
BRCS#	59	O	A chip select signal for the external EPROM (BootROM) or flash memory. The BootROM contains codes that can be usually executed for a system boot function.
BRD0/EEDI	60	I/O	A multiplexed signal for BootROM data bit 0 and Serial ROM Data input.
BRD1/EEDO	61	I/O	A multiplexed signal for BootROM data bit 1 and Serial ROM Data output.
BRD2/EECK	62	I/O	A multiplexed signal for BootROM data bit 2 and Serial ROM Clock signal.
BRD[7:3]	70 - 69, 66 - 65, 63	I/O	BootROM data bus from bit 3 to bit 7.
BRA[16:0]	89- 80, 77 - 71	O	BootROM address bus from bit 0 to bit 16.
Misc. Interface			
WAKEUP/ STSCHG	53	O/Z	Wakeup Pin/CardBus STSCHG Pin. In PCI application, this pin is the Wakeup pin to signal the host system of an wakeup event happened. In Card bus application, this pin is used as the STSCHG pin to signal the system of any status changed. This pin is enabled as STSCHG pin if the PME_Enable bit of the power management control register is set and the FMR.GWAKE, FMR.WAKE are both set.
ByPass#	96	I	EEPROM Bypass Mode. When asserted low, the EEPROM function will be disable. This is useful for testing purpose. For normal operation, it should be connected to VDD.

Name	Pin #	I/O	Descriptions
EpSel	97	I	EEPROM selection pin. EpSel is to determine which type of EEPROM is chosen. 93C46 is used when EpSel connects to VSS, while 93C66 is selected if EpSel connects to VDD.
ISOLATE#	91	I	ISOLATION pin. This pin should connect to the PCI stable power signal (VDD). When PCI Bus is in B3 state, the power signal becomes deasserted, however the ISOLATION pin is active. Under this condition, the PCIRST# and PCICLK are ignored and all the PCI output signals except PME# are isolated from the PCI Bus.
RSTOUT#	92	O	Reset Output pin. A active-low pulse is generated when Power-On or Hardware reset is detected. The pulse width is 245us. The PHY can use this output pin as its reset signal, then PHY can avoid to keep being reset during D3 state.
Power Supply & Ground			
VDD_M, VSS_M	67, 102 68, 103	P/G	Digital 3.3V power and ground for internal SRAM.
VDD	7, 16, 17, 40, 54,64, 78, 93, 94, 112, 123	P	Digital 3.3V power supply.
VSS	8, 18, 19, 39, 55, 79, 90, 95, 113, 125	G	Digital Ground.

3.0 FUNCTIONAL DESCRIPTION

3.1 PCI Bus Operation

The peripheral component interconnect (PCI) is a high-speed backplane in modern PC. The MTD800 uses the PCI bus to communicate with the host CPU and main memory to achieve high performance network computation. The MTD800 is directly compatible with revision 2.2 of the PCI Local Bus Specification and supports a subset of the PCI bus transactions. It contains I/O read/write, Memory read/write and Configuration read/write operations. Besides that, all kinds of termination cycle are also supported. The MTD800 is acting as a PCI bus target when handshaking with the host, while operating as a PCI bus initiator when communicating with the host memory.

3.2 DMA Transmit Function

The DMA Transmit Function is responsible for fetching data from the host's memory into the on-chip transmit FIFO, and then signalling MAC transmit interface to relay the transmitted data onto the network if the fullness of FIFO reaches the predefined threshold. The structure for the data to be transmitted is described in a format of chained link list(see figure 3.1). Descriptors that reside in the host memory act as pointers to these transmit buffers. The transmit descriptor format is shown as figure 3.2. It consists of four long words. The first two words contain the transmit frame status, frame length and the descriptor ownership information. The last two words are the address pointers for the current data buffer and the next descriptor. The bit field definition of the descriptor words are given in table 3.1 and table 3.2 respectively. Note that the transmit buffer address are not necessary to be in alignment of longword while the descriptors address should be longword aligned. The ownership of buffer is indicated in the "own" bit of the first descriptor. When driver has completed the preparation of being transmitted packet, it sets the "own" bit to represent the buffer that belongs to the MTD800, and demands MTD800 to fetch the buffer and the associated descriptor. After the packet has been transmitted onto the network, the MTD800 clears the "own" bit and issues an interrupt to notify the driver that the buffer can be reused. Meanwhile, the driver is able to acquire the transmit status by reading the "TSW" in the first descriptor. The MTD800 also has an advanced feature to enhance the transmit performance by "closing" the first descriptor early once the packet has been transferred into the FIFO completely.
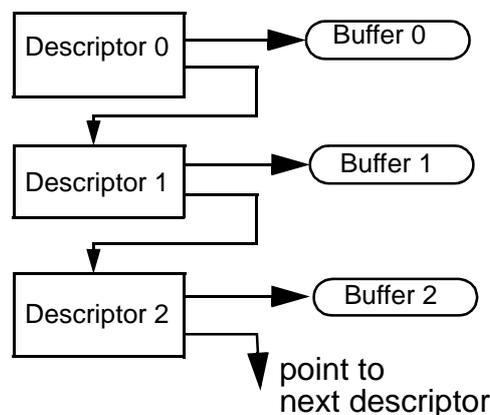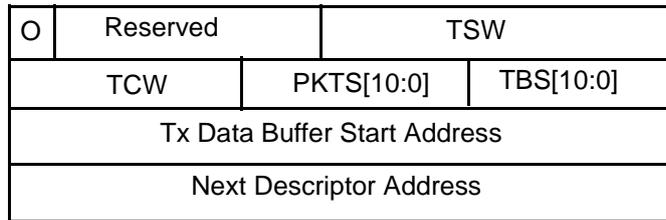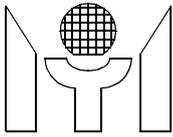

Figure 3.1 Descriptor chained structure

O	Reserved		TSW	
TCW		PKTS[10:0]		TBS[10:0]
Tx Data Buffer Start Address				
Next Descriptor Address				

Figure 3.2 The Transmit Descriptor Format

Table 3.1 Transmit Descriptor 0 (TDES0)

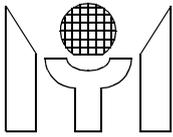| Bit	Symbol	Description
31	OWN	Owner: This bit is controlled by driver, When set, identifies that the descriptor is owned by the MTD800. When reset, indicates that the descriptor is owned by the host; Driver must reset this bit when initialization.
30 -13	-	Reserved
Transmit Status Word (TSW)		
13	ABORT	Abort: This bit is set when the current transmitting packet is aborted due to the excessive collision or late collision,
12	CSL	Carrier Sense Lost: When set, the carrier is lost during the transmission of packet.
11	LC	Late Collision: This bit is set when late collision occurs.
10	EC	Excessive Collisions: This bit is set when the successive collision count exceeds 16 or 256 and the transmitting packet will be aborted.
9	DFR	Deferred: When set, indicates that MTD800 has to defer while ready to transmit a frame because of carrier sense asserted.
8	HF	Heart-beat Failure: This bit is only effective in 10Base-T mode. When set, indicates a heartbeat collision check failure.
7- 0	NCR[7:0]	Collision Retry Count: This 8-bit counter indicates that the number of collisions have occurred.

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Table 3.2 Transmit Descriptor 1 (TDES1)

Bit	Symbol	Description
		Transmit Configure Word (TCW)
31	IC	Interrupt Control: This bit supports for interrupt Pacing. When set, indicates that MTD800 will issue interrupt after the packet has been transmitted.
30	EIC	Early Interrupt Control: This bit supports for interrupt Pacing. When set, indicates that MTD800 will issue interrupt after the packet has been transferred into the internal FIFO.
29	LD	Last Descriptor: When set, it means the pointed buffer contains the last segment of a frame.
28	FD	First Descriptor: When set, it means the buffer contains the first segment of a frame. In descriptor ring structure, each buffer is classified as follows : FD LD Description 1 1 Single buffer descriptor 1 0 First buffer descriptor, further buffer chained 0 1 Chained buffer packet end 0 0 Intermediate buffer.
27	CRC	CRC append : When set, the MTD800 will generate a CRC field to append to the transmitted packet.
26	PAD	PAD control : When set, the MTD800 will automatically pad zero's to the end of packet whose length is less than 64 bytes.
25	RTLC	Retry Late Collision : When set, the late collision will be considered as a normal collision and the MTD800 just increases a collision count instead of aborting the packet.
24 - 22	-	Reserved.
21 - 11	PKTS[10:0]	Packet Size : This field contains the length of the transmitted packet. The value should be valid for the first descriptor. The size is indicated in bytes.
10 - 0	TBS	Transmit Buffer Size : This field contains the size information of buffer. If the transmitted packet only use one single buffer, the TBS should be equal to PKTS. The size is also indicated in bytes.

3.3 DMA Receive Function

The DMA Receive Function is responsible for collecting the network nibble-stream into the on-chip receive FIFO, and then transferring the data onto the host's memory if the fullness of FIFO reaches the predefined PCI burst length. The data structure for the receive buffer is a forward-link buffer chain which is similar to the transmit buffer. Descriptors that reside in the host memory act as pointers to these receive buffers. The descriptor format is shown as figure 3.3. It consists of four long words. The first two words contain the receive frame status, frame length and the descriptor ownership information. The last two words are the address pointers for the current data buffer and the next descriptor. The bit field definition of the descriptor words are given in table 3.3 and table 3.4 respectively. Note that the receive buffers and descriptors address both should be longword aligned. At the beginning, the driver allocates a set of free buffers and makes the ownership of these buffers belong to the chip. The MTD800 starts to fetches the first descriptor into its internal registers.
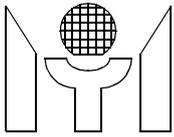
Once the packet has arrived in, the received data can be immediately transferred onto the dedicated location of the host memory by means of the predefined address which contains in the third word of the descriptor. After the receive buffer has been filled up with the received packet, the MTD800 clears the "own" bit in the descriptor and issues an interrupt to notify the driver that the data in the buffer are ready to be taken away. The MTD800 also has an advanced feature to boost the receiving process. That is so-called "receive early interrupt" operation, which demands the driver to move the data earlier than the completion of receiving the whole packet.
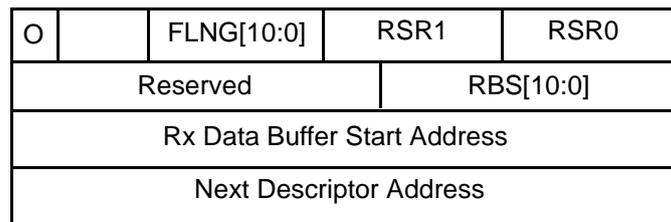
O		FLNG[10:0]	RSR1	RSR0
Reserved			RBS[10:0]	
Rx Data Buffer Start Address				
Next Descriptor Address				

Figure 3.3 The Receive Descriptor Format

Table 3.3 Receive Descriptor 0 (RDES0)

Bit	Symbol	Description
31	OWN	Owner : This bit is controlled by driver, When set, identifies that the descriptor is owned by the MTD800. When reset, indicates that the descriptor is owned by the host; Driver must reset this bit when initialization.
30 - 28	-	Reserved.
27 - 16	FLNG[11:0]	Frame Length : Indicates that the frame length of received packet. This field is valid only when the descriptor contains the last segment of a frame.
Receive Status Register 1(RSR1)		
15	-	Reserved.
14	MAR	Multicast Address Received : The MTD800 receives a multicast address packet.
13	BAR	Broadcast Address Received : The MTD800 receives a broadcast address packet.
12	PHY	Physical Address Received : The MTD800 receives a physical address packet.
11	FSD	First Descriptor : When set, indicates that the descriptor contains the first segment of a received frame.
10	LSD	Last Descriptor : When set, indicates that the descriptor contains the last segment of a received frame.
9 - 8	-	Reserved.
Receive Status Register 0 (RSR0)		
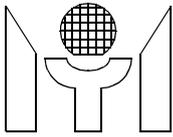
Bit	Symbol	Description
7	ES	Error Summary: This bit is set to 1 for receive error, the errors include the following - Runt packet Error (RUNT), - Long packet Error (LONG) , - Frame Alignment Error (FAE), - CRC Error (CRC), and - Receive coding Error (RXER).
6	RUNT	Runt Packet Received : When set, indicates the MTD800 receives a packet whose length is less than 64 bytes.
5	LONG	Long Packet Received : When set, indicates that the received frame length exceeds the maximum Ethernet-specified size of 1518 bytes.
4	FAE	Frame Align Error : When set, indicates that the received frame has an alignment Error.
3	CRC	CRC Error : When set, indicates a CRC error occurred on the received frame.
2	RXER	Receive Error : When set, indicates a receive coding error occurred on the received frame.
1 - 0	-	Reserved

Table 3.4 Receive Descriptor 1 (RDES1)

Bit	Symbol	Description
31 - 11	-	Reserved
10 - 0	RBS	Receive buffer size : Receive buffer size for this descriptor, the size is measured in bytes. The buffer size must be a multiple of 4.

3.4 Network Interface and MAC Protocol Handler

The network interface for transmit and receive function are both in a format of MII and ready for the interconnection to PHY chip. The MTD800 defines a simple and efficient protocol for transforming the FIFO data back and forth to a nibble-stream that is directly connected to MII. Meanwhile, the built-in Media Access Controller (MAC), which is compliant to IEEE 802.3, performs the following functions ;

(i) transmit function : encapsulates the nibble-stream coming from transmit DMA with preambles, Start Frame Delimiter (SFD), the frame check sequence and the padding zeroes if necessary;

(ii) receive function : delimits the incoming packet , extracts the destination address for recognition and checks frame validation before transferring data onto the internal receive FIFO;

(iii) CSMA/CD function : executes the listening before transmission, makes sure 96-bit time for interframe gap , detects collision and enforces the event by issuing jam pattern, enters into backoff state after collision and waits for retransmission .

The MAC of the MTD800 also supports full-duplex function and IEEE 802.3x flow control protocol. If the incoming packet with the predefined flow control destination address (.i.e. 01-80-c2-00-00-01) and length/
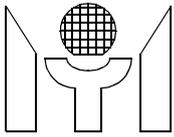
type field (.i.e. 88-08), the MAC detects to receive the flow control packet and then pauses the transmission process after the completion of the current transmitted packet. The MAC continues to transmit packets after the pause-time has expired. On the other hand, the MAC can automatically send out a flow control packet once the fullness of receiving FIFO has reached a predefined threshold to prevent the FIFO from overflowing and rendering packet loss.

3.5 EEPROM and BootROM Interface

The MTD800 uses EEPROM to store configuration data, Ethernet and Wake-up-Lan address etc. For Card-Bus application, the CIS can also be saved in the EEPROM. The BootROM contains the codes for executing a system boot function. Since EEPROM and BootROM share some I/O pins, these two devices can not be ena
bled at the same time.

3.5.1 EEPROM Contents

For desktop PCI application, the MTD800 only use 12 words to store configuration and address information. Therefore, an EEPROM with the size of 64 x 16 bits (i.e., 93C46) is enough to convey the data for such an application. However, in the system of CardBus, it needs more space to save CIS data and usually a large size of EEPROM (e.g. 93C66) is required. The memory map of EEPROM and the bit field description for configuration words are shown in the following tables.
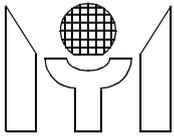
Table 3.5   EEPROM Memory Map

Offset	D15 ——— D8	D7 ——— D0	offset from Mem Base
00H	73H	Last Word Pointer	200H
01H		CFG 0	202H
02H	CIS Pointer 1	CIS Pointer 0	204H
03H	CIS Pointer 3	CIS Pointer 2	206H
04H	MAX_LAT	MIN_GNT	208H
05H	SubSystem ID1	SubSystem ID 0	20AH
06H	SubSystem Vendor ID1	SubSystem Vendor ID0	20CH
07H	Reserved	Reserved	20EH
08H	Ethernet Address 1	Ethernet Address 0	210H
09H	Ethernet Address 3	Ethernet Address 2	212H
0AH	Ethernet Address 5	Ethernet Address 4	214H
0BH	Reserved	Reserved	216H
0CH	Wake-up Lan Address 1	Wake-up Lan Address 0	218H
0DH	Wake-up Lan Address 3	Wake-up Lan Address 2	21AH
0EH	Wake-up Lan Address 5	Wake-up Lan Address 4	21CH
0FH	Reserved	Reserved	21EH
10H	CFG 2	CFG 1	220H
11H	Reserved	Reserved	
12H | 3FH	Reserved for future use		222H | 27EH
40H | FFH	Used for Card Bus Information Tuples		280H | 3FFH

Note:
(1) The above figure shows the layout of serial EEPROM which takes the size of 4K bits.
(2) The low order byte of the first word contains the pointer to the last word of implementation specific area. In this case, the value is "10H". For different implementation, the area can be extended to "3FH' in maximum.
(3) The high order byte of the first word will be written as "73H" if the EEPROM has been programmed.
(4) The Card Bus CIS data are stored in the range addressed from 280H to 3FFH. The address is an offset from Memory Base Address. The CIS can only be accessed from memory address space.

Table 3.6   Bit-Field Description of the Configuration words

Bit	Symbol	Description
		Configuration Register 0
7	PMC	Power Management Capability. Corresponding to Bit 4 of CFSR.
6	NDFA	Not Defined Flow control Address. Corresponding to Bit 12 of RCR.
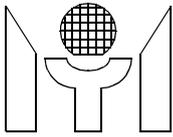
| Bit	Symbol	Description
5	TFCEN	Transmit Flow Control packet Enable. Corresponding to Bit 8 of TCR
4 - 2	BRSZ[2:0]	Indicates the Boot ROM size. Corresponding to Bit 28 -26 of BROM_CR.
1 - 0	BRSPD[1:0]	Boot ROM Speed Select. Corresponding to Bit 25 - 24 of BROM_CR.
		Configuration Register 1
7	RFCEN	Receive Flow Control packet Enable. Corresponding to Bit 13 of RCR.
6	PME	PME_Enable. When set, indicates that the chip can assert wake-up event pin. Corresponding to Bit 8 of CFPMR.
5	PSD3c	PME Support D3cold. Corresponding to Bit 31 of CFPMR.
4	PSD1	PME Support D1. Corresponding to Bit 28 of CFPMR.
3	WPP	Wake-up pin property. When set, the wake-up pin is asserted high, while cleared, the wake-up pin is asserted low.
2	-	Reserved.
1	MPE	Magic Packet Enable. Corresponding to Bit 1 of WUECSR.
0	STSCHG	Status Change Enable. When set, the STSCHG pin is active, otherwise it acts as a wake-up pin.
		Configuration Register 2
7 - 2	-	Reserved.
1	WPPN	Wake-up pin pattern. When set, the wake-up output pin is a level signal, while cleared, the wake-up output pin is a pulse signal with the width of 160ms.
0	-	Reserved.

3.5.2 Direct Programming of EEPROM

The MTD800 features a easy way to program external EEPROM in-suit. When the RESET is active and if the upper byte of 00H on EEPROM is not 73H, the SROMPS bit in CSR40 register will be cleared to indicate that the current EEPROM has not been programmed yet. This allows the MTD800 to enter into Direct Programming mode if DPM bit is also set. In this mode the user can directly control the EEPROM interface signals by writing to the SROM_CR Port and the value on the EECS, ESK and EDI bits will be driven onto the ECS, EECLK(BRD2) and EEDI(BRD0) outputs respectively. These outputs will be latched so the user can generate a clock on EECLK by repetitively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals as per the 93C46 or 93C66 data sheet.

To read out the EEPROM data, users have to generate EEPROM interface signals into ECS, EECLK and EEDI as described above and in the mean time read the data from EEDO(BRD1) input via pin BRD1/EEDO. Reading Data Transfer Port during programming will not affect the latched data on ECS, EECLK and EEDI outputs. When the EEPROM has been programmed and verified (remember to program the upper byte of 00H with 73H), the user can give MTD800 a power-on reset to return to normal operation or set AUTOLD bit to read in the new data.

The Direct Programming mode is mainly used for production to program every bit of the blank EEPROM. The MTD800 also provides a flexible feature to allow the driver to reprogram the content of EEPROM, even the EEPROM has already been programmed.

3.5.3 BootROM Interface and Operation
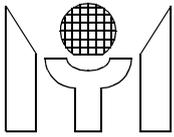
The MTD800 offers the address , data and control signals which can directly connected to BootROM without external logic on board. The BootROM size and speed can be configured beforehand and stored in the EEP-ROM. The access time ranges from 120ns to 300ns and the size achieves to 128KBytes at a maximum are all feasible to the MTD800. During machine boot, the system software identifies bootable devices by searching a specific signature (55AA) in BootROM. Once found, the system copies the code from the BootROM to a shadow RAM in the host memory and executes the code from the RAM.

3.6 Wake-up Frame Controller and ACPI

The MTD800 is compliant to ACPI specification by providing D0/D1/D3cold power states and a wake-up mechanism to transit from lower power state to higher power state. When the MTD800 enters into D1 power down state, only the PCI configuration registers can be accessed and other circuits except MAC and wake-up controller are all disabled to save power. The most saving power state is under the D3cold condition. In this state, all power to the PCI interface is cut off and the PCI clock is stopped, and requires an auxiliary power source to maintain MAC and wake-up controller to work normally. Once the MTD800 receives a wake-up packet, the chip will issue a PME# interrupt to notify system to be back to the D0 state or assert WAKEUP signal to ATX power PS-ON(refer to ATX specification v2.01) or mother board' s wake up interrupt line like ring-in to power on the whole system.

The wake-up frame controller supports the capabilities of recognizing AMD Magic packet frame and Microsoft OnNow Network Device wake-up frames. The Magic Packet is defined by the AMD for using to wake up the system during the powerdown session. This packet contains a special pattern which is composed by 16 duplications of Wake-up LAN address. In general, the address is the IEEE address of this node. This pattern can be located anywhere within the packet, but must be preceded by a synchronization stream which is defined as 6 bytes of FFH. Meanwhile, A network wake-up frame is typically a frame that is sent by existing network protocols. There are ARP request frame, unicast IP frame, direct IPX frame, NETBIOS name-lookup frame and so on. Each protocol has its own signature pattern. A network frame filter is designed to check the received frame if the signature pattern is embedded or not. The filter is parameterized with the byte offset, byte mask, CRC-16 and filtering commands. The MTD800 supports two such filters which are defined in the command and status registers (i.e., CSR4C, CSR50, CSR54 and CSR58).

4.0 REGISTERS DESCRIPTION

4.1 PCI Configuration Space

The operation of PCI configuration enables a full software-driven initialization and configuration. This permits the software to identify and query the MTD800. For keeping the contents of configuration registers intact after power-up, a software reset has no effect on them. There are total 15 long-word configuration registers. Of the configuration registers, 13 are standard registers that are defined in the PCI Local Bus Specification, while the other 2 are MTD800-specific registers. Following is the structure of configuration registers.
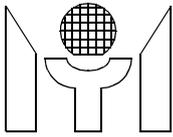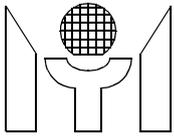
Table 4.1 PCI Configuration Space for MTD 800

	31:24	24:16	15:8	7:0
00H	Device ID		Vendor ID	
04H	Status		Command	
08H	Class Code			Revision ID
0CH	Reserved		Latency Timer	Cache Line Size
10H	Base Address Register (I/O Map)			
14H	Base Address Register (Memory Map)			
18H - 24H	Reserved			
28H	Cardbus CIS Pointer			
2CH	Subsystem ID		Subsystem Vendor ID	
30H	Expansion ROM Base Address Register			
34H	Reserved			Capabilities Pointer
38H	Reserved			
3CH	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line
40H	Remote Wake-Up-LAN Addr. 4	Remote Wake-Up-LAN Addr. 3	Remote Wake-Up-LAN Addr. 2	Remote Wake-Up-LAN Addr. 1
44H	Reserved		Remote Wake-Up-LAN Addr. 6	Remote Wake-Up-LAN Addr. 5
48H - 84H	Reserved			
88H	Power Management Capabilities		Next Item Pointer	Capabilities Identification
8CH	Reserved		Power Management Control & Status	

4.1.1 ID Registers - (CFVID , CFDID, CFRID, CFSVID, CFSID)
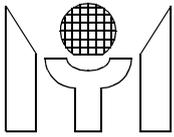
Table 4.2   Some PCI Identification Registers

Name	Location	Width	Description
Vendor ID	00H	16-Bit	**This field is hardwired to 1516H** This field indicates the device is manufactured by Myson. The valid identification is unique and allocated by the PCI SIG.
Device ID	02H	16-Bit	**This field is hardwired to 800H** This register identifies the one of the devices manufactured by Myson. The value is allocated by Myosn.
Revision ID	08H	8-Bit	**This field is hardwired to 00H** This register specifies that the device's revision identifier.
Subsystem Vendor ID	2CH	16-Bit	**The value is 00H after hardware reset** At final state, this field is loaded from EEPROM. This register provides an identification to identify the add-in card is manufactured by which one of subsystem house, although they has the same PCI controller. Its value can be allocated by PCI SIG.
Subsystem ID	2EH	16-Bit	**The value is 00H after hardware reset.** At final state, this field is loaded from EEPROM. This register is subsystem vendor specific to identify the add-in card.

4.1.2 Command Register - (CFCR)

The command register is located at configuration address of 04H. A value of 0 in CFCR means that the device is logically isolated from PCI bus for all access except configuration cycle.

Table 4.3   Bit Definition of the Command Register

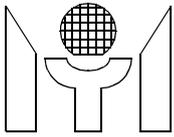| Name	Field	Description
IO Space	Bit 0	**The value is 0 after hardware reset.** This bit is readable and writable. A value of 1 allows the device to response an IO access. Otherwise, a value of 0 disables the device to echo.
Memory Space	Bit 1	**The value is 0 after hardware reset.** This bit is readable and writable. A value of 1 allows the device to response Memory transaction. Otherwise, a value of 0 disables the device to echo.
Bus Master	Bit 2	**The value is 0 after hardware reset.** This bit is readable and writable. A value of 1 enables the device's master function, else a value of 0 disables the function.

Name	Field	Description
Reserved	Bit 3	**This field is hardwired to 0.**
Memory Write and Invalidate	Bit 4	**The value is 0 after hardware reset.** This bit is readable and writable. A value of 1 allows the device to generate Memory Write and Invalidate command, else a value of 0 prohibits generating the command.
Reserved	Bit 5	**This field is hardwired to 0.**
Parity Error Response	Bit 6	**The value is 0 after hardware reset.** This bit is readable and writable. A value of 1 allows the device to take a normal action, like asserting PERR_, when parity error is detected. Otherwise it ignores the detection and continues to operate.
Reserved	Bit 7~15	**This field is hardwired to 0.**

4.1.3 Status Register - 06H (CFSR)

The status register is located at the configuration address of 06H.

Table 4.4   Bit Definition of the Status Register

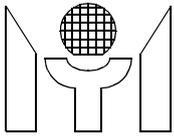| Name	Field	Description
Reserved	Bit 0~3	**This field is hardwired to 0.**
Power Management Capability	Bit 4	**The value of this field is loaded from EEPROM.** A value of 1 indicates that Power Management function is implemented in the device. And it meets the requirement of PCI Bus Power Management Interface Specification.
Reserved	Bit 5~6	**This field is hardwired to 0.**
Fast Back-to-Back Capable	Bit 7	**This field is hardwired to 1.** A value of 1 indicates the device is able to accept the operation of Fast Back-to-Back which is activated by different masters.

Name	Field	Description
Data Parity Error Detected	Bit 8	**The value is 0 after hardware reset.** This field is read only and write-one to clear. This bit is set when three conditions are true concurrently. (1) The device asserts PERR_ itself or it detects asserted PERR_. (2) The device is as a bus master during a operation in which a error occurred. (3) The Parity Error Response bit is set.
DEVSEL_ Timing	Bit 9~10	**This field is hardwired to 01H.** A value of 01H indicates the device asserts DEVSEL_ with medium speed.
Reserved	Bit 11	**This field is hardwired to 0.**
Received Target Abort	Bit 12	**The value is 0 after hardware reset.** This field is read only and write-one to clear. This bit is set whenever the device's master detects a termination with Target Abort.
Received master Abort	Bit 13	**The value is 0 after hardware reset.** This field is read only and write-one to clear. This bit is set whenever the devices's master terminates the transaction with Master Abort.
Reserved	Bit 14	**This field is hardwired to 0.**
Detected Parity Error	Bit 15	**The value is 0 after hardware reset.** This field is read only and write-one to clear. This bit is set whenever the device detects a parity error.

4.1.4 Burst Register (CFBR)

Table 4.5   The contents of Burst Registers

4.1.5 Base Address Register

Name	Location	Width	Description
Cache Line Size	0CH	8-Bit	**The value is 00H after hardware reset.** This field is readable and writable. This register specifies the cache line size for one burst. All of Memory Write and Invalidate, Memory Read Line and Memory Read Multiple cache-oriented commands must transfer data in a burst limited by Cache Line Size. The chip only supports CLS of 8, 16 and 32 longwords. If an attempt is made to write an unsupported value to this register, the chip behaves as if a value of zero was written.
Latency Timer	0DH	8-Bit	**The value is 00H after hardware reset.** This field is readable and writable. This register limits the maximum time in which the device is permitted to access the bus.
Min_Gnt	3EH	8-Bit	**The value is 0 after hardware reset.** At final state, this field is loaded from EEPROM. This register indicates how long the device needs to convey the data in a burst . It is in a unit of 0.25us
Max_Lat	3FH	8-Bit	**The value is 0 after hardware reset.** At final state, this field is loaded from EEPROM. This register indicates how often the device needs to convey the data. It is in a unit of 0.25us.

There are three base address registers. They are located at configuration address of 10H, 14H and 30H respectively. Following are the descriptions of these registers.

Table 4.6   I/O Map Base Address Register (CFIOBR)

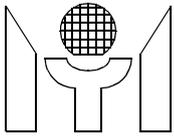| Name	Field	Description
IO Space Indicator	Bit 0	**This Field is hardwired to 1.** A value of 1 indicates that the register presents IO Base Address
Reserved	Bit 1	**This field is hardwired to 0.**
IO Space Size	Bit 2~6	**This field is hardwired to 0.** These bits are hardwired to 0 to indicate the device requires IO space in size of 128 longwords.
IO Base Address	Bit 7~31	**The value is 0 after hardware reset.** These bits is readable and writable. This field can be programmed by BIOS to specify the base address.

Table 4.7   Memory Map Base Address Register (CFMBR)
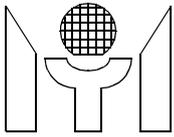
Name	Field	Description
Memory Space Indicator	Bit 0	**This field is hardwired to 0.** The value of 0 indicates that the register presents Memory Base Address
Reserved	Bit 1~3	**This field is hardwired to 0.**
Memory Space Size	Bit 4~9	**This field is hardwired to 0.** These bits are hardwired to 0 to indicate the Memory space size that the device requires.
Memory Base Address	Bit 10~31	**A value is 0 after hardware reset.** These bits is readable and writable. This field can be programmed by BIOS to specify the base address.

Table 4.8   Expansion ROM Base Address Register (CFERBR)

Name	Field	Description
Address Decode Enable	Bit 0	**The value is 0 after hardware reset.** This field is readable and writeable.This bit is set to 1 if the device requires the expansion ROM space, else it is set to 0. After the loading of ROM size from EEPROM, the value is set 1 if the ROM size is not equals to zero,
Reserved	Bit 1~10	**This field is hardwired to 0.**
Expansion ROM Size and Base Address	Bit 11~31	**The value is 0 after hardware reset.** This field is partitioned to two parts, one is for size and another is for base address. Size field is hardwired to 0 dependent on ROM size. Base Address field is read-write bits which can be allocated by BIOS.

4.1.6 CardBus CIS Pointer Register - 28H, 32-Bit Width.(CFCISPR)

The CardBus CIS pointer register is located at the configuration address of 28H.

Table 4.8 The Content of CardBus CIS Pointer Register

Name	Field	Description
Address Space Indicator	Bit 0~2	**The value is 0 after hardware reset.** This field is read only and loaded from EEPROM. These bits indicate the location of CIS base address. (1) The value of 2 indicates that the CIS is stored in EEPROM (2) The value of 7 indicates that the CIS is stored in expansion ROM.
Address Space Off-set	Bit 3~27	**The value is 0 after hardware reset.** This field is read only and loaded from EEPROM. These bits contains the address offset within the address space indicated by the Address Space Indicator.
ROM Image	Bit 28~31	**The value is 0 after hardware reset.** This field is read only and loaded from EEPROM. The 4-Bit ROM image field value when the CIS is in an expansion ROM.

4.1.7 Interrupt Register (CFIR)

Table 4.8   The Content of Interrupt Register

Name	Location	Width	Description
Interrupt Line	3CH	8-Bit	**The value is 0 after hardware reset.** These bits is readable and writable. This field contains the routing information of system interrupt controller.
Interrupt Pin	3DH	8-Bit	**This field is hardwired to 01H.** The value of 01H indicates the device uses INTA_ to interrupt.

4.1.8 Class Code Register (CFCCR)

Table 4.8   The Content of Class Code Register

4.1.9 Capabilities Pointer Register (CFCPR)

Table 4.9   The Content of Capabilities Pointer Register
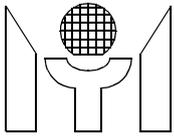
Name	Location	Description
Class Codes	09H ~ 0BH	**This field is hardwired to 020000H.** The value of 020000H indicates the device is a ethernet controller.

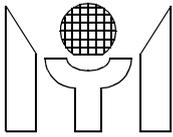| Name	Location	Description
Capabilities Pointer	34H	This register stores a pointer to the power-management register block in the PCI configuration space. This pointer is in effect only when the power management capabilities bit in the status register is set. Otherwise, the pointer is set to "00H". **The value of this field is "88H" when power-management bit is set.**

4.1.10 Wake-Up-LAN / Power Management Registers (CFWUAR, CFPMR)

The Wake-Up-LAN register stores the address for matching the magic packet under power-down mode and locates at the configuration address of 40H and 44H. The Power Management register defines the associated control and status bits with the power management event and octets at the configuration address of 88H and 8CH. When the chip works in power down mode, these two registers can not be accessed. Any read or write action is ignored during D1/D3HOT states.

Table 4.10   The Content of Wake-Up-LAN / Power Management Registers

Name	Field	Description
Remote Wake-Up-LAN Address Register (offset 40H)		
WUL_Addr3	31 - 24	**The 4th byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.
WUL_Addr2	23 - 16	**The 3rd byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.
WUL_Addr1	15 - 8	**The 2nd byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.
WUL_Addr0	7 - 0	**The 1st byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.
(offset 44H)		
Reserved	31 - 16	**This field is hardwired to 0.**
WUL_Addr5	15 - 8	**The 6th byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.
WUL_Addr4	7 - 0	**The 5th byte in the Wake-Up-LAN Address.** The value is loaded from EEPROM.

| Name	Field	Description
Power Management Block (offset 88H)		
PME Support D3cold	31	If this bit is set, the chip asserts PME in D3cold power state. Otherwise, the chip does not asset PME in this power state. The value is loaded from EEPROM.
PME Support D3hot	30	**This field is hardwired to 1.** The chip dose support D3hot power state.
PME Support D2	29	**This field is hardwired to 0.** The chip dose not support D2 power state.
PME Support D1	28	If this bit is set, the chip asserts PME in D1 power state. Otherwise, the chip does not asset PME in this power state. The value is loaded from EEPROM.
PME Support D0	27	**This field is hardwired to 0.** The chip dose not support PME during power state D0.
D2 Support	26	**This field is hardwired to 0.** The chip dose not support D2 power state.
D1 Support	25	**This field is hardwired to 1.** The chip supports D1 power state.
Reserved	24 - 22	**This field is hardwired to 0.**
Device Specific Initialization	21	**This field is hardwired to 0,** indicating that the chip does not require a special initialization code sequence in order to be configured correctly.
Reserved	20	**This field is hardwired to 0.**
Power Management Event Clock	19	**This field is hardwired to 0,** indicating that the chip does not rely on the presence of the CardBus clock in order to generate a PME.
Power Management PCI Version	18 - 16	**This field is hardwired to "001",** indicating that the chip complies with revision 1 of the *PCI Power Management Specification.*
Next Item Pointer	15 - 8	**This field is hardwired to 8' h00,** indicating that this is the last item of the Capability linked list.
Capabilities ID	7 - 0	**This field is hardwired to 8' h01,** indicating that this is the power-management register block.
Power-Management Control and Status Register (offset 8CH)		
PME_status	Bit 15	When set, indicates that the chip has detected a power-management event. This bit is cleared on power-up reset or by write 1. It is not modified by software reset.
PME_Enable	Bit 8	When set, indicates that the chip can assert wake-up event pin. This bit is cleared on power-up reset. The value of this field is loaded from EEPROM.
Power State	Bit 1 - 0	The definition of the field values are 0 -D0, 1 - D1, 2 - Not defined and 3 - D3cold. The field gets a value of 0 after power-up.
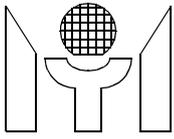
4.2 Command and Status Registers

The MTD800 Command and Status Registers (CSRs) are mapped into the host I/O or the host memory address space through the base addresses defined in the PCI configuration registers. The CSRs are quad-byte aligned, 32-bit long, and must be accessed using longword instructions with quadbyte-aligned addresses only. Following is the word layout table for CSRs.

Table 4.11 MTD800 Internal Command and Status Registers Layout

Offset Address					Operation
00	PAR3	PAR2	PAR1	PAR0	RW
04	-	-	PAR5	PAR4	RW
08	MAR3	MAR2	MAR1	MAR0	RW
0C	MAR7	MAR6	MAR5	MAR4	RW
10	FAR3	FAR2	FAR1	FAR0	RW
14	-	-	FAR5	FAR4	RW
18	TCR		RCR		RW
1C	BCR				RW

Offset Address			Operation
20	Transmit poll demand		WO
24	Receive poll demand		WO
28	Receive current word pointer		RO
2C	Transmit list base address		WO
30	Receive list base address		WO
34	Interrupt Status Register		RW
38	Interrupt Mask Register		RW
3C	Flow Control High Threshold	Flow Control Low Threshold	RW
40	BROM_CR	SROM_CR	MII management	RW
44	Tally Counter CRC	Tally Counter MPA	RO
48	Tally Counter TSR		RO

Offset Address			Operation
4C	Filter A Byte Mask		WO
50	Filter A offset	Filter A Cmd	Filter A CRC-16	RW
54	Filter B Byte Mask		WO
58	Filter B offset	Filter B Cmd	Filter B CRC-16	RW
5C	Wake-up Events CSR		RW

Offset Address	Operation
78	TX FIFO Dump Register	RO
7C	RX FIFO Dump Register	RO

Offset Address	Operation
80	Function Event Register	RW
84	Function Event Mask Register	RW
88	Function Present State Register	RO
8C	Function Force Event Register	WO
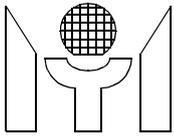
4.2.1 Physical Address Registers (PAR)

These registers store the NIC card's Ethernet Physical Address. The location of PAR is mapped into an offset address ranges from 00H to 05H. During the receiving process, the pre-stored physical node address is used for Address Recognition Logic to filter out the incoming packets which are not belong to this addressed station. The Physical Address registers are loaded from EEPROM during initialization and can also be changed by software driver when the chip is not during operation, but it remains unchanged after software reset is applied. Note that the single-byte write is not supported to this register.

4.2.2 Multicast Address Registers (MAR)

These registers store 64 bits serving as hash bucket heads. The location of MAR is mapped into an offset address range from 08H to 0FH. For any incoming packet with a multicast destination address, the MTD800 applies the standard Ethernet Cyclic Redundancy Check (CRC) function to the destination address field, then it uses the most significant 6 bits of the result as a bit index into the table. If the indexed bit is set, the frame is accepted. If the bit is cleared, the frame is rejected. The value in this register is undetermined after hardware reset and can not be changed by software reset. Note that the single-byte write is not supported to this register.
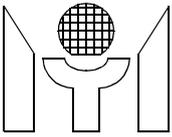
4.2.3 Flow-control Address Registers (FAR)

These registers stores a special destination address for the flow control packet. The location of FAR is mapped into an offset address range from 10H to 15H. During full-duplex operation, the incoming packet's DA will be compared to this flow control address, if matched, then the chip will take the appropriate action. According to the IEEE 802.3x standard, the contents of these address registers should be written with 01-80-c2-00-00-01 by driver. The value in this register is undetermined after hareware reset and can not be changed by software reset. Note that the single-byte write is not supported to this register.

4.2.4 Receive Configuration Register (RCR)

This register is located in an offset address of 18H and the access type is read/writable. The receive configuration register reflects the NIC receive configuration and can be cleared to the default value by hardware/software reset. Following is the bit description of RCR.

Table 4.12   The Content of Receive Configuration Register

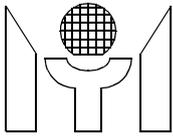| Bit	Symbol	Description
15	RxS	Receive Status. When "1", indicates the receive process is running. When "0", indicate the receive process is stopped. This is a read-only bit and the default value is "0".
14	EIEN	Early Interrupt Enable. When set, the chip will work under early interrupt mode. When cleared, it will operate in normal interrupt mode. The default value is "0".
13	RFCEN	Receive Flow Control packet Enable. When set, the flow control packet will be recognized during full duplex operation. When cleared, it will be considered as a normal packet. The default value is "0", but may be changed by loading from EEPROM.
12	NDFA	Not Defined Flow control Address. For the legacy flow control device, a 802.3x special DA was not defined at that time. For the reason of backward compatibility, only the length/type field is checked when this bit is set. The default value is "0".
11	RBLEN	Receive Burst Length Enable. When set, the receive burst transaction will use the following receive programmable burst length. When cleared, the PBL defined in the bus command register will be adopted. The default value is "1".

10- 8	RPBL[2:0]	Receive Programmable Burst Length
		
		RPBL2 RPBL1 RPBL0 Length
		  0 0 0 1 words
		  0 0 1 4
		  0 1 0 8
		  0 1 1 16
		  1 0 0 32
		  1 0 1 64
		  1 1 0 128
		  1 1 1 512
		
		The default value is "011".

7	PROM	Promiscuous Mode Bit. If PROM equals to 1, all valid packets with any physical destination address are accepted. If PROM equals to 0, the physical address of incoming packet must match the node address programmed in the PAR0 ~ 5, otherwise it will be rejected. The default value is "0".
6	AB	Accept Broadcast Bit. If AB equals to 1, all packets with broadcast destination address are accepted. If AB equals to 0, any packet with broadcast address is rejected. The default value is "1".
5	AM	Accept Multicast Bit. If AM equals to 1, all packets with desired multicast destination address are accepted. If AM equals to 0, any packet with multicast address is rejected. The default value is "1".
4		Reserved.
3	ARP	Accept Runt Packet. If ARP equals to 1, all packets with their length less than 64 bytes are accepted. If ARP equals to 0, any packet whose length is less than 64 bytes is rejected. The default value is "0".

Bit	Symbol	Description
2	ALP	Accept Long Packet. If ALP equals to 1, all packets with their length larger than 1518 bytes are accepted. If ALP equals to 0, any packet whose length is larger than 1518 bytes is rejected. The default value is "0".
1	SEP	Set Error Packet. If SEP equals to 1, all packets with receive errors are accepted. If SEP equals to 0, any packet with receive errors is rejected. The default value is "0".
0	RE	Receive Enable. When set, the receive process enters into the running state. The MTD800 attempts to acquire a descriptor from the receive list and processes the incoming frame. When cleared, the receive process is placed in the stopped state after completing the reception of current frame. The default value is "0".

4.2.5 Transmit Configuration Register (TCR)

This register is located in an offset address of 1AH and the access type is read/writable. The transmit configuration register reflects the NIC transmit configuration and can be cleared to the default value by hardware or software reset. Following is the bit description of TCR.

Table 4.13   The Content of Transmit Configuration Register

Bit	Symbol	Description
15	TxS	Transmit Status. When "1", indicates the transmit process is running. When "0", indicate the transmit process is stopped. This is a read-only bit and the default value is "0".
14-13		Reserved
12	BACKOPT	Optional Backoff. When set, a non-standard algorithm will be used. The default value is "0".
11	FBACK	Fast Back-off. When "1", indicates the back off algorithm will not count up to one slot time instead of one bit time. It will speed up the process of retransmitting data and mainly used for debugging.
10	-	Reserved
9	Enhanced	When set, the chip will work under enhanced mode, otherwise, a normal operation mode is selected. The default value is "0".
8	TFCEN	Transmit Flow Control packet Enable. When set, the chip is able to transmit the flow-control packet during full duplex operation. When cleared, it will not transmit any flow-control packet. The default value is "0", but may be changed by loading from EEPROM.

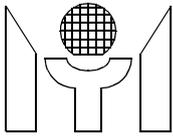| Bit	Symbol	Description

7 - 5	TFT[2:0]	Transmit FIFO Threshold
		
		TFT2 TFT1 TFT0 Threshold
		  0 0 0 64 bytes
		  0 0 1 32
		  0 1 0 128
		  0 1 1 256
		  1 0 0 512
		  1 0 1 768
		  1 1 0 1024
		  1 1 1 transmit store and forward
		The default value is "000".

4	FD	Full-Duplex Mode. The half-duplex operation is selected when FD is cleared, while the full-duplex operation is selected when FD is set. The default value is "0".
3	PS	Port Speed. When auto-negotiation is enabled, this bit reflects the status of current connection speed. "1" means 10Mb/s while "0" indicates as 100Mb/s. The default value is "0".
2	TE	Transmit Enable. When set, the transmission process enters into the running state, and the MTD800 checks the transmit list at the current position for a frame to be transmitted. When cleared, the transmission process is placed in the stopped state after the completion of the current frame transmission.The default value is "0".

1 - 0	LB[1:0]	Loopback mode selection.
		  0 0 Normal
		  1 0 MII loopback
		 The default value is "00".

4.2.6 Bus Command Registers (BCR)

The register is located in an offset address of 1CH. The access type of BCR is read/writable. The bus command register is used to control the operation of PCI bus transaction by means of adjusting the burst length or enabling the read/write cache commands. The register can be cleared to the default value by hardware or software reset. Following are the bit description of BCR.

Table 4.14   The Content of Bus Configuration Register

Bit	Symbol	Description
31- 10	-	Reserved
9	Prog	Programming. This bit is totally controlled by driver and not affect the hardware operation. It is a tag bit for driver to differentiate the programming status when multiple cards installed in a platform. The default value is "0".
8	RLE	Read Line command Enable. When set, this cache-oriented command will be used if cache-alignment occurs. The default value is "0".
7	RME	Read Multiple command Enable. When set, this cache-oriented command will be used if cache-alignment occurs. The default value is "0".
6	WIE	Write and Invalidate command Enable. When set, this cache-oriented command will be used if cache-alignment occurs. The default value is "0".

5 - 3	PBL	Programmable Burst Length. Determines the allowable number of long-words to be transferred during one PCI transaction initiated by the MTD800. There are eight permissible values used for burst length. The relationship between the value in PBL and burst length is shown below;
		
		 PBL2 PBL1 PBL0 Length
		  0 0 0 1
		  0 0 1 4
		  0 1 0 8
		  0 1 1 16
		  1 0 0 32
		  1 0 1 64
		  1 1 0 128
		  1 1 1 512.
		
		 The default value is "011".

2 - 1	-	Reserved.
0	SWR	When set, the MTD800 resets all internal hardware except that the configuration registers and address registers like PAR, FAR and MAR etc. are not affected. The default value is "0".

4.2.7 Transmit Poll Demand Register (TxPDR)

The TxPDR is used for software driver to command MTD800 to poll the transmit descriptor list. This register is located at an offset address 20H and the access type is WRITE ONLY.

Table 4.15 Transmit Poll Demand Register

Bit	Symbol	Description
31 - 0	-	When written with any value, the MTD800 begins to check the frame for transmission.
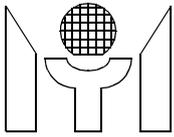
4.2.8 Receive Poll Demand Register (RxPDR)

The RxPDR is used for software driver to command MTD800 to poll the receive descriptor list. This register is located at an offset address 24H and the access type is WRITE ONLY.

Table 4.16 Receive Poll Demand Register

Bit	Symbol	Description
31 - 0	-	When written with any value, the MTD800 begins to check if any available descriptor for the reception.

4.2.9 Receive Current Word Pointer (RxCWP)

The RxCWP allows the driver to read the current address value in the Rx DMA address counter register. This counter will keep the track of location in the host memory for the last moved-in received word. This register is useful when operates in the receive early interrupt mode. It must be cleared after hardware or software reset. The location of RxCWP is at an offset address 28H and the access type is READ ONLY.

Table 4.17 The Content of Receive Current Word Pointer Register

Bit	Symbol	Description
31- 2	RxCWP	Indicates the current word pointer of received word in the host memory.
1-0	MBZ	This field must be zero since the address have to be longword alignment.

4.2.10 Transmit List Base Address (TxLBA)

The TxLBA stores the base address for the transmit descriptor list. This register is located at an offset address 2CH and the access type is read/writable. The base address is used for MTD800 to point to the start of the transmit descriptor list. It must be cleared after hardware or software reset and the access type is WRITE ONLY.

Table 4.18 Transmit List Base Address Register

Bit	Symbol	Description
31- 2	BA	Indicates the base address that points to the start of the transmit list.
1-0	MBZ	This field must be zero since the descriptors have to be longword alignment.

4.2.11 Receive List Base Address (RxLBA)

The RxLBA stores the base address for the receive descriptor list. This register is located at an offset address 30H and the access type is read/writable. The base address is used for MTD800 to point to the start of the receive descriptor list. It must be cleared after hardware or software reset and the access type is WRITE ONLY.
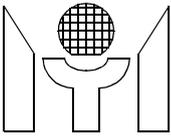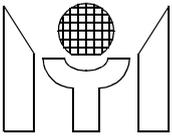
Table 4.19 Receive List Base Address Register

Bit	Symbol	Description
31- 2	BA	Indicates the base address that points to the start of the receive list.
1-0	MBZ	This field must be zero since the descriptors have to be longword alignment.

4.2.12 Interrupt Status Register (ISR)

The interrupt status register reflects the NIC's interrupt status. The host reads from this register to determine the cause of the interrupt. Individual bit is cleared by writing a "1" to the corresponding bit. It must be cleared after hardware or software reset. ISR is located in an offset address of 34H. The access type are read/writable. Following is the bit description of the register.

Table 4.20 The Content of Interrupt Status Register

Bit	Symbol	Description
31-18	-	Reserved.
17	RFCON	Receive Flow Control Xon Packet. When asserted, indicates that the flow control Xon packet is received.
16	RFCOFF	Receive Flow Control Xoff Packet. When asserted, indicates that the flow control Xoff packet is received.
15 - 14	-	Reserved.
13	FBE	Fatal Bus Error. Indicates that a bus error occurs. The type of error is shown in the following bits.
12 - 11	ET	Error Type. Indicates the type of error that causes bus error. They are valid only when FBE is set. These two bits are READ ONLY. Following is their definition, ET1 ET0 Error Type 0 0 Parity Error 0 1 Master Abort 1 0 Target Abort 1 1 Reserved.
10	TUNF	Transmit Underflow. When asserted, indicates that the Tx FIFO underflow condition occurs during frame transmission.
9	ROVF	Receive Overflow. When asserted, indicates that the Rx FIFO overflow condition occurs during frame reception.
8	ETI	Early Transmit Interrupt. Indicate that the frame to be transmitted is fully transferred into the Tx FIFO but not transmitted onto the network.
7	ERI	Early Receive Interrupt. Indicates that the received packet has filled the first data buffer of the frame.
6	CNTOVF	Counter Overflow. When asserted, indicates that CRC or MPA tally counter encounters overflow condition.
5	RBU	Receive Buffer Unavailable. When asserted, indicates that the next descriptor is owned by the host and cannot be acquired by the MTD800.

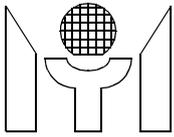| Bit	Symbol	Description
4	TBU	Transmit Buffer Unavailable. When asserted, indicates that the next descriptor is owned by the host and cannot be acquired by the MTD800.
3	TI	Transmit Interrupt. When asserted, indicates that the frame transmission has completed.
2	RI	Receive Interrupt. When asserted, indicates that the frame reception has completed.
1	RxErI	Receive Error Interrupt. This bit takes effective only in the receive early interrupt mode. When set, indicates that the current received frame is erroneous.
0	-	Reserved.

4.2.13 Interrupt Mask Register (IMR)

The interrupt mask register is used for masking the interrupt which is reflected in the corresponding bit in the interrupt status register. After power up, all bits are reset to " 0". To set the individual bit will enable the corresponding interrupt. It must be cleared after hardware or software reset. IMR is located in an offset addresses of 38H.The access type is read/writable. Following is the bit description of the register.

Table 4.21   The Content of Interrupt Mask Register

Bit	Symbol	Description
31 - 18	-	Reserved.
17	MRFCON	Mask Receive Flow Control Xon Packet. When set, the RFCON interrupt is masked.
16	MRFCOFF	Mask Receive Flow Control Xoff Packet. When set, the RFCOFF interrupt is masked.
15 - 14	-	Reserved.
13	MFBE	Mask Fatal Bus Error. When set, the FBE interrupt is masked.
12-11	-	Reserved.
10	MTUNF	Mask Transmit Underflow. When set, the TUNF interrupt is masked.
9	MROVF	Mask Receive Overflow. When set, the ROVF interrupt is masked.
8	METI	Mask Early Transmit Interrupt. When set, the ETI is masked.
7	MERI	Mask Early Receive Interrupt. When set, the ERI is masked.
6	MCNTOVF	Mask Counter Overflow. When set, the CNTOVF interrupt is masked.
5	MRBU	Mask Receive Buffer Unavailable. When set, the RBU interrupt is masked.
4	MTBU	Mask Transmit Buffer Unavailable. When set, the TBU interrupt is masked.
3	MTI	Mask Transmit Interrupt. When set, the TI is masked.
2	MRI	Mask Receive Interrupt. When set, the RI is masked.

Bit	Symbol	Description
1	MRxErI	Mask Receive Error Interrupt. When set, the RxErI is masked.
0	-	Reserved.

4.2.14 Flow Control High / Low Threshold Registers (FCHT / FCLT)

The chip can generate a Flow Control Pause frame (here a Xon frame) when the fullness of its RX FIFO is beyond the high threshold. After the data in the RX FIFO have been consumed a lot, such that the fullness is below the low threshold, then a Xoff frame is issued. These registers hold the high/low threshold value which determine the number of words left in the RX FIFO. The contents of these registers can not be changed by software reset. The location of register is mapped to an offset address 3CH.

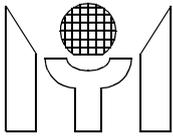Table 4.22   The Content of Flow Control Threshold Registers

Bit	Symbol	Description
31-25	-	Reserved.
24-16	FCHT	Flow Control High Threshold register. The default value is " 180H" after hardware reset.
15-9	-	Reserved.
8-0	FCLT	Flow Control Low Threshold register. The default value is " 80H" after hardware reset.

4.2.15 BootROM / EEPROM and MII Management Registers(BROM_CR/SROM_CR/ MIImgt)

The BROM_CR, SROM_CR and MIImgt registers provide an interface for the driver to access the Boot ROM, Serial EEPROM and the MII management port. They are respectively located at the offset address of 43H, 42H and 40H. BROM_CR defines the Boot ROM size, speed and the control mode. SROM_CR provides the direct programming mode for the driver to read and write the EEPROM. The MIImgt selects an operation mode for reading and writing the MII PHY registers through the MII management interface. The register must be cleared to the default value after hardware or software reset except that the " BRWE" bit is not changed by software reset.

Table 4.23   The Content of BootROM / EEPROM and MII Management Registers

Bit	Symbol	Description
BROM_CR (offset 43H)		
31 - 30	-	Reserved
29	BRWE	Boot ROM Write Enable. This bit is effective only when a flash memory is used instead of EPROM. When set, a write operation will be executed. The default value is " 0" and can not be changed by software reset.

Bit	Symbol	Description
28 - 26	BRSZ[2:0]	Indicates the Boot ROM size. BRSZ[2] BRSZ[1] BRSZ[0] Size 0 0 0 0 (means NO Boot ROM) 0 0 1 8K Bytes 0 1 0 16K Bytes 0 1 1 32K Bytes 1 0 0 64K Bytes 1 0 1 128K Bytes 1 1 X Reserved. The default value is "0" but may be changed by loading from EEPROM.
25 - 24	BRSPD[1:0]	Boot ROM Speed Select. BRSPD[1] BRSPD[0] Access time 0 0 120 ns 0 1 180 ns 1 0 240 ns 1 1 300 ns The default value is "0" but may be changed by loading from EEPROM.
		SROM_CR (offset 42H)
23	DPM	Direct Programming Mode. When set, it allows the driver to directly access EEPROM. The default value is "0".
22	SROMPS	Serial EEPROM Programming Status. This bit is read-only. When "1", indicates that the EEPROM has been programmed. When "0", means that the EEPROM is not programmed yet. The default value is "0".
21	-	Reserved.
20	AUTOLD	Auto Load. When set, it allows the chip to dynamically reload EEPROM contents. After auto-load completed, this bit will be self-cleared. The default value is "0".
19	ECS	EEPROM interface CS signal . This bit is effective only when direct pro-gramming mode is enabled. The default value is "0".
18	ECK	EEPROM interface CK signal. This bit is effective only when direct pro-gramming mode is enabled. The default value is "0".
17	EDI	EEPROM interface DI signal. This bit is effective only when direct pro-gramming mode is enabled. The default value is "0".
16	EDO	EEPROM interface DO signal (read-only). This bit is effective only when direct programming mode is enabled. The default value is "0" but may be changed due to the pin value.
		MIImgt (offset 40H)
15-4	-	Reserved
3	MOUT	MDIO output enable indicator while in direct programming mode. The default value is "0".
2	MDO	MII management port data output status while in direct programming mode. The default value is "0".
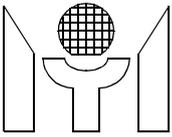
Bit	Symbol	Description
1	MDI	MII management port data input status while in direct programming mode (read-only). The default value is "0" but may be changed due to the pin value.
0	MDC	MII management port clock status while in direct programming mode. The default value is "0".

4.2.16 Tally Counters for CRC and MPA (TC_CRC / TC_MPA)

The tally counter CRC is used to count the number of events that CRC error occurs within the received packet, while the tally counter MPA accumulates the number of discarded frames because that the receive buffer is unavailable or the receive fifo overflows. These registers are located at the offset address of 44H and 46H respectively. The access type is READ ONLY and the content is cleared after read. The default value is 0 after hardware reset and can not be changed by software reset.

Table 4.24   The Content of Tally Counters for CRC and MPA

Bit	Symbol	Description
31	TCOVF	When set, indicates that CRC tally counter overflows.
30 - 16	CRC_C	Indicates the number of events that CRC error occurs.
15	TMOVF	When set, indicates that MPA tally counter overflows.
14 - 0	MPA_C	Indicates the number of discard frame because of buffer unavailable or fifo overflow.

### 4.2.17 Tally Counters for Transmit Status Report (TC_TSR)

The tally counter TSR is used to count the number of events that the transmitting packet is aborted due to the excess collisions, the number of events that occurring late collision and the retry counts that ever happened. These registers are located at the offset address of 48. The access type is READ ONLY and the content is cleared after read.The default value is 0 after hardware reset and can not be changed by software reset.

Table 4.24   The Content of Tally Counters for TSR

Bit	Symbol	Description
31- 24	Abort_C	Indicates the number of aborted packets.
23 - 16	LCOL_C	Indicates the number of late collisions.
15 - 0	NCR	Indicates the number of transmission retry.

4.2.18 Network Wake-up Frame Configuration Registers

The MTD800 supports OnNow Network Device Class Wake-up frames such as IP , IPX and SNAP frames. These registers are used to load the filtering parameters for matching the dedicated patterns which are embedded in each type of network frame. Two filters are provided to check the incoming frames. Each filter can operate in conjunction with another filter to recognize a frame with complicated patterns. Filter A is located at an offset address 4CH while the filter B is mapped to an offset of 54H. Both are in the same format
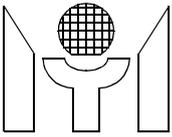
and can be read/writable. The contents of these registers is cleared to the default value after hardware reset but can not be changed by software reset.

Table 4.25 Fileter Byte Mask (A : offset 4CH , B : offset 54H)

Bit	Symbol	Description
31	-	Reserved
30 - 0	BM[30:0]	Byte Mask. When BM[i] is set, it allows the ith byte to be checked. When BM[i] is reset, the filter will not do any operation on the ith byte. The default value is "0".

Table 4.26 Filter Offset, Command and CRC-16 (A : offset 54H , B : offset 5C)

Bit	Symbol	Description
31 - 24	BO[7:0]	Byte Offset. Indicates the offset position from the first byte of frame to be examined by the filter. The minimum value allowed for this field is "12" in decimal. The default value is "12" in decimal.
Filter Command		
23 - 19	-	Reserved
18	CONJ	Conjuction. When set, a logic AND operation will be performed on the result of previous filter and the current one. When cleared, the matching result of each filter is independent. The default value is "0".
17	IOM	Inverse Operation Mode. When set, the frames which satisfy the dedicated pattern will be reject. It renders that the frame dose not match the filter considered as a network wake-up frame. The default value is "0".
16	FE	Filter Enable. When set, the filtering parameters are only effective, otherwise, the filter is disabled. The default value is "0".
15 - 0	CRC16	This field contains the 16-bit CRC value which is calculated according to the dedicated pattern specified by the offset and byte-mask. he default value is "0".

4.2.19 Wake-Up Events Control and Status Register (WUECSR)

The WUECSR stores the control bits for commanding the ability of wake-up operation and the status bits for monitoring the occurrence of wake-up events. This register is located at an offset address 5CH and the access type is read/writable. The register can be cleared to the default value after hardware or software reset.

Table 4.27 The Content of Wake-Up Events Control and Status Register

Bit	Symbol	Description
31 - 12	-	Reserved.
11	FrcWUP	Force Wake Up Lan mode. When set, the chip is forced to receive only magic packet or wake-up frame under D0 state. It is useful for debugging purpose. The default value is "0".
10	STSCHG	Status Change Enable. When set, the STSCHG pin is active, otherwise it acts as a wake-up pin. The default value is "0" but may be changed by loading from EEPROM.
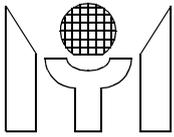
Bit	Symbol	Description
9	AGU	Accept Global Unicast. When set, any unicast packet accepted by the MTD800 will be considered as a wake-up event. The default value is "0".
8	WPPN	Wake-Up pin output pattern. When set, the wake-up output pin is a level signal, while cleared, the wake-up output pin is a pulse signal with the width of 160ms. The default value is "1" but may be changed by loading from EEPROM.
7	WPP	Wake-up pin property. When set, the wake-up pin is asserted high, while cleared, the wake-up pin is asserted low. The default value is "1" but may be changed by loading from EEPROM.
6	-	Reserved.
5	MPR	Magic Packet Received. When set, indicates that a wake-up event is generated by the reception of magic packet.It is cleared by writing 1 to this bit.The default value is "0".
4	WUFR	Wake-Up Frame Received. When set, indicates that a wake-up event is generated by the reception of wake-up frame.It is cleared by writing 1 to this bit.The default value is "0".
3 - 2	-	Reserved.
1	MPE	Magic Packet Enable. A 1 enables the wake-up event due to the reception of magic packet while a 0 disables this function. The default value is loaded from EEPROM.
0	WUFE	Wake-Up Frame Enable. A 1 enables the wake-up event due to the reception of wake-up frame while a 0 disables this function. The default value is "0".

4.2.20 TX/RX FIFO Dump Registers

These two registers are used for internal test only. When transmit or receive process is stopped, the driver can directly access these dump registers for debugging purpose.

4.2.21 CardBus Status Changed Registers

For complying to CardBus specification, the chip implements four Status Changed registers. These registers are accessed by the CardBus system software and typically not reached by the MTD800 driver. The Status Changed registers are mapped only to the memory space and not to the I/O space. The four registers take effect to the operation of chip only when the "STSCHG" bit of the EEPROM is set. Note that the unspecified bits in the following register should be hardwired to zero.
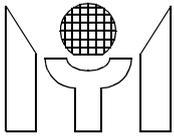
Table 4.28   The Content of CardBus Status Changed Registers

1. Function Event Register

| Bit	Symbol	Description
15	Interrupt	This bit is set in response to interrupt pending. It is cleared by write one.
4	GWUE	General Wake-Up Event. When the chip has detected a power management event, this bit is set accordingly. This bit is also automatically cleared upon that the PME_status bit in the configuration register is reset. It is cleared by write one.

2. Function Event Mask Register

Bit	Symbol	Description
15	IntEn	Interrupt Enable. When set, enables the assertion of the card bus interrupt pin.
14	WUESEn	Wake-Up Event Summary Enable. When set together with the General Wake-Up Event Enable bit, allows the assertion of the STSCHG pin.
4	GWUEEn	General Wake-Up Event Enable. When set together with the Wake-Up Event Summary Enable bit, allows the assertion of the STSCHG pin.

3. Function Preset State Register

Bit	Symbol	Description
15	IntSTS	Interrupt Status. This bit reflects the status of interrupt line.
4	GWUE	General Wake-Up Event. This bit reflects the current state of the wake-up event.

4. Function Force Event Register

Bit	Symbol	Description
15	FrceInt	Force Interrupt. The interrupt pin is asserted by writing 1 to this bit, but the interrupt bit in Function Present Register is not affected.
4	FrceWU	Force Wake-Up. The STSCHG pin is asserted by writing 1 to this bit, but the wake-up event field in the Function Present Register is not affected.
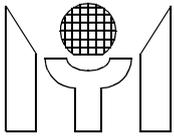
5.0 ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	RATING	Unit
V_{CC}	Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to Vcc+0.3	V
V_{OUT}	Output Voltage	-0.3 to Vcc+0.3	V
T_{STG}	Storage Temperature	-55 to 150	^{o}C

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage	0	-	Vcc	V
T_{OPR}	Commercial Junction Operating Temperature	0	25	115	^{o}C
	Industrial Junction Operating Temperature	-40	25	125	^{o}C

5.1.3 DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	no pull-up or down	-1		1	uA
I_{OZ}	Tri-state Leakage Current		-1		1	uA
C_{IN}	Input Capacitance			2.8		pF
C_{OUT}	Output Capacitance		2.7		4.9	pF
C_{BID3}	Bi-direction buffer Capacitance		2.7		4.9	pF
V_{IL}	Input Low Voltage	CMOS			0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc			V
V_{OH}	Output High Voltage	I_{OL}=2,4,8,12,16,24mA	2.4			V
V_{OL}	Output Low Voltage	I_{OH}=2,4,8,12,16,24mA			0.4	V
R_{I}	Input Pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		75		KOhm

5.2 AC Characteristics

5.2.1 MII Timing
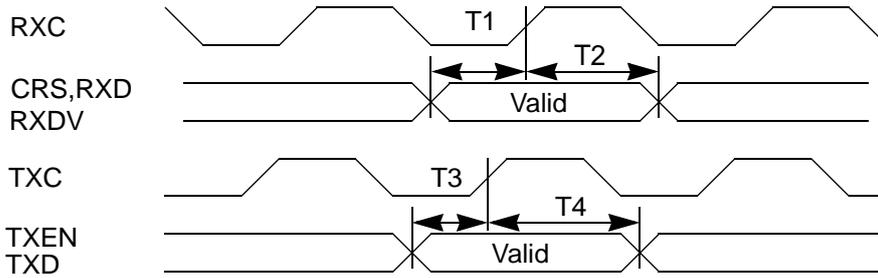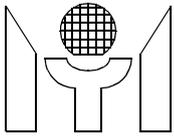
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	MII input setup time	10			nS	
T2	MII input hold time	10			nS	
T3	MII output setup time	20		35	nS	
T4	MII output hold time	5		20	nS	

5.2.2 PCI Timing

• Read Cycle
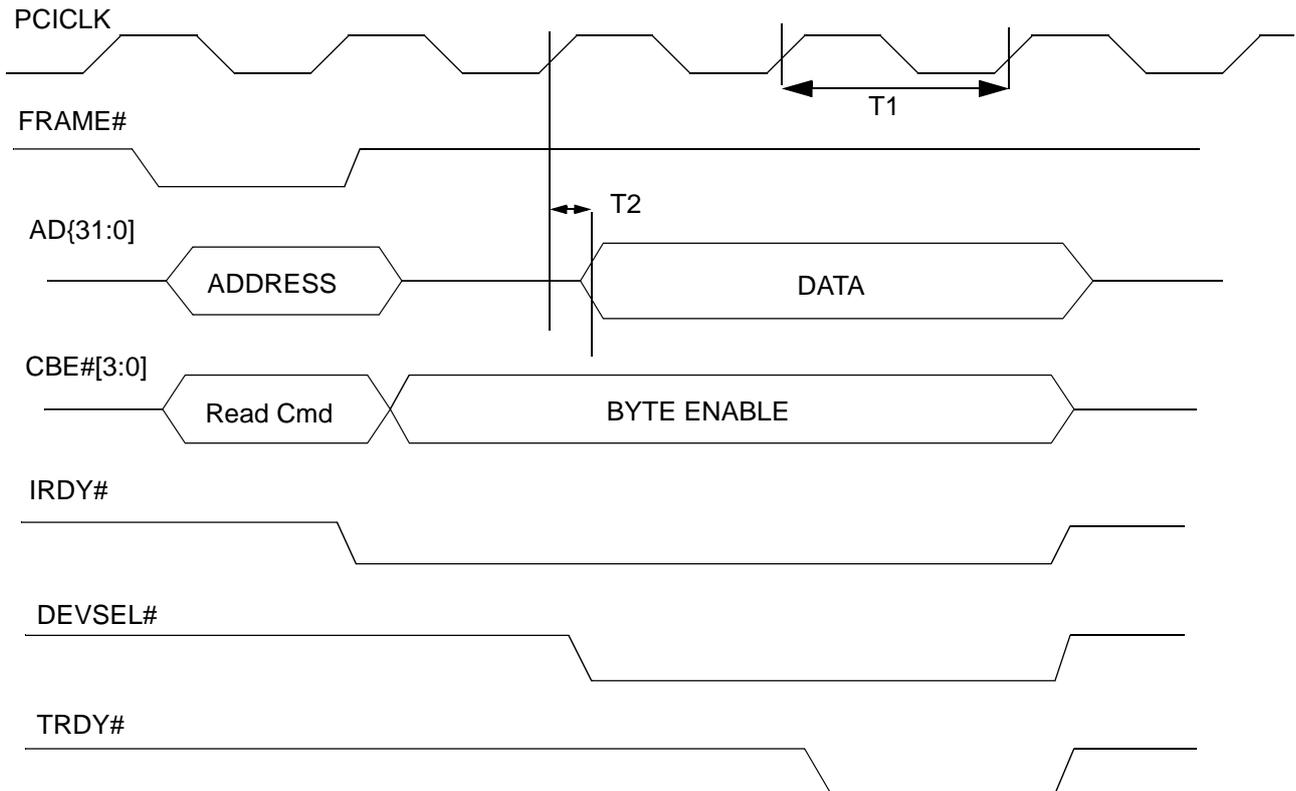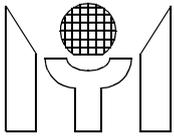
• Write Cycle
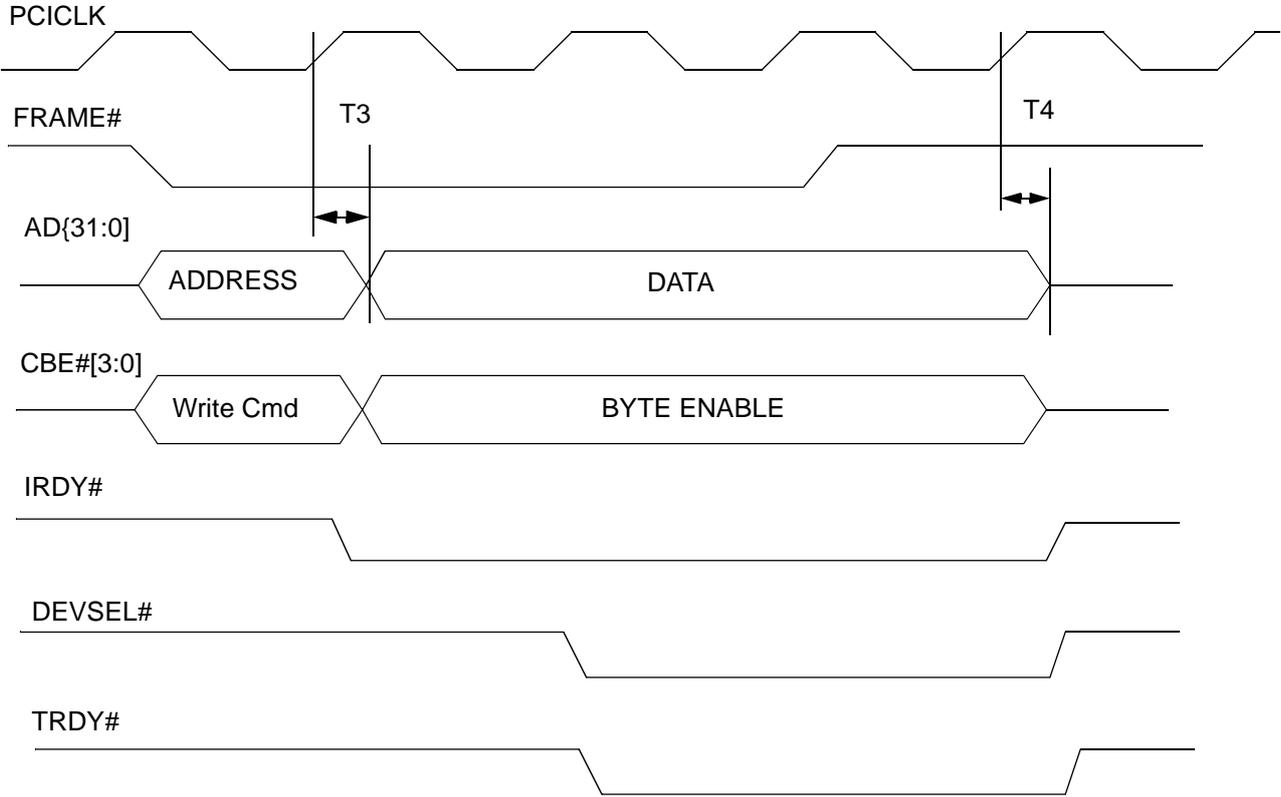
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	PCI CLK Cycle Time	30		40	nS	
T2	CLK to Signal Valid Delay	2		11	nS	
T3	Input Setup Time to CLK	7			nS	
T4	Input Hold Time to CLK	0			nS	
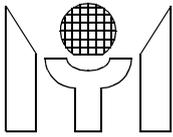
6.0 PACKAGE DIMENSION

6.1 128 pin PQFP
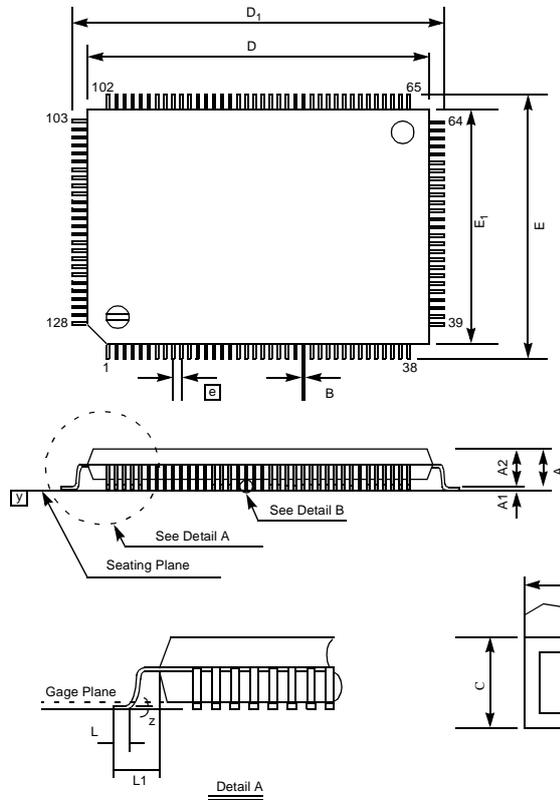
Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
z	0°	-	7°	0°	-	7°

Note:
1. Dimension D1 & E1 do not include mold protrusion.
   But mold mismatch is included. Allowable protrusion is .25mm/.010" per side.
2. Dimension B does not include dambar protrusion. Allowable dambar protrusion .08mm/.003". Total in excess of the B dimemsion at maximum material condition. Dambar cannot be located on the lower radius or the foot.
3. Controlling dimension : Millimeter.

Detail A

Detail B