

FEATURES

- Advanced trench process technology
- Ultra low R_{ds(on)}, typical 8mohm
- High avalanche energy, 100% test
- Fully characterized avalanche voltage and current
- Lead free product

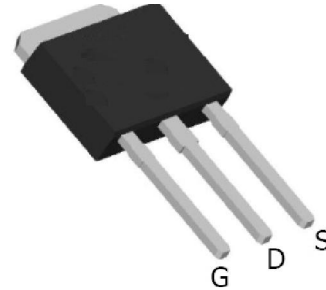
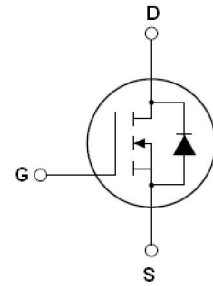
DESCRIPTION

The SSF5510G is a new generation of middle voltage and high current N-Channel enhancement mode trench power MOSFET. This new technology increases the device reliability and electrical parameter repeatability. SS5510G is assembled in high reliability and qualified assembly house.

APPLICATIONS

- Power switching application

ID =56A
BV=55V
R_{DS(ON)} =8mohm (typ.)



SSF5510G Top View

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @T _c =25°C	Continuous drain current, V _{GS} @10V	56	A
I _D @T _c =100C	Continuous drain current, V _{GS} @10V	40	
I _{DM}	Pulsed drain current ①	224	
P _D @T _c =25C	Power dissipation	90	W
	Linear derating factor	0.9	W/C
V _{GS}	Gate-to-Source voltage	±20	V
dv/dt	Peak diode recovery voltage	5.0	v/ns
E _{AS}	Single pulse avalanche energy ②	405	mJ
E _{AR}	Repetitive avalanche energy	TBD	
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

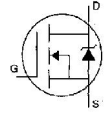
	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-case	—	—	1.4	°C/W
R _{θJA}	Junction-to-ambient	—	—	62	

Electrical Characteristics @T_J=25 °C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source breakdown voltage	55	—	—	V	V _{GS} =0V, I _D =250μA
R _{DS(on)}	Static Drain-to-Source on-resistance	—	8	10	mΩ	V _{GS} =10V, I _D =34A
V _{GS(th)}	Gate threshold voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{DSS}	Drain-to-Source leakage current	—	—	2	μA	V _{DS} =55V, V _{GS} =0V
		—	—	10		V _{DS} =44V, V _{GS} =0V, T _J =150°C

I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source reverse leakage	—	—	-100		$V_{GS}=-20V$
Q_g	Total gate charge	—	72	—	nC	$I_D=34A$
Q_{gs}	Gate-to-Source charge	—	18	—		$V_{DD}=44V$
Q_{gd}	Gate-to-Drain("Miller") charge	—	20	—		$V_{GS}=10V$
$t_{d(on)}$	Turn-on delay time	—	14	—	nS	$V_{DD}=28V$
t_r	Rise time	—	110	—		$I_D=34A$
$t_{d(off)}$	Turn-Off delay time	—	53	—		$R_G=6.8\Omega$
t_f	Fall time	—	76	—		$V_{GS}=10V$
C_{iss}	Input capacitance	—	2580	—	pF	$V_{GS}=0V$
C_{oss}	Output capacitance	—	480	—		$V_{DS}=25V$
C_{rss}	Reverse transfer capacitance	—	110	—		$f=1.0MHZ$

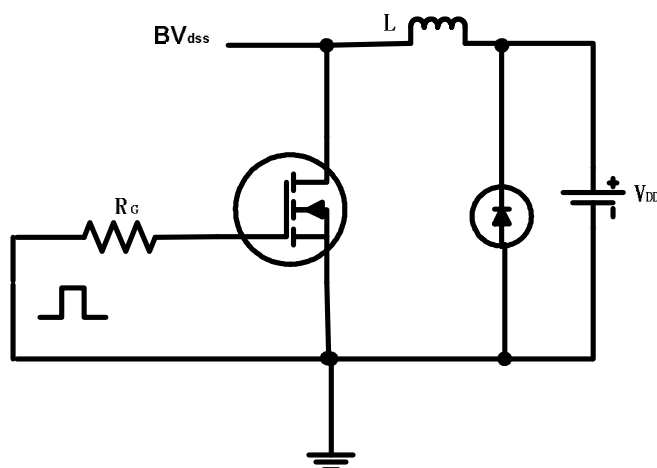
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	52	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	203		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J=25^\circ C, I_S=34A, V_{GS}=0V$ ③
t_{rr}	Reverse Recovery Time	—	60	—	nS	$T_J=25^\circ C, I_F=34A$ $di/dt=100A/\mu s$ ③
Q_{rr}	Reverse Recovery Charge	—	156	—	nC	
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_s + L_D$)				

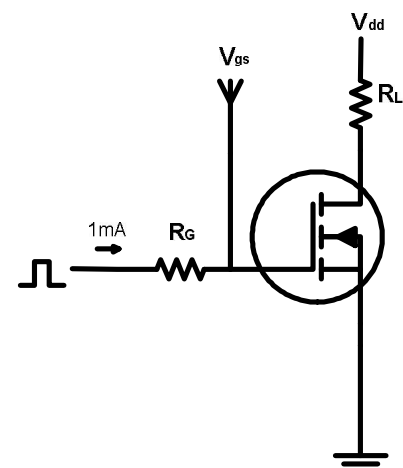
Notes:

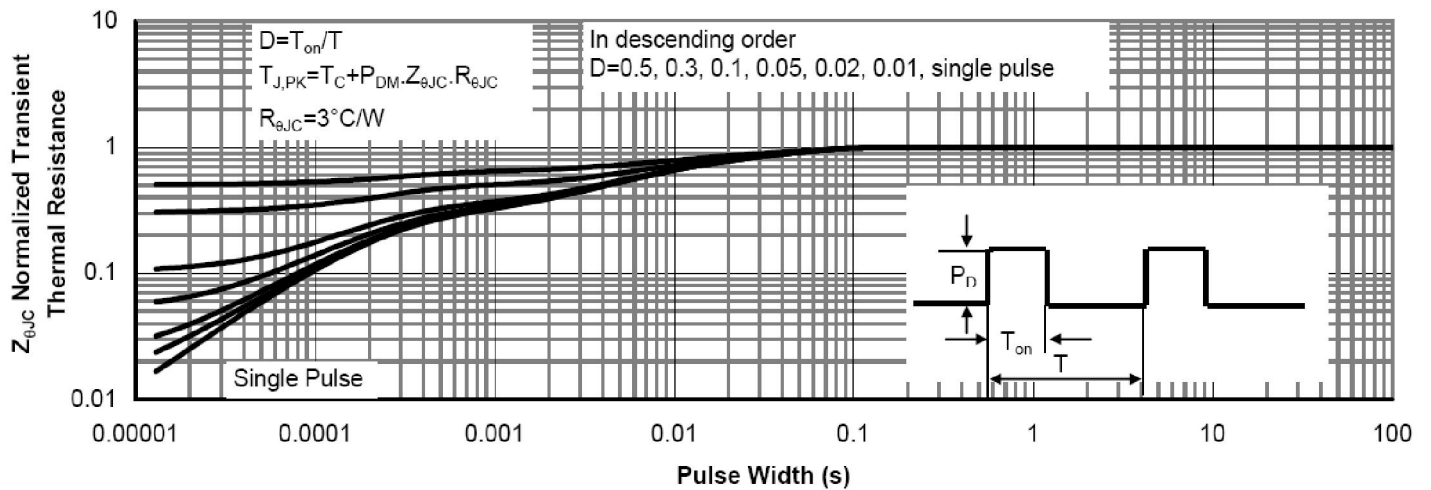
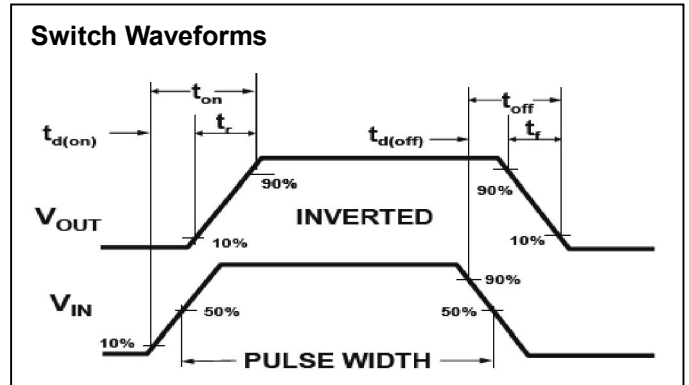
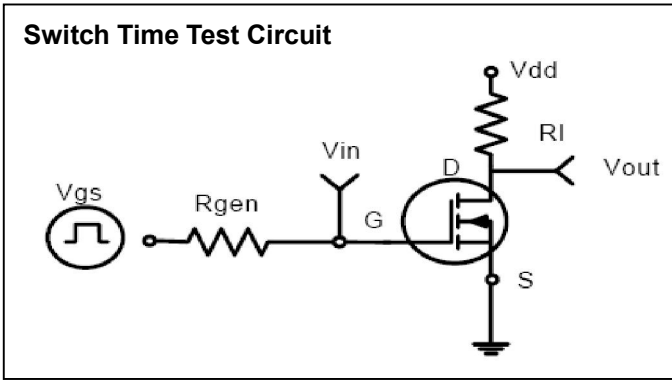
- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Test condition: $L = 0.3mH, I_D = 52A, V_{DD} = 30V$
- ③ Pulse width $\leq 300\mu s$, duty cycle $\leq 1.5\%$; $R_G = 25\Omega$ Starting $T_J = 25^\circ C$

EAS test circuit



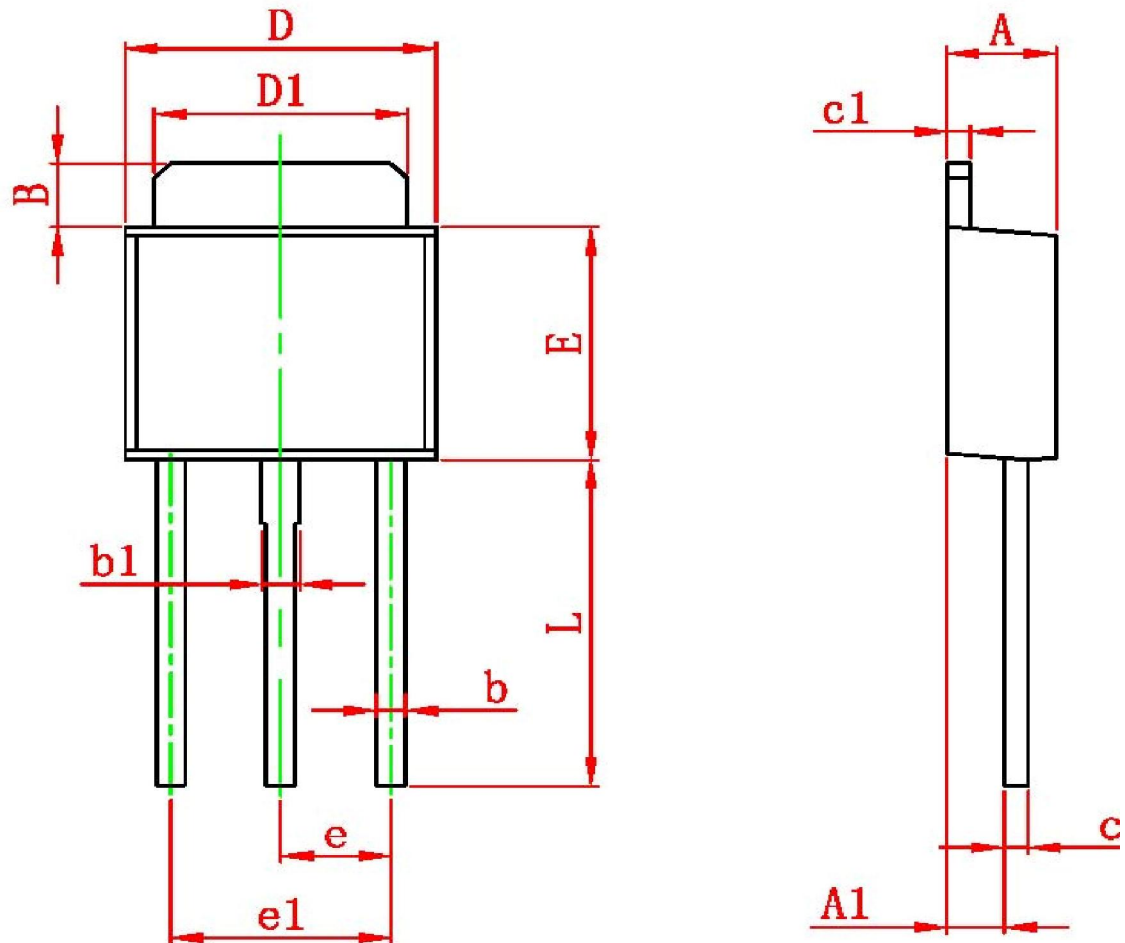
Gate charge test circuit





Transient Thermal Impedance Curve

TO-251 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311