

N-channel 800 V, 0.95 Ω typ., 5 A MDmesh™ K5 Power MOSFET in a I²PAKFP package

Datasheet - production data

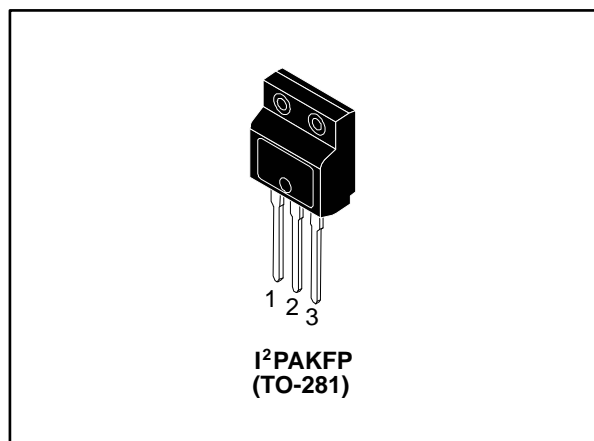


Figure 1: Internal schematic diagram

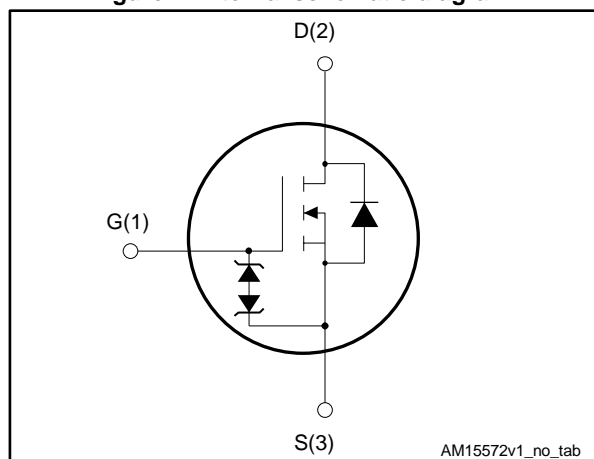


Table 1: Device summary

| Order code | Marking | Package | Packing |
|-------------|---------|-------------------------------|---------|
| STFI7LN80K5 | 7LN80K5 | I ² PAKFP (TO-281) | Tube |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|-------------|-----------------|--------------------------|----------------|
| STFI7LN80K5 | 800 V | 1.15 Ω | 5 A |

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|-------------|------------------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 5 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 3.4 | A |
| $I_D^{(2)}$ | Drain current (pulsed) | 20 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 25 | W |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C=25\text{ }^\circ\text{C}$) | 2500 | V |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_{stg} | Storage temperature | - 55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature | | |

Notes:

⁽¹⁾Limited by maximum junction temperature.

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾ $I_{SD} \leq 5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 640\text{ V}$

⁽⁴⁾ $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 5 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | $^\circ\text{C}/\text{W}$ |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 1.5 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 200 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 800 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}$ | | | 50 | μA |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$ | | 0.95 | 1.15 | Ω |

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 270 | - | pF |
| C_{oss} | Output capacitance | | - | 22 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 0.5 | - | pF |
| $C_{o(er)}^{(1)}$ | Equivalent capacitance energy related | $V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 17 | - | nC |
| $C_{o(tr)}^{(2)}$ | Equivalent capacitance time related | | - | 48 | - | nC |
| R_g | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 7.5 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 640\text{ V}$, $I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$ See (Figure 15: "Test circuit for gate charge behavior") | - | 12 | - | nC |
| Q_{gs} | Gate-source charge | | - | 2.6 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 8.6 | - | nC |

Notes:

⁽¹⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Time related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ See (Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform") | - | 9.3 | - | ns |
| t_r | Rise time | | - | 6.7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 23.6 | - | ns |
| t_f | Fall time | | - | 17.4 | - | ns |

Table 8: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 5 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 20 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ See Figure 16: "Test circuit for inductive load switching and diode recovery times" | - | 276 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.13 | | μC |
| I_{RRM} | Reverse recovery current | | - | 15.4 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ See Figure 16: "Test circuit for inductive load switching and diode recovery times" | - | 402 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.79 | | μC |
| I_{RRM} | Reverse recovery current | | - | 13.9 | | A |

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$ | 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

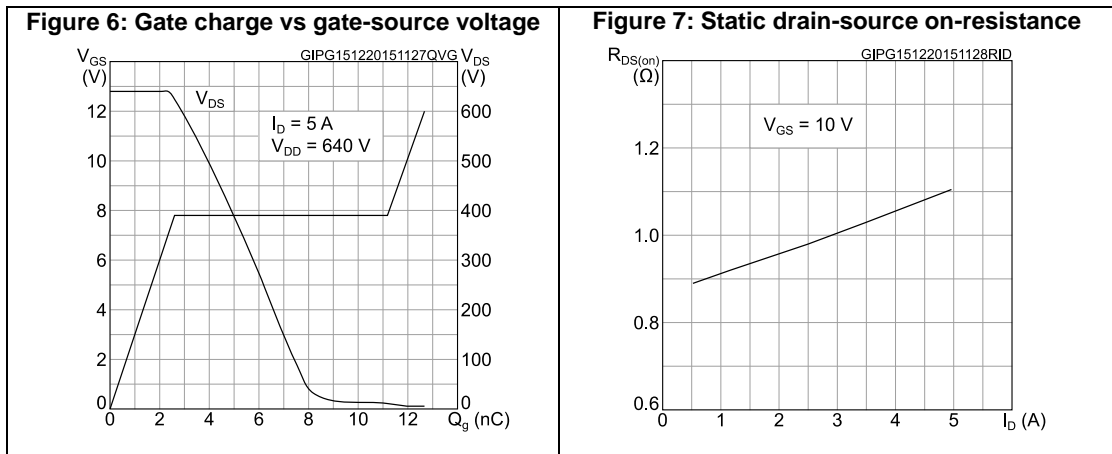
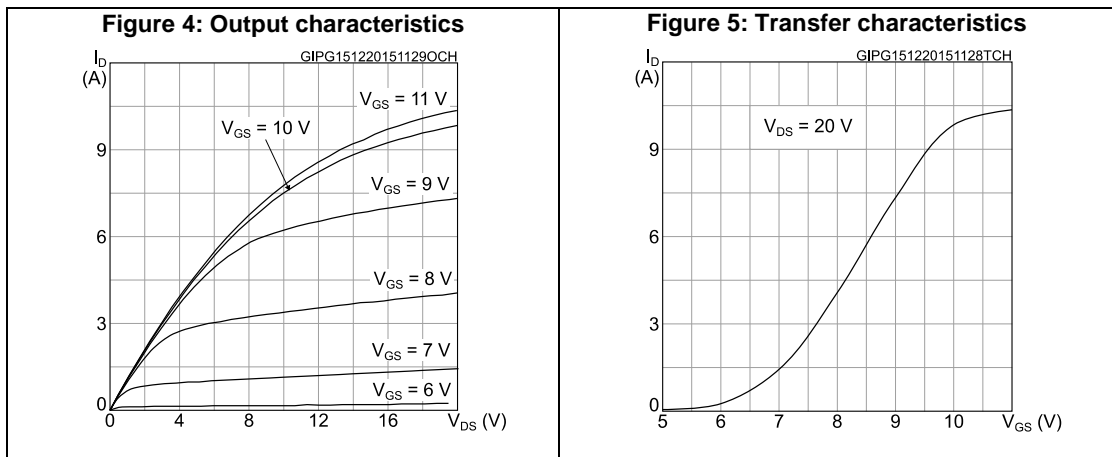
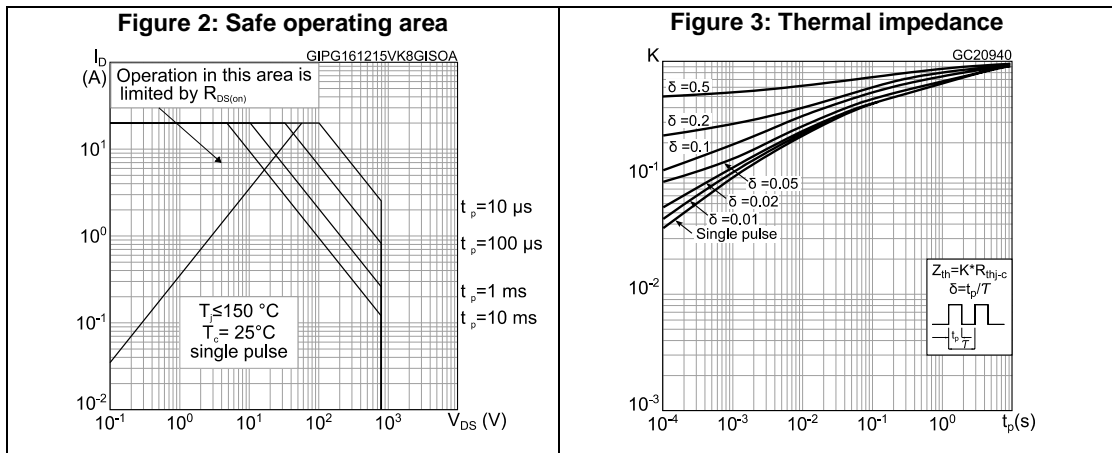


Figure 8: Capacitance variations

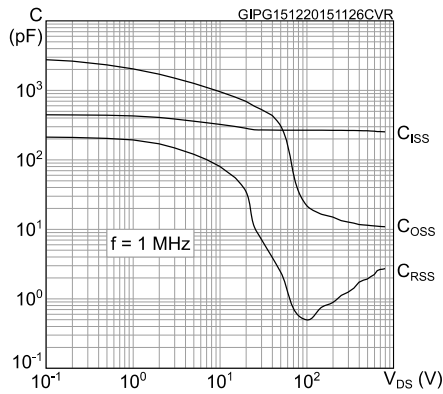


Figure 9: Normalized gate threshold voltage vs temperature

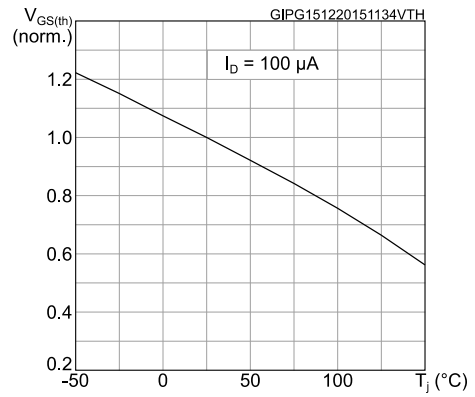


Figure 10: Normalized $V_{(BR)DSS}$ vs temperature

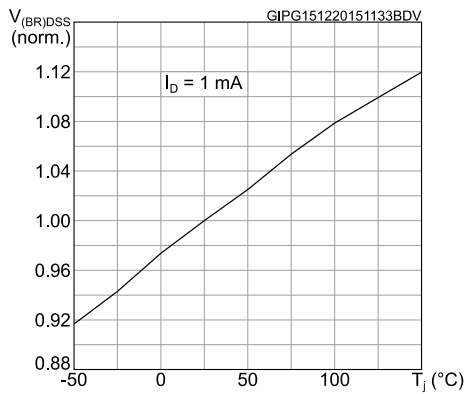


Figure 11: Normalized on-resistance vs temperature

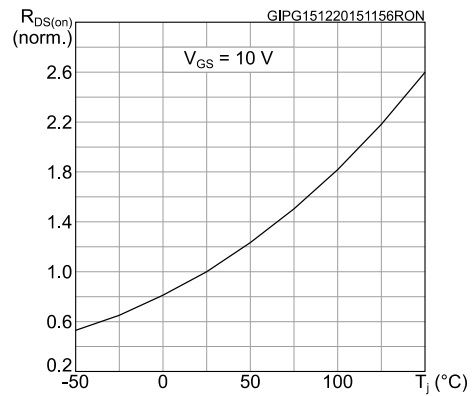


Figure 12: Source-drain diode forward characteristics

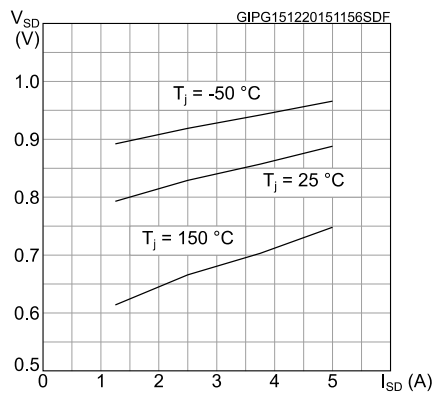
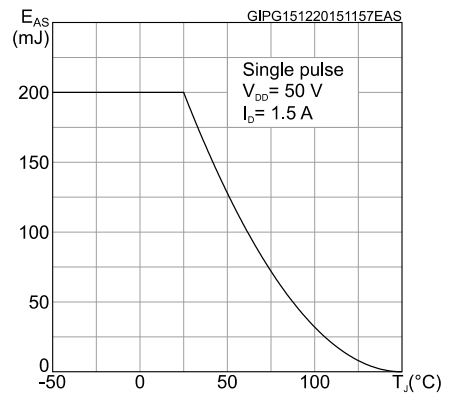


Figure 13: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 14: Test circuit for resistive load switching times



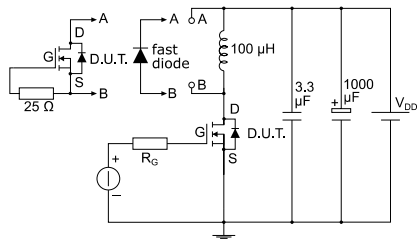
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Figure 15: Test circuit for gate charge behavior



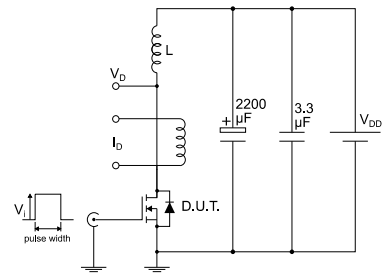
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Figure 16: Test circuit for inductive load switching and diode recovery times



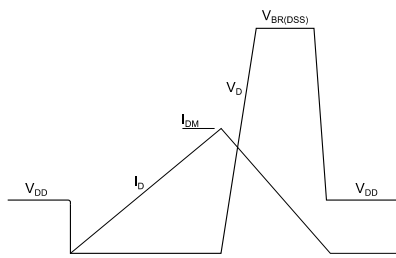
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Figure 17: Unclamped inductive load test circuit



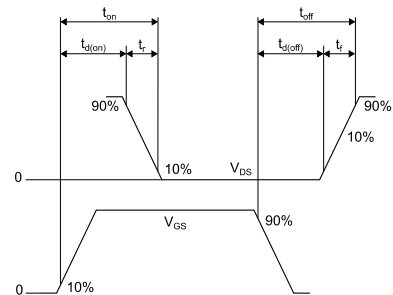
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Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAKFP (TO-281) package information

Figure 20: I²PAKFP (TO-281) package outline

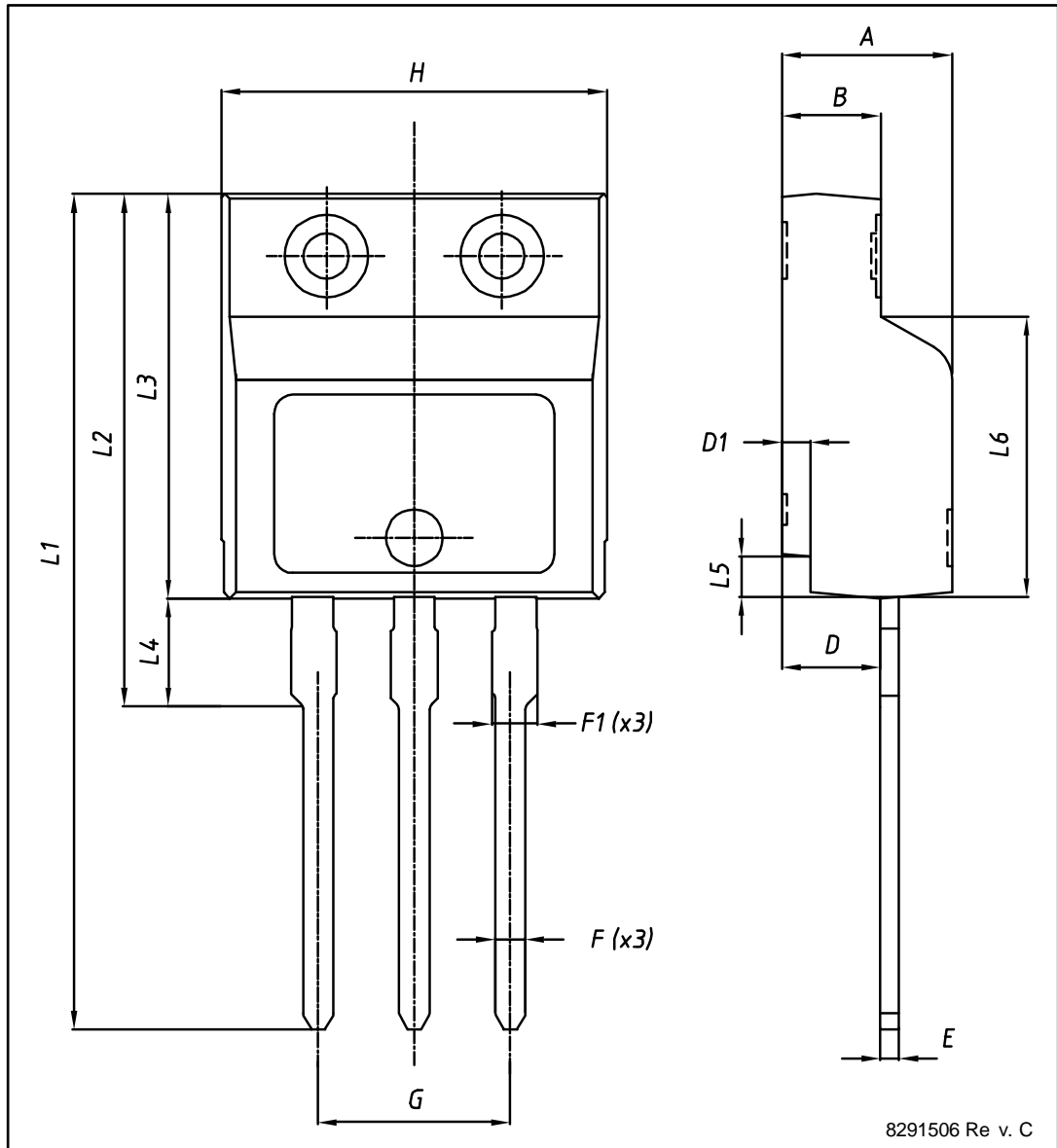


Table 10: I²PAKFP (TO-281) mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| D1 | 0.65 | | 0.85 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | | | 1.20 |
| G | 4.95 | | 5.20 |
| H | 10.00 | | 10.40 |
| L1 | 21.00 | | 23.00 |
| L2 | 13.20 | | 14.10 |
| L3 | 10.55 | | 10.85 |
| L4 | 2.70 | | 3.20 |
| L5 | 0.85 | | 1.25 |
| L6 | 7.50 | 7.60 | 7.70 |

5 Revision history

Table 11: Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------|
| 15-Dec-2015 | 1 | First release. |

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